

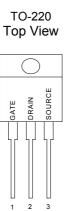
## **GENERAL DESCRIPTION**

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage-blocking capability without degrading performance over time. In addition, this advanced MOSFET is designed to withstand high energy in avalanche and commutation modes. The new energy efficient design also offers a drain-to-source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional and safety margin against unexpected voltage transients.

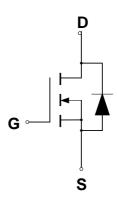
### FEATURES

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I<sub>DSS</sub> and V<sub>DS</sub>(on) Specified at Elevated Temperature

# **PIN CONFIGURATION**



#### SYMBOL



N-Channel MOSFET

### **ABSOLUTE MAXIMUM RATINGS**

Rating		Value	Unit
Drain to Current - Continuous		10	А
- Pulsed		40	
Gate-to-Source Voltage - Continue		±20	V
- Non-repetitive	$V_{GSM}$	±40	V
Total Power Dissipation		125	W
Derate above 25		1.0	W/
Operating and Storage Temperature Range		-55 to 150	
Single Pulse Drain-to-Source Avalanche Energy - $T_J = 25$		300	mJ
$(V_{DD} = 100V, V_{GS} = 10V, I_L = 10A, L = 6mH, R_G = 25\Omega)$			
Thermal Resistance - Junction to Case		1.7	/W
- Junction to Ambient	θ <sub>JA</sub>	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	TL	260	



#### **ORDERING INFORMATION**

Part Number	Package	
CMT10N40N220	TO-220	

# **ELECTRICAL CHARACTERISTICS**

Unless otherwise specified,  $T_{\rm J}$  = 25  $\,$  .

			CMT10N40			
Characteristic		Symbol	Min	Тур	Max	Units
Drain-Source Breakdown Voltage		V <sub>(BR)DSS</sub>	400			V
$(V_{GS} = 0 V, I_D = 250 \mu A)$						
Drain-Source Leakage Current		I <sub>DSS</sub>				μA
$(V_{DS} = 400 \text{ V}, V_{GS} = 0 \text{ V})$					25	
$(V_{DS} = 400 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 125)$					250	
Gate-Source Leakage Current-Forward		I <sub>GSSF</sub>			100	nA
$(V_{gsf} = 20 V, V_{DS} = 0 V)$						
Gate-Source Leakage Current-Reverse		I <sub>GSSR</sub>			100	nA
$(V_{gsr} = 20 \text{ V}, V_{DS} = 0 \text{ V})$						
Gate Threshold Voltage		$V_{GS(th)}$	2.0		4.0	V
$(V_{DS} = V_{GS}, I_{D} = 250 \ \mu A)$						
Static Drain-Source On-Resistance (V <sub>GS</sub> =	= 10 V, I <sub>D</sub> = 5.0A) *	R <sub>DS(on)</sub>			0.55	Ω
Drain-Source On-Voltage (V <sub>GS</sub> = 10 V)		$V_{\text{DS(on)}}$			6.0	V
(I <sub>D</sub> = 5.0 A)						
Forward Transconductance (V <sub>DS</sub> = 50 V, I	<sub>D</sub> = 5.0A) *	<b>g</b> fs	5.8			mhos
Input Capacitance	$(V_{DS} = 25 V, V_{GS} = 0 V,$	Ciss		1570		pF
Output Capacitance	f = 1.0  MHz	C <sub>oss</sub>		230		pF
Reverse Transfer Capacitance	1 = 1.0 MHZ)	C <sub>rss</sub>		55		pF
Turn-On Delay Time	$(1) = 200 \times 1 = 10.0 A$	t <sub>d(on)</sub>		25		ns
Rise Time	$(V_{DD} = 200 \text{ V}, \text{ I}_{D} = 10.0 \text{ A},$ $V_{GS} = 10 \text{ V},$ $R_{G} = 10\Omega) *$	tr		37		ns
Turn-Off Delay Time		t <sub>d(off)</sub>		75		ns
Fall Time	$R_G = 10\Omega_2$	t <sub>f</sub>		31		ns
Total Gate Charge		Qg		46	63	nC
Gate-Source Charge	(V <sub>DS</sub> = 320 V, I <sub>D</sub> = 10.0 A, V <sub>GS</sub> = 10 V)*	$Q_gs$		10		nC
Gate-Drain Charge	$V_{GS} = 10 V$	$Q_{gd}$		23		nC
Internal Drain Inductance		L <sub>D</sub>		4.5		nH
(Measured from the drain lead 0.25" fro	m package to center of die)					
Internal Drain Inductance		Ls		7.5		nH
(Measured from the source lead 0.25" from package to source bond pad)						
SOURCE-DRAIN DIODE CHARACTERIS	STICS					
Forward On-Voltage(1)		V <sub>SD</sub>			1.5	V
Forward Turn-On Time	$(I_{\rm S} = 10.0 \text{ A}, V_{\rm GS} = 0 \text{ V},$	t <sub>on</sub>		**		ns
Reverse Recovery Time	$d_{IS}/d_t = 100A/\mu s)$	t <sub>rr</sub>		250		ns

\* Pulse Test: Pulse Width 300µs, Duty Cycle 2%

\*\* Negligible, Dominated by circuit inductance



# **TYPICAL ELECTRICAL CHARACTERISTICS**

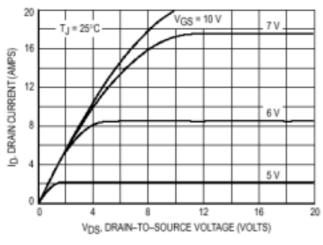


Figure 1. On–Region Characteristics

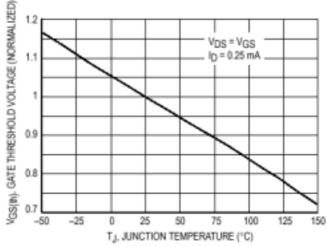


Figure 2. Gate–Threshold Voltage Variation With Temperature

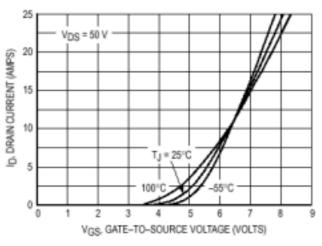


Figure 3. Transfer Characteristics

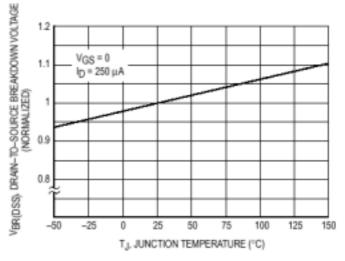
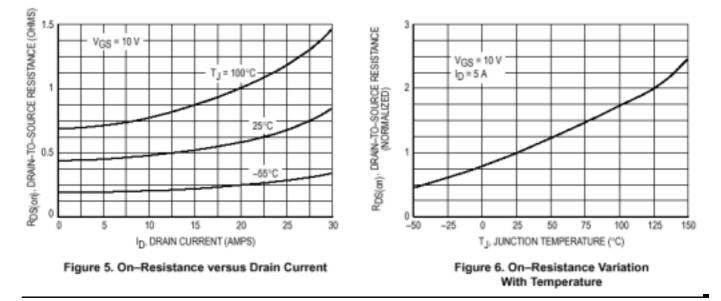
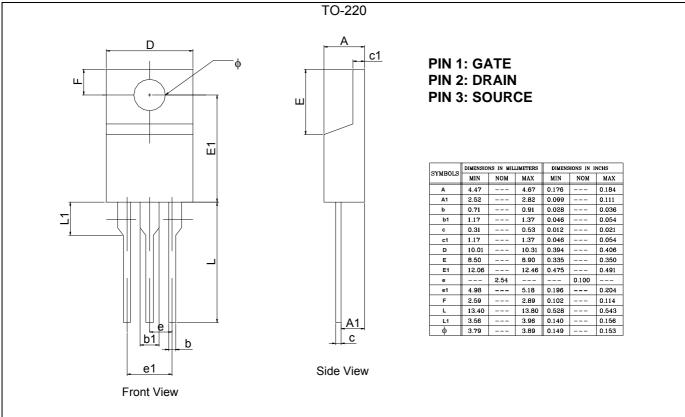


Figure 4. Breakdown Voltage Variation With Temperature





### **PACKAGE DIMENSION**





## **IMPORTANT NOTICE**

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