CMOSTEK CMT2119B

+ 20 dBm High Power Sub-1G RF Transmitter

Features

- Frequency range: 127 - 1020 MHz
- Modulation: OOK, (G)FSK and (G)MSK
- Data rate: 0.5 - 300 kbps
- Voltage range: 1.8 - 3.6 V
- Transmitting current: 23 mA @ 13 dBm, 433.92 MHz, FSK
  72 mA @ 20 dBm, 433.92 MHz, FSK
- Support auto Tx mode
- Sleep current
  - 300 nA (deep sleep)
  - 800 nA (automatic operating)
- 3-wire SPI interface
- Support for direct mode and packet mode
- Configurable packet processor and 64-byte FIFO
- Codec with supports for non-return-to-zero, Manchester and data whitening functions
- Support for forward error correction
- 16-pin QFN3x3 packaging

Application

- Home security and building automation
- ISM band data communication
- Industrial monitoring and control
- Remote control and security system
- Remote key entry
- Wireless sensor node
- Tag reader

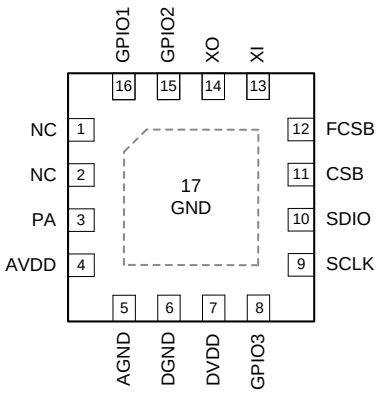
Ordering Information

Product Model	Frequency	Package	Minimum Order Quantity
CMT2119B-EQR	433.92 MHz	QFN16	3,000 pcs
Refer to Section 9 for more ordering information.			

Description

The CMT2119B is an OOK and (G)FSK based high performance RF transmitter with a transmitting power up to 20 dBm, applying to 127 - 1020 MHz band wireless applications. The product is part of the CMOSTEK NextGenRF™ product family which covers a complete product line consisting of transmitters, receivers and transceivers. Employed with high integration density and simplified peripheral designs, it can deliver up to 20 dBm power, improving application link performance remarkably. The support of multiple packet formats and codec makes it flexible to meet different application requirements per different packet formats and encoding methods. In addition, the CMT2119B provides functions such as 64-byte Tx FIFO, rich GPIO and interrupt configuration, auto Tx operation mode, low voltage detection, power-on reset, low-frequency clock output, manual fast frequency hopping, which helps fulfill flexible application design thus deliver differentiated products. Operating with a supply range of 1.8 - 3.6 V, it consumes only 23 mA and 77 mA current while delivering +13 dBm and +20 dBm power respectively.

QFN16 (3x3) Packaging



CMT2119B Top View

Table of Contents

1 Electrical Specifications

V_{DD} = 3.3 V，T_{OP} = 25 °C，F_{RF} = 433.92 MHz. All measurement results are obtained using the evaluation board CMT2119B-EM if nothing else stated.

1.1 Recommended Operating Conditions

Table 1. Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating supply voltage	V_{DD}		1.8		3.6	V
Operating temperature	T_{OP}		- 40		85	℃
Supply voltage slope			1			mV/us

1.2 Absolute Maximum Ratings

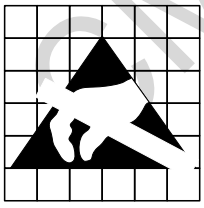
Table 2. Absolute Maximum Ratings[1]

Parameter	Symbol	Condition	Min.	Typ.	Max.
Supply voltage	V_{DD}		-0.3	3.6	V
Interface voltage	V_{IN}		-0.3	3.6	V
Junction temperature	T_J		-40	125	℃
Storage temperature	T_{STG}		-50	150	℃
Soldering temperature	T_{SDR}	Lasts for at least 30 seconds		255	℃
ESD rating[2]		Human body model (HBM)	-2	2	kV
Latch-up current		@ 85 ℃	-100	100	mA

Notes:

[1]. Exceeding *the Absolute Maximum Ratings* may cause permanent damage to the equipment. This value is a pressure rating and does not imply that the function of the equipment is affected under this pressure condition, but if it is exposed to absolute maximum ratings for extended periods of time, it may affect equipment reliability.

[2]. The CMT2119B is a high performance RF integrated circuit. The operation and assembly of this chip should only be performed on a workbench with good ESD protection.



Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent performance degradation or loss of functionality.

1.3 Power Consumption

Table 3. Power Consumption Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Sleep current	I_{SLEEP}	Sleep mode, sleep counter off		300		nA
		Sleep mode ,sleep counter on		800		nA
Standby current	$I_{Standby}$	Crystal oscillator on		1.45		mA
TFS current	I_{TFS}	433 MHz		5.6		mA
		868 MHz		5.9		mA
		915 MHz		5.9		mA
TX current	I_{Tx}	FSK, 433 MHz, +20 dBm		72		mA
		FSK, 433 MHz, +13 dBm		23		mA
		FSK, 433 MHz, +10 dBm		18		mA
		FSK, 433 MHz, -10 dBm		8		mA
		FSK, 868 MHz, +20 dBm		87		mA
		FSK, 868 MHz, +13 dBm		27		mA
		FSK, 868 MHz, +10 dBm		19		mA
		FSK, 868 MHz, -10 dBm		8		mA
		FSK, 915 MHz, +20 dBm		70		mA
		FSK, 915 MHz, +13 dBm		28		mA
		FSK, 915 MHz, +10 dBm		19		mA
		FSK, 915 MHz, -10 dBm		8		mA

1.4 Transmitter

Table 4. Transmitter Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output power	P_{OUT}	Different frequency bands require specific peripheral materials	- 20		+ 20	dBm
Output power step	P_{STEP}			1		dB
GFSK Gaussian filter factor	BT		0.3	0.5	1.0	-
Output power change at different temperatures	$P_{OUT-TOP}$	- 40 ~ + 85 °C		1		dB
Transmission spurious emission		P_{OUT} = +13 dBm，433MHz，F_{RF} < 1 GHz			-42	dBm
		1 GHz ~ 12.75 GHz, including harmonic wave			-36	dBm
Harmonic output for F_{RF}= 433 MHz	$H2_{433}$	2nd harmonic , +20 dBm P_{OUT}		- 46		dBm
	$H3_{433}$	3rd harmonic, +20 dBm P_{OUT}		- 50		dBm
Harmonic output for F_{RF} = 868 MHz	$H2_{868}$	2nd harmonic, +20 dBm P_{OUT}		- 43		dBm
	$H3_{868}$	3rd harmonic, +20 dBm P_{OUT}		- 52		dBm
Harmonic output for F_{RF} = 915 MHz	$H2_{915}$	2nd harmonic, +20 dBm P_{OUT}		- 48		dBm
	$H3_{915}$	3rd harmonic, +20 dBm P_{OUT}		-53		dBm

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Harmonic output For F_{RF} = 433 MHz	$H2_{433}$	2nd harmonic, +13 dBm P_{OUT}		-52		dBm
	$H3_{433}$	3rd harmonic, +13 dBm P_{OUT}		-52		dBm
Harmonic output For F_{RF} = 868 MHz	$H2_{868}$	2nd harmonic, +13 dBm P_{OUT}		-52		dBm
	$H3_{868}$	3rd harmonic, +13 dBm P_{OUT}		-52		dBm
Harmonic output For F_{RF} = 915 MHz	$H2_{915}$	2nd harmonic, +13 dBm P_{OUT}		-52		dBm
	$H3_{915}$	3rd harmonic, +13 dBm P_{OUT}		-52		dBm

1.5 Settling Time

Table 5. Settling time

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Settling Time	T_{SLP-TX}	From Sleep to TX		1000		us
	T_{STB-TX}	From Standby to TX		300		us
	T_{TFS-TX}	From TFS to TX		10		us

1.6 RF Frequency Synthesizer

Table 6. RF Frequency Synthesizer Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency range	F_{RF}		760		1020	MHz
			380		510	MHz
			190		340	MHz
			127		170	MHz
Frequency resolution	F_{RES}			25		Hz
Frequency tuning time	t_{TUNE}			150		us
Phase noise @ 433 MHz	PN_{433}	10 kHz deviation		-94		dBc/Hz
		100 kHz deviation		-99		dBc/Hz
		500 kHz deviation		-118		dBc/Hz
		1MHz deviation		-127		dBc/Hz
		10 MHz deviation		-134		dBc/Hz
Phase noise @ 868 MHz	PN_{868}	10 kHz deviation		-92		dBc/Hz
		100 kHz deviation		95		dBc/Hz
		500 kHz deviation		-114		dBc/Hz
		1MHz deviation		-121		dBc/Hz
		10 MHz deviation		-130		dBc/Hz
Phase noise@ 915 MHz	PN_{915}	10 kHz deviation		-89		dBc/Hz
		100 kHz deviation		-92		dBc/Hz
		500 kHz deviation		-111		dBc/Hz
		1MHz deviation		-121		dBc/Hz
		10 MHz deviation		-130		dBc/Hz

1.7 Low Battery Detection

Table 7. Low Battery Detection Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Low battery detection resolution	LBD_{RES}			50		mV

1.8 Crystals

Table 8. Crystals Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Crystal frequency[1]	F_{XTAL}			26		MHz
Crystal frequency tolerance[2]	ppm			20		ppm
Load capacitance	C_{LOAD}			15		pF
Crystal equivalent resistance	Rm			60		Ω
Crystal startup time[3]	t_{XTAL}			400		us

Notes:

[1]. For CMT2119B, an external reference clock can be used to drive the XI pin directly through a coupling capacitor. The peak-to-peak level of the external reference clock is required between 0.3 and 0.7 V.

[2]. It involves:(1) initial tolerance, (2) crystal loading, (3) aging, and (4) temperature changing. The acceptable crystal frequency tolerance is subject to the bandwidth of the receiver and the RF tolerance between the receiver and its paired transmitter.

[3]. This parameter is largely related to the crystal

1.9 Low-frequency Oscillator

Table 9. Low-frequency Oscillator Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Calibration frequency [1]	F_{LPOSC}			32		kHz
Frequency precision		After calibration		1		%
Temperature factor [2]				- 0.02		%/°C
Supply voltage factor[3]				+ 0.5		%/V
Initial calibration time	$t_{LPOSC-CAL}$			4		ms

Notes:

[1]. During the PUP phase, the low-frequency oscillator is calibrated automatically to the crystal oscillator frequency and the calibration is performed periodically.

[2]. The frequency drifts with the temperature change after calibration.

[3]. The frequency drifts with the supply voltage change after calibration.

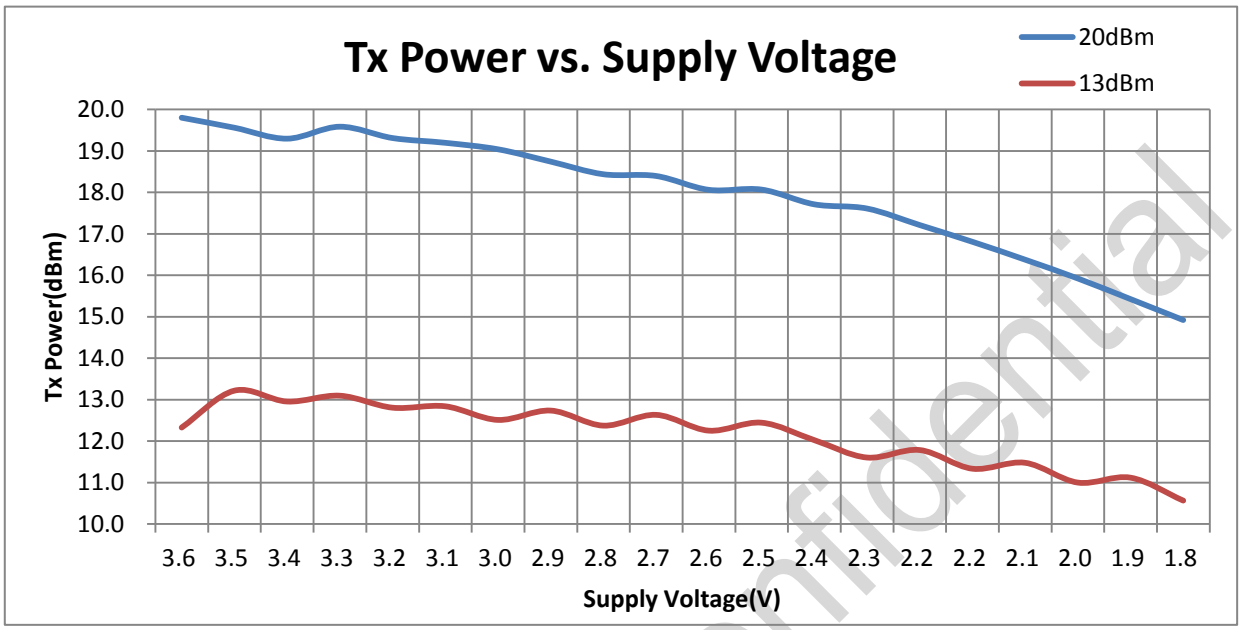
1.10 Digital Interface

Table 10. Digital Interface Specification

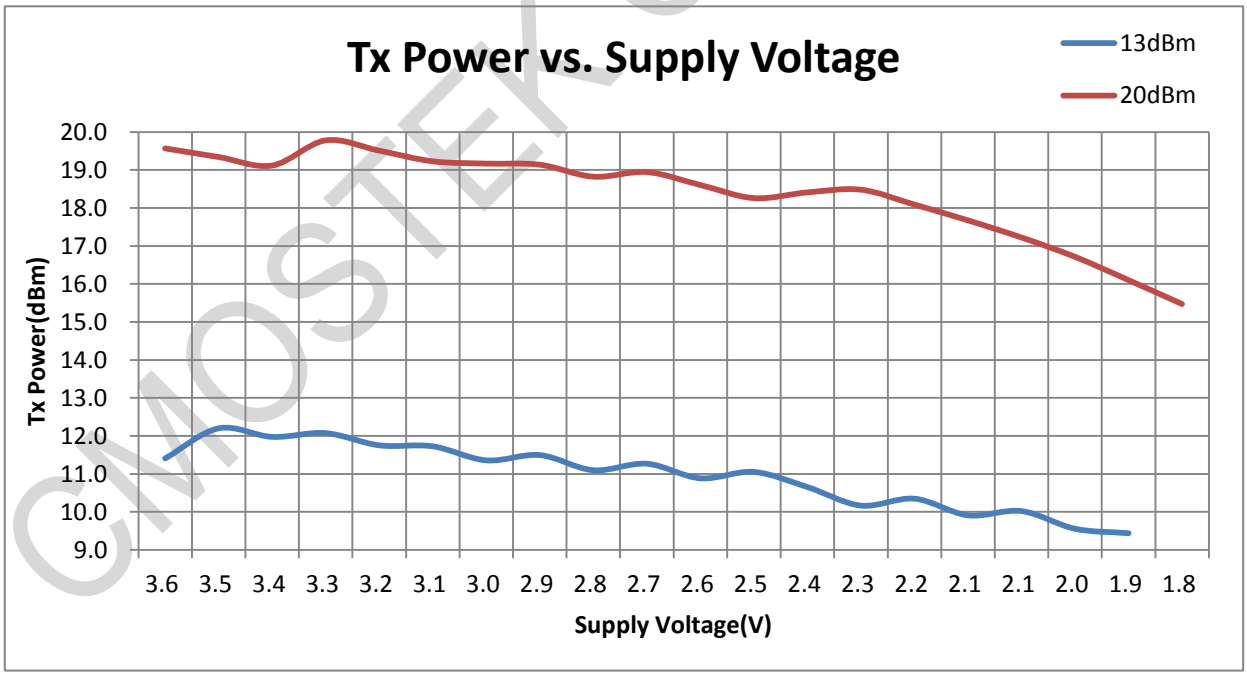
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Digital signal input high level	V_{IH}		0.8			V_{DD}
Digital signal input low level	V_{IL}				0.2	V_{DD}
Digital signal output high level	V_{OH}	@I_{OH}= -0.5 mA	Vdd-0.4			V
Digital signal output low level	V_{OL}	@I_{OL}= 0.5 mA			0.4	V
SCL frequency	F_{SCL}				5	MHz
Time for SCL high	T_{CH}		50			ns
Time for SCL low	T_{CL}		50			ns
Time for SCL rising edge	T_{CR}		50			ns
Time for SCL falling edge	T_{CF}		50			ns

1.11 Typical Parameter Chart

1.11.1 Tx Power and Supply Voltage Correlation



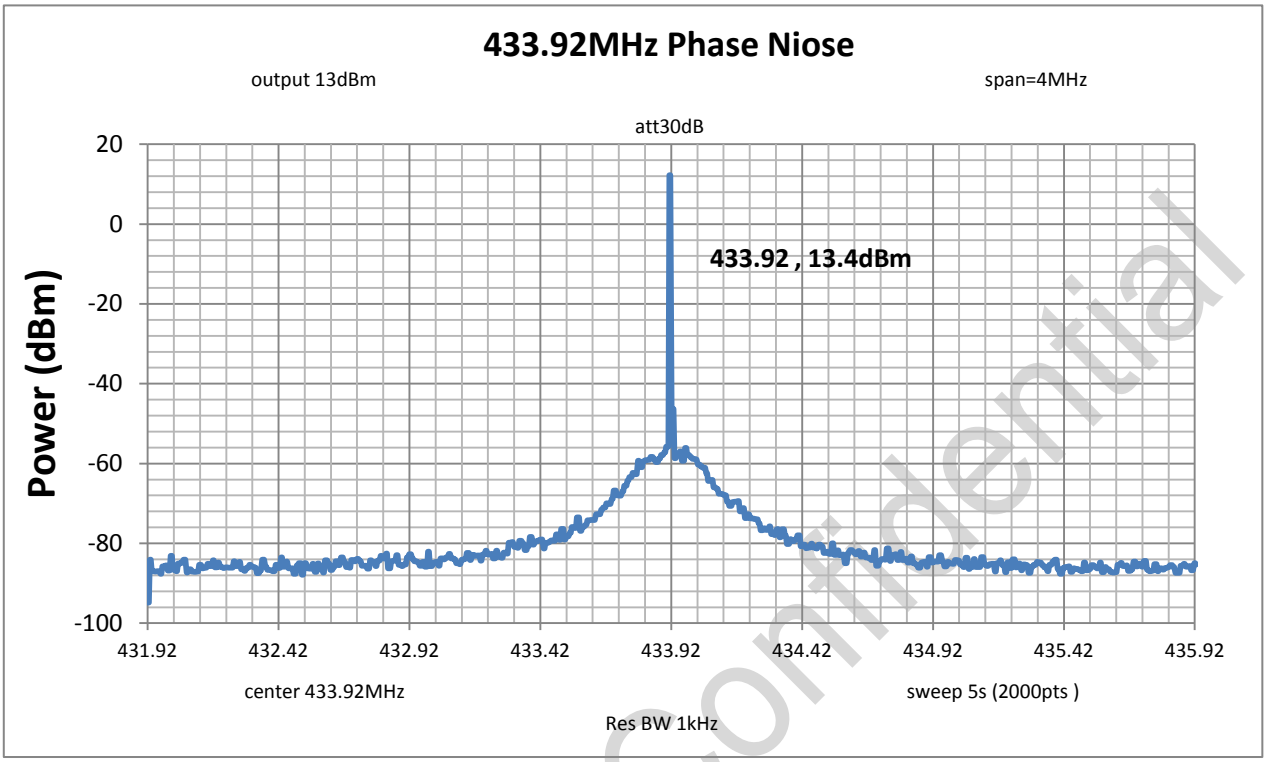
Test Conditions: Freq = 434 MHz, 20 dBm / 13 dBm matching network



Test Conditions: Freq = 868 MHz, 20 dBm / 13 dBm matching network

Figure 1. Tx Power and Supply Voltage Correlation Chart

1.11.2 Tx Phase Noise



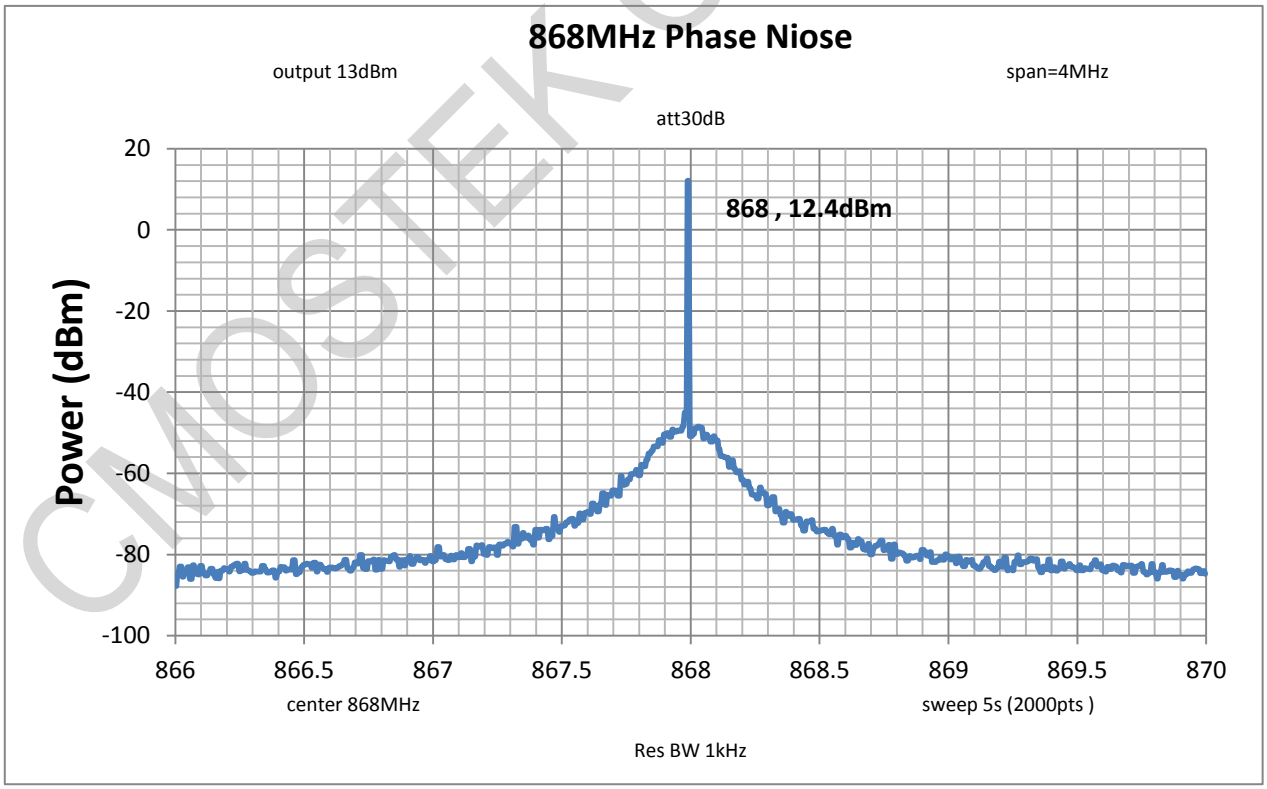


Figure 2. Tx Phase Noise Chart

2 Pin Description

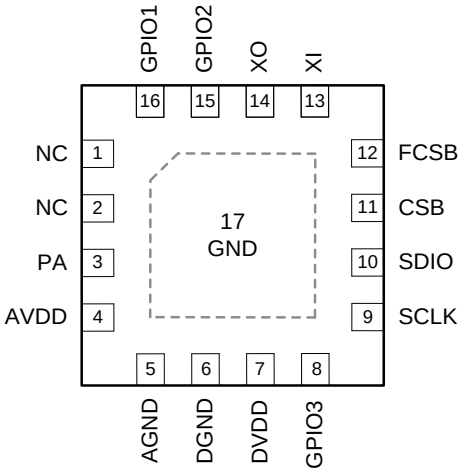


Figure 3. CMT2119B Pin Arrangement Diagram

Table 11. CMT2119B Pin Description

Pin #	Pin Name	I/O	Description
1	NC	-	Not connected
2	NC	-	Not connected
3	PA	O	PA output
4	AVDD	IO	Analog VDD
5	AGND	IO	Analog GND
6	DGND	IO	Digital GND
7	DVDD	IO	Digital VDD
8[1]	GPIO3	IO	Can configure as : CLKO, INT2 or DCLK (TX).
9	SCLK	I	Clock for SPI
10	SDIO	IO	Data input and output for SPI
11	CSB	I	Chip selection for SPI register access
12	FCSB	I	Chip selection for SPI FIFO access
13	XI	I	Crystal circuit input
14	XO	O	Crystal circuit output
15[1]	GPIO2	IO	Can configure as : INT1, INT2 or DCLK (TX).
16[2]	GPIO1	IO	Can configure as : DIN, INT1, INT2 or DCLK (TX).
17	GND	I	Analog GND, must connect ground

Notes:

[1]. INT1 and INT2 refer to RF interrupts. DCLK (TX) refers to modulated data rate synchronous clock, which is switched automatically upon Tx mode switching.

[2]. DIN is the external modulation data input port in the direct mode. Only the GPIO1 pin has this function.

3 Typical Application Schematic

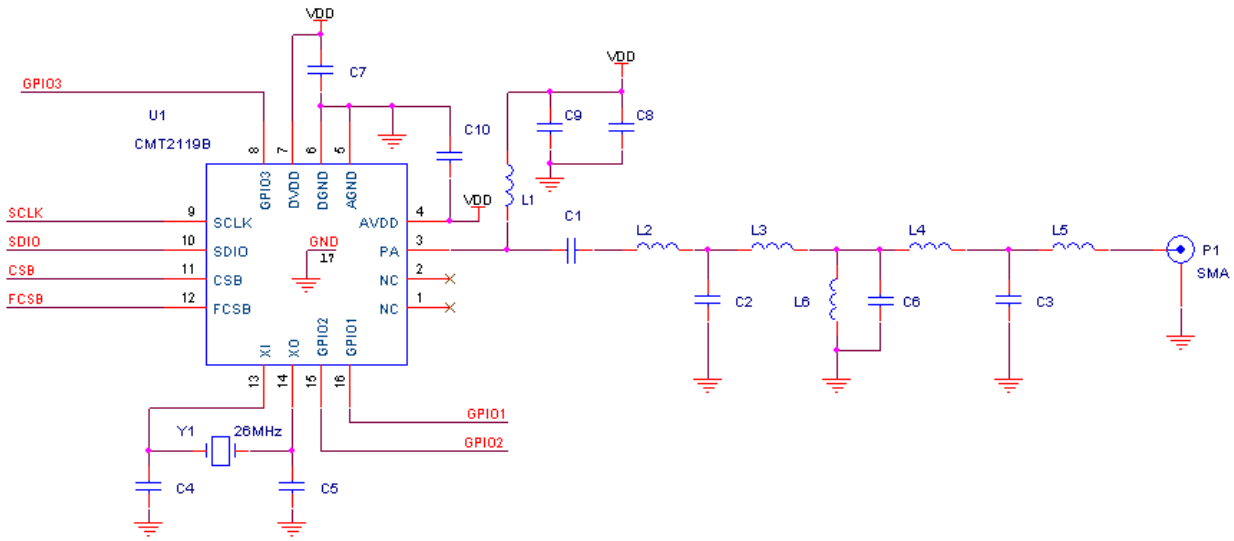


Figure 4. Typical Application Schematic

Table 12. Typical Application BOM

Label	Description	Component Value			Unit	Supplier
		433 MHz +20 dBm	868 MHz +20 dBm	915 MHz +20 dBm		
C1	±5%, 0603 NP0, 50 V	15	18	18	_	-
C2	±5%, 0603 NP0, 50 V	3	3.6	3.6	pF	-
C3	±5%, 0603 NP0, 50 V	6.2	3.3	3.3	pF	-
C4	±5%, 0603 NP0, 50 V	27	27	27	pF	-
C5	±5%, 0603 NP0, 50 V	27	27	27	pF	-
C6	±5%, 0603 NP0, 50 V	4.7	2	1.8	pF	-
C7	±5%, 0603 NP0, 50 V	0.1			uF	-
C8	±5%, 0603 NP0, 50 V	4.7			uF	-
C9	±5%, 0603 NP0, 50 V	470			pF	-
C10	±5%, 0603 NP0, 50 V	0.1			uF	-
L1	±5%, 0603 multilayer chip inductor	180	100	100	nH	Sunlord SDCL
L2	±5%, 0603 multilayer chip inductor,	22	12	12	nH	Sunlord SDCL
L3	±5%, 0603 multilayer chip inductor	15	15	15	nH	Sunlord SDCL
L4	±5%, 0603 multilayer chip inductor	33	6.2	6.2	nH	Sunlord SDCL
L5	±5%, 0603 multilayer chip inductor	33	6.2	6.2	nH	Sunlord SDCL
L6	±5%, 0603 multilayer chip inductor	27	15	15	nH	Sunlord SDCL
Y1	±10 ppm, SMD32*25 mm	26			MHz	EPSON
U1	CMT2119B, +20 dBm high power Sub-1GHz RF transmitter	-			-	CMOSTEK

4 Function Description

The CMT2119B is a high-performance transmitter suitable for 127 to 1020 MHz applications, which supports OOK, (G)FSK and (G)MSK modulation. The product is part of the CMOSTEK NextGenRF^{TM} product family, which covers a complete product line consisting of transmitters, receivers and transceivers. The internal system block diagram of the CMT2119B is shown in the below figure.

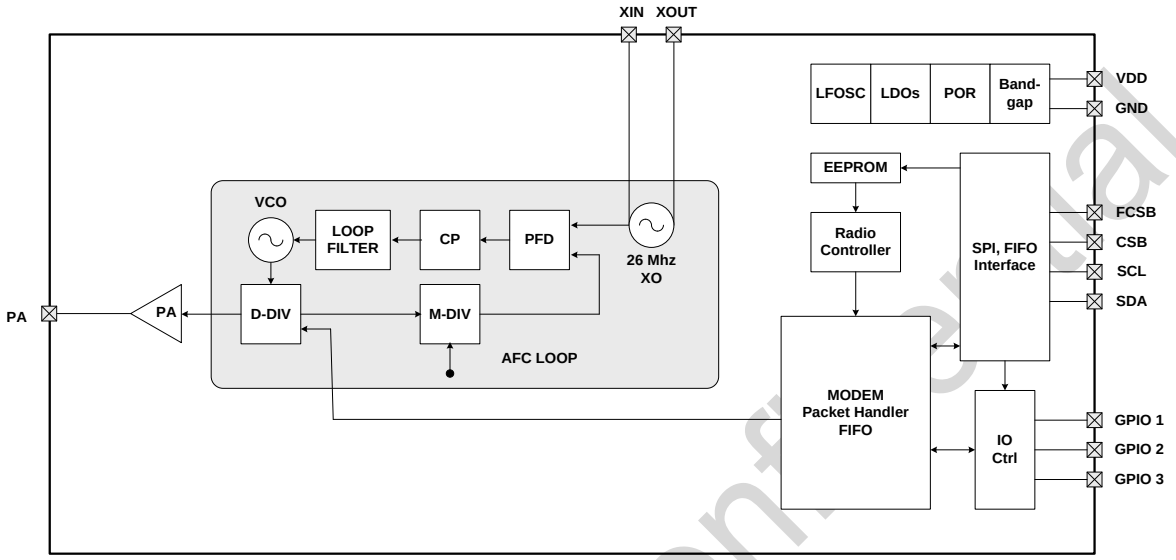


Figure 5. System Function Block Diagram

In the transmitter system, the digital circuit encodes and processes data, and sends the processed data to the modulator (data can also be sent directly to the modulator without encoding and packaging). The modulator directly controls PLL and PA to modulate the data with (G)FSK or OOK modulation then transmit it out.

4.1 Transmitter

The CMT2119B transmitter is synthesized directly based on RF frequencies with its carrier frequency generated by a low noise fractional frequency synthesizer.

The modulated data is transmitted by an efficient single-ended power amplifier (PA). The output power can be read and written from the register and can be configured to values between -10 to + 20 dBm in 1 dB step.

When PA switches quickly, its changed input impedance interferes instantaneously with the output frequency of VCO. This effect becomes a VCO pull that produces spur and glitch near the desired carrier. By slowly ramping the PA output power, it can help reduce the instantaneous glitch of PA to a minimal level. The CMT2119B has a built-in PA slow-and-drop mechanism. When the PA Ramp is turned on, the PA output power can be slowly increased and decreased at the set rate to reduce the unexpected spectral components.

Users can design a PA matching network to optimize the transmission efficiency at the required output power according to application requirements. Please refer to *Typical ApplicationSschematics* and *Typical Application BOM* in Section 3 for details. For more application schematic details and layout guidelines, please refer to *AN168 CMT2119B Schematic and PCB Layout Design Guide*.

The transmitter can operate in both direct mode and packet mode. In the direct mode, the data to be transmitted is sent to the chip directly through the DIN pin of the chip and transmitted directly. In the packet mode, data can be preloaded into the FIFO of the chip in STBY, TFS, and Tx states, and then transmitted out along with other packet elements.

4.2 Assisting Modules

4.2.1 Crystal Oscillator

The crystal oscillator provides a reference clock for the phase locked loop as well as a system clock for digital circuits. The value of load capacitance depends on the crystal specified CL parameter. The total load capacitance between XI and XO should be equal to CL, so as to make the crystal accurately oscillate at 26 MHz.

$$C_L = \frac{1}{1/C11 + 1/C12} + C_{par} + 2.5pF$$

C15 and C16 are the load capacitances placed at both ends of the crystal. Cpar is the parasitic capacitance on the PCB. Each crystal pin has 5 pF internal parasitic capacitance with a equivalent differential capacitance as 2.5 pF. The equivalent series resistance of the crystal must be within the specifications so that the crystal can have a reliable oscillation. Also, an external signal source can be connected to the XI pin to replace the conventional crystal. The recommended peak value of this clock signal is from 300 mV to 700 mV. In addition, the clock is coupled to the XI pin via a capacitor.

4.2.2 Sleep Timer

The CMT2119B integrates a sleep timer driven by 32 kHz low power oscillator (LPOSC). When this function is enabled, the timer wakes up the chip from sleep periodically. When the chip operates in the duty-cycle mode, the sleep time can be configured as a value between 0.03125 ms and 41922560 ms. Due to the low power oscillator frequency will change with the temperature and voltage drift, it will be calibrated automatically during power-on and will be calibrated periodically since then. These calibrations will make the frequency tolerance of the oscillator within + 1%.

4.2.3 Low Battery Detection

The chip supports low battery detection settings. The LBD test is performed once the chip is tuned to a certain frequency. Frequency tuning occurs when the chip switches from the SLEEP/STBY state to the RFS/TFS/TX/RX state. The test result can be read through the LBD_VALUE register.

If LBD_STOP_EN is set to 1, when the detected power supply voltage is lower than the preset value, the chip will stop at LOW_VDD (CHIP_MODE_STA<3:0> = 1000, Addr=0x61), waiting for the MCU sending the command to the chip via SPI then to switch to SLEEP or Standby. .

4.2.4 Fast Frequency Hopping

In applications requiring multiple channels, users only need to configure a register on the base frequency with no need for complex register configuration upon each frequency change,.

$$\mathbf{FREQ} = \mathbf{base\ frequency} + \mathbf{2.5\ kHz} \times \mathbf{FH\_OFFSET} < 7:0 > \times \boldsymbol{FH\_CHANNEL} < 7:0 >$$

In general, users can configure FH_OFFSET<7:0> during the chip initialization process, then perform channel switching by changing FH_CHANNEL<7:0> in the application.

5 Chip Operation

5.1 SPI Interface

The chip communicates with outside through a 4-wire SPI interface. CSB is the active-low signal for accessing chip registers. FCSB is the active-low signal for accessing FIFO. They cannot be set to low at the same time. SCLK is a serial clock with a highest speed of 5 MHz..The chip itself and the external MCU send the data during the falling edge of SCLK and capture the data during the rising edge of SCLK. The SDA is a bidirectional pin for data input and output. The address and data are transferred starting from the MSB.

When accessing registers, CSB is pulled low. A R/W bit is sent first, followed by a 7-bit register address. After the external MCU pulls down CSB, it must wait for at least half a SCL cycle, and then sends the R/W bit. After the MCU sends out the last falling edge of SCLK, it must wait for at least half a SCLK cycle, and then pulls CSB high.

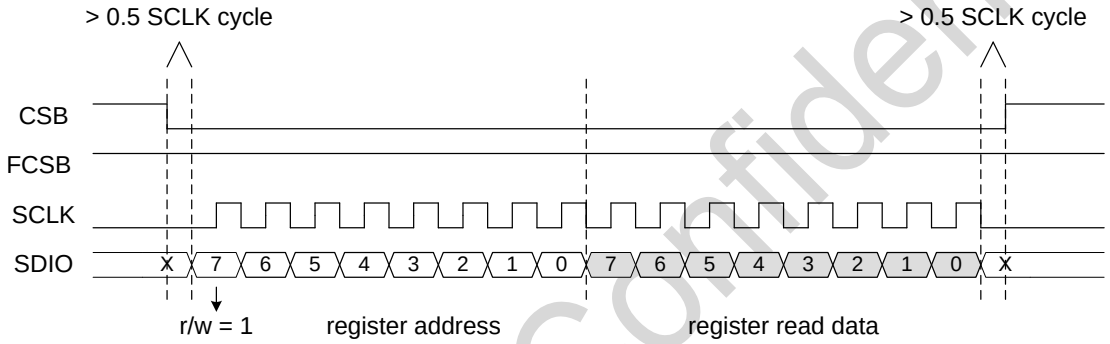


Figure 6. SPI Register Reading Timing

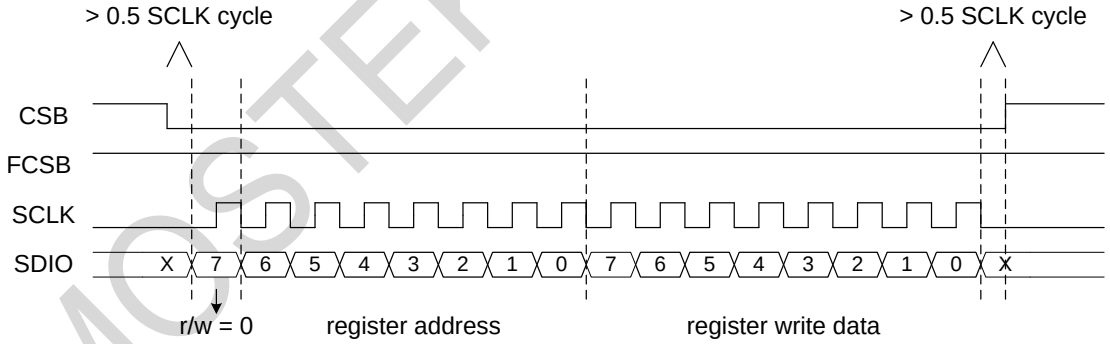


Figure 7. SPI Register Writing Timing

5.2 FIFO

FIFO is used to store the data to be transmitted. The FIFO can be accessed via the SPI interface. Users can clear FIFO by setting FIFO_CLR_TXor FIFO_CLR_RX to 1. Users can re-send the data filled previously by setting FIFO_RESTORE to 1, with no need for re-filling the data.

By setting the register FIFO_MERGE_EN (Addr=0x69), users can choose different FIFO depths , 32 bytes or 64 bytes. When the FIFO is 64-byte, it means that the maximum data that can be stored in the chip is 64 bytes.

5.2.1 FIFO Read Operation

During reading data from the FIFO, the internal read pointer is automatically increased by 1 each time a byte is read. The MCU must pull FCSB low for 1 SCLK cycle to release the first rising edge of SCLK. After sending the last SCLK falling edge, the MCU must wait at least 2 us then pulls back the FCSB to high. In addition, the FCSB needs to be pulled to high for at least 4 us before reading the next byte of the FIFO, which allows the chip to generate corresponding FIFO interrupts based on the current situation.

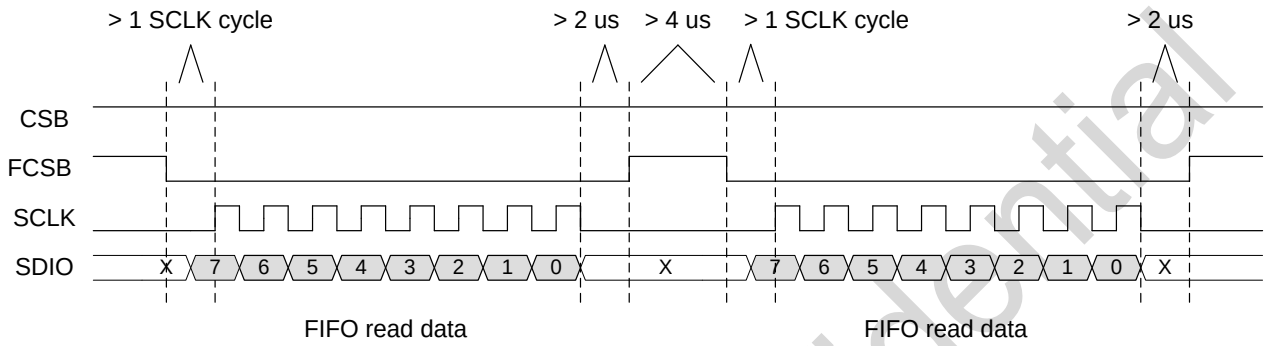


Figure 8. SPI FIFO Reading Timing

5.2.2 FIFO Write Operation

During writing to the FIFO, the internal reading pointer is automatically increased by 1 each time a byte is written. The data on SDIO is collected on the rising edge of SCLK. The MCU must pull FCSB low for 1 SCLK cycle to release the first rising edge of SCLK. After sending the last SCLK falling edge, the MCU must wait at least 2 us to pull back FCSB high. In addition, FCSB needs to be pulled high for at least 4 us before writing the next byte to the FIFO, which allows the chip to generate corresponding FIFO interrupts based on the current situation.

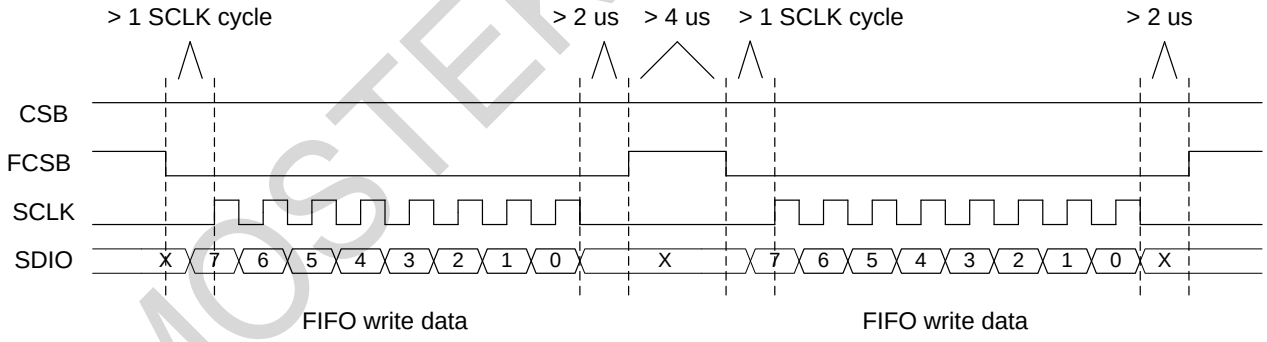


Figure 9. SPI FIFO Writing Timing

5.2.3 FIFO Associated Interrupt

CMT2119B provides rich interrupt sources associated with the FIFO. The interrupt timing for the Tx FIFO is shown in the below figure.

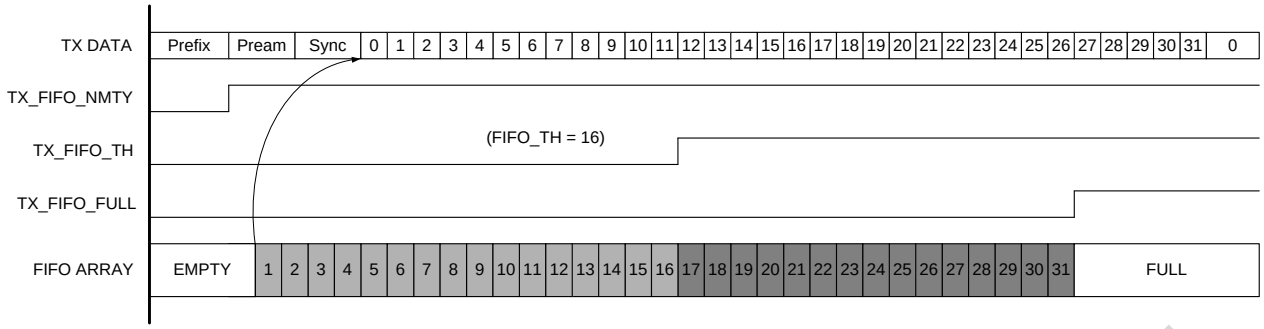


Figure 10. TX FIFO Interrupt Timing Diagram

5.3 Operating State, Timing and Power Consumption

5.3.1 Startup Timing

After chip power up, it usually needs to wait about 1 ms to let POR be released. The crystal will start after then with a default startup time of N ms (N is depends on the characteristics of the crystal itself). After crystal starting, it needs to wait for the crystal being settled, then the system starts operating. The default settling time is 2.48 ms. This time can be modified by writing XTAL_STB_TIME <2:0> afterward. The chip remains in the IDLE status until the crystal is settled. After then, the chip will leave the IDLE state and begin to perform the calibration of each module. When the calibration completes, the chip will stay in the SLEEP and wait until users perform initialization configuration. Whenever the soft reset is performed, the chip will go back to the IDLE and be powered up again.

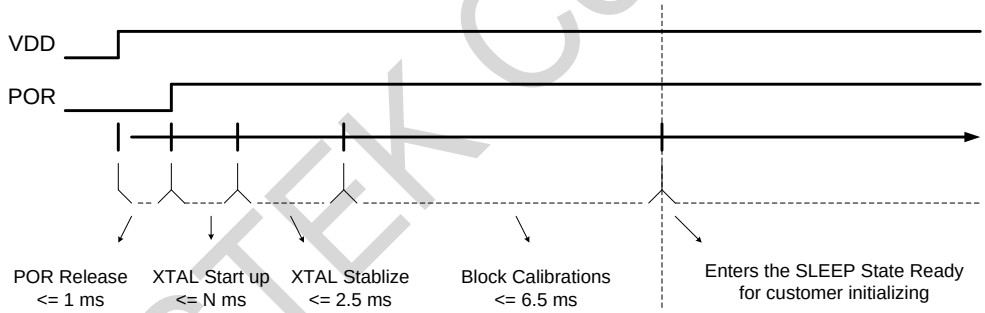


Figure 11. Power-up Timing

When the calibration completes, the chip enters the SLEEP mode. From now on, the MCU can switch the chip to different operating states by setting the register CHIP_MODE_SWT<7:0>.

5.3.2 Operating State

The CMT2119B supports 5 operating states: IDLE, SLEEP, STBY, TFS and TX, as listed in the below table.

Table 13. CMT2119B Operating State and Corresponding Modules On

State	Binary Code	Switching Command	Modules On	Optional Modules On
IDLE	0000	soft_rst	SPI, POR	None
SLEEP	0001	go_sleep	SPI, POR, FIFO	LFOSC, Sleep Timer
STBY	0010	go_stby	SPI, POR, XTAL, FIFO	CLKO
TFS	0100	go_tfs	SPI, POR, XTAL, PLL, FIFO	CLKO
TX	0110	go_tx	SPI, POR, XTAL, PLL, PA, FIFO	CLKO

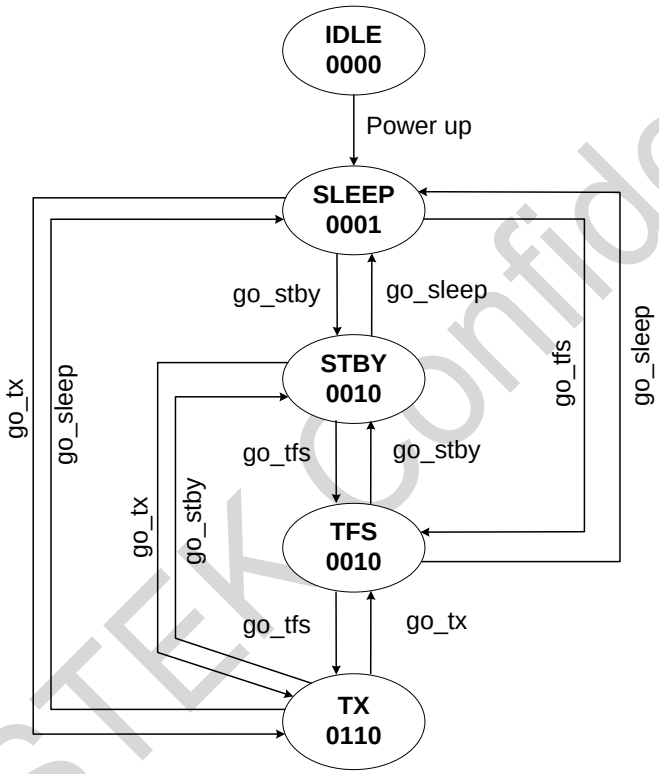


Figure 12. State Transition Diagram

■ SLEEP state

The chip power consumption remains the lowest in SLEEP state with almost all the modules off. SPI is on and the registers of the configuration bank and control bank 1 can be accessed. The contents filled in the FIFO before will remain unchanged. However, users cannot operate the FIFO. If users enable the wake-up function, LFOSC and the sleep counter will be turned on and start operating. The time required to switch from IDLE to SLEEP is the power-up time. Switching from the other states to SLEEP will be completed immediately.

■ STBY state

In the STBY state, the crystal is turned on, the LDO of the digital circuit will also be turned on, the current will be slightly increased, and the FIFO can be operated. Users can choose whether to output CLKO (system clock) to GPIOn pin. As the crystal and LDO are turned on, compared with the SLEEP, the time switching from the STBY to Tx or Rx will be relatively short. Switching from SLEEP to STBY will be completed after the crystal is turned on and settled. Switching from the other states to STBY will be completed immediately.

■ RFS state

RFS is a transition state before switching to Rx. Except that the receiver RF module is off, all the other modules are turned on, and the current will be larger than that tin STBY. Because PLL is locked in the Rx frequency, RFS cannot switch to Tx. Switching from STBY to RFS probably requires a PLL calibration and stability time of 350 us. Switching from SLEEP to RFS needs to add the crystal start-up and stability time. Switching from the other state to RFS will be completed immediately.

■ Tx State

All modules on the transmitter will be turned on in the Tx state. Switching from TFS to Tx requires only 20 us. Switching from STBY to Tx requires to add the PLL calibration and settling time of 350 us. Switching from SLEEP to Tx needs to add the crystal start-up and settling time.

5.4 GPIO and Interrupt

CMT2119B has 3 GPIO ports. Each GPIO can be configured as a different input or output. The CMT2119B has 2 interrupt ports. They can be configured as different GPIO outputs.

Table 14. CMT2119B GPIO

Pin #	Name	I/O	Function
16	GPIO1	IO	Configure as: DIN，INT1，INT2，DCLK (TX)
15	GPIO2	IO	Configure as: INT1，INT2，DCLK (TX)
8	GPIO3	IO	Configure as: CLKO，INT2，DCLK (TX)

Interrupt mapping table is as below. INT1 and INT2 mapping is the same. It takes INT1 as an example in the below table..

Table 15. CMT2119B Interrupt Mapping Table

Name	INT1_SEL	Descriptions	Clearing Methods
TX_ACTIVE	00001	Indicates the chip is entering TX and is already in TX. It is 1 in PLL tuning	Auto
RX_TMO	01001	Indicates that the RX counter timed out.	by MCU
TX_DONE	01010	Indicates that the TX operation is completed.	by MCU
TX_FIFO_NMTY	10000	Indicates that the TX FIFO is not empty.	Auto
RX_FIFO_TH	10001	Indicates the number of unread bytes of the TX FIFO is over FIFO	Auto
RX_FIFO_FULL	10010	Indicates TX FIFO is full.	Auto
STATE_IS_STBY	10011	Indicates that the current state is STBY.	Auto
STATE_IS_FS	10100	Indicates that the current state is RFS or TFS.	Auto
STATE_IS_RX	10101	Indicates that the current state is RX.	Auto
STATE_IS_TX	10110	Indicates that the current state is TX.	Auto
LBD	10111	Indicates that low battery is detected (VDD is lower than TH)	Auto

By default, an Interrupt is active high (logic 1 is valid). Users can set the INT_POLAR register bit to 1 to make all interrupts active low (logic 0 is valid). The control and selection of all the available interrupt sources is shown in the below figure (take INT1 as an example.). The control and mapping of INT1 and INT2 is the same.

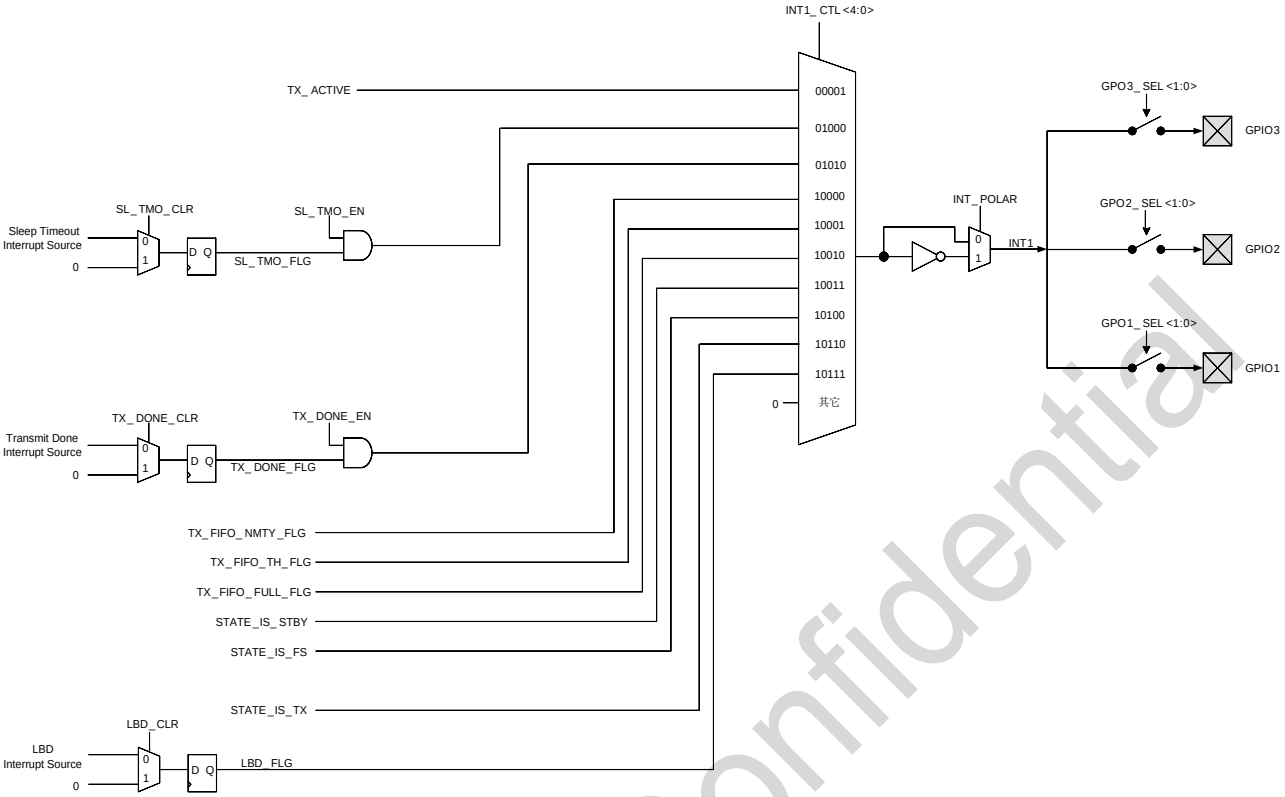


Figure 13. CMT2119B INT1 Interrupt Mapping Diagram

6 Packet Handler

6.1 Packet Format

The CMT2119B provides typical and flexible packet formats including variable packet with Length in front of Node ID, variable packet with Length behind Node ID and fixed packet. The 3 packet formats are shown in the below figures.

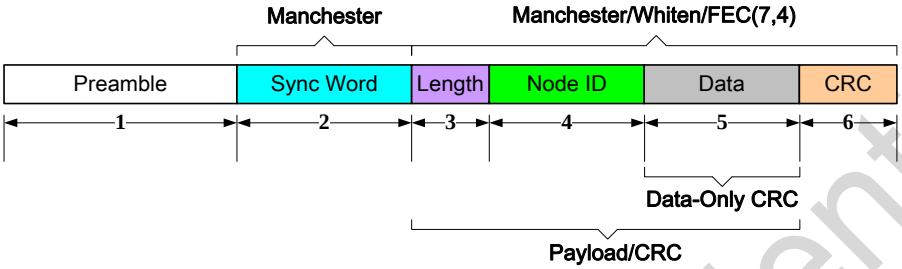


Figure 14. Variable Packet with Length in front of Node ID

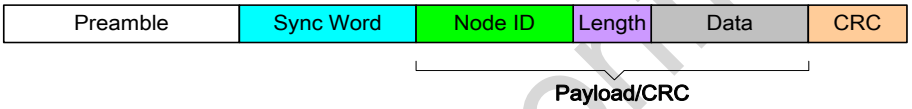


Figure 15. Variable Packet with Length behind Node ID

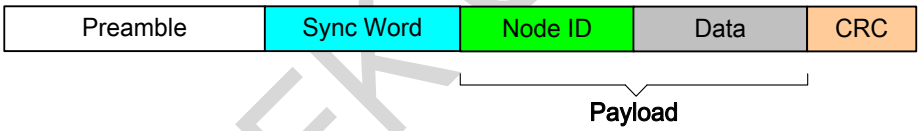


Figure 16. Fixed Packet

6.2 Data Mode

The CMT2119B supports direct mode and packet mode:

Data Mode refers to how the external MCU inputs transmitted data. The CMT2119B supports both the direct mode and the packet mode. The difference is as follows.

- Direct mode - in the direct mode, FIFO does not operate
- Packet mode – in the packet mode, it supports all the packet formats with FIFO operating.

6.2.1 Direct Mode

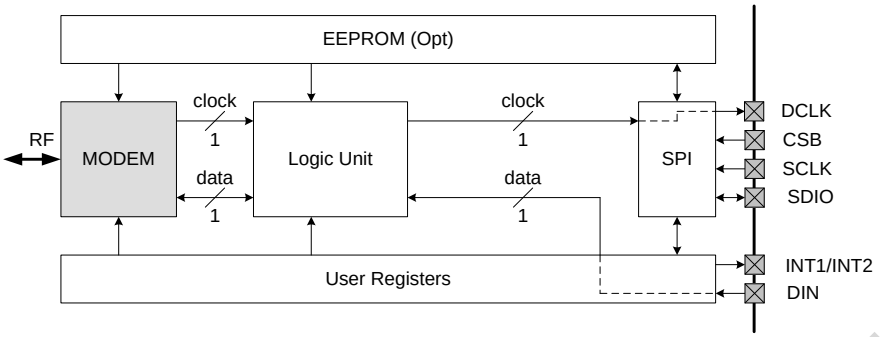


Figure 17. Direct Mode Data Path

In the direct mode, the data to be transmitted is sent directly to the chip from the external MCU via DIN pin. The MCU can specify data rates in the range of chip specification. If the GFSK modulation is used, the data rate of the chip needs to be configured in advance, and the data rate transmitted by the MCU should be within the specified tolerance range. The typical Tx operating flow in the direct mode is as follows.

1. Drive DIN (namely the GPIO1 pin) with logic 0 or 1 (the system uses GPIO1 pin as DIN pin by default. In fact, only the GPIO1 pin has DIN function. Keep register value of TX_DIN_EN and TX_DIN_SEL (Addr=0x69) as 0 by default.).
2. Send go_tx command, then the chip starts sending data of DIN pin.
3. Keep sending data to the DIN pin and the data is being transmitted immediately.
4. Send go_sleep/go_stby/go_rfs command to stop receiving for power saving.

6.2.2 Packet Mode

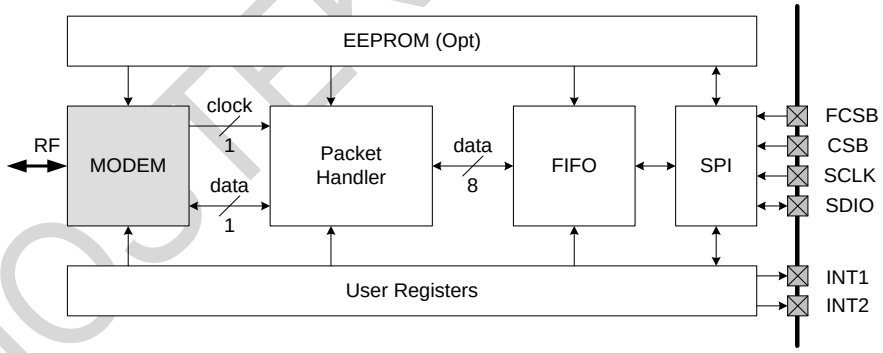


Figure 18. Packet Mode Data Path

In the packet mode, the MCU can fill the data in FIFO in advance in the STBY and TFS state, or fill them in FIFO while thechip sends the data, or use the combination of the above two methods. The typical Tx packet mode operating flow is as follows.

1. Configure GPIO using the CUS_IO_SEL (Addr=0x65) register.
2. Send go_stby/go_tfs command when the data is filled in FIFO in advance.
3. Send go_tx command.
4. Write the data into FIFO according to the relevant interrupt status.
5. Sends go_sleep/go_stby/go_rfs command to save power.

7 Automatic Operating Mode

The CMT2119B saves chip power by controlling the Tx function to run in the automatic operating mode through configuring relevant registers. It include 3 modes.

1. Automatically exit Tx

2. Automatically wake up from SLEEP and automatically exit Tx

3. Fully automatic Tx

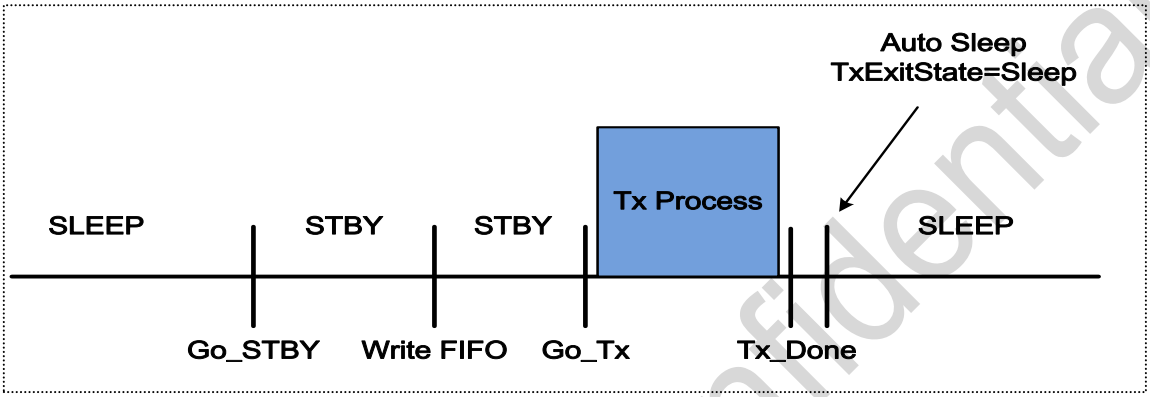


Figure 19. Automatically Exit Tx

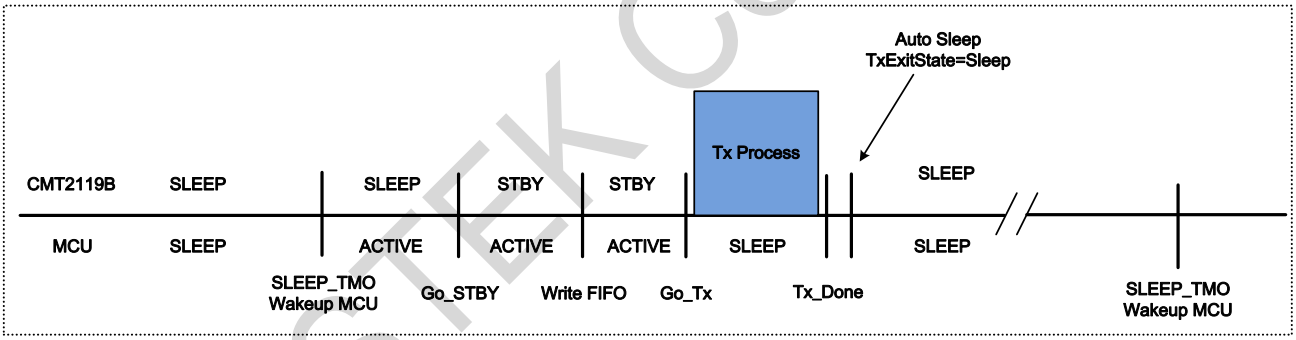


Figure 20. Automatically Wakeup from Sleep to Tx and Exit Tx Automatically

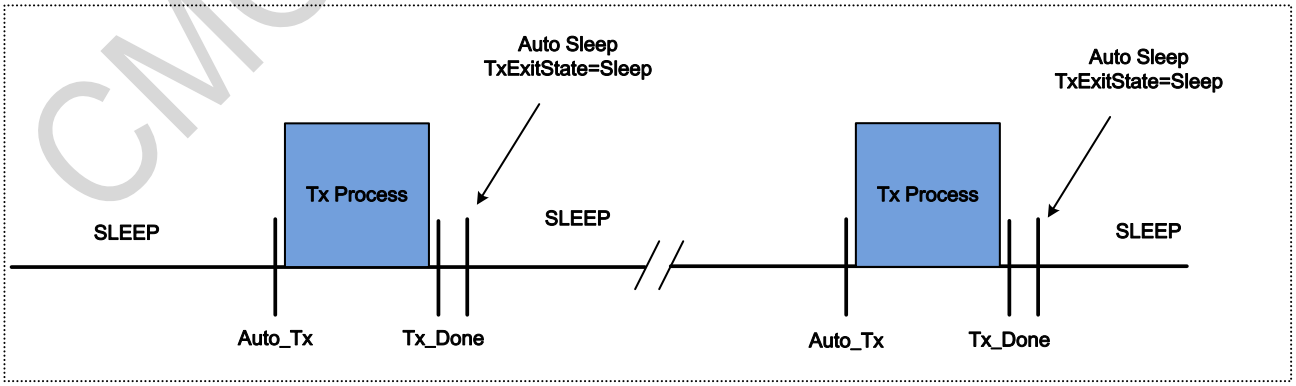


Figure 21. Fully Automatic Tx - fill data to be transmitted in advance and sends the same data each time

8 User Registers

User registers are listed in the below table. Please refer to *AN167 CMT2119B Quick Start Guide* for more register details. All register banks can be accessed in the SLEEP state except for control bank 2.

Table 16. Register Bank Partitioning

Address	Bank Name		Bank Name in RFPDK Export File	Function
0x00-0x0B	Configuration bank (RFPDK exports the register values）	CMT bank	CMT bank	Export through RFPDK. Not suggest users to change them.
0x0C-0x17		System bank	System bank	Mainly for Duty-Cycle operating configuration.
0x18-0x1F		Frequency bank	Frequency bank	Mainly for Tx frequency configuration.
0x20-0x37		Data rate bank	Data rate bank	Mainly related to communication data rate.
0x38-0x54		Baseband bank	Baseband bank	Mainly related to packet formats (encoding format, packet structure checksum, error correction, sync word, etc.).
0x55-0x5F		TX bank	TX bank	Mainly related to Tx deviation and power.
0x60-0x6A	Control bank 1 (set by MCU in application, not generated by RFPDK)		-	Mainly related to chip operating state, frequency hopping, GPIOs and interrupt source on/off control.
0x6B-0x71	Control bank 2 (set by MCU in application, not generated by RFPDK)		-	Mainly for interrupt source flags and RSSI value.

8.1 CMT Bank

The CMT bank mainly stores product-related information and functional registers as well as some registers used by the chip internally.

Table 17. CMT Bank

Addr	R/W	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	RW	CUS_CMT1	Users do not need to understand them. They can be imported from RFPDK generated data.							
0x01	RW	CUS_CMT2								
0x02	RW	CUS_CMT3								
0x03	RW	CUS_CMT4								
0x04	RW	CUS_CMT5								
0x05	RW	CUS_CMT6								
0x06	RW	CUS_CMT7								
0x07	RW	CUS_CMT8								
0x08	RW	CUS_CMT9								
0x09	RW	CUS_CMT10								
0x0A	RW	CUS_CMT11								
0x0B	RW	CUS_RSSI								

8.2 System Bank

The system bank mainly configures timer-related parameters to implement the duty cycle mode.

Table 18. System Bank

Addr	R/W	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0C	RW	CUS_SYS1	RESV							
0x0D	RW	CUS_SYS2	LFOSC_RECAL_EN	LFOSC_CAL1_EN	LFOSC_CAL2_EN	0	SLEEP_TIMER_EN	TX_DC_EN	0	DC_PAUSE
0x0E	RW	CUS_SYS3	SLEEP_BYPASS_EN	XTAL_STB_TIME [2:0]			TX_EXIT_STATE [1:0]		0	
0x0F	RW	CUS_SYS4	SLEEP_TIMER_M [7:0]							
0x10	RW	CUS_SYS5		SLEEP_TIMER_M [10:8]			SLEEP_TIMER_R [3:0]			
0x11	RW	CUS_SYS6	RESV							
0x12	RW	CUS_SYS7	RESV							
0x13	RW	CUS_SYS8	RESV							
0x14	RW	CUS_SYS9	RESV							
0x15	RW	CUS_SYS10	RESV							
0x16	RW	CUS_SYS11	RESV							
0x17	RW	CUS_SYS12	RESV		CLKOUT_EN	CLKOUT_DIV [4:0]				

8.3 Frequency Bank

The frequency bank mainly stores registers implementing the frequency tuning function.

Table 19. Frequency Bank

Addr	R/W	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x18	RW	CUS_RF1	Users do not need to understand them. They can be imported from RFPDK generated data.							
0x19	RW	CUS_RF2								
0x1A	RW	CUS_RF3								
0x1B	RW	CUS_RF4								
0x1C	RW	CUS_RF5								
0x1D	RW	CUS_RF6								
0x1E	RW	CUS_RF7								
0x1F	RW	CUS_RF8								

8.4 Data Rate Bank

The data rate bank stores registers related to data rate, FSK and OOK.

Table 20. Data Rate Bank

Addr	R/W	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x20	RW	CUS_RF9	Users do not need to understand them. They can be imported from RFPDK generated data.							
0x21	RW	CUS_RF10								
0x22	RW	CUS_RF11								
0x23	RW	CUS_RF12								
0x24	RW	CUS_FSK1								
0x25	RW	CUS_FSK2								
0x26	RW	CUS_FSK3								
0x27	RW	CUS_FSK4								
0x28	RW	CUS_FSK5								
0x29	RW	CUS_FSK6								
0x2A	RW	CUS_FSK7								
0x2B	RW	CUS_CDR1								
0x2C	RW	CUS_CDR2								
0x2D	RW	CUS_CDR3								
0x2E	RW	CUS_CDR4								
0x2F	RW	CUS_AGC1								
0x30	RW	CUS_AGC2								
0x31	RW	CUS_AGC3								
0x32	RW	CUS_AGC4								
0x33	RW	CUS_OOK1								
0x34	RW	CUS_OOK2								
0x35	RW	CUS_OOK3								
0x36	RW	CUS_OOK4								
0x37	RW	CUS_OOK5								

8.5 Baseband Bank

The baseband bank stores registers related to packet format settings.

Table 21. Baseband Bank

Addr	R/W	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x38	RW	CUS_PKT1	RESV					PREAM_LENG_UNIT	DATA_MODE [1:0]	
0x39	RW	CUS_PKT2	TX_PREAM_SIZE [7:0]							
0x3A	RW	CUS_PKT3	TX_PREAM_SIZE [15:8]							
0x3B	RW	CUS_PKT4	PREAM_VALUE [7:0]							
0x3C	RW	CUS_PKT5	RESV	SYNC_TOL [2:0]			SYNC_SIZE [2:0]			SYNC_MAN_EN
0x3D	RW	CUS_PKT6	SYNC_VALUE [7:0]							
0x3E	RW	CUS_PKT7	SYNC_VALUE [15:8]							
0x3F	RW	CUS_PKT8	SYNC_VALUE [23:16]							
0x40	RW	CUS_PKT9	SYNC_VALUE [31:24]							
0x41	RW	CUS_PKT10	SYNC_VALUE [39:32]							
0x42	RW	CUS_PKT11	SYNC_VALUE [47:40]							
0x43	RW	CUS_PKT12	SYNC_VALUE [55:48]							
0x44	RW	CUS_PKT13	SYNC_VALUE [63:56]							
0x45	RW	CUS_PKT14	RESV	PAYLOAD_LENG [10:8]			AUTO_ACK_EN	NODE_LENG_POS_SEL	PAYLOAD_BIT_ORDER	PKT_TYPE
0x46	RW	CUS_PKT15	PAYLOAD_LENG [7:0]							
0x47	RW	CUS_PKT16	RESV	RESV	NODE_FREE_EN	NODE_ERR_MASK	NODE_SIZE [1:0]		NODE_DET_MODE [1:0]	
0x48	RW	CUS_PKT17	NODE_VALUE [7:0]							
0x49	RW	CUS_PKT18	NODE_VALUE [15:8]							
0x4A	RW	CUS_PKT19	NODE_VALUE [23:16]							
0x4B	RW	CUS_PKT20	NODE_VALUE [31:24]							
0x4C	RW	CUS_PKT21	FEC_TYPE	FEC_EN	CRC_BYTE_SWAP	CRC_BIT_INV	CRC_RANGE	CRC_TYPE [1:0]		CRC_EN
0x4D	RW	CUS_PKT22	CRC_SEED [7:0]							
0x4E	RW	CUS_PKT23	CRC_SEED [15:8]							
0x4F	RW	CUS_PKT24	CRC_BIT_ORDER	WHITEN_SEED [8]	WHITEN_SEED_TYPE	WHITEN_TYPE [1:0]		WHITEN_EN	MANCH_TYPE	MANCH_EN
0x50	RW	CUS_PKT25	WHITEN_SEED [7:0]							
0x51	RW	CUS_PKT26	RESV						TX_PREFIX_TYPE [1:0]	
0x52	RW	CUS_PKT27	TX_PKT_NUM [7:0]							
0x53	RW	CUS_PKT28	TX_PKT_GAP [7:0]							
0x54	RW	CUS_PKT29	FIFO_AUTO_RES_EN	FIFO_TH [6:0]						

8.6 Tx Bank

The Tx bank stores registers related to transmission power and deviation.

Table 22. Tx Bank

Addr	R/W	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x55	RW	CUS_TX1	Users do not need to understand them. They can be imported from RFPDK generated data.							
0x56	RW	CUS_TX2								
0x57	RW	CUS_TX3								
0x58	RW	CUS_TX4								
0x59	RW	CUS_TX5								
0x5A	RW	CUS_TX6								
0x5B	RW	CUS_TX7								
0x5C	RW	CUS_TX8								
0x5D	RW	CUS_TX9								
0x5E	RW	CUS_TX10								
0x5F	RW	CUS_LBD								

8.7 Control Bank 1

The control 1 bank stores registers for various function modules enabling and function selection.

Table 23. Control Bank 1

Addr	R/W	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x60	RW	CUS_MODE_CTL	CHIP_MODE_SWT [7:0]							
0x61	RW	CUS_MODE_STA	RESV	RESV	RSTN_IN_EN	CFG_RETAIN	CHIP_MODE_STA [3:0]			
0x62	RW	CUS_EN_CTL	RESV	RESV	UNLOCK_STOP_EN	LBD_STOP_EN	RESV	RESV	RESV	RESV
0x63	RW	CUS_FREQ_CHNL	FH_CHANNEL [7:0]							
0x64	RW	CUS_FREQ_OFS	FH_OFFSET [7:0]							
0x65	RW	CUS_IO_SEL	GPIO4_SEL [1:0]		GPIO3_SEL [1:0]		GPIO2_SEL [1:0]		GPIO1_SEL [1:0]	
0x66	RW	CUS_INT1_CTL	RF_SWT1_EN	RF_SWT2_EN	INT_POLAR	INT3_SEL [4:0]				
0x67	RW	CUS_INT2_CTL	RESV	LFOSC_OUT_EN	TX_DIN_INV	INT2_SEL [4:0]				
0x68	RW	CUS_INT_EN	SL_TMO_EN	0	TX_DONE_EN	0	0	0	0	0
0x69	RW	CUS_FIFO_CTL	TX_DIN_EN	TX_DIN_SEL [1:0]		FIFO_AUTO_CLR_DIS	FIFO_TX_RD_EN	1	FIFO_MERGE_EN	SPI_FIFO_RD_WR_SEL
0x6A	W	CUS_INT_CLR1	RESV	RESV	SL_TMO_FLG	RESV	TX_DONE_FLG	TX_DONE_CLR	SL_TMO_CLR	RESV

8.8 Control Bank 2

The control area 2 stores the registers related to flag bits, RSSI and LBD. Note that registers in this bank cannot be accessed in the SLEEP state.

Table 24. Control Bank 2

Addr	R/W	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x6B	W	CUS_INT_CLR2	RESV	RESV	LBD_CLR	RESV				
0x6C	W	CUS_FIFO_CLR						FIFO_RESTORE	0	FIFO_CLR_TX
0x6D	R	CUS_INT_FLAG	LBD_FLG	RESV						
0x6E	R	CUS_FIFO_FLAG	RESV					TX_FIFO_FULL_FLG	TX_FIFO_NMTY_FLG	TX_FIFO_TH_FLG
0x6F	R	CUS_RSSI_CODE	RESV							
0x70	R	CUS_RSSI_DBM	RESV							
0x71	R	CUS_LBD_RESULT	LBD_RESULT [7:0]							

9 Ordering Information

Table 25. CMT2119B Ordering Information

Model	Description	Packaging	Packaging Option	Operating Condition	Minimum Order Quantity
CMT2119B-EQR[1]	The CMT2119B, ultra-low power sub-1 GHz RF transmitter	QFN16 (3x3)	Tape and tray	1.8 to 3.6 V, - 40 to 85 °C	3,000

Notes:

[1]. E refers to extended Industrial product rating, which supports temperature range from -40 to +85 °C.

Q refers to the package type QFN16.

R refers to tape and tray type, and the minimum order quantity (MOQ) is 3,000 pieces.

Please visit www.cmostek.com for more product/product line information.

Please contact sales@cmostek.comor your local sales representative for sales or pricing requirements.

10 Packaging Information

The packaging information of the CMT2119B is shown in the below figure.

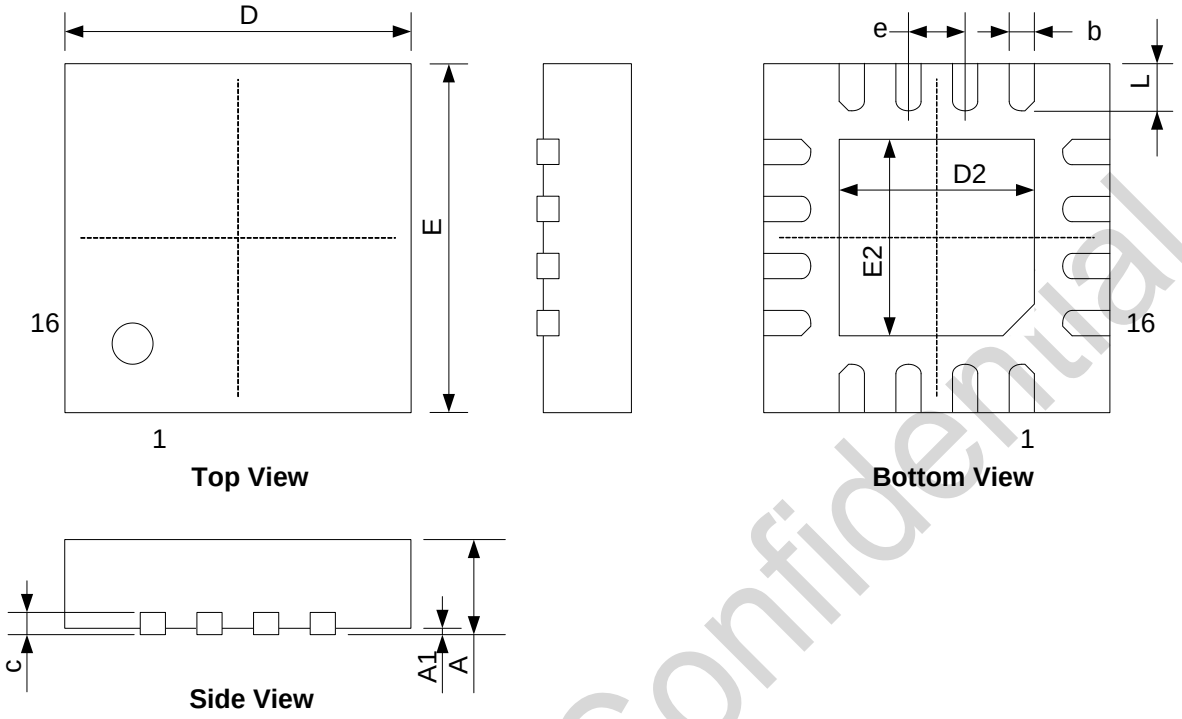


Figure 22. 16-Pin QFN 3x3 Packaging

Table 26. 16-Pin QFN 3x3 Packaging Scale

Symbol	Scale (mm)	
	Min.	Max.
A	0.7	0.8
A1	—	0.05
b	0.18	0.30
c	0.18	0.25
D	2.90	3.10
D2	1.55	1.75
e	0.50 BSC	
E	2.90	3.10
E2	1.55	1.75
L	0.35	0.45

11 Top Marking

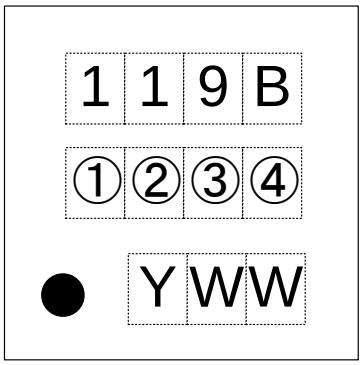


Figure 23. The CMT2119B Top Marking

Table 27. The CMT2119B Top Marking Information

Marking Method	Laser
Pin 1 Mark	Diameter of the circle = 0.3 mm
Font Size	0.5 mm, align right
Line 1 Marking	119B refers to model CMT2119B
Line 2 Marking	①②③④ is internal tracing code
Line 3 Marking	The date code is assigned by the package factory. Y is the last digit of the year. WW is the working week.

12 Related Documents

Table 28. Related Documents

Doc No.	Doc Name	Description
AN167	CMT2119B Quick Start Guide	Help users to understand and operate the CMT2119B
AN168	CMT2119B Schematic and PCB Layout Design Guide	Discuss CMT2119B PCB schematic and layout design rules and RF matching network & other layout design related design considerations

13 Revise History

Table 29. Revise History Records

Version No.	Chapter	Description	Date
Initial version	All	Initial version	2017-09-07
0.5	2, 5.4	Modify GPIO x pin description in table 11 and Table 14, remove the information for GPIO2 and GPIO3 multiplexing as DIN function. When the CMT2119B is used in direct mode, the external modulated data can only be input from the GPIO1 pin	2018-11-30

14 Contacts

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