CMOSTEK CMT2159A

FSK/OOK Transmitter Targeting for Micro-energy-harvesting

Features

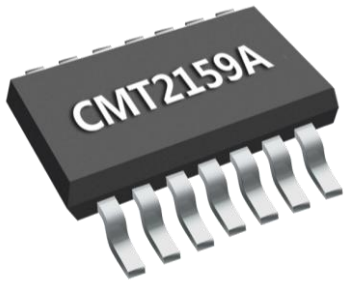
- Built-in EEPROM
  - Easy development through utilizing RFPDK tool
  - Fully configurable functions
- Operating frequency: 240 - 960 MHz
- Modulation mode: GFSK, FSK, OOK
- Symbol rate:
  - 0.5 - 40 ksps (OOK)
  - 0.5 - 300 ksps (FSK)
- Frequency deviation range: 1 - 200 kHz
- Output power: -10 ~ +13 dBm
- Operating current: 8.5 mA @ +10 dBm
- Sleep current: < 20 nA
- Built-in micro-energy-harvesting element, which runs as independent chip with no need for MCU control
- Support 1920, 1527 and 2262 data encoding formats.
- LED display for Tx information.
- Conform to RoHS standard.
- 14 pin SOP packaging.

Application

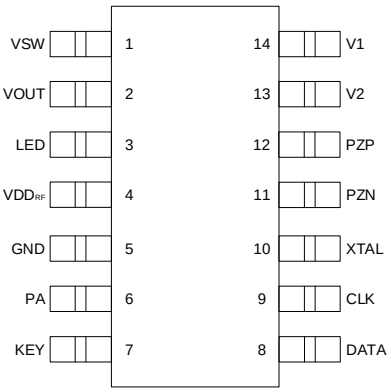
- Self-powered doorbell transmitter
- Self-powered pager transmitter
- Self-powered kinetic switch transmitter

Ordering Information

Product Model	Frequency	Package	Minimum Order Quantity
CMT2159A-ESR	868.35 MHz	SOP14/Tape	2,500 pcs
Please refer to Table 13 for more ordering information.			



SOP14



CMT2159A Pin Arrangement

Description

Built in a high-performance FSK/OOK RF transmitter, the CMT2159A is a transmitter chip targeting for micro-energy-harvesting applications in 240 - 960 MHz frequency range. The encoder integrated in the chip can adapt to the 1527 and 2262 encoding formats that are commonly used in market as well as the 1920 encoding format defined by CMOSTEK™ . All encoding formats supported by the chip and the RF related configurations can be programmed to the chip EEPROM by users via CMOSTEK™ USB Writer and RFPDK software. As part of CMOSTEK NextGenRFTM series product, the CMT2159A co-working with CMT221x series receiving-only receiver can achieve low-cost and environment-friendly battery-free solutions for remote control applications.

Terminology

The terms used in this document are described as follows.

AN	application notes	PA	power amplifier
BOM	bill of materials	PC	personal computer
BSC	basic spacing between centers	PCB	printed circuit board
BW	bandwidth	PLL	phase-locked loop
DC	direct current	PN	phase noise
EEPROM	electrically erasable programmable read-only memory	RBW	resolution bandwidth
ESD	electro-static discharge	RCLK	reference clock
ESR	equivalent series resistance	RF	radio frequency
GUI	graphical user interface	RFPDK	RF product development toolkit
IC	integrated circuit	RoHS	restriction of hazardous substances
LDO	low dropout regulators	RSSI	received signal strength indicator
Max	maximum	Rx	receive, receiver
MCU	micro-controller unit	SOP	small out-line package
Min	minimum	Tx	transmit, transmitter
MOQ	minimum order quantity	Typ	typical
NP0	negative-positive 0 with temperature compensation	XOSC	crystal oscillator
OBW	occupied bandwidth	XTAL/Xtal	crystal
OOK	on-off keying		

Table of Contents

1 Electrical Specifications

The test conditions are that V1= 5 V，TOP= 25 ° C，FRF = 433.92 MHz, out power being +10 dBm and matching to 50 Ω impedance, if nothing else stated. All measurement results are obtained using the evaluation board CMT2159A-EM V1.0 if nothing else stated.

1.1 Recommended Operating Conditions

Table 1. Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating temperature	T_{OP}		-40		85	℃
Supply voltage slope			1			mV/us

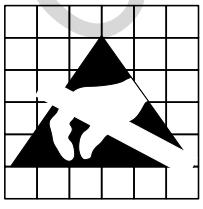
1.2 Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Condition	Min.	Typ.	Max.
AC input voltage	VAC_{IN}	Input from PZN and PZP		6	V
The output voltage	V_{OUT}			2.4	V
Output current	I_{OUT}			150	mA
Interface voltage			-0.3	V_{DD} + 0.3	V
Junction temperature	T_J		-40	125	℃
stored temperature	T_{STG}		-50	150	℃
Welding temperature	T_{SDR}	Lasting for at least 30 s		255	℃
ESD rating [2]		Human body model (HBM)	-2	2	kV
Latch-up current		@ 85 ℃	-100	100	mA

Notes:

[1]. Exceeding *the Absolute Maximum Ratings* may cause permanent damage to the equipment. This value is a pressure rating and does not imply that the function of the equipment is affected under this pressure condition, but if it is exposed to absolute maximum ratings for extended periods of time, it may affect equipment reliability.



Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent performance degradation or loss of functionality.

1.3 Transmitter Specification

Table 3. Transmitter Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency range [1]	F_{RF}		240		960	MHz
Frequency synthesizer resolution	F_{RES}	F_{RF} ≤ 480 MHz		198		Hz
		F_{RF} ≥ 480 MHz		397		Hz
Symbol rate	SR	OOK	0.5		40	ksps
		FSK / GFSK	0.5		300	ksps
FSK modulation frequency deviation	F_{DEV}		1		200	kHz
Time-bandwidth product	BT	GFSK modulation mode	--	0.5	--	--
Max output power	$P_{OUT(Max)}$			+13		dBm
Min output power	$P_{OUT(Min)}$			-10		dBm
Output power step	P_{STEP}			1		dB
PA Ramping time [2]	t_{RAMP}		0		1024	us
Operating current [3] @ 433.92 MHz	$I_{DD-433.92}$	OOK 0 dBm		5.1		mA
		OOK +10 dBm		8.5		mA
		FSK 0 dBm		7.1		mA
		FSK +10 dBm		15.8		mA
Operating current [3] @ 868.35 MHz	$I_{DD-868.35}$	OOK 0 dBm,		5.8		mA
		OOK +10 dBm		9.3		mA
		FSK 0dBm		8.3		mA
		FSK +10 dBm		20.3		mA
Sleep current	I_{SLEEP}			20		nA
Frequency tuning time	t_{TUNE}	From XO stable to ready to transmit, include the frequency calibration		370		us
Phase noise	PN	100 kHz frequency deviation		-80		dBc/Hz
		200 kHz frequency deviation		-81		dBc/Hz
		400 kHz frequency deviation		-91		dBc/Hz
		600 kHz frequency deviation		-96		dBc/Hz
		1.2 MHz frequency deviation		-108		dBc/Hz
315 MHz Harmonic output [4]	$H2_{315}$	2^{nd} harmonic @ 630 MHz, +13 dBm P_{OUT}		-48		dBm
	$H3_{315}$	3^{rd} harmonic @ 945 MHz, +13 dBm P_{OUT}		-60		dBm
433.92 MHz Harmonic output [4]	$H2_{433.92}$	2^{nd} harmonic @ 867.84 MHz, +13 dBm P_{OUT}		-38		dBm
	$H3_{433.92}$	3^{rd} harmonic @ 1301.76 MHz, +13 dBm P_{OUT}		-56		dBm
OOK extinction ratio				60		dB
315 MHz occupied bandwidth	F_{OBW315}	Measured under the condition of -20 dBc, RBW = 1 kHz, SR = 1.2 ksps, t_{RAMP} = 256		6		kHz

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
		us.				
433.92 MHz occupied bandwidth	$F_{OBW433.92}$	Measured under the condition of -20 dBc, RBW = 1 kHz, SR = 1.2 ksps, t_{RAMP} = 256 us.		7		kHz

Notes:

[1]. Frequency is continuous in the specified range.

[2]. 0 and 2^n us (n = 0 ~10). When set to 0, the PA output power will rise/fall to the set value at a speed that is as high as possible.

[3]. The operating current is measured under the condition of: 1527 packet format, normal button mode, 1 button, Sync ID = 0, no LED.

[4]. The harmonic output is measured in the application as shown in Figure 8.

1.4 Crystal Oscillator

Table 4. Crystal Oscillator Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Crystal frequency [1]	F_{XTAL}			26		MHz
Crystal frequency precision [2]				± 20		ppm
Load resistance [3]	C_{LOAD}		10	15	20	pF
Crystal equivalent resistance	Rm				60	Ω
Crystal startup time [3]	t_{XTAL}			400		us

Notes:

[1]. The CMT2159A utilizes external reference clock to directly drive XIN pin through coupling capacitor. The peak-to-peak value of external clock signal is required between 0.3 and 0.7 V.

[2]. It involves:(1) initial tolerance, (2) crystal loading, (3) aging, and (4) temperature changing. The acceptable crystal frequency tolerance is subject to the bandwidth of the receiver and the RF tolerance between the receiver and its paired transmitter.

[3]. The required crystal load capacitor is built in the chip to reduce the amount of external components.

[4]. This parameter is to a large degree crystal dependent.

1.5 DC-DC Specification

Table 5. DC-DC Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
DC input voltage	VDC_{IN}	Input from V1 or V2		5	6	V
Load adjusting percentage				0.5		%
Linearity adjusting percentage				0.5		%
Efficiency	EFFI	PZN or PZP = 4 V		90		%
Quiescent current		PZN or PZP = 4 V		30		uA
Switch oscillator frequency				1		MHz
Max duty ratio				100		%

2 Pin Description

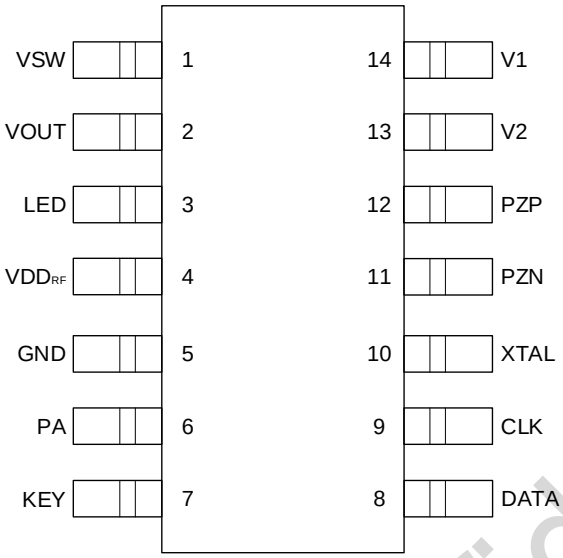


Figure 1. CMT2159A Pin Arrangement

Table 6. CMT2159A Pin Arrangement

Pin #	Pin Name	I/O	Description
1	VSW	O	Internal DC-DC switch control port.
2	VOUT	O	VOUT output end.
3	LED	O	LED driving port, low active.
4	VDD_{RF}	I	Power supply input.
5	GND	I	Ground.
6	PA	O	Power amplifier output.
7	KEY	I	Press key/button.
8	DATA	IO	Data pin for accessing EEPROM, pulling up to VDD internally.
9	CLK	I	Clock pin for accessing EEPROM, pulling up to VDD internally.
10	XTAL	I	26 MHz single-ended crystal oscillator input.
11	PZN	I	Micro-energy AC input end.
12	PZP	I	Micro-energy AC input end.
13	V2	O	Micro-energy DC output 2.
14	V1	O	Micro-energy DC output 1.

3 Typical Performance

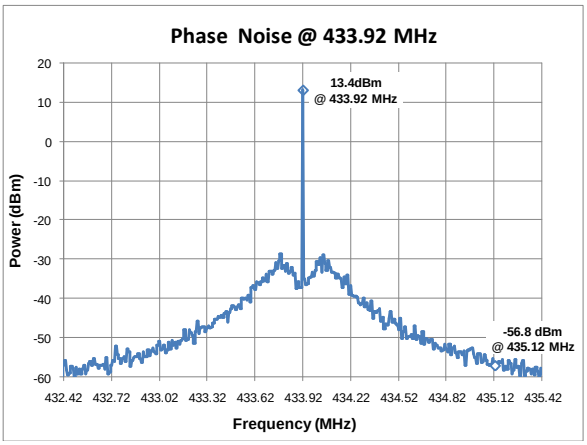


Figure 3. Phase noise, F_{RF} = 433.92 MHz, P_{OUT} = + 13 dBm, RBW = 10 kHz, single carrier

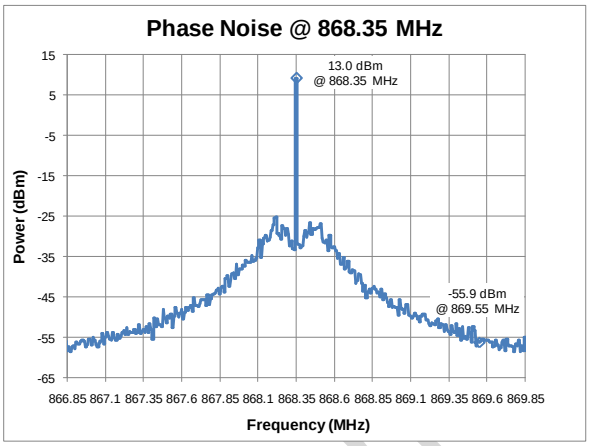


Figure 2. Phase noise, F_{RF} = 868.35 MHz P_{OUT} = + 13 dBm, RBW = 10 kHz, single carrier

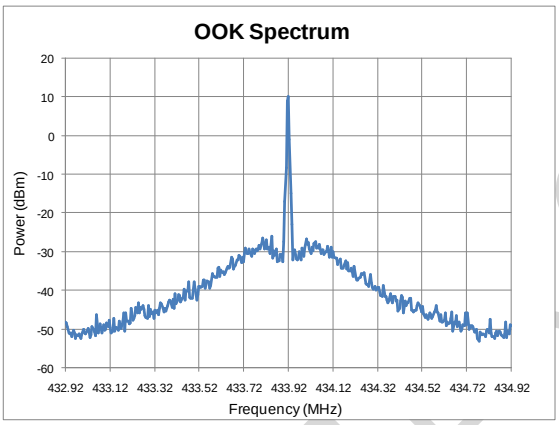


Figure 5. OOK frequency spectrum, P_{OUT} = +10 dBm, t_{RAMP} = 32 us

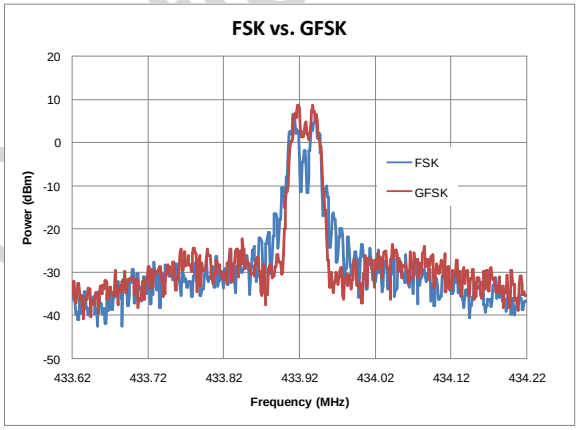


Figure 4.PA Ramping frequency spectrum, DR = 9.6 ksps, P_{OUT} = +10 dBm, F_{DEV} = 15kHz

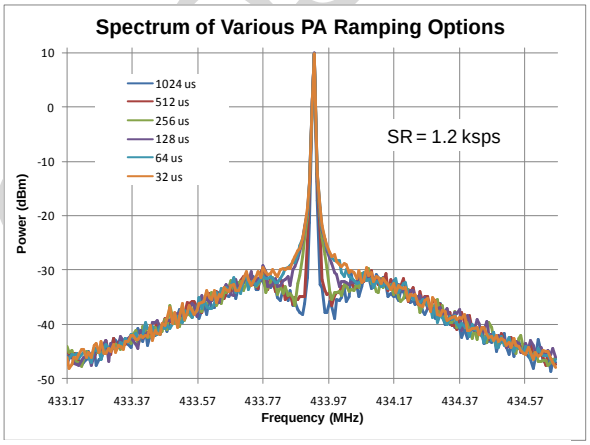


Figure 6. PA Ramping frequency spectrum, SR = 1.2 ksps, P_{OUT} = +10 dBm

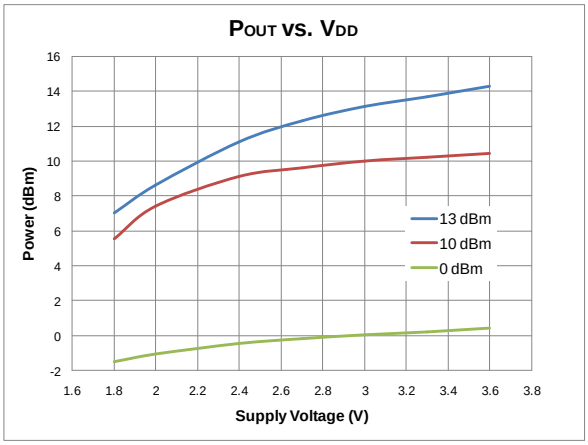
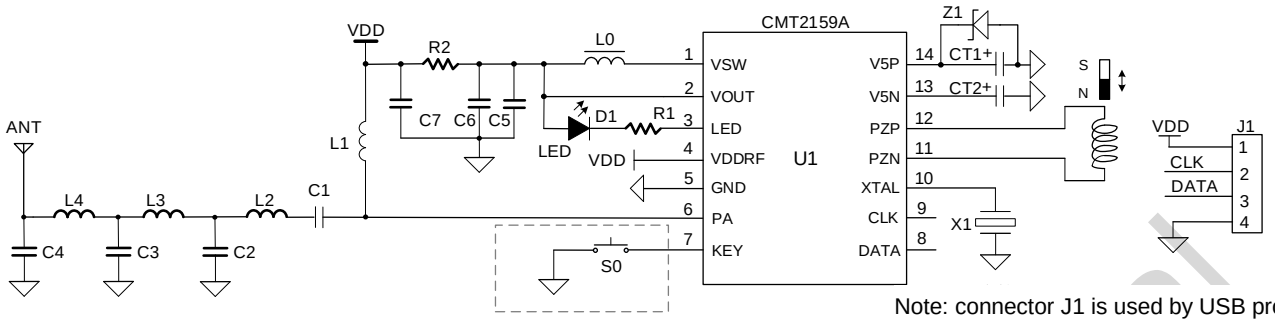


Figure 7. Output power vs. supply voltage, F_{RF} = 433.92 MHz

4 Typical Application



Note: connector J1 is used by USB programmer

Figure 8. CMT2159A Typical Application Schematic Diagram

Application considerations:

1. During developing and production, J1 connector is required for EEPROM programming.
2. The general PCB design principles are as follows:
   - Apply continuous ground plane as large as possible in design.
   - Make as many ground vias as possible (especially on the area near GND pin) to reduce the series parasitic inductance between GND pin and ground plane.
   - Try to avoid using long or thin transmission lines to connect components.
   - Adjacent inductors should be placed perpendicular to each other.
   - Try to place C5, C6, C7 close to the CMT2159A chip to get better filtering performance.
   - Try to place crystal X1 near the chip. Make metal casings ground and place them far away from RF output signal and digital signal.

Table 7. Typical Application BOM

Label	Description	Component Value				Unit	Supplier
		315 MHz	434 MHz	868 MHz	915 MHz		
U1	CMT2159A, FSK/OOK encoding based transmitter with micro-energy-harvesting function	-				-	CMOSTEK
X1	±20 ppm, SMD32*25 mm, crystal	26				MHz	EPSON
R1	±10%, 0402/0603	3.3				kΩ	--
R2	±10%, 0402/0603	27				Ω	--
CT1	Filter capacitor	47				uF	

Label	Description	Component Value				Unit	Supplier
		315 MHz	434 MHz	868 MHz	915 MHz		
CT2	Filter capacitor	100				uF	
C1	±5%, 0402 NP0, 50 V	30	30	8.2	8.2	uF	Murata GRM15
C2	±5%, 0402 NP0, 50 V	8.2	12	5.6	3.9	pF	Murata GRM15
C3	±5%, 0402 NP0, 50 V	8.2	10	--	--	pF	Murata GRM15
C4	±5%, 0402 NP0, 50 V	--	--	--	--	pF	Murata GRM15
C5	±20%, 0603 X7R, 25 V	1				uF	Murata GRM15
C6	±20%, 0603 X7R, 25 V	0.1				uF	Murata GRM15
C7	±20%, 0603 X7R, 25 V	--				uF	Murata GRM15
L0		10				uH	
L1	±5%, 0603 multilayer chip inductor	220	180	100	100	nH	Murata LQG18
L2	±5%, 0603 multilayer chip inductor	68	18	6.8	5.6	nH	Murata LQG18
L3	±5%, 0603 multilayer chip inductor	47	10	10pF	8.2	nH	Murata LQG18
L4	±5%, 0603 multilayer chip inductor	56	220pF	220pF	220pF	nH	Murata LQG18
Z1	voltage regulation diode	5.1				V	
D1	D0603, red LED	-				-	-
S0	Button	-				-	-

5 Function Description

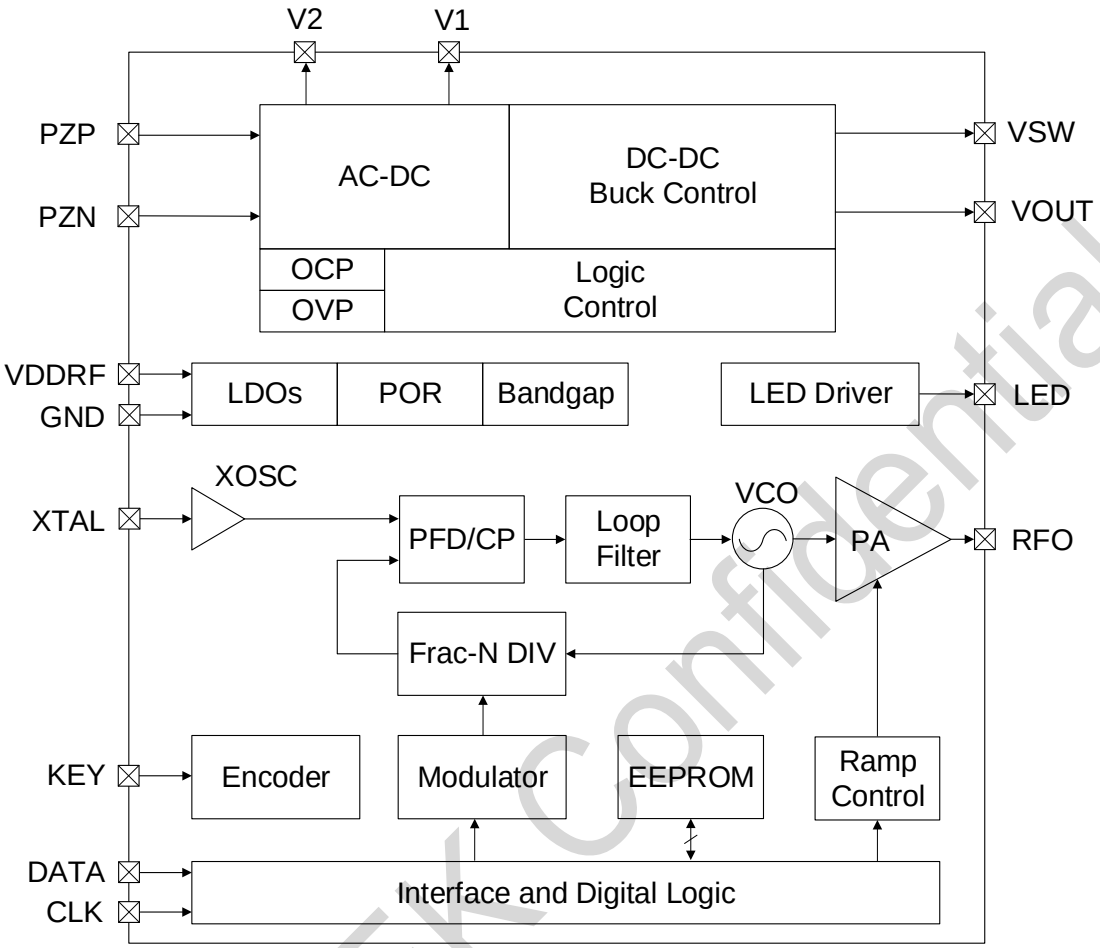


Figure 9. Functional Block Diagram

5.1 Function Overview

The CMT2159A is a highly flexible, high-performance （G）FSK / OOK based RF transmitter with encoder function, integrated with kinetic energy harvesting function, suitable for 240 - 960 MHz wireless transmission applications. It is a part of CMOSTEK NextGenRF™ series product, which is a complete product line including transmitters, receivers, and transceivers. Built in with the 527 and 1527 encodings that are commonly used in market, the CMT2159A becomes an ideal replacement of chip encoder solutions like xx527, xx1527 and xx2240. With its high-density and low-power design, the chip fits well in kinetic energy powered battery-free wireless transmission applications.

As shown in the above function block diagram in Figure 9, the RF frequency is directly synthesized through a fully integrated low-noise fractional frequency synthesizer in the CMT2159A. A single-pin crystal oscillator circuit is used to reduce the number of external components with the load capacitor required for crystal oscillation integrated inside the chip. Upon each power-on reset (POR), the analog module inside the chip is calibrated adapting to an internal reference voltage source. Such calibration can make the chip work better under different thermometer voltages. The data transmission is triggered by a button action. The transmitted data is modulated and transmitted through a high-efficiency power amplifier with its transmission power supporting set value between -10 to +13 dBm in 1dB step. Users can program frequency, output power and other product parameters into the built-in EEPROM of the chip through USB Programmer and RFPDK, which can simplify development and production much thus reducing cost efficiently. Besides, during production, to save the production programming work, users can directly use inventory, which adopts default parameters such as 433.92 MHz,.

The CMT2159A is built in with a micro-energy-harvesting component, which can directly connect with various micro-energy

power generation devices or materials, such as mechanical/kinetic energy generators, deformation plates, piezoelectric ceramics. The chip can fulfill AC-to-DC conversion, as well as perform high-efficiency DC voltage regulation, which outputs DC to the on-chip encoder for high-frequency transmission, thus achieving battery-free and power-free transmitter product design.

5.2 Modulation, Frequency and Data Rate

The CMT2159A supports (G) FSK / OOK modulation with data rate up to 40 ksps (OOK) or 300 ksps (G / FSK) and a continuous frequency covering in 240 - 960 MHz range, including free ISM frequency ranges near 315 MHz, 433.92 MHz, 868.35 MHz and 915 MHz. The chip integrates a high-frequency spectral purity and low-power fractional frequency synthesizer with output signal frequency accuracy better than 198 Hz (≤480MHz) or 397 Hz (> 480 MHz). The supported modulations, frequency range and data rates are listed in the below table.

Table 8. Modulations, Frequency Range and Data Rate

Parameter	Value	Unit
Modulation type	(G)FSK/OOK	-
Frequency	240 to 960	MHz
Frequency deviation	1 – 200	kHz
Frequency resolution（F_{RF}≤480MHz）	198	Hz
Frequency resolution（F_{RF}>480MHz）	397	Hz
Data rate (OOK)	0.5 - 40	ksps
Data rate（G/FSK）	0.5 – 300	ksps

5.3 RFPDK and EEPROM

RFPDK (RF Products Development Kit) is a user-friendly software providing visualized configuration operation of CMT2159A。Users only need to input or select proper value of each parameter then click Burn to complete overall CMT2159A chip configuration with no need for direct register access or control. The EEPROM access method is shown in the figure below.

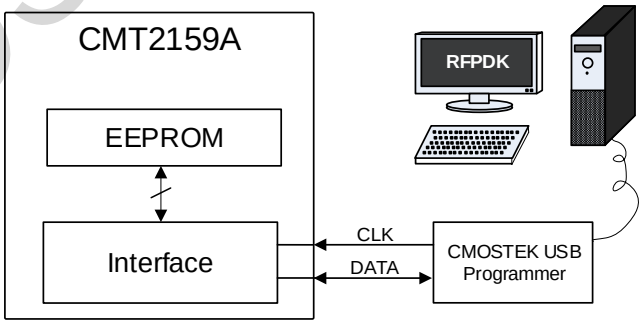


Figure 10. Access Built-in EEPROM

5.4 Power Amplifier

The CMT2159A integrates a high-efficiency single-ended power amplifier supporting configuration from -10 to 13 dBm in 1 dB step. Users can have configuration on RFPDK and program the configuration to chip EEPROM through RFPDK. Please refer to *Typical Application Schematic* in Section 3 for the power amplifier matching reference details.

5.5 Ramping

When a PA is quickly turned on or off, the varying input impedance will instantly interfere with the VCO's output frequency. This phenomenon is called frequency traction, which causes spectral spurs in the output spectrum around the desired carrier frequency. By gradually ramping the on and off of power amplifier, it can minimize the transient pulse of the power amplifier, namely reduce frequency traction. The PA built in CMT2159A supports configuration options of 0, 1, 2, 4, 8, 16, 32, 64, 128, 256, 512 and 1024 us, as shown in Figure 11. When the option 0 is selected, the PA output power will increase to its set value as quickly as possible. The ramp-down time is the same as the corresponding ramp-up time.

CMOSTEK suggests that the maximum symbol rate should be not more than half of PA ramping rate as shown in the below formula.

$$SR_{Max} \le 0.5 * \left(\frac{1}{t_{RAMP}}\right)$$

In above, PA ramping rate is $1/t_{RAMP}$, namely the PA ramping time can be calculated from a given maximum symbol rate as shown in the below formula.

$$t_{RAMP} \le 0.5 * \left(\frac{1}{SR_{MAX}}\right)$$

Users can select a proper option value of t_{RAMP} in the option list mentioned above. If t_{RAMP} is somehow configured as more than $0.5*(1/SR_{Max})$, it may bring extra challenge to OOK demodulation in Rx device.

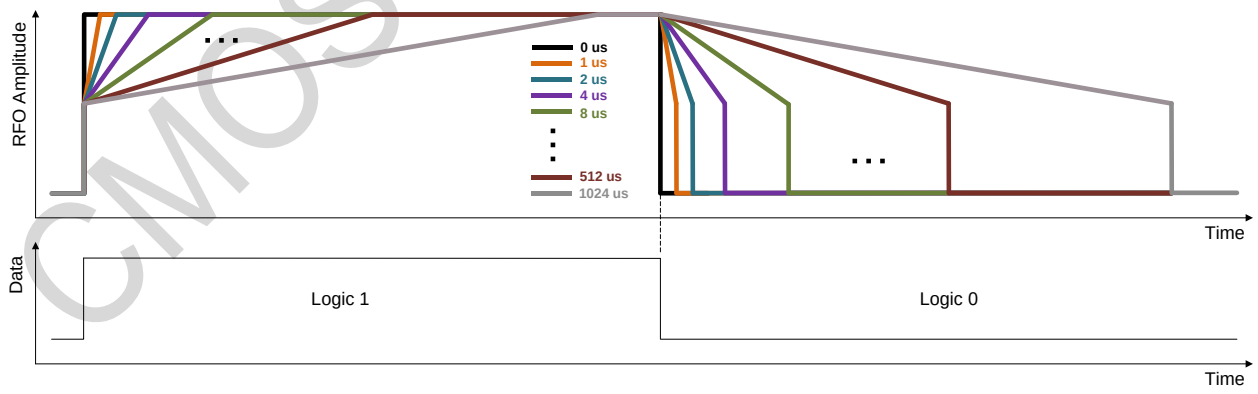


Figure 11. PA Ramping Time

5.6 Operating State

CMT2159A supports 4 operating states including sleep, oscillation starting, tuning and Tx. When no transmission is performed, the system stays in the sleep state.

- In button triggered Tx mode, when a button is pressed, the system will follow the state transition as sleep -> oscillation starting -> tuning -> Tx. When Tx is completed, the system returns to the sleep state.
- In the periodic Tx mode, the device will wake up from the sleep state periodically, then follow the same sequence, namely perform transmission then return to the sleep state.

Sleep state

When the CMT2159A is in this state, all internal modules are off with a minimum current consumption of 20 nA.

Oscillation starting

Once the CMT2159A detects valid button press or periodic Tx counter value being reached, it will enter oscillation starting state and the crystal oscillator circuit starts to operate. T_{XTAL} is the settling time for oscillation, which is largely related to crystal itself. The typical values of t_{XTAL} are listed in Table 9.

Tuning state

Frequency synthesizer will tune the frequency of the CMT2159A to a required frequency in t_{TUNE} time. PA is opened to transmit the data generated by embedded encoder only when frequency tuning is completed.

Tx state

In this state, the CMT2159A performs modulation and data transmission. The data packet is generated by the embedded encoder. Data packet content depend on the selected encoder, button mode and which key is pressed.

Table 9. Time Parameters for Different Operating States

Parameter	Symbol	Min.	Typ.	Max.	Unit
Crystal oscillation time [1]	t_{XTAL}		400		us
Time for tuning to target frequency [2]	t_{TUNE}		370		us

Notes:

[1]. This parameter depends on crystal itself.

[2]. The time duration from frequency tuning start to the time when it's stable and ready for Tx.

5.7 Encoder

The encoder supports 3 encoding formats, 1920, 1527 and 2262. The 3 formats have different structures as discussed in below sections. The main difference among the 3 formats are listed in the below table.

Table 10. Characteristics of 3 Encoding Formats

Encoding	Code Element (sym/bit)	Sync Head Length (bits)	Data Length (bits)	CRC	ID Study	Button Mode [1]
1920	3/4/5/6	1 – 32	1 – 7	Support	Support	Normal mode
1527	4	20	1 – 7	Not support	Support	Normal mode
2262	8	6 – 11	1 – 6	Not support	Not support	Normal mode

The below sections provide brief information only. For content in below, some elements in data packet are measured in symbol unit, some other ones are measured in bit unit. As for the ones in bit unit, it is composed of a number of symbol codes. In the below figures, SYM represents symbol.

5.7.1 1920 Encoding Structure

The 1920 data packet format structure is shown in the below table.

Table 11. Configurable Items in 1920 Data Packet

Parameter	Description	Default	Mode
Preamble	Preamble length can be configured as *16 symbols* or *disable*.	Disable	Basic advanced
Address (Sync ID) length	ID length, the value range is 1 ～32 symbols.	32 bits	Basic advanced
Address (Sync ID) value	ID value, the value range is 0 ～ 2^{Length}-1.	0	Basic advanced

A 1920 packet includes 16 Preambles, a Head with 32 symbol, a Sync ID, a configurable Data field and then CRC with 8 symbols as shown in the below figure.

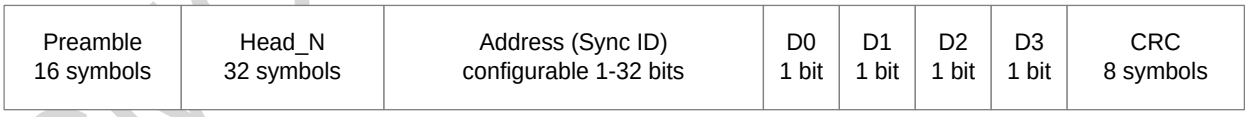


Figure 12. 1920 Encoding Format Data Packet Structure

Bit format：

In 1920 encoding format, one bit can consist 3，4，5 or 6 symbols (namely codes). Users can select required bit format parameter value on RFPDK. Please be noted that only Sync ID field and D0、D1、D2、D3、D4、D5、D6 are defined based on bit.

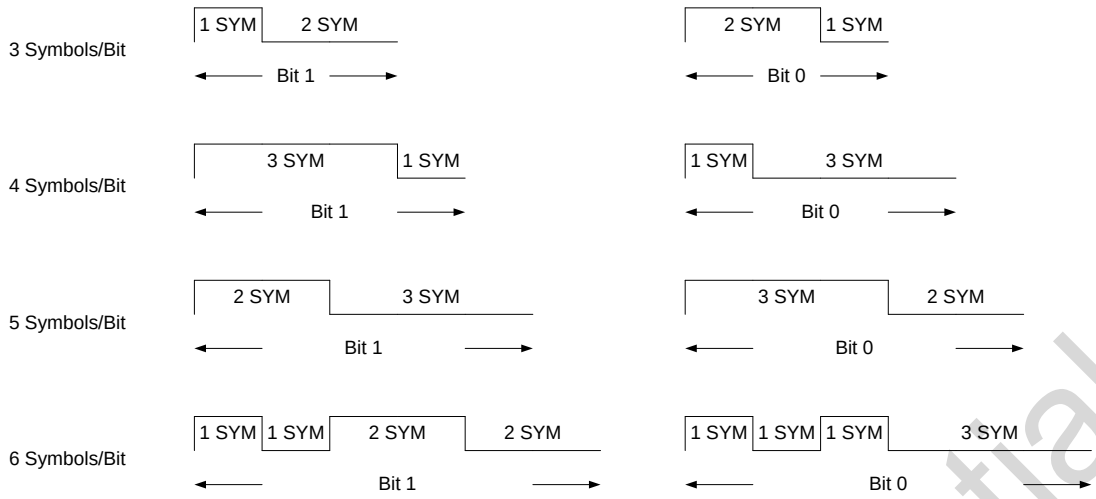


Figure 13. 1920 Bit Format Options

5.7.2 1527 Encoding Structure

The configurable items of 1527 encoding data format are listed in the below table.

Figure 14. Configurable Items of 1527 Encoding Format

Parameter	Description	Default	Mode
Sync ID Value	Sync ID value range is 0 ~ 2^20-1. The 1527 Sync ID length is fixed to 20 bits.	0	Basic advanced

Notes:

[1]. In typical 1527 encoding chip, T_{CLK} is 8 on-chip RC-OSC clock cycles and 1 symbol (SYM) is defined as 4 T_{CLK}. In 1527 encoding, 1 bit is composed of 4 symbols, namely 16 T_{CLK}. However, on RFPDK for CMT2159A, the rate is configured in SYM unit, which is different from the T_{CLK} based rate in typical 1527 encoding chip.

According to typical 1527 data format structure, it includes Synch with 20 symbols, Synch Id address with 20 bits and Data with 4 bits.

Sync 32 symbols	Address (Sync ID) configurable 20 bits	D0 1 bit	D1 1 bit	D2 1 bit	D3 1 bit

Figure 15. 1527 Data Packet Structure Schematic

Bit Format:

In 1527 encoding format, a bit is fixed to consist of 4 symbols as shown in the below figure. Please be noted that, Sync ID and D0，D1，D2，D3 are all defined in bit unit.

Figure 16. 1527 Bit Encoding Schematic Diagram

5.7.3 2262 Encoding Structure

The configurable items for 2262 encoding format are listed in the below table.

Table 12. Configurable Parameter of 2262 Encoding Structure

Parameter	Description	Default	Mode
Sync ID Length	Sync ID length. The value range is 6 - 11 and the total bit number of Sync ID and data is fixed to 12.	8-bit	Basic advanced
Sync ID Value	Indicate which bit is available for use in Sync ID, representing with 0, 1 and F encoding.	00000000	Basic advanced

The standard 2262 data packet includes Address with 8 -11 bits, Data with 1 - 4 bits and Sync with 32 symbols as shown in the below figure.

Figure 17. 2262 Data Packet Structure Schematic Diagram

Bit Format:

In 2262 encoding format, a single bit consists of 8 symbols as shown in the below figure. Please be noted that Sync ID and Data are defined in bit.

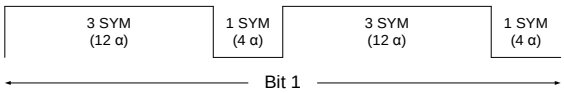


Figure 18. Bit Value 1 Encoding of 2262 Encoding

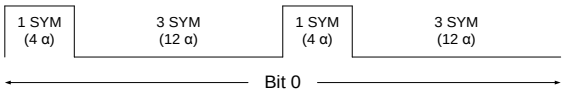


Figure 19. Bit Value 0 Encoding of 2262 Encoding

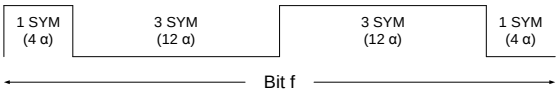


Figure 20. Bit Value F Encoding of 2262 Encoding

5.8 LED Transmission Indication

It supports configurations of enabling/disabling LED pin and current driving capability. When LED pin is configured enabled, LED light turns on upon data transmission and keeps on until Tx ends.

6 Ordering Information

Table 13. CMT2159A Ordering Information

Model	Description	Packaging	Package	Operating Condition	Minimum Order Quantity
CMT2159A-ESR[1]	OOK based transmitter for micro-energy-harvesting	SOP14	Tape and Reel	-40 to 85 ℃	2,500 pcs

Notes:

[1]. E refers to extended Industrial product rating, which supports temperature range from -40 to +85 °C.

[2]. S refers to the package type SOP14.

[3]. R refers to tape and reel type, and the minimum ordering quantity (MOQ) is 2,500 pieces.

Please visit www.cmostek.com for more product/product line information.

Please contact sales@cmostek.comor your local sales representative for sales or pricing requirements.

7 Packaging Information

The packaging information of the CMT2159Ais shown in the below figure.

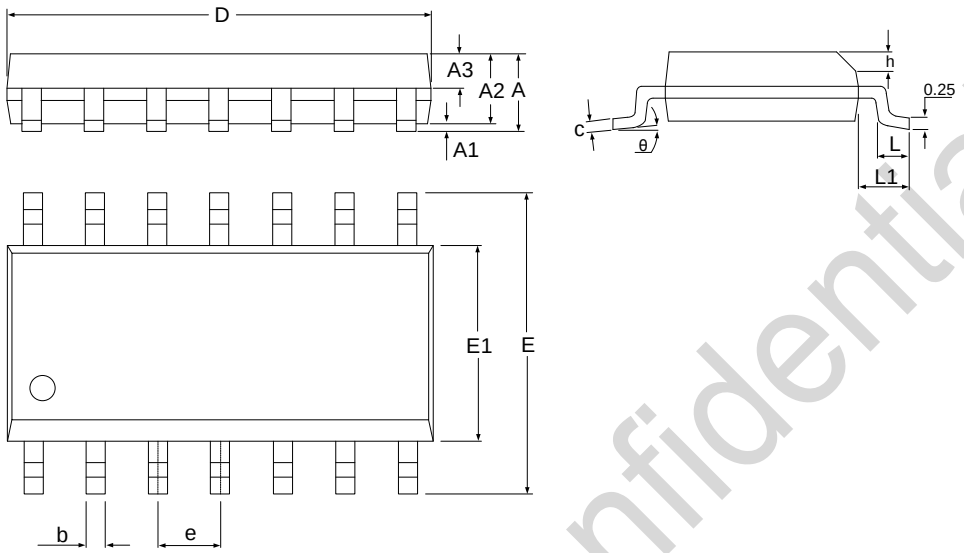


Figure 21. SOP14 Packaging

Table 14. SOP14 Packaging Scale

Symbol	Scale (mm) Maximum		
	Min.	Typ.	Min.
A	-	-	1.75
A1	0.05	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.48
c	0.21	-	0.26
D	8.45	8.65	8.85
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27 BSC		
h	0.25	-	0.50
L	0.50	-	0.80
L1	1.05 BSC		
θ	0	-	8°

8 Top Marking

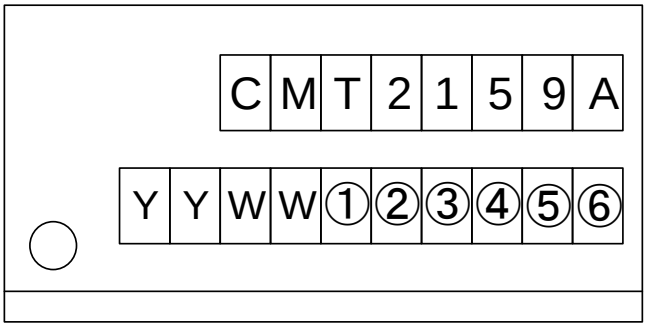


Figure 22. CMT2159A Top Marking

Table 15. CMT2159A Top Marking Information

Marking Method	Laser
Pin 1 Mark	Diameter of the circle = 1 mm
Font Height	0.35 mm, align right
Line 1 Marking	CMT2159A refers to model CMT2159A.
Line 2 Marking	YYWW is the date code assigned by the package factory. YY is the last 2 digits of the year. WW is the working week. ①②③④⑤⑥ is internal tracing code.

9 Revise History

Table 16. Revise History Records

Version No.	Chapter	Description	Date
0.8	All	Initial version	2020-02-28
0.9	4	Section 4: change typical application schematic diagram and BOM table	2020-03-27
1.0	4	Section 4: change typical application schematic diagram	2020-03-30
1.1	4	Table 7, change the values of CT1, CT2	2020-05-15
1.1	4	Table 7, change the value of R2.	2020-09-07
1.3	All	Change to 1 button Remove related documents information	2021-08-24

10 Contacts

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