CMOSTEK

CMT2189C

240 – 960 MHz SoC (G)FSK/OOK Transmitter

Features

- High-Performance RISC CPU
  - PIC16-likeInstruction-set
  - Only 37 instructions to learn:
    - All Single-Cycle Except Branches
  - Operating speed:
    - Up to 16 MHz Clock
    - 125nsinstruction cycle
    - F_{SYS} = 8MHz @ 2.0V~3.6V
    - F_{SYS} = 16MHz @ 2.7V~3.6V
  - Interrupt capability
  - 8-level deep hardware stack
  - 2048 Words Flash / 128B SRAM / 256B EEPROM
  - 2 x 8-bit timers/counters with programmable prescaler
  - 4 I/O pins with individual direction control:
    - Interrupt-on-pin change
    - Individually programmable weak pull-ups
    - Push-pull output except PA5
- High-Performance OOK Transmitter
  - All Features Configurable
  - Frequency Range: 240 to 960 MHz
  - FSK, GFSK and OOK Modulation
  - Symbol Rate up to 100 kbps
  - Configurable Single-Ended or Differential PA Output
  - Output Power:-10 to +13 dBm
- Supply Voltage: 2.0 to 3.6 V
- FCC / ETSI Compliant
- RoHS Compliant

Applications

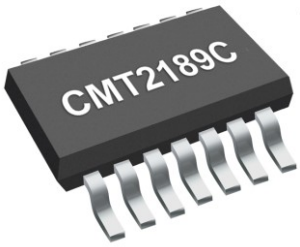
- Remote Keyless Entry (RKE)
- Garage and gate door openers
- Home/Building Automation and Security
- Industrial Monitoring and Controls
- Remote Lighting Control
- Wireless Alarm and Security Systems
- Consumer Electronics Applications

Descriptions

The CMT2189C devices are fully integrated, highly flexible, high performance, SoC (G)FSK/OOK transmitters with embedded RISC microcontroller core for various 240 to 960 MHz wireless applications. They are part of the CMOSTEK NextGenRF™ family, which includes a complete line of transmitters, receivers and transceivers. The CMT2189C uses a 1-pin crystal oscillator circuit with the required crystal load capacitance integrated on-chip to minimize the BOM counts. The device can deliver up to +13 dBm output power and the PA output can be either single-ended or differential. The device operates from 2.0 V to 3.6 V. Its low power design enables superior operation life for battery powered application. The CMT2189C transmitter together with CMOSTEK NextGenRF™ receiver enables a highly flexible, low cost RF link.

Ordering Information

Part Number	Frequency	Package Option	MOQ
CMT2189C-ESR	868.35 MHz	T&R	2,500 pcs
CMT2189C-ESB	868.35 MHz	Tube	1,000 pcs
More Ordering Info: See Page 30			



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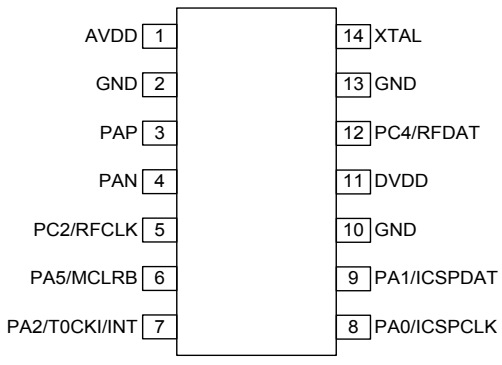


CMT2189C

Typical Application

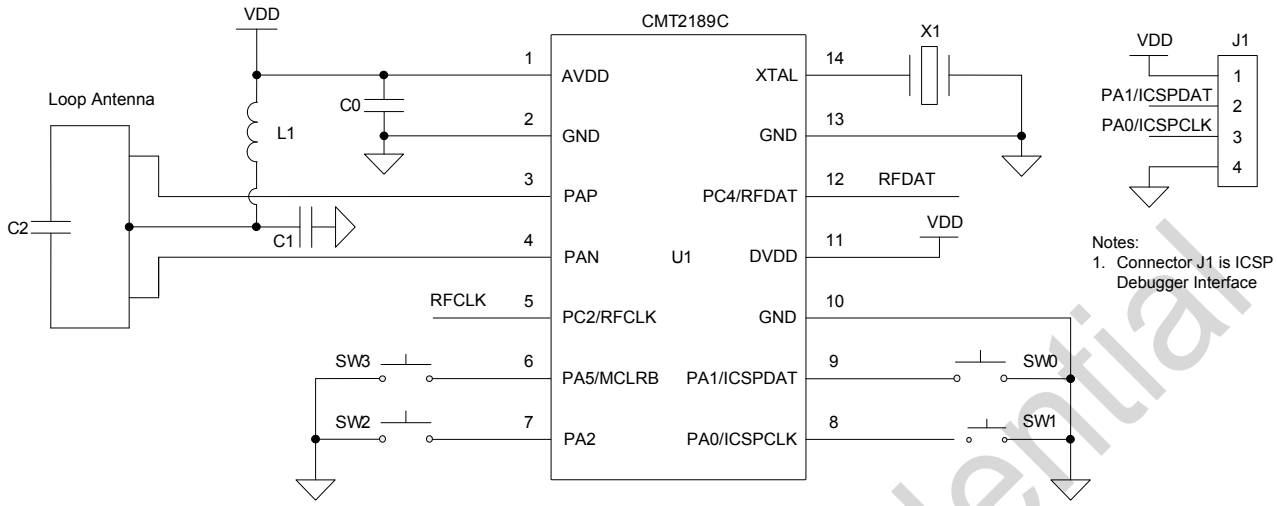


Figure 1.CMT2189C Typical Application with Differential PA Output

Table 1.BOM of 868.35 MHz Application with Differential PA Output

Designator	Descriptions	Value	Unit	Manufacturer
U1	CMT2189C, 240 – 960 MHz SoC(G) FSK/OOK transmitter	-	-	CMOSTEK
X1	±20 ppm, SMD32*25 mm crystal	26	MHz	EPSON
SW[3:0]	Push buttons	-	-	
D1	MBR0520LT1, SOD123 (Optional)	-	-	IR
R1	±5%, 0402	10	kΩ	
C0	±20%, 0402 X7R, 25 V	0.1	uF	Murata GRM15
C1	±0.25 pF, 0402 NP0, 50 V	2.2	pF	Murata GRM15
C2	±0.25 pF, 0402 NP0, 50 V	1.5	pF	Murata GRM15
L1	±5%, 0603 multi-layer chip inductor	100	nH	Murata LQG18

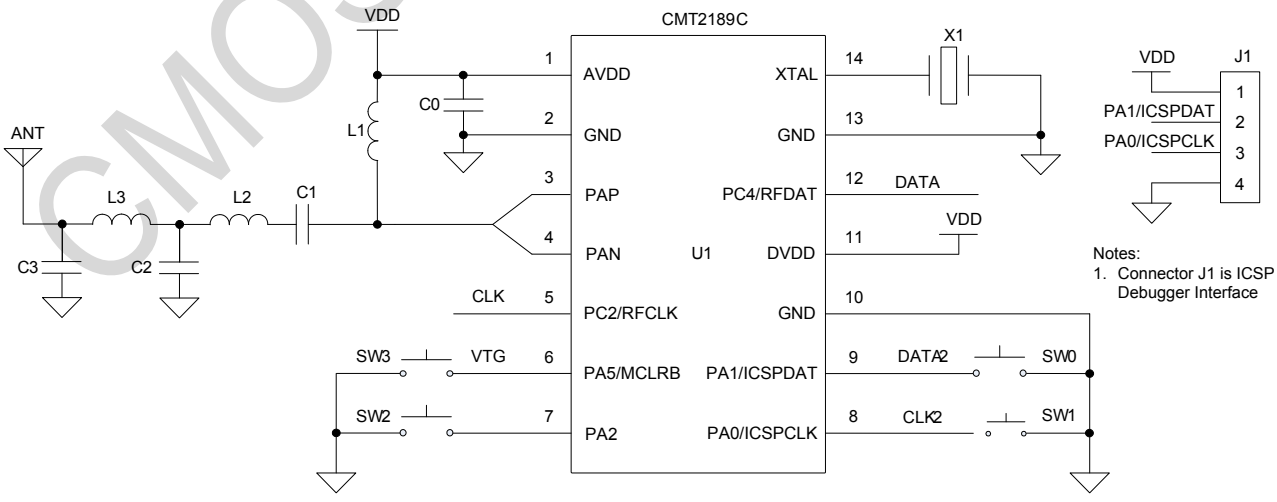


Figure 2. CMT2189C Typical Application with Single-ended PA Output

Table 2. BOM of868.35 MHz Application with Single-ended PA Output

Designator	Descriptions	Value	Unit	Manufacturer
U1	CMT2189C, 240 – 960 MHz SoC (G)FSK/OOK transmitter	-	-	CMOSTEK
X1	±20 ppm, SMD32*25 mm crystal	26	MHz	EPSON
SW[3:0]	Push buttons	-	-	
D1	MBR0520LT1, SOD123 (Optional)	-	-	IR
R1	±5%, 0402	10	kΩ	
C0	±20%, 0402 X7R, 25V	0.1	uF	Murata GRM15
C1	±5%, 0402 NP0, 50V	68	pF	Murata GRM15
C2	±5%, 0402 NP0, 50V	9.1	pF	Murata GRM15
C3	±5%, 0402 NP0, 50V	8.2	pF	Murata GRM15
L1	±5%, 0603 multi-layer chip inductor	100	nH	MurataLQG18
L2	±5%,0603 multi-layer chip inductor	8.2	nH	MurataLQG18
L3	±5%,0603 multi-layer chip inductor	8.2	nH	MurataLQG18

Abbreviations

Abbreviations used in this data sheet are described below

AN	Application Notes
BOM	Bill of Materials
BSC	Basic Spacing between Centers
BW	Bandwidth
DC	Direct Current
EEPROM	Electrically Erasable Programmable Read-Only Memory
ESD	Electro-Static Discharge
ESR	Equivalent Series Resistance
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission
FSK	Frequency Shift Keying
GFSK	Gauss Frequency Shift Keying
GUI	Graphical User Interface
IC	Integrated Circuit
LDO	Low Drop-Out
Max	Maximum
MCU	Microcontroller Unit
Min	Minimum
MOQ	Minimum Order Quantity
NP0	Negative-Positive-Zero
OBW	Occupied Bandwidth
OOK	On-Off Keying
PA	Power Amplifier
PC	Personal Computer
PCB	Printed Circuit Board
PLL	Phase Lock Loop
PN	Phase Noise
RBW	Resolution Bandwidth
RCLK	Reference Clock
RF	Radio Frequency
RFPDK	RF Product Development Kit
RoHS	Restriction of Hazardous Substances
Rx	Receiving, Receiver
SOT	Small-Outline Transistor
TBD	To Be Determined
Tx	Transmission, Transmitter
Typ	Typical
XO/XOSC	Crystal Oscillator
XTAL	Crystal

Table of Contents

1. Electrical Characteristics

V_{DD} = 3.3 V, T_{OP} = 25 ℃, F_{RF} = 868.35 MHz, FSK modulation, output power is +10 dBm terminated in a matched 50 Ω impedance with single-ended PA output, unless otherwise noted.

1.1 Recommended Operating Conditions

Table 3. Recommended Operation Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operation Voltage Supply	V_{DD}		2.0		3.6	V
Operation Temperature	T_{OP}		-40		85	℃
Supply Voltage Slew Rate			1			mV/us

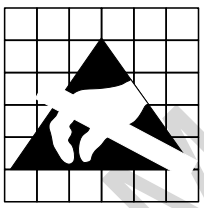
1.2 Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings[1]

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	V_{DD}		-0.3	3.6	V
Interface Voltage	V_{IN}		-0.3	V_{DD} +0.3	V
Junction Temperature	T_J		-40	125	℃
Storage Temperature	T_{STG}		-50	150	℃
Soldering Temperature	T_{SDR}	Lasts at least 30 seconds		255	℃
ESD Rating		Human Body Model (HBM)	-2	2	kV
Latch-up Current		@ 85 ℃	-100	100	mA

Note:

[1]. Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.



Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.

1.3 Transmitter Specifications

Table 5. Transmitter Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Frequency Range[1]	F_{RF}		240		960	MHz
Synthesizer Frequency Resolution	F_{RES}			198		Hz
Symbol Rate	SR	OOK	0.5		30	ksps
		FSK/GFSK	0.5		100	ksps
Deviation	F_{DEV}		1		200	ksps
Bandwidth-Time Product	BT			0.5		-
Maximum Output Power[2]	$P_{OUT(Max)}$			+13		dBm
Minimum Output Power	$P_{OUT(Min)}$			-10		dBm
Output Power Step Size	P_{STEP}			1		dB
PA Ramping Time[3]	t_{RAMP}		0		1024	us
Current Consumption, Single-ended	$I_{DD\text{-}S\text{-}433.92}$	0 dBm, 50% duty cycle		9.1		mA
		+10 dBm, 50% duty cycle		20.5		mA
		+13 dBm, 50% duty cycle		27.4		mA
	$I_{DD\text{-}S\text{-}868.35}$	0 dBm, 50% duty cycle		10		mA
		+10 dBm, 50% duty cycle		21.3		mA
		+13 dBm, 50% duty cycle		28		mA
Current Consumption, Differential	$I_{DD\text{-}D\text{-}433.92}$	0 dBm, 50% duty cycle		5.8		mA
		+10 dBm, 50% duty cycle		13.1		mA
		+13 dBm, 50% duty cycle		15.3		mA
	$I_{DD\text{-}D\text{-}868.35}$	0 dBm, 50% duty cycle		6.5		mA
		+10 dBm, 50% duty cycle		14.3		mA
		+13 dBm, 50% duty cycle		16.7		mA
Sleep Current	I_{SLEEP}			2.5		uA
Frequency Tune Time	t_{TUNE}			370		us
Phase Noise @433.92 MHz	$PN_{433.92}$	100 kHz offset from F_{RF}		-80		dBc/Hz
		600 kHz offset from F_{RF}		-98		dBc/Hz
		1.2 MHz offset from F_{RF}		-107		dBc/Hz
Phase Noise @868.35 MHz	$PN_{868.35}$	100 kHz offset from F_{RF}		-80		dBc/Hz
		600 kHz offset from F_{RF}		-98		dBc/Hz
		1.2 MHz offset from F_{RFI}		-107		dBc/Hz
Harmonics Output for 315 MHz[4]	$H2_{315}$	2^{nd} harm @ 630 MHz, +13 dBm P_{OUT}		-60		dBm
	$H3_{315}$	3^{rd} harm @ 945 MHz, +13 dBm P_{OUT}		-65		dBm
Harmonics Output for 433.92 MHz[4]	$H2_{433.92}$	2^{nd} harm @ 867.84 MHz, +13 dBm P_{OUT}		-52		dBm
	$H3_{433.92}$	3^{rd} harm @ 1301.76 MHz, +13 dBm P_{OUT}		-60		dBm
OOK Extinction Ration				60		dB

Notes:

[1]. The frequency range is continuous over the specified range.

[2]. Measured with single-ended PA output, and it is not applicable for when the device is configured as differential PA output.

[3]. 0 and 2^n us, n = 0 ~10, when set to "0", the PA output power will ramp to its configured value in the shortest possible time.

[4]. The harmonics output is measured with the application shown as Figure 11.

1.4 RF Crystal Oscillator

Table 6. Crystal Oscillator Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Crystal Frequency[1]	F_{XTAL}		26	26	26	MHz
Crystal Tolerance[2]				±20		ppm
Load Capacitance[3]	C_{LOAD}		12		20	pF
Crystal ESR	Rm				60	Ω
XTAL Startup Time[4]	t_{XTAL}			400		us

Notes:

[1]. The CMT2189C can directly work with external 26 MHz reference clock input to XTAL pin (a coupling capacitor is required) with amplitude 0.3 to 0.7 Vpp.

[2]. This is the total tolerance including (1) initial tolerance, (2) crystal loading, (3) aging, and (4) temperature dependence. The acceptable crystal tolerance depends on RF frequency and channel spacing/bandwidth.

[3]. The required crystal load capacitance is integrated on-chip to minimize the number of external components.

[4]. This parameter is to a large degree crystal dependent.

1.5 Internal High Frequency Oscillator

Table 7. IHRC Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
IHRC Frequency	F_{IHRC}	3.3V, 27℃		15.99		MHz
Temperature-dependent		-20℃~ +80℃, 3.3V		4.2%/100℃		
Voltage-dependent		2~3.6V		±3		%/V
Setup Time				2.2	10	us
Leakage Current				0.8	2	nA
Triming Range		Step 0.625%		±20%		

1.6 Internal Low Frequency Oscillator

The ILRCsupport two frequency: 32KHz or 256KHz. It can be selected by LFMOD in OSCCON register, 0 is the 32KHz, and the 1 is the 256KHz.

Table 8. ILRC Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
ILRC Frequency	F_{ILRC}	2.5V, 25℃, 32K		32.3		KHz
		2.5V, 25℃, 256K		258.5		KHz
Temperature-dependent		-20℃~ +80℃, 2.5V		22.3%/100℃		
Voltage-dependent		2~3.6V		±11.1		%/V
Setup Time		2.5V, 25℃		4.6	10	us
Leakage Current		Disable		0.15	1	nA

1.7 LVD/LVR

Table 9. LVD/LVR Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LVD Voltage				2.0		V
				2.2		
				2.8		
LVR delay				125	157	us

1.8 POR

Table 10. POR Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
POR Current	I_{POR}	3.3V		50		nA
Temperature-dependent		3.3V		2.0		V

1.9 I/O PAD

Table 11. I/OPAD Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Low Voltage	VIL				0.3	VDD
Input High Voltage	VIH		0.7			VDD
Output High Current	I_{OH}	3.3V, 25℃		10		mA
Output Low Current	I_{OL}	3.3V, 25℃		15		mA
Weak Pull-up		3.3V		41.7		KΩ

1.10 MCU Supply Current

Table 12. Supply Current

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operation Mode		3.3V, F_{SYS} = 2MHz		310		uA
		3.3V, F_{SYS} = 32KHz		50		uA
Sleep Mode with WDT_ON		3.3V		3		uA
Sleep Mode with WDT_OFF		3.3V		0.8		uA
Sleep Mode with LVD_ON		3.3V		15		uA

Notes:
1. All the IO is input mode, and with pull-down resistance.
2.Comparator is disable, CM<2:0> = 111

2. Pin Descriptions

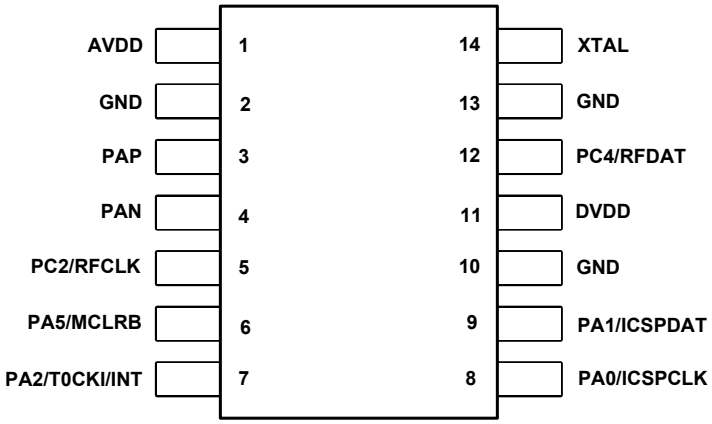


Figure 3.CMT2189C Pin Assignments

Table 13.CMT2189C Pin Descriptions

Pin Number	Name	I/O	Descriptions	
1	AVDD	I	RF power supply input	
2	GND	I	Ground	
3	PAP	O	The differential power amplifier output, when using as singled-ended output, PAN/PAP should be connected together before connecting to the matching network	
4	PAN	O		
5	PC2/RFCLK	IO	PC2	PORTC I/O
			RFCLK	TWI's Clock for the RFconfiguration, internally pulled up to VDD
6	PA5/MCLRB	I	PA5	PORTA input with pull-up and interrupt-on-change
			MCLRB	Master Clear w/internal pull-up
7	PA2/T0CKI/INT	IO	PA2	PORTA I/O w/programmable pull-up and interrupt-on-change
			T0CKI	Timer0 clock input
			INT	External Interrupt
8	PA0/ICSPCLK	IO	PA0	PORTA I/O w/programmable pull-up and interrupt-on-change
			ICSPCLK	Serial Programming and debugging Data I/O
9	PA1/ICSPDAT	IO	PA1	PORTA I/O w/programmable pull-up and interrupt-on-change
			ICSPDAT	Serial Programming and debugging Clock
10	GND	I	Ground	
11	DVDD	I	Digital power supply input	
12	PC4/RFDAT	IO	PC4	PORTC I/O
			RFDAT	TWI's DATA for RF configuration, internally pulled down to GND
13	GND	I	Ground	
14	XTAL	I	26 MHz single-ended crystal oscillator input or external 26 MHz reference clock input	

3. Typical Performance Characteristics

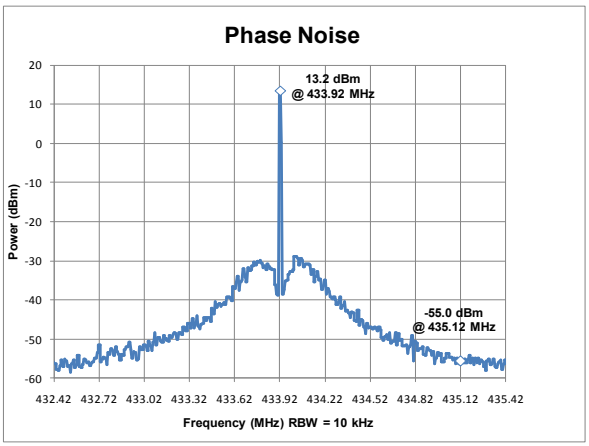


Figure 4.Phase Noise, F_{RF} = 433.92 MHz,

P_{OUT} = +13 dBm, Unmodulated

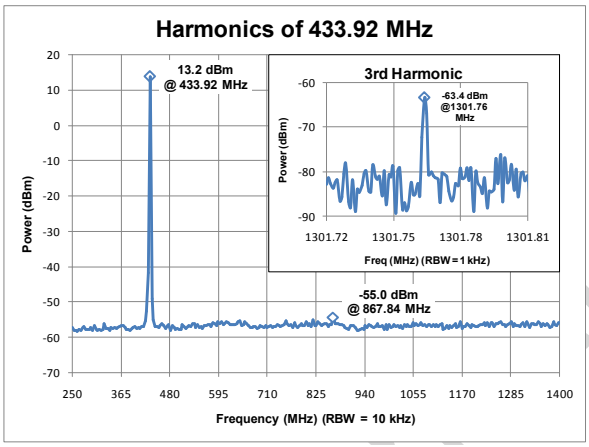


Figure 5.Harmonics of 433.92 MHz,

P_{OUT} = +13 dBm

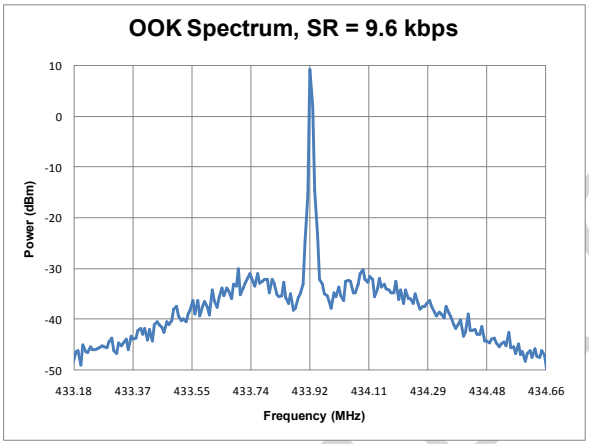


Figure 7. OOK Spectrum,SR = 9.6 ksps,

P_{OUT} = +10 dBm, t_{RAMP} = 32 us

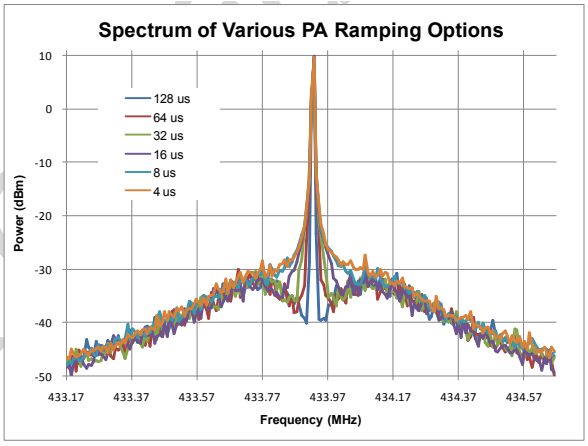


Figure 6.Spectrum of PA Ramping,

SR = 9.6 ksps, P_{OUT} = +10 dBm

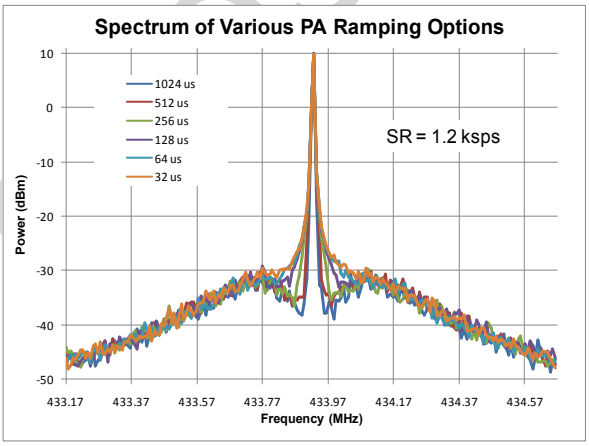


Figure 8.Spectrum of PA Ramping,

SR = 1.2 ksps, P_{OUT} = +10 dBm

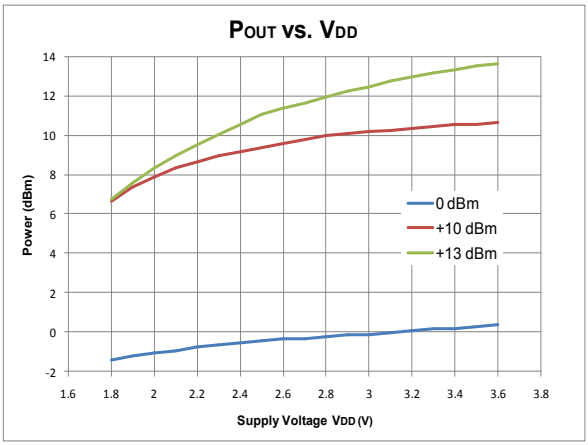


Figure 9.Output Power vs. Supply

Voltages, F_{RF} = 433.92 MHz

4. Typical Application Schematics

4.1 Typical Application with Differential PA Output

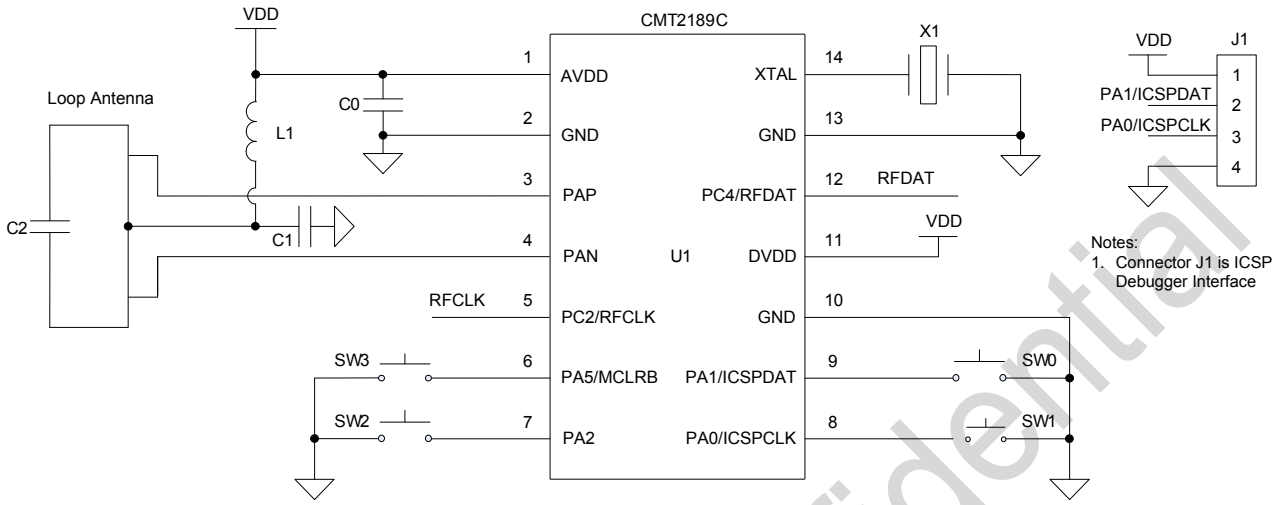


Figure 10.CMT2189C Typical Application with Differential PA Output

Notes:

1. Connector J1 is a must for the CMT2189C chip programming during development or manufacture.
2. The general layout guidelines are listed below. For more design details, please refer to “AN100CMT211x-5x-8x Schematic and PCB Layout Design Guideline”.
   - Use as much continuous ground plane metallization as possible.
   - Use as many grounding vias (especially near to the GND pins) as possible to minimize series parasitic inductance between the ground pour and the GND pins.
   - Avoid using long and/or thin transmission lines to connect the components.
   - Avoid placing the nearby inductors in the same orientation to reduce the coupling between them.
   - Place C0 as close to the CMT2189C as possible for better filtering.
3. The table below shows the BOM of 868.35Application with Differential PA Output.

Table 14.BOM of 868.35 MHz Application with Differential PA Output

Designator	Descriptions	Value	Unit	Manufacturer
U1	CMT2189C, 240 – 960 MHz SoC (G)FSK/OOK transmitter	-	-	CMOSTEK
X1	±20 ppm, SMD32*25 mm crystal	26	MHz	EPSON
SW[3:0]	Push buttons	-	-	
D1	MBR0520LT1, SOD123 (Optional)	-	-	IR
R1	±5%, 0402	10	kΩ	
C0	±20%, 0402 X7R, 25 V	0.1	uF	Murata GRM15
C1	±0.25 pF, 0402 NP0, 50 V	2.2	pF	Murata GRM15
C2	±0.25 pF, 0402 NP0, 50 V	1.5	pF	Murata GRM15
L1	±5%, 0603 multi-layer chip inductor	100	nH	Murata LQG18

4.2 Typical Application with Single-ended PA Output

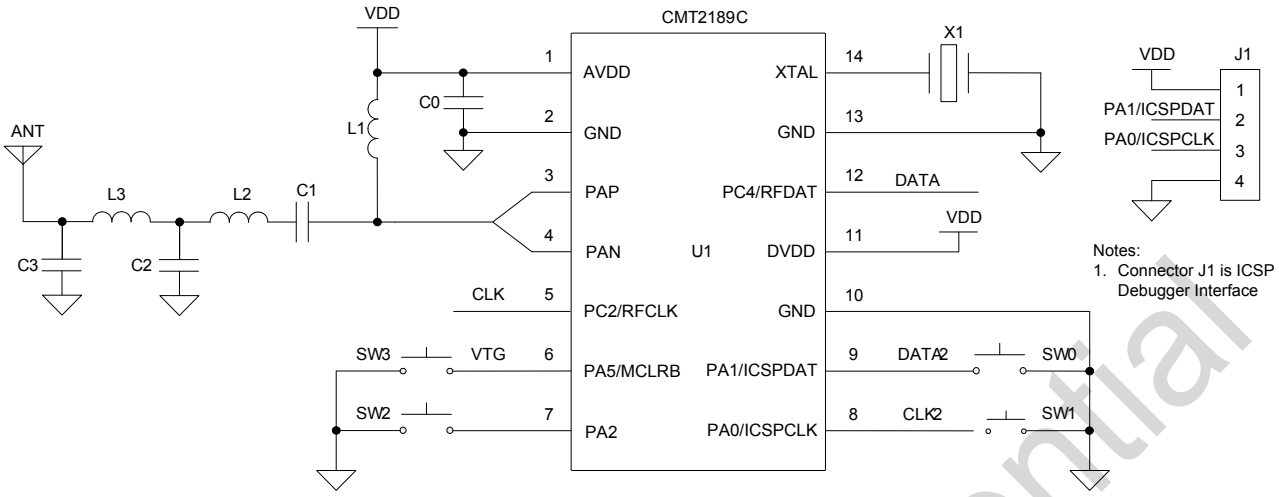


Figure 11. CMT2189C Typical Application with Single-ended PA Output

Notes:

1. Connector J1 is a must for the CMT2189C chip programming during development or manufacture.
2. The general layout guidelines are listed below. For more design details, please refer to "AN100CMT211x-5x-8x Schematic and PCB Layout Design Guideline".
   - Use as much continuous ground plane metallization as possible.
   - Use as many grounding vias (especially near to the GND pins) as possible to minimize series parasitic inductance between the ground pour and the GND pins.
   - Avoid using long and/or thin transmission lines to connect the components.
   - Avoid placing the nearby inductors in the same orientation to reduce the coupling between them.
   - Place C0 as close to the CMT2189C as possible for better filtering.
3. The table below shows the BOM of868.35 Application with single-ended PA output.

Table15. BOM of868.35 MHz FCC/ETSI Compliant Application

Designator	Descriptions	Value	Unit	Manufacturer
U1	CMT2189C, 240 – 960 MHz SoC(G)FSK/OOK transmitter	-	-	CMOSTEK
X1	±20 ppm, SMD32*25 mm crystal	26	MHz	EPSON
SW[3:0]	Push buttons	-	-	
D1	MBR0520LT1, SOD123 (Optional)	-	-	IR
R1	±5%, 0402	10	kΩ	
C0	±20%, 0402 X7R, 25V	0.1	uF	Murata GRM15
C1	±5%, 0402 NP0, 50V	68	pF	Murata GRM15
C2	±5%, 0402 NP0, 50V	9.1	pF	Murata GRM15
C3	±5%, 0402 NP0, 50V	8.2	pF	Murata GRM15
L1	±5%, 0603 multi-layerchip inductor	100	nH	MurataLQG18
L2	±5%,0603 multi-layerchip inductor	8.2	nH	MurataLQG18
L3	±5%,0603 multi-layerchip inductor	8.2	nH	MurataLQG18

5. Functional Descriptions

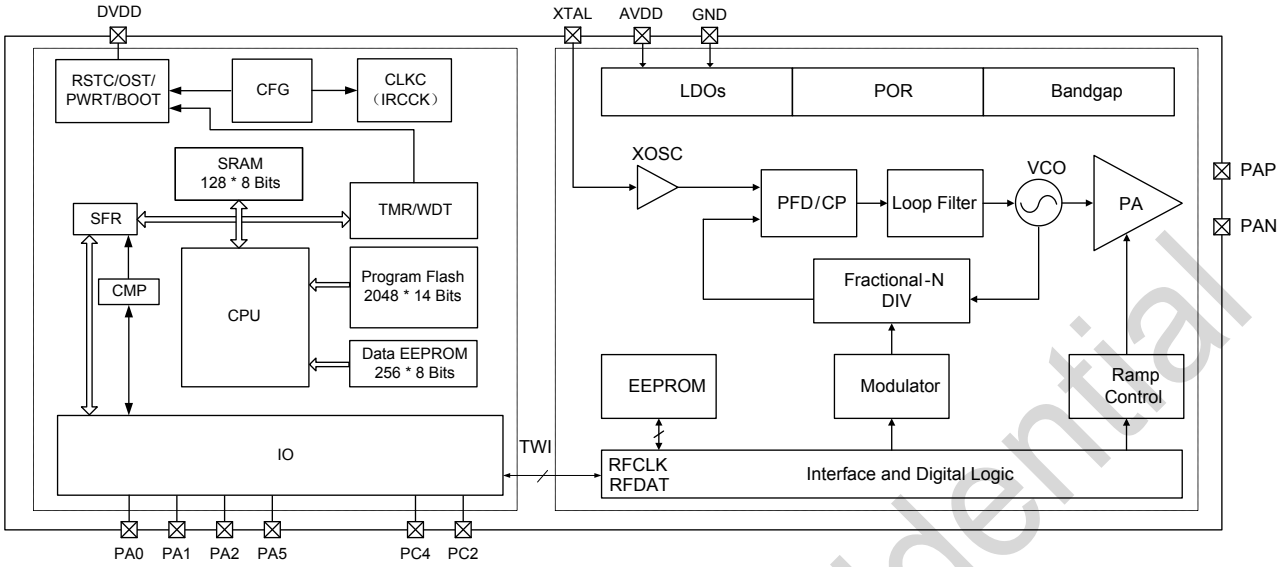


Figure 12. CMT2189C Functional Block Diagram

5.1 Overview

The CMT2189C devices are fully integrated, highly flexible, high performance, SoC (G)FSK/OOK transmitters with an embedded RISC microcontroller designed for various 240 to 960 MHz wireless applications. They are part of the CMOSTEK NextGenRF^{TM} family, which includes a complete line of transmitters, receivers and transceivers. The chip is optimized for the low system cost, low power consumption, battery powered application with its highly integrated and low power design.

The functional block diagram of the CMT2189C is shown in the figure above. The CMT2189C is based on direct synthesis of the RF frequency, and the frequency is generated by a low-noise fractional-N frequency synthesizer. It uses a 1-pin crystal oscillator circuit with the required crystal load capacitance integrated on-chip to minimize the number of external components. Every analog block is calibrated on each Power-on Reset (POR) to the reference voltage generated by Bandgap. The calibration can help the chip to finely work under different temperatures and supply voltages. The CMT2189C has a highly efficient PA built in, the PA can be configured as single-ended or differential outputs, and the output power can be configured from -10 to +13 dBm in 1 dB step size. The RISC microcontroller has2048-word flash program space. Up to 4 I/O are supported with their functions customized by the user program. RF Frequency, PA output power, other product features and unique transmit IDs can be programmed into the embedded EEPROM. This saves the cost and simplifies the product development and manufacturing effort. Alternatively, in stock products of 868.35 MHz is available for immediate demands. The CMT2189C operates from 2.0 to 3.6 V, only consumes 12.4 mA when transmitting +10 dBm power under 3.3 V supply voltage. The device together with CMOSTEK NextGenRF^{TM} receiver enables a highly flexible, low cost RF link.

5.2 Modulation, Frequency, Deviation and Symbol Rate

The CMT2189C supports OOK modulation with the symbol rate up to 30 ksps, as well as the (G)FSK modulation with the symbol rate up to 100 ksps. The supported deviation frequency is from 1 kHz to 200 kHz. The CMT2189C continuously covers the frequency range from 240 to 960 MHz, including the license free ISM frequency band around 315 MHz433.92 MHz, 868.35 MHz and915 MHz. The device contains a high spectrum purity low power fractional-N frequency synthesizer with output frequency resolution better than 198 Hz when the RF frequency is lower than 480 MHz, and is 397 Hz when the RF frequency is higher than 480 MHz, see the table below for the modulation, frequency, Deviation and symbol rate specifications.

Table 16. Modulation, Frequency, Deviation and Symbol Rate

Parameter	Value	Unit
Modulation	(G)FSK/OOK	-
Frequency	240 to960	MHz
Deviation	1 to 200	kHz
Frequency Resolution (F_{RF}≤ 480 MHz)	<198	Hz
Frequency Resolution (F_{RF}> 480 MHz)	397	Hz
(G)FSK Symbol Rate	0.5 to100	ksps
OOK Symbol Rate	0.5 to30	ksps

5.3 Power Amplifier

A highly efficient Power Amplifier (PA) is integrated in the CMT2189C to transmit the modulated signal out. Depending on the application, the PA can be configured as single-ended or differential output on the RFPDK, and the user can design a matching network for the PA to exhibit optimum efficiency at the desired output power for a wide range of antennas, such as loop or monopole antenna. Typical application schematics and the required BOM are shown in “Chapter 4 Typical Application Schematic”. For the schematic, layout guideline and the other detailed information please refer to “AN100CMT211x-5x-8x Schematic and PCB Layout Design Guideline”.

The output power of the PA can be configured by the user within the range from -10 dBm to +13 dBm in 1 dB step size using the CMOSTEK USB Programmer and the RFPDK(just as CMT2119A), and also can be configured by software using the TWI.

5.4 PA Ramping

When the PA is switched on or off quickly, its changing input impedance momentarily disturbs the VCO output frequency. This process is called VCO pulling, and it manifests as spectral splatter or spurs in the output spectrum around the desired carrier frequency. By gradually ramping the PA on and off, PA transient spurs are minimized. The CMT2189C has built-in PA ramping configurability with options of 0, 1, 2, 4, 8, 16, 32, 64, 128, 256, 512 and 1024 us, as shown in Figure. When the option is set to “0”, the PA output power will ramp up to its configured value in the shortest possible time. The ramp down time is identical to the ramp up time in the same configuration.

CMOSTEK recommends that the maximum symbol rate should be no higher than 1/2 of the PA ramping “rate”, as shown in the formula below.

$$SR_{Max} \le 0.5 * \left(\frac{1}{t_{RAMP}}\right)$$

In which the PA ramping “rate” is given by ($1/t_{RAMP}$). In other words, by knowing the maximum symbol rate in the application, the PA ramping time can be calculated by formula below.

$$t_{RAMP} \le 0.5 * \left(\frac{1}{SR_{MAX}}\right)$$

The user can select one of the values of the t_{RAMP} in the available options that meet the above requirement. If somehow the t_{RAMP} is set to be longer than “0.5 * ($1/SR_{Max}$)”, it will possibly bring additional challenges to the OOK demodulation of the Rxdevice. For more detail of calculating t_{RAMP}, please refer to “AN132 CMT2180/89AConfiguration Guideline”.

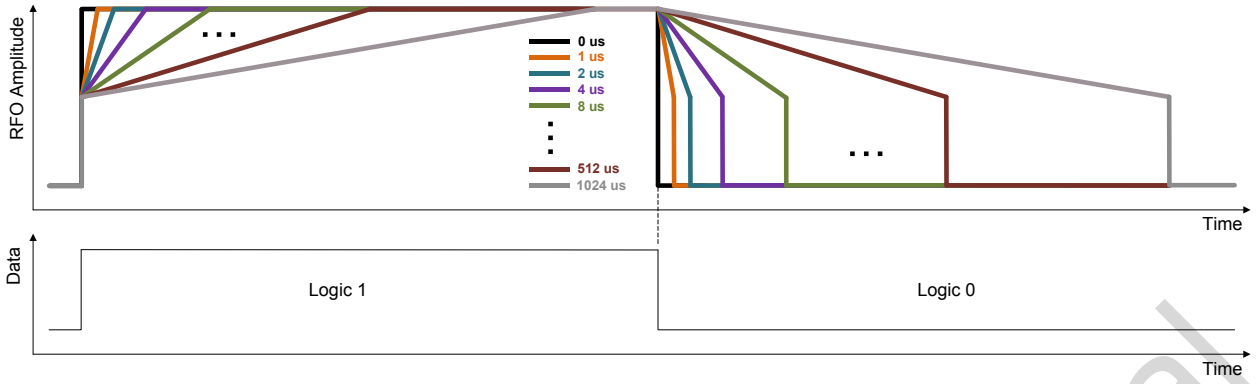


Figure 13. PA Ramping Time

5.5 Crystal Oscillator and RCLK

The CMT2189C uses a 1-pin crystal oscillator circuit with the required crystal load capacitance integrated on-chip. Figure 15 shows the configuration of the XTAL circuitry and the crystal model. The recommended specification for the crystal is 26 MHz with ±20 ppm, ESR (Rm) < 60 Ω, load capacitance C_{LOAD} ranging from 12 to 20 pF. To save the external load capacitors, a set of variable load capacitors C_L is built inside the CMT2189C to support the oscillation of the crystal.

The value of load capacitors is configurable with the CMOSTEK USB Programmer and RFPDK. To achieve the best performance, the user only needs to input the desired value of the XTAL load capacitance C_{LOAD} of the crystal (can be found in the datasheet of the crystal) to the RFPDK, then finely tune the required XO load capacitance according to the actual XO frequency.

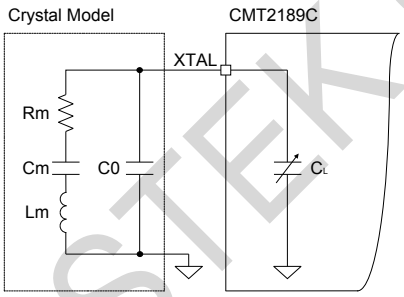


Figure 15.XTAL Circuitry and Crystal Model

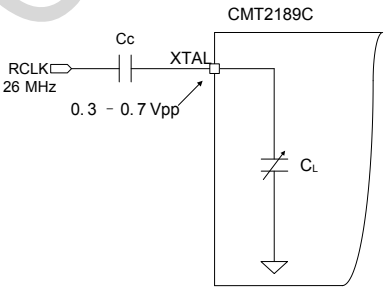


Figure 14.RCLK Circuitry

If a 26 MHz RCLK (reference clock) is available in the system, the user can directly use it to drive the CMT2189C by feeding the clock into the chip via the XTAL pin. This further saves the system cost due to the removal of the crystal. A coupling capacitor is required if the RCLK is used. The recommended amplitude of the RCLK is 0.3 to 0.7 Vpp on the XTAL pin. Also, the user should set the internal load capacitor C_L to its minimum value. See Figure 14for the RCLK circuitry.

6. RFWorking States and Control Interface

6.1 Working States

The CMT2189C's RF has following 4 different working states: SLEEP, XO-STARTUP, TUNE and TRANSMIT.

SLEEP

When the CMT2189C is in the SLEEP state, all the internal blocks are turned off and the current consumption is minimized.

XO-STARTUP

Once the modulator of the CMT2189C detect valid signal on the D_{RAW} wire (see Figure 12), the RF section will go into the XO-STARTUP state, and the internal XO starts to work. The user has to wait for the t_{XTAL} to allow the XO to get stable. The t_{XTAL} is to a large degree crystal dependent. A typical value of t_{XTAL} is provided in the Table .

TUNE

The frequency synthesizer will tune the CMT2189C to the desired frequency in the time t_{TUNE}.The PA can be turned on to transmit the data only after the TUNE state is done, before that the data will not be transmitted. See Figure 16 and Figure 17for the details.

TRANSMIT

The CMT2189C starts to modulate and transmit the data (D_{RAW}) generated by the microcontroller core responding to the push buttons. The transmission can be ended in 2 methods: firstly, driving the DATA pin low for t_{STOP} time, where the t_{STOP} can be configured from 20 to 90 ms on the RFPDK; secondly, issuing SOFT_RST command over the two-wire interface, this will stop the transmission in 1 ms. See section 6.2.3for details of the two-wire interface.

Table 17.Timing in Different Working States

Parameter	Symbol	Min	Typ	Max	Unit
XTAL Startup Time [1]	t_{XTAL}		400		us
Time to Tune to Desired Frequency	t_{TUNE}		370		us
Hold Time After Rising Edge	t_{HOLD}	10			ns
Time to Stop The Transmission[2]	t_{STOP}	2		90	ms

Notes:

[1]. This parameter is to a large degree crystal dependent.

[2]. Configurable from 2 to 9 in 1 ms step size and 20 to 90 ms in 10 ms step size.

6.2 Transmission Control Interface

The CMT2189C uses the D_{RAW} wire for the microcontroller core to send in data for modulation and transmission. The D_{RAW} wire, which also connects to the DATA pin, can be used as pin for EEPROM programming, data transmission, as well as controlling the transmission. The transmission can be started by detecting rising or falling edge on the D_{RAW} wire (DATA Pin), and stopped by driving the D_{RAW} wire low for t_{STOP} as shown in the table above. Besides communicating over the D_{RAW} wire, the microcontroller core can also communicate with the RF section over the two-wire interface, so that the transmission is more robust, and consumes less current.

Please note that the user is recommended to use the Tx Enabled by DATA pin Rising Edge, which is described in Section 6.2.1.

6.2.1 Tx Enabled by DATA Pin Falling Edge

As shown in the figure below, once the CMT2189C detects a falling edge on the D_{RAW} wire (can be observed on DATA pin), it goes into XO-STARTUP state and the XO starts to work. During the XO-STARTUP state, the D_{RAW} wire needs to be pulled low. After the XO is settled, the CMT2189C goes to the TUNE state. The logic state of the D_{RAW} wire is “Don’t Care” during the TUNE state. In the TRANSMIT state, PA sends out the data generated by the microcontroller core after they are modulated. The user has to pull the D_{RAW} wire low for t_{STOP} in order to end the transmission. Before starting the next transmit cycle, the user has to pull the D_{RAW} wire back to high.

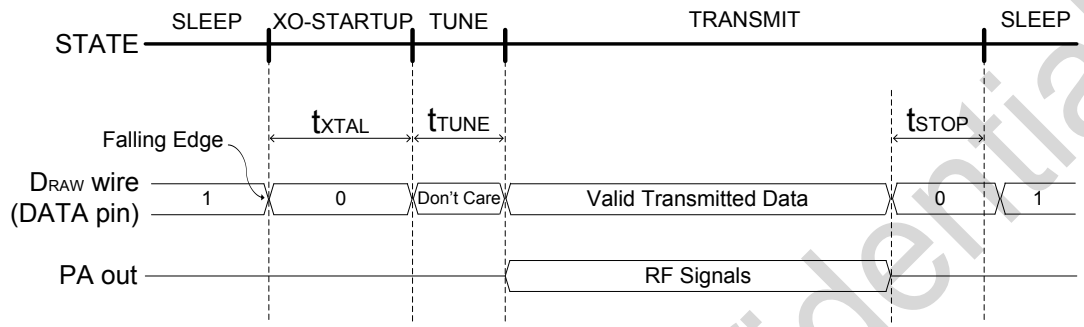


Figure 16. Transmission Enabled by DATA Pin Falling Edge

6.2.2 Tx Enabled by DATA Pin Rising Edge

As shown in the figure below, once the CMT2189C detects a rising edge on the D_{RAW} wire(DATA pin), it goes into the XO-STARTUP state. The user has to pull the D_{RAW} wire high for at least 10 ns (t_{HOLD}) after detecting the rising edge, as well as wait for the sum of t_{XTAL} and t_{TUNE} before sending any useful information (data to be transmitted) into the chip on the D_{RAW} wire. The logic state of the D_{RAW} wire is “Don’t Care” from the end of t_{HOLD} till the end of t_{TUNE}. In the TRANSMIT state, PA sends out the input data after they are modulated. The user has to pull the D_{RAW} wire low for t_{STOP} in order to end the transmission.

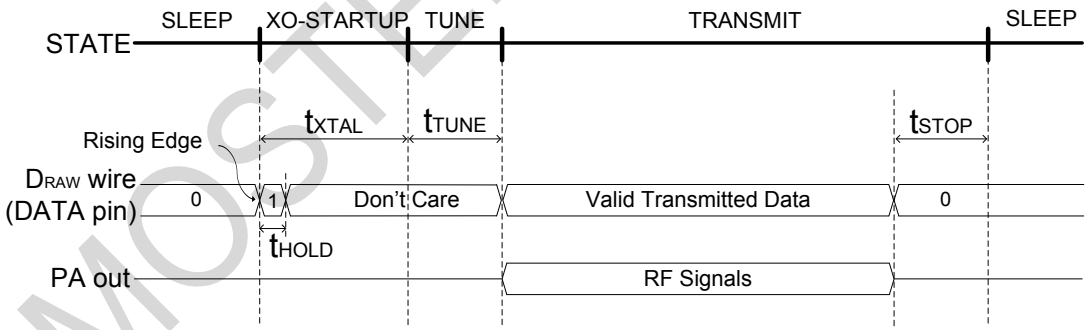


Figure 17. Transmission Enabled by DATA Pin Rising Edge

6.2.3 Two-wire Interface(TWI)

For power-saving and reliable transmission purposes, the CMT2189C is recommended to communicate with the microcontroller core over a two-wire interface (TWI): D_{RAW} (DATA) and CLK. The TWI is designed to operate at a maximum of 1 MHz. The timing requirement and data transmission control through the TWI are shown in this section.

Table 18.TWI Requirements

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Digital Input Level High	V_{IH}		0.8			V_{DD}
Digital Input Level Low	V_{IL}				0.2	V_{DD}
CLK Frequency	F_{CLK}		10		1,000	kHz
CLK High Time	t_{CH}		500			ns
CLK Low Time	t_{CL}		500			ns
CLK Delay Time	t_{CD}	CLK delay time for the first falling edge of the TWI_RST command, see Figure 20	20		15,000	ns
DATA Delay Time	t_{DD}	The data delay time from the last CLK rising edge of the TWI command to the time DATA return to default state			15,000	ns
DATA Setup Time	t_{DS}	From DATA change to CLK falling edge	20			ns
DATA Hold Time	t_{DH}	From CLK falling edge to DATA change	200			ns

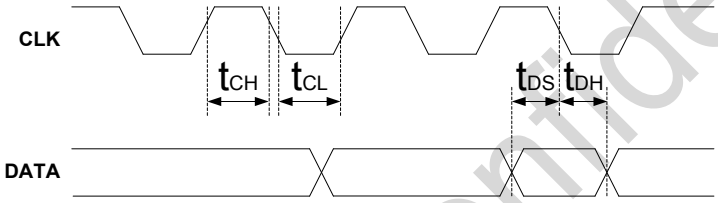


Figure 18.Two-wire Interface Timing Diagram

Once the device is powered up, TWI_RST and SOFT_RST should be issued to make sure the device works in SLEEP state robustly. On every transmission, TWI_RST and TWI_OFF should be issued before the transmission to make sure the TWI circuit functions correctly. TWI_RST and SOFT_RST should be issued again after the transmission for the device going back to SLEEP state reliably till the next transmission. The operation flow with TWI is shown as the figure below.

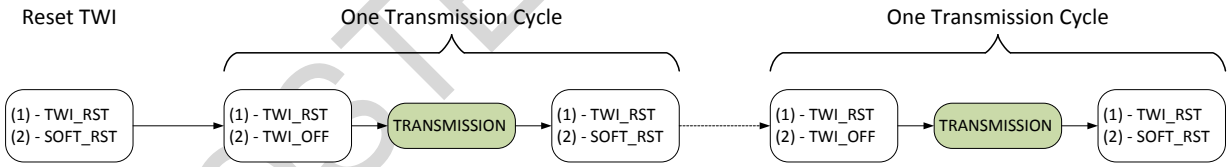


Figure 19. CMT2189C Operation Flow with TWI

Table 19. TWI Commands Descriptions

Command	Descriptions
TWI_RST	Implemented by pulling the DATA pin low for 32 clock cycles and clocking in 0x8D00, 48 clock cycles in total. It only resets the TWI circuit to make sure it functions correctly. The DATA pin cannot detect the Rising/Falling edge to trigger transmission after this command, until the TWI_OFF command is issued. **Notes:** a) Please ensure the DATA pin is firmly pulled low during the first 32 clock cycles. b) When the device is configured as Transmission Enabled by DATA Pin Falling Edge, in order to issue the TWI_RST command correctly, the first falling edge of the CLK should be sent t_{CD} after the DATA falling edge, which should be longer than the minimum DATA setup time 20 ns, and shorter than 15 us,

Command	Descriptions
	as shown in Figure 20. c) When the device is configured as Transmission Enabled by DATA Pin Rising Edge, the default state of the DATA is low, there is no t_{CD} requirement, as shown in Figure 21.
TWI_OFF	Implemented by clocking in 0x8D02, 16 clock cycles in total. It turns off the TWI circuit, and the DATA pin is able to detect the Rising/Falling edge to trigger transmission after this command, till the TWI_RST command is issued. The command is shown as Figure 22.
SOFT_RST	Implemented by clocking in 0xBD01, 16 clock cycles in total. It resets all the other circuits of the chip except the TWI circuit. This command will trigger internal calibration for getting the optimal device performance. After issuing the SOFT_RST command, the host MCU should wait 1 ms before sending in any new command. After that, the device goes to SLEEP state. The command is shown as Figure 23.

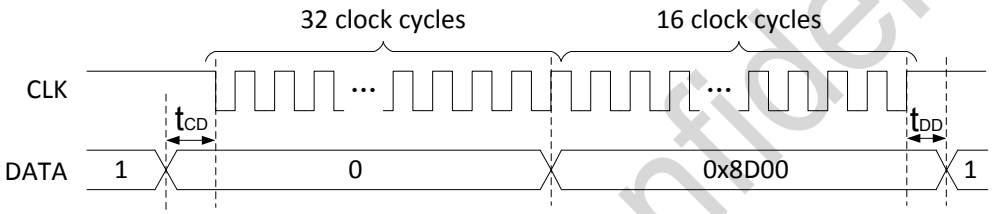


Figure 20. TWI_RST Command When Transmission Enabled by DATA Pin Falling Edge

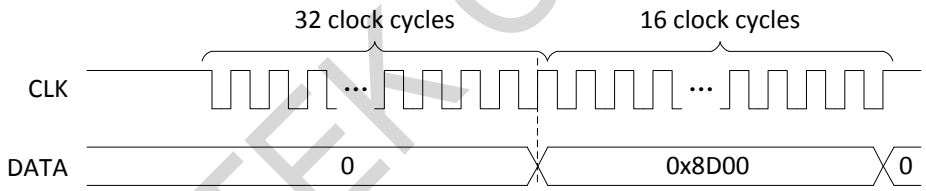


Figure 21. TWI_RST Command When Transmission Enabled by DATA Pin Rising Edge

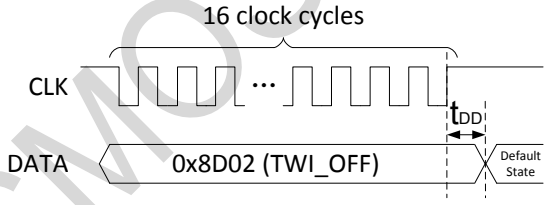


Figure 22. TWI_OFF Command

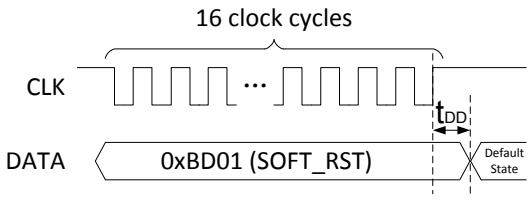


Figure 23. SOFT_RST Command

The DATA is generated by the host MCU on the rising edge of CLK, and is sampled by the device on the falling edge. The CLK should be pulled up by the host MCU during the TRANSMISSION shown in Figure 19. The TRANSMISSION process should refer to Figure 16 or Figure 17 for its timing requirement, depending on the “Start By” setting configured on the RFPDK.

The device will go to SLEEP state by driving the DATA low for t_{STOP}, or issuing SOFT_RST command. A helpful practice for the device to go to SLEEP is to issue TWI_RST and SOFT_RST commands right after the useful data is transmitted, instead of waiting the t_{STOP}, this can save power significantly.

7. RISC Microcontroller Core

The embedded high-performance RISC Microcontroller has the following features:

High-Performance RISC CPU

- 2048 words Flash ROM, 128B SRAM
- 256B EEPROM
- All single-cycle instructions except branches
- Operating Speed
  - DC - 16MHz oscillator
  - 125 ns instruction cycle
- Interrupt Capability
- 8-Level Deep Hardware Stack
- Power-Saving Sleep mode
- Power-on Reset (POR)
- Multiplexed MCLRB/Input Pin

Peripheral Features

- 4 I/O Pins
  - Individual Direction Control
  - Interrupt-on-Pin Change
  - Individual Programmable Weak Pull-ups
- Timer0: 8-bit timer with 3-bit prescaler
- Timer2: 8-bit timer with 3-bit prescaler
- Watchdog timer with on-chip RC oscillator

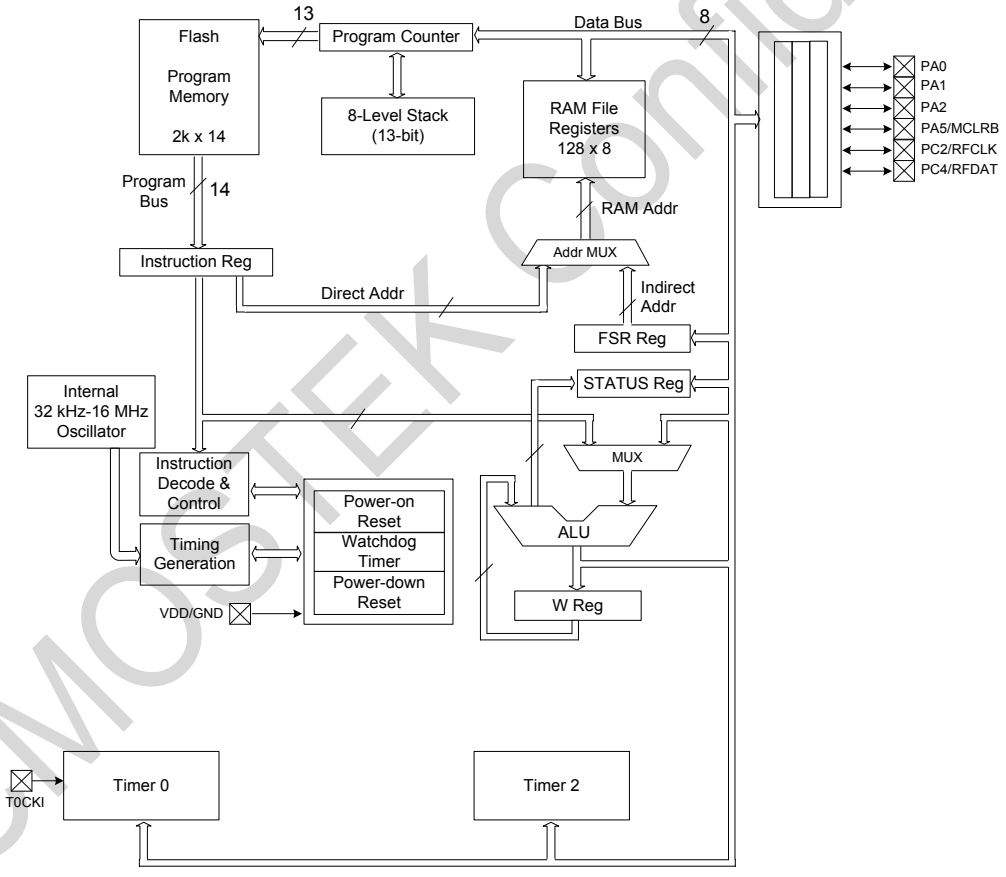


Figure 24.Microcontroller Core Block Diagram

7.1 Memory Organization

7.1.1 Program Memory Organization

The CMT2189C device has 2k x 14 (0000h-07FFh) space for program memory. Accessing a location above these boundaries will cause a wrap-around within the first 2k x 14 space. The Reset Vector is at 0000h and the Interrupt Vector is at 0004h (see figure below).

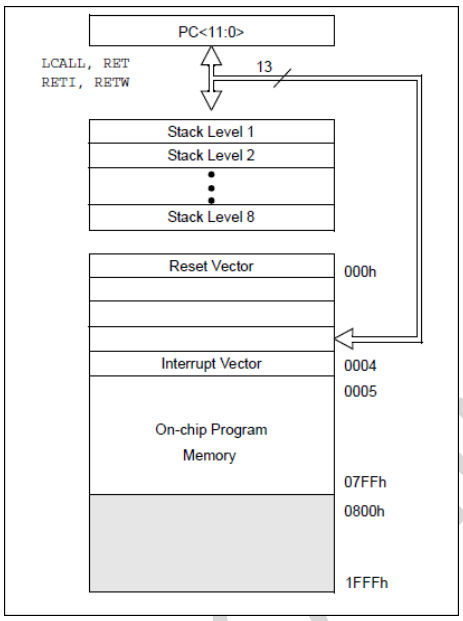


Figure 25. Program Memory Map and Stack

7.1.2 Data Memory Organization

The data memory (see Figure 26) is partitioned into two banks: The General-Purpose Registers and the Special Function Registers. The Special Function Registers are located in the first 32 locations of each bank. Register locations 20h-5Fh are General Purpose Registers, implemented as static RAM and are mapped across both banks. All other RAM is unimplemented and returns '0' when being read. PAGE(STATUS<5>) is the bank select bit.

- PAGE0 = 0 Bank 0 is selected.
- PAGE0 = 1 Bank 1 is selected.

7.1.2.1 General Purpose Register File

The register file is organized as 64 x 8 in theCMT2189C. Each register is accessed, either directly or indirectly, through the FSR.

7.1.2.2 Special Function Register File

The Special Function Registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device. These registers are static RAM. The special registers can be classified into two sets: core and peripheral. The Special Function Registers associated with the "core" are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

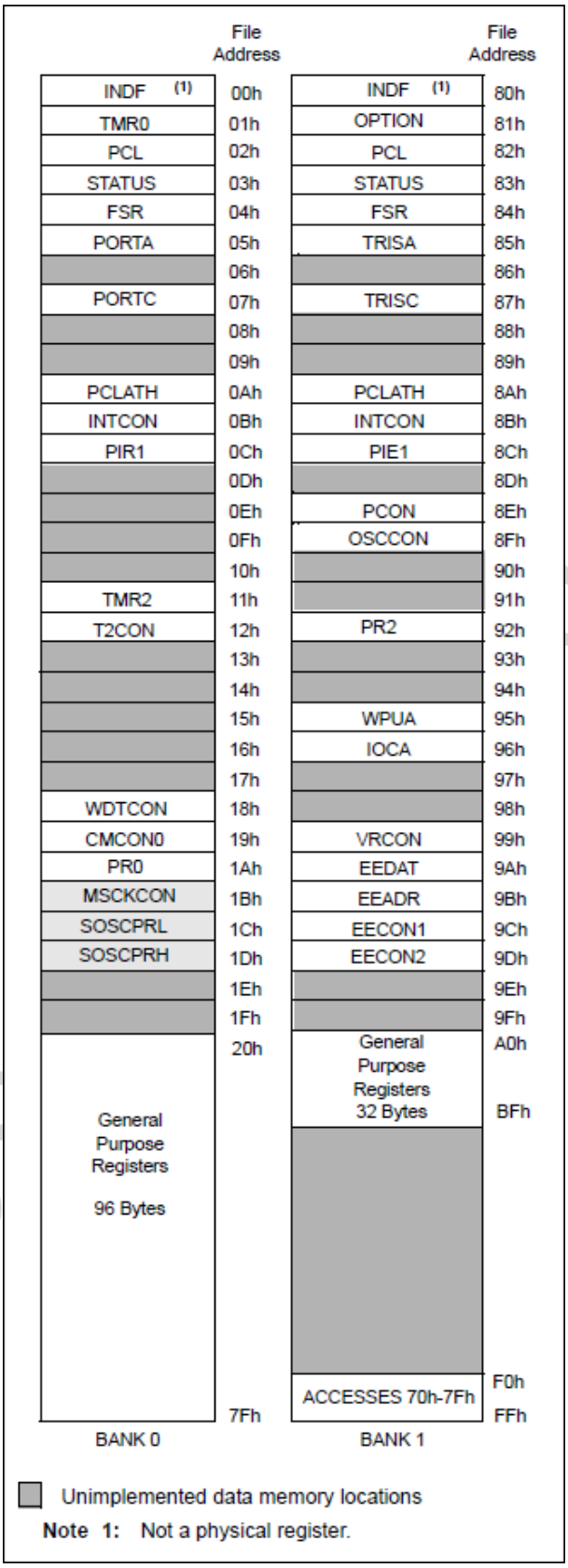


Figure 26. Data Memory Map of the CMT2189C

Table 20. CMT2189C Special Registers Summary Bank0

ADDR	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	POR reset
0	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx
1	TMR0	Timer0 Module's register, Timer0<7:0>								xxxx xxxx
2	PCL	Program Counter's (PC) Least Significant Byte, PC<7:0>								0000 0000
3	STATUS	-	-	PAGE	/TF	/PF	Z	HC	C	--01 1xxx
4	FSR	Indirect Data Memory Address Pointer								
5	PORTA	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	00x0 0000
6										---- ----
7	PORTC	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	0000 0000
8										---- ----
9										---- ----
A	PCLATH	-	-	-	Write Buffer for upper 5 bits of Program Counter, PC<13:8>					---0 0000
B	INTCON	GIE	PEIE	T0IE	INTE	PAIE	T0IF	INTF	PAIF	0000 0000
C	PIR1	EEIF	CKMEAIF	-	C2IF	C1IF	OSFIF	TMR2IF	-	00-0 000-
D										---- ----
E										---- ----
F										---- ----
10										---- ----
11	TMR2	Timer2 Module register, Timer2<7:0>								0000 0000
12	T2CON	-	TOUTPS<3:0>				TMR2ON	T2CKPS<1:0>		-000 0000
13										---- ----
14										---- ----
15										---- ----
16										---- ----
17										---- ----
18	WDTCON	-	-	-	WDTPS<3:0>				SWDTEN	---0 1000
19	CMCON0	C2OUT	C1OUT	C2INV	C1INV	CIS	CM<2:0>			0000 0000
1A	PR0	PR0<7:0>								1111 1111
1B	MSCKCON	-	-	-	SLVREN	-	CKMAVG	CKCNTI	-	---0 -00-
1C	SOSCPPRL	SOSCPR<7:0>								1111 1111
1D	SOSCPRH	-	-	-	-	SOSCPR<11:8>				---- 1111
1E										---- ----
1F										---- ----

Table 21. CMT2189C Special Function Registers Summary Bank1

ADDR	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	POR reset
80	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx
81	OPTION	/PAPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111
82	PCL	Program Counter's (PC) Least Significant Byte, PC<7:0>								0000 0000
83	STATUS	-	-	PAGE	/TF	/PF	Z	HC	C	--01 1xxx
84	FSR	Indirect Data Memory Address Pointer								
85	TRISA	TRISA<7:6>		--	TRISA<4:0>					11x1 1111
86										---- ----
87	TRISC	TRISC<7:0>								1111 1111
88										---- ----
89										---- ----
8A	PCLATH	-	-	-	Write Buffer for upper 5 bits of Program Counter, PC<13:8>					---0 0000
8B	INTCON	GIE	PEIE	T0IE	INTE	PAIE	T0IF	INTF	PAIF	0000 0000
8C	PIE1	EEIE	CKMEAIE	-	C2IE	C1IE	OSFIE	TMR2IE	-	00-0 000-
8D										---- ----
8E	PCON							/POR	/BOR	---- --qq
8F	OSCCON	LFMOD	IRCF[2:0]			OSTS	HTS	LTS	SCS	0101 x000
90										---- ----
91										0000 0000
92	PR2	PR2[7:0], Timer2 period register								1111 1111
93										---- ----
94										---- ----
95	WPUA	WPUA<7:6>		-	WPUA<4:0>					11-1 1111
96	IOCA	IOCA<7:0>								---- ----
97										---- ----
98										---- ----
99	VRCON	VREN	-	VRR	-	VR<3:0>				0-0- 0000
9A	EEDAT	EEDAT<7:0>								0000 0000
9B	EEADR	EEADR<7:0>								0000 0000
9C	EECON1	-	-	WREN3	WREN2	WRERR	WREN1	-	RD	--00 x0-0
9D	EECON2	-	-	-	-	-	-	-	WR	---- ---0
9E										---- ----
9F										---- ----

7.2 Port A

There have four general purpose I/O pins available, PA0~PA2, and PA5, as shown in the table below. Depending on which peripherals are enabled, some or all of the pins may not be available as general purpose I/O. In general, when a peripheral is enabled, the associated pin may not be used as a general purpose I/O pin.

Table 22. Mapping from the GPIOs to the Pinouts

GPIO	Pinout
PA0	PA0/ICSPCLK
PA1	PA1/ICSPDAT
PA2	PA2
PA5	PA5/MCLRB

7.2.1 PORTA and the CPIOA Registers

PORTA is a 6-bit wide, bidirectional port. The corresponding data direction register is TRISA. Setting a TRISA bit (= 1) will make the corresponding PORTA pin as input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin as output (i.e., put the contents of the output latch on the selected pin). The exception is PA5, which is input only and its TRISA bit will always read as '1'.

Reading the PORTA register reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read; this value is modified and then written to the PORT data latch. PA5 reads '0' when MCLRE = 1.

7.2.2 Additional Pin Functions

Every PORTA pin on the CMT2189C has an interrupt-on-change(IOC) option and every PORTA pin has a pull-up option.

7.2.2.1 Pull-up

Each of the PORTA pinshas an individually configurable internal pull-up. Control bits WPUA enable or disable each pull-up.

7.2.2.2 Interrupt-On-Change

Each of the PORTA pins is individually configurable as an interrupt-on-change pin. Control bits IOCA enable or disable the interrupt function for each pin. The interrupt-on-change is disabled on a Power-on Reset. For enabled interrupt-on-change pins, the values are compared with the old value latched on the last read of PORTA. The 'mismatch' outputs of the last read are OR'd together to set, the PORTA Change Interrupt Flag bit (PAIF) in the INTCON register. This interrupt can wake the device from Sleep. The user, in the Interrupt Service Routine, can clear the interrupt by:

1) Any read or write of PORTA. This will end the mismatch condition, then.
2) Clear the flag bit PAIF.

A mismatch condition will continue to set flag bit PAIF. Reading PORTA will end the mismatch condition and allow flag bit PAIF to be cleared. The latch holding the last read value is not affected by a MCLR nor BOD Reset. After these resets, the PAIF flag will continue to be set if a mismatch is present.

7.3 PORTC

PORTC is a general purpose I/O port consisting of 6bidirectional pins. The pins can be configured for either digital I/O, but only PC2 and PC4 has been pin out. PC2 is connected to the TWI's CLK, and PC4 is connected to the TWI's DAT. Both are used to configuration the RF parameters.

Table 23. Mapping from the TWI to the Pinouts

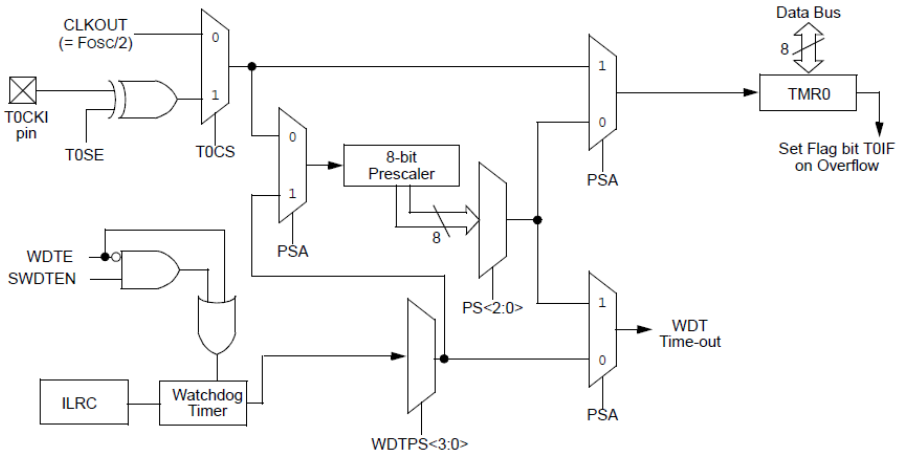
GPIO	RF Part
PC2	CLK
PC4	DAT

7.4 Timer0 Module

The Timer0 module timer/counter has the following features.

- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

Figure 27is a block diagram of the Timer0 module and the prescaler shared with the WDT.



Note 1: T0SE, T0CS, PSA, PS<2:0> are bits in the Option register, WDTPS<3:0> are bits in the WDTCON register.

Figure 27. Block Diagram of the Timer0/WDT Prescaler

7.4.1 Timer0 Operation

Timer mode is selected by clearing the T0CS bit(OPTION<5>). In Timer mode, the Timer0module will increment every instruction cycle (without prescaler). If TMR0 is written, the increment is in habited for the following two instruction cycles. The user can work around this by writing an adjusted value to theTMR0 register.

Counter mode is selected by setting the T0CS bit(OPTION<5>). In this mode, the Timer0 module will increment either on every rising or falling edge of pin PA2/T0CKI. The incrementing edge is determined by the source edge (T0CE) control bit(OPTION<4>). Clearing the T0CE bit selects the rising edge.

7.4.2 Timer0 Interrupt

A Timer0 interrupt is generated when the TMR0register timer/counter overflows from FFh to 00h. This overflow sets the T0IF bit. The interrupt can be masked by clearing the T0IE bit (INTCON<5>). The T0IF bit(INTCON<2>) must be cleared in software

by theTimer0 module Interrupt Service Routine before re-enabling this interrupt. The Timer0 interrupt can not wake the processor from Sleep, since the timer is shutoff during Sleep.

7.4.3 Using Timer0 with an External Clock

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI, with the internal phase clocks, is accomplished by sampling the prescaler output on the Q2 andQ4 cycles of the internal phase clocks. Therefore, it is necessary for T0CKI to be high for at least $2T_{OSC}$(and a small RC delay of 20 ns) and low for at least $2T_{OSC}$(and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

7.4.4 Prescaler

An 8-bit counter is available as a prescaler for theTimer0 module, or as a postscaler for the Watchdog Timer. For simplicity, this counter will be referred to as “prescaler” throughout this Datasheet. The prescaler assignment is controlled in software by the control bit PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. Prescale values are selectable via the PS2:PS0 bits (OPTION<2:0>). The prescaler is not readable or writable. When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRR 1, STWR 1,BSR 1, x....etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the Watchdog Timer.

7.5 Timer2 Module

Figure 28shows the basic block diagram of the Timer2 module.

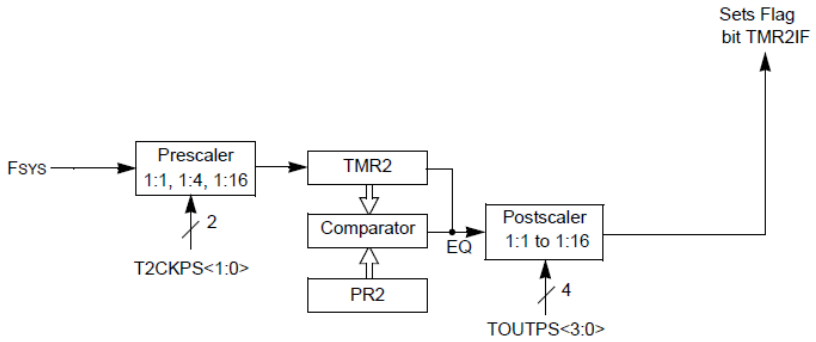


Figure 28. Timer2 Block Diagram

8. Ordering Information

Table 24. CMT2189C Ordering Information

Part Number	Descriptions	Package Type	Package Option	Operating Condition	MOQ / Multiple
CMT2189C-ESR[1]	240 – 960 MHz SoC (G)FSK/OOK Transmitter	SOP14	Tape & Reel	2.0 to 3.6 V, -40 to 85 ℃	2,500
CMT2189C-ESB[1]	240 – 960 MHz SoC (G)FSK/OOK Transmitter	SOP14	Tube	2.0 to 3.6 V, -40 to 85 ℃	1,000

Notes:

[1]. "E" stands for extended industrial product grade, which supports the temperature range from -40 to +85 ℃.
"S" stands for the package type of SOP14.
"R" stands for the tape and reel package option, the minimum order quantity (MOQ) for this option is 2,500 pcs. "B" stands for the tube package option, with the MOQ of 1,000 pcs.

Visit www.cmostek.com/products to know more about the product and product line.
Contact sales@cmostek.com or your local sales representatives for more information.

9. Package Outline

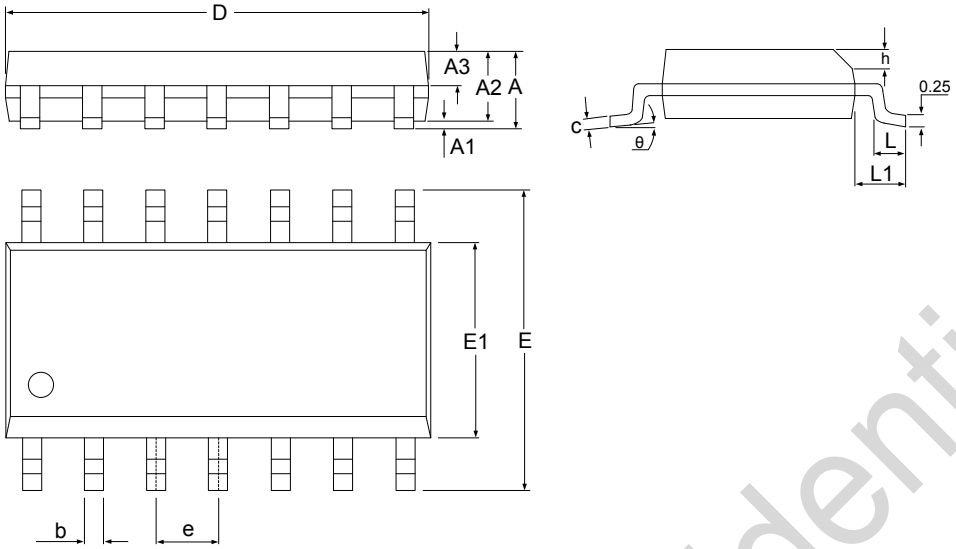


Figure 29.14-Pin SOP Package

Table 25.14-Pin SOP Package Dimensions

Symbol	Size (millimeters)		
	Min	Typ	Max
A	-	-	1.75
A1	0.05	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.48
C	0.21	-	0.26
D	8.45	8.65	8.85
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27 BSC		
h	0.25	-	0.50
L	0.30	-	0.60
L1	1.05 BSC		
θ	0	-	8°

10. Top Marking

10.1 CMT2189C Top Marking

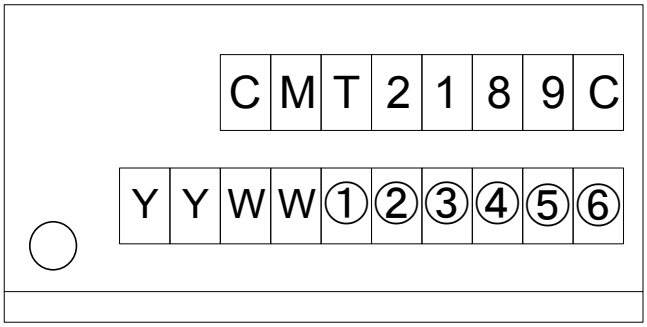


Figure 30.CMT2189C Top Marking

Table 26. CMT2189C Top Marking Explanation

Mark Method :	Laser
Pin 1 Mark :	Circle's diameter = 1 mm.
Font Size :	0.35 mm, right-justified.
Line 1 Marking :	CMT2189C represents part number CMT2189C
Line 2 Marking :	YYWW is the Date code assigned by the assembly house. YY represents the last two digits of the mold year and WW represents the workweek. ①②③④⑤⑥is the internal tracking number.

11. Other Documentations

Table 27. Other Documentations for CMT2189C

Brief	Name	Descriptions
AN100	CMT211x-5x-8x Schematic and PCB Layout Design Guideline(CN)	Details of CMT211x, CMT215x & CMT218x PCB schematic and layout design rules, RF matching network and other application layout design related issues.
AN132	CMT2180/89AConfiguration Guideline(EN)	Details of configuring CMT2180/89A features on the RFPDK.
AN202	CMT2189C User Guide(CN)	Details of using the CMT2189C

12. Document Change List

Table 28. Document Change List

Rev. No.	Chapter	Description of Changes	Date
0.8	All	Initial Released	2018-1-1

13. Contact Information

CMOSTEK Microelectronics Co., Ltd.
Room 202, Honghai Building, Qianhai Road. Nanshan District
Shenzhen, Guangdong, China PRC
Zip Code: 518000
Tel: 0755- 83235017
Fax: 0755- 82761326
Sales: sales@cmostek.com
Technical support: support@cmostek.com
www.cmostek.com