CML Semiconductor Products

Calling Line Identifier *plus* Call Waiting (Type II) CMX602A

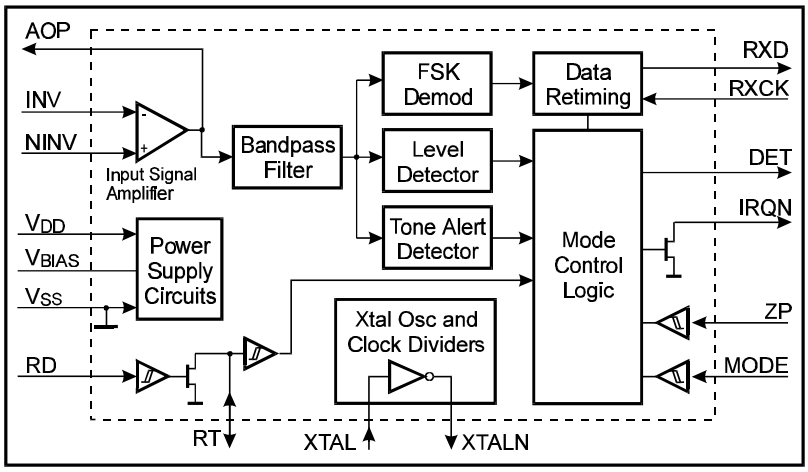
D/602A/4 February 1998 Provisional Issue

Features

- **CLI and CIDCW System Operation**
- **Low Power Operation 0.5mA at 2.7V**
- **Zero-Power Ring or Line Reversal Detector**
- **FSK Demodulator with Data Retiming**
- **High Sensitivity CAS Tone Detection**
- **Low CAS Tone Falsing in CIDCW Mode**

Applications

- **CLI and CIDCW Adjunct Boxes**
- **CLI and CIDCW Feature Phones**
- **Bellcore, ETSI, British Telecom and Mercury Systems**
- **Computer Telephone Integration**
- **Call Logging Systems**
- **Voice-Mail Equipment**



1.1 Brief Description

The CMX602A is a low power CMOS integrated circuit for the reception of the physical layer signals used in BT's Calling Line Identification Service (CLIP), Bellcore's Calling Identity Delivery System (CID), the Cable Communications Association's Caller Display Services (CDS), and similar evolving systems. It also meets the requirements of emerging Caller Identity with Call Waiting services (CIDCW).

The device includes a 'zero-power' ring or line reversal detector, a dual-tone (2130Hz plus 2750Hz) Tone Alert Signal and a 1200-baud FSK V23/Bell202 compatible asynchronous data demodulator with a data retiming circuit which removes the need for a UART in the associated µController.

It is suitable for use in systems to BT specifications SIN227 and SIN242, Bellcore GR-30-CORE and SR-TSV-002476, CCA TW/P&E/312, ETSI ETS 300 659 parts 1 and 2, ETS 300 778 parts 1 and 2 and Mercury Communications MNR 19.

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1.2 Block Diagram

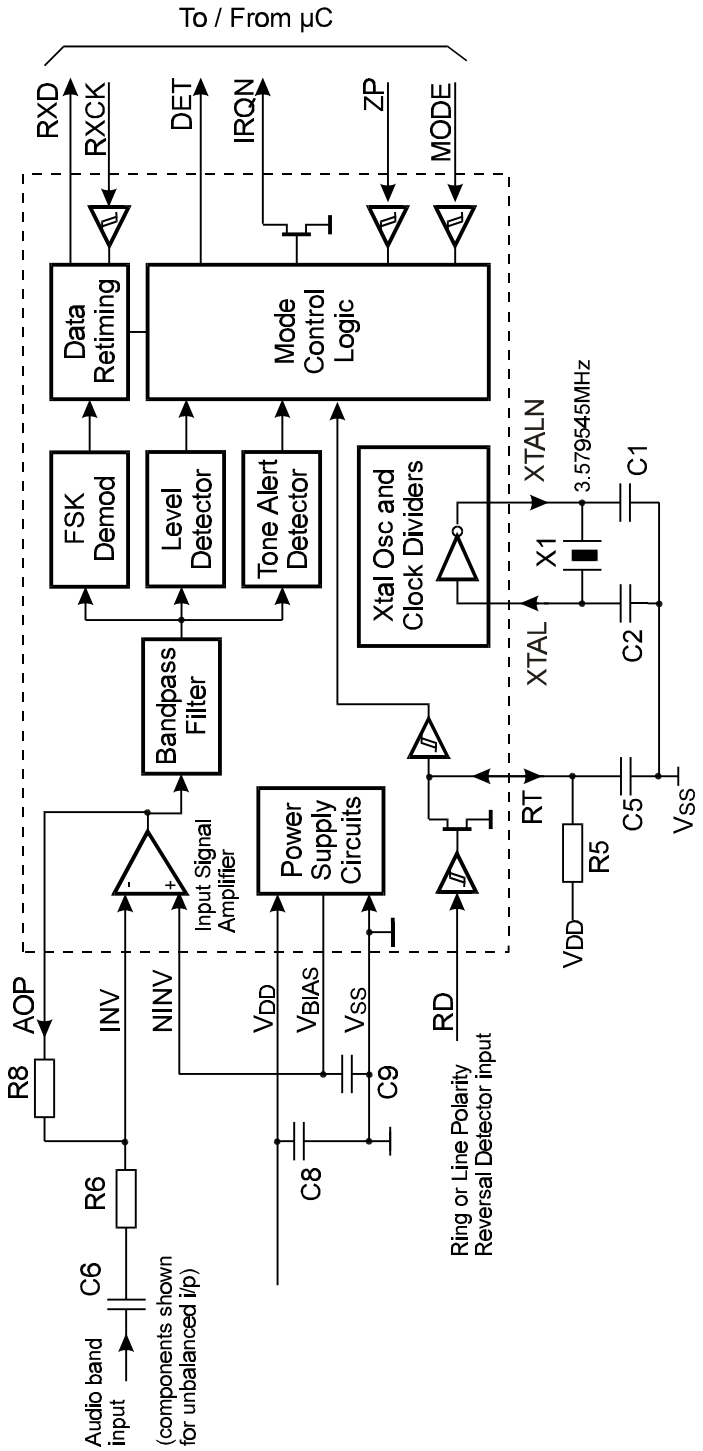


Figure 1 Block Diagram

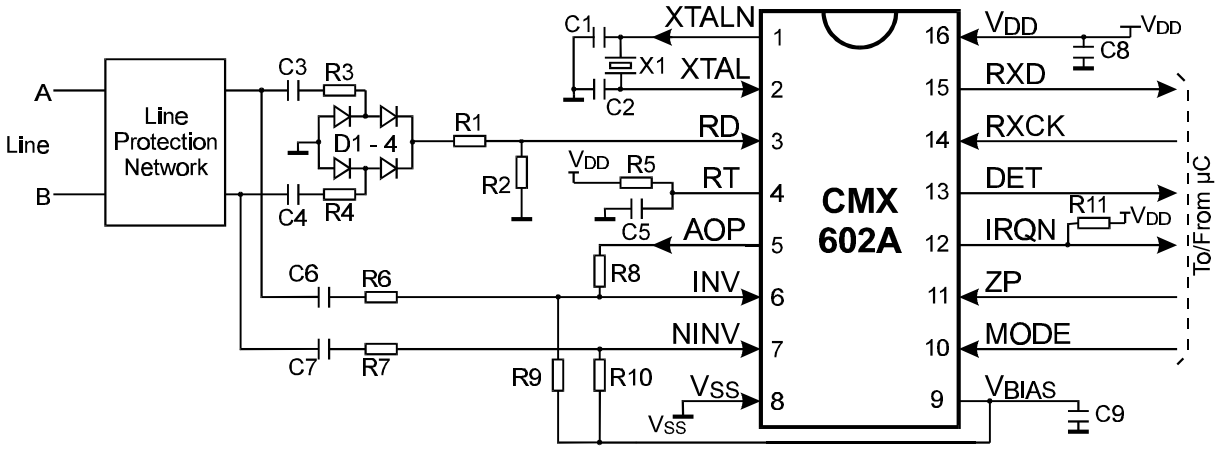
1.3 Signal List

Packages D4 / P3	Signal		Description
Pin No.	**Name**	**Type**	
1	XTALN	O/P	The output of the on-chip Xtal oscillator inverter.
2	XTAL	I/P	The input to the on-chip Xtal oscillator inverter.
3	RD	I/P (S)	Input to the Ring or Line Polarity Reversal Detector.
4	RT	BI	Open-drain output and Schmitt trigger input forming part of the Ring or Line Polarity Reversal detector. An external resistor to V_{DD} and a capacitor to V_{SS} should be connected to RT to filter and extend the RD input signal.
5	AOP	BI	The output of the on-chip Input Signal Amplifier and the input to the Bandpass Filter.
6	INV	I/P	The inverting input to the on-chip Input Signal Amplifier.
7	NINV	I/P	The non-inverting input to the on-chip Input Signal Amplifier.
8	V_{SS}	Power	Negative supply rail (signal ground).
9	V_{BIAS}	O/P	Internally generated bias voltage, held at $V_{DD}/2$ when the device is not in 'Zero-Power' mode. Should be decoupled to V_{SS} by a capacitor mounted close to the device pins.
10	MODE	I/P (S)	Input used to select the operating mode. See section 1.5.1.
11	ZP	I/P (S)	A high level on this input selects 'Zero-Power' mode, a low level enables the V_{BIAS} supply, the Input Signal Amplifier, the Bandpass Filter and either the FSK or the Tone Alert circuits depending on the MODE input.

Packages D4 / P3	Signal		Description
Pin No.	**Name**	**Type**	
12	IRQN	O/P	An open-drain active low output that may be used as an Interrupt Request / Wake-up input to the associated µC. An external pull-up resistor should be connected between this output and V_{DD}.
13	DET	O/P	A logic level output driven by the Ring or Line Polarity Reversal Detector, the Tone Alert Detector or the FSK Level detect circuits, depending on the operating mode. See section 1.5.1.
14	RXCK	I/P (S)	An input which may be used to clock received data bits out of the FSK Data Retiming block.
15	RXD	O/P	A logic level output carrying either the raw output of the FSK Demodulator or re-timed 8-bit characters depending on the state of the RXCK input. See section 1.5.6
16	V_{DD}	Power	The positive supply rail. Levels and thresholds within the device are proportional to this voltage. Should be decoupled to V_{SS} by a capacitor mounted close to the device pins.

Notes: I/P = Input
I/P (S) = Schmitt trigger input
O/P = Output
BI = Bidirectional

1.4 External Components



R1	470kΩ		
R2	See section 1.5.8	C1, C2	18pF
R3, R4, R5	470kΩ	C3, C4	0.1µF
R6, R7	470kΩ	C5	0.33µF
R8	470kΩ for V_{DD} = 3.3V 680kΩ for V_{DD} = 5.0V (See section 1.5.2)	C6, C7	680pF
		C8,C9	0.1µF
R9	240kΩ for V_{DD} = 3.3V 200kΩ for V_{DD} = 5.0V (See section 1.5.2)		
R10	160kΩ	X1	3.579545MHz
R11	100kΩ ±20%	D1 - D4	1N4004

Resistors ±1%, capacitors ±20% unless otherwise stated.

Figure 2 Recommended External Components for Typical Application

It is recommended that the printed circuit board is laid out with a ground plane in the CMX602A area to provide a low impedance ground connection to the V_{SS} pin and to the decoupling capacitors C8 and C9.

1.5 General Description

1.5.1 Mode Control Logic

The CMX602A's operating mode and the source of the DET and IRQN outputs are determined by the logic levels applied to the MODE and ZP input pins;

ZP	MODE	Mode	DET o/p from	IRQN o/p from
0	0	Tone Alert Detect	Tone Alert Signal Detection	Valid 'off-hook' CAS. Ring or Line Polarity Reversal Detector.
0	1	FSK Receive	FSK Level Detector	FSK Data Retiming [1]. Ring or Line Polarity Reversal Detector.
1	0	'Zero-Power'	Ring or Line Polarity Reversal Detector.	Ring or Line Polarity Reversal Detector.
1	1	'Zero-Power'	Ring or Line Polarity Reversal Detector.	-

[1] If enabled.

In the 'Zero-Power' modes, power is removed from all of the internal circuitry except for the Ring or Line Polarity Reversal Detector and the DET and IRQN outputs.

1.5.2 Input Signal Amplifier

This amplifier is used to convert the balanced FSK and Tone Alert signals received over the telephone line to an unbalanced signal of the correct amplitude for the FSK receiver and Tone Alert Detector circuits.

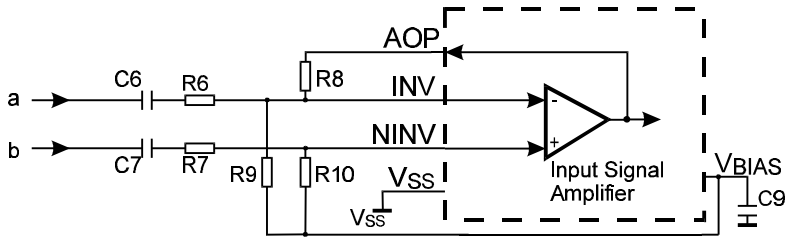


Figure 3a : Input Signal Amplifier, balanced input configuration

The design equations for this circuit are;

Differential voltage gain V_{AOP} / V(b-a) = R8/R6
R6 = R7 = 470kΩ
R10 = 160kΩ
R9 = R8 x R10 / (R8 - R10)

The target differential voltage gain depends on the expected signal levels between the A and B wires and the CMX602A's internal threshold levels, which are proportional to the supply voltage.

The CMX602A has been designed to meet the applicable specifications with R8 = 430kΩ at V_{DD} = 3.0V nominal, rising to 680kΩ at V_{DD} = 5.0V, and R9 should be 240kΩ at V_{DD} = 3.0V and 200kΩ at V_{DD} = 5.0V as shown in section 1.4 and Fig 3c.

The Input Signal Amplifier may also be used with an unbalanced signal source as shown in Figure 3b. The values of R6 and R8 are as for the balanced input case.

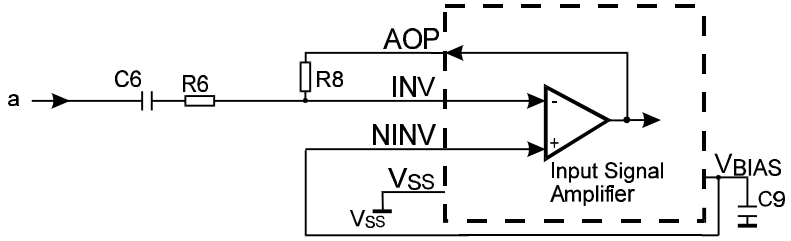


Figure 3b : Input Signal Amplifier, unbalanced input configuration

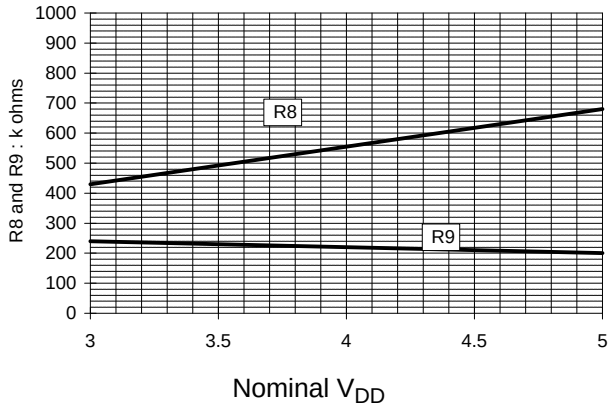


Figure 3c : Input Signal Amplifier, optimum values of R8 and R9 vs V_{DD}

1.5.3 Bandpass Filter

Is used to attenuate out of band noise and interfering signals which might otherwise reach the FSK Demodulator, Tone Alert Detector and Level Detector circuits. The characteristics of this filter differ in FSK and Tone Alert modes. Most of the filtering is provided by Switched Capacitor stages clocked at 57.7kHz.

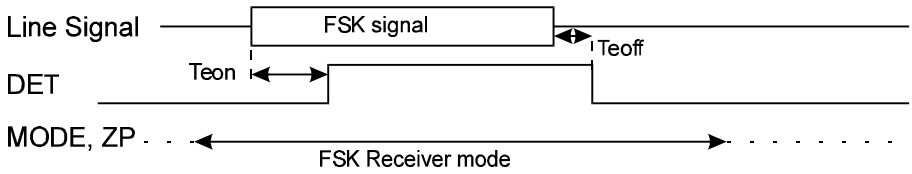
1.5.4 Level Detector

This block operates by measuring the level of the signal at the output of the Bandpass Filter, and comparing it against a threshold which depends on whether FSK Receive or Tone Alert Detect mode has been selected.

In Tone Alert Detect mode the output of the Level Detector block provides an input to the Tone Alert Signal Detector.

In FSK Receive mode the CMX602A DET output will be set high when the level has exceeded the threshold for sufficient time. Amplitude and time hysteresis are used to reduce chattering of the DET output in marginal conditions.

Note that in FSK Receive mode this circuit may also respond to non-FSK signals such as speech.



See section 1.7.1 for definitions of Teon and Teoff

Figure 4 : FSK Level Detector operation

1.5.5 FSK Demodulator

This block converts the 1200 baud FSK input signal to a logic level received data signal which is output via the RXD pin as long as the Data Retiming function is not enabled (see section 1.5.6). This output does not depend on the state of the FSK Level Detector output.

Note that in the absence of a valid FSK signal, the demodulator may falsely interpret speech or other extraneous signals as data.

1.5.6 FSK Data Retiming

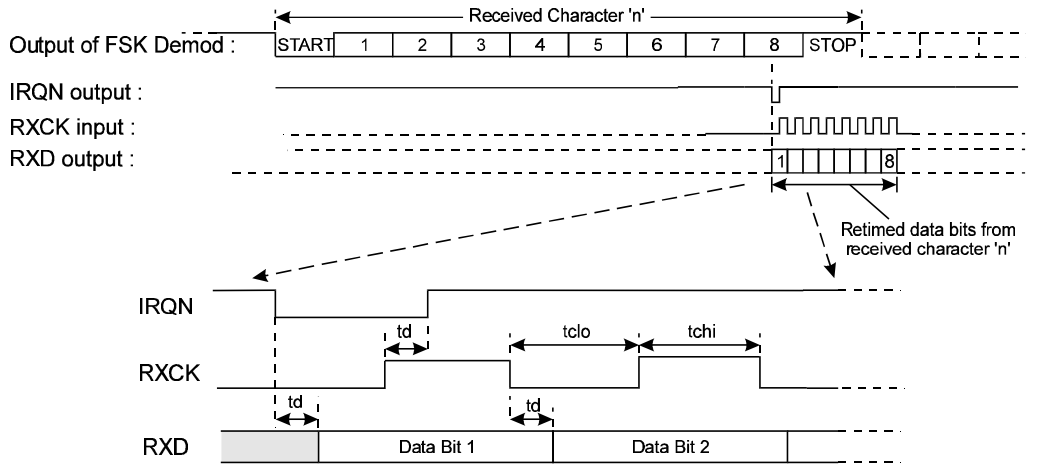
The Data Retiming block extracts the 8 data bits of each character from the received asynchronous data stream, and presents them to the µC under the control of strobe pulses applied to the RXCK input. The timing of these pulses is not critical and they may easily be generated by a simple software loop. This facility removes the need for a UART in the µC without incurring an excessive software overhead.

The block operates on a character by character basis by first looking for the mark to space transition which signals the beginning of the start bit, then, using this as a timing reference, sampling the output of the FSK Demodulator in the middle of each of the following 8 received data bits, storing the results in an internal 8-bit shift register.

When the eighth data bit has been clocked into the internal shift register, the CMX602A examines the RXCK input. If this is low then the IRQN output will be pulled low and the first of the stored data bits put onto the RXD output pin. On detecting that the IRQN output has gone low, the µC should pulse the RXCK pin high 8 times. The high to low transition at the end of the first 7 of these pulses will be used by the CMX602A to shift the next data bit from the shift register onto the RXD output. At the end of the eighth pulse the FSK Demodulator output will be reconnected to the RXD output pin. The IRQN output will be cleared the first time the RXCK input goes high.

Thus to use the Data Retiming function, the RXCK input should be kept low until the IRQN output goes low; if the Data Retiming function is not required the RXCK input should be kept high.

The only restrictions on the timing of the RXCK waveform are those shown in Figure 5a and the need to complete the transfer of all eight bits into the µC within 8.3ms (the time of a complete character at 1200 baud).



td = Internal CMX602A delay; max. 1µS tclo = RXCK low time; min 1µS tchi = RXCK high time; min 1µS

Figure 5a : FSK Operation With Data Retiming

Note that, if enabled, the Data Retiming block will interpret the FSK Channel Seizure signal (a sequence of alternating mark and space bits) as valid received characters, with values of 55 (hex). Similarly it may interpret speech or other signals as random characters.

If the Data Retiming facility is not required, the RXCK input to the CMX602A should be kept high. The asynchronous data from the FSK Demodulator will then be connected directly to the RXD output pin, and the IRQN output will not be activated by the FSK signal. This case is illustrated in Figure 5b.

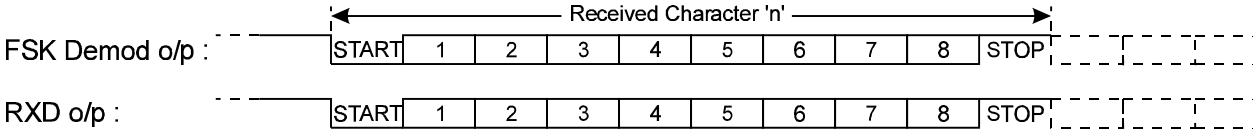


Figure 5b : FSK Operation Without Data Retiming (RXCK always high)

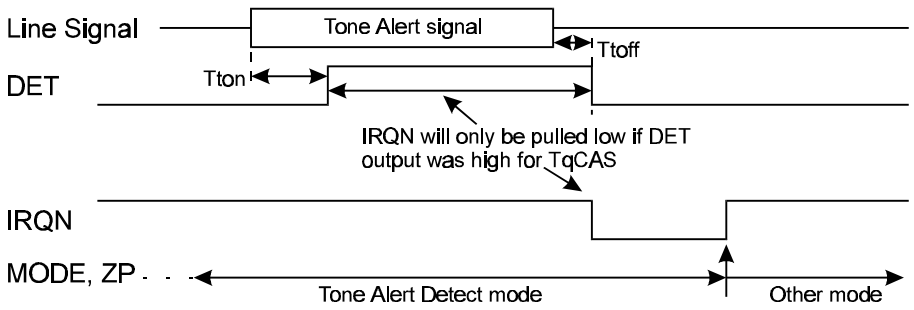
1.5.7 Tone Alert Detector

This block is enabled when the CMX602A is set to Tone Alert Detect mode. It will then monitor the received signal for the presence of simultaneous 2130 and 2750Hz tones of sufficient level and duration.

Two digital bandpass filters, centred around 2130Hz and 2750Hz, are used within the block to give additional rejection of interfering signals.

The CMX602A DET output will be set high while a Tone Alert signal is detected.

When the DET output goes low at the end of the Tone Alert signal, then if the DET output had been high for a time within the CAS qualifying time TqCAS limits (see 1.7.1) , then the IRQN output will be pulled low and will remain low until the CMX602A is switched out of Tone Alert Detect mode. Note that the TqCAS timing has been optimised for the detection of 75 to 85ms Tone Alert (CAS) signals used in off-hook applications, the longer (88 to 110ms) Tone Alert signal employed by BT for on-hook applications will not necessarily cause IRQN to go low.



See section 1.7.1 for definitions of Tton, Ttoff and TqCAS

Figure 6 : Tone Alert Detector operation

1.5.8 Ring or Line Polarity Reversal Detector

These circuits are used to detect the Line Polarity Reversal and Ringing signals associated with the Calling Line Identification protocol.

Figure 7 illustrates their use in a typical application.

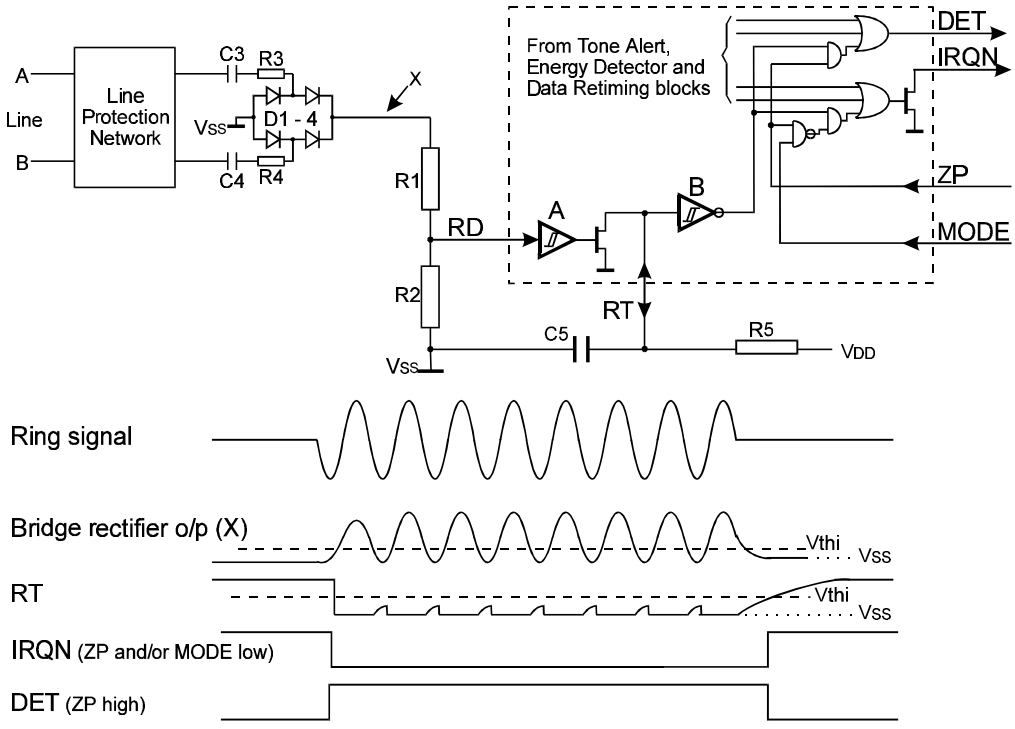


Figure 7 : Ring or Line Polarity Reversal operation

When no signal is present on the telephone line, RD will be at V_{SS} and RT pulled to V_{DD} by R5 so the output of the Schmitt trigger 'B' will be low.

The ring signal is usually applied at the subscriber's exchange as an ac voltage inserted in series with one of the telephone wires and will pass through either C3 and R3 or C4 and R4 to appear at the top end of R1 (point X in Figure 7) in a rectified and attenuated form.

The signal at point X will be further attenuated by the potential divider formed by R1 and R2 before being applied to the CMX602A input RD . If the amplitude of the signal appearing at RD is greater than the input threshold (Vthi) of Schmitt trigger 'A' then the N transistor connected to RT will be turned on, pulling the voltage at RT to V_{SS} by discharging the external capacitor C5. The output of the Schmitt trigger 'B' will then go high, activating the DET and/or IRQN outputs depending on the states of the MODE and ZP inputs.

The minimum amplitude ringing signal that is certain to be detected is

$$(0.7 + Vthi \times [R1 + R2 + R3] / R2) \times 0.707 \quad Vrms$$

where Vthi is the high-going threshold voltage of the Schmitt trigger A (see section 1.7).

With R1, R3 and R4 all 470kΩ as Figure 2, then setting R2 to 68kΩ will guarantee detection of ringing signals of 40Vrms and above for V_{DD} over the range 2.7 to 5.5V.

A line polarity reversal may be detected using the same circuit but there will be only one pulse at RD. The BT specification SIN242 says that the circuit must detect a +15V to -15V reversal between the two lines slewing in 30ms. For a linearly changing voltage at the input to C3 (or C4), then the voltage appearing at the RD pin will be

$$dV/dt \times C3 \times [1 - \exp(-t/T)] \times R2$$

where T = C3 x (R1 + R2 + R3) and dV/dt is the input slew rate.

For dV/dt = 500V/sec (15V in 30ms), R1, R3 and R4 all 470kΩ and C3, C4 both 0.1µF as Figure 2, then setting R2 to 390kΩ will guarantee detection at V_{DD} = 5.5V.

If the time constant of R5 and C5 is large enough then the voltage on RT will remain below the threshold of the 'B' Schmitt trigger keeping the DET and/or IRQN outputs active for the duration of a ring cycle
The time for the voltage on RT to charge from V_{SS} towards V_{DD} can be derived from the formula

$$V_{RT} = V_{DD} \times [1 - \exp(-t/(R5 \times C5))]$$

As the Schmitt trigger high-going input threshold voltage (Vthi) has a minimum value of 0.56 x V_{DD} , then the Schmitt trigger B output will remain high for a time of at least 0.821 x R5 x C5 following a pulse at RD.

Using the values given in Figure 2 (470kΩ and 0.33µF) gives a minimum time of 100 ms (independent of V_{DD}), which is adequate for ring frequencies of 10Hz or above.

If necessary, the µC can distinguish between a ring and a reversal by timing the length of the IRQN or DET output.

1.5.9 Xtal Osc and Clock Dividers

Frequency and timing accuracy of the CMX602A is determined by a 3.579545MHz clock present at the XTAL pin. This may be generated by the on-chip oscillator inverter using the external components C1, C2 and X1 of Figure 2, or may be supplied from an external source to the XTAL input, in which case C1, C2 and X1 should not be fitted.

The oscillator is turned off in the 'Zero-Power' modes.

If the clock is provided by an external source which is not always running, then the ZP input must be set high when the clock is not available. Failure to observe this rule may cause a significant rise in the supply current drawn by CMX602A as well as generating undefined states of the RXD, DET and IRQN outputs.

1.6 Application Notes

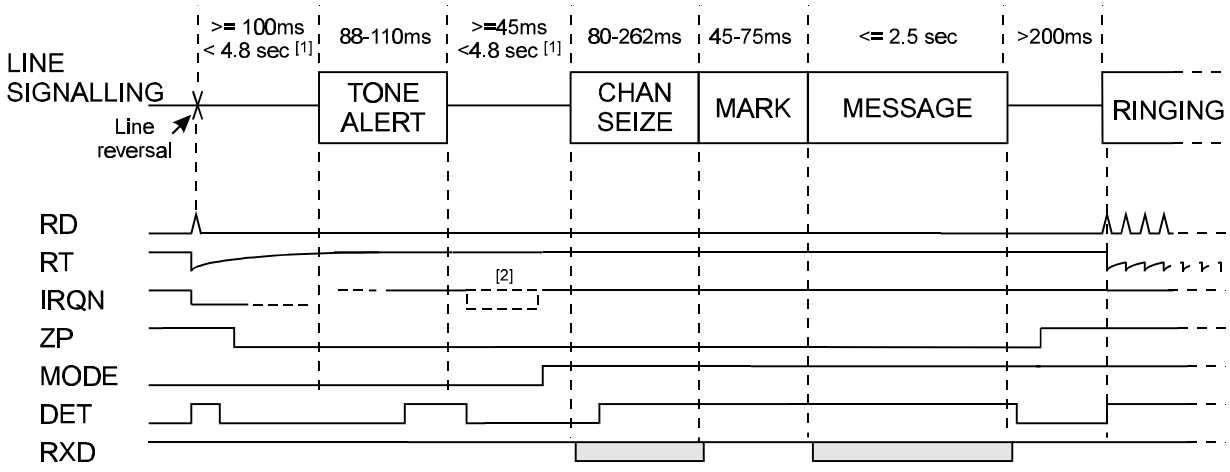
1.6.1 'On-Hook' Operation

The systems described in this section operate when the telephone set is not in use (on-hook) to display the number of a calling party before the call is answered.

British Telecom System

Figure 8a illustrates the line signalling and CMX602A I/O signals for the BT on-hook Calling Line ID system as defined in BT specifications SIN227 and SIN242 part 1. A similar system is described in ETS 300 659-1 section 6.1.2c.

The Tone Alert signal consists of simultaneous 2130Hz and 2750Hz tones, the 'Chan Seize' signal is a '1010..' FSK bit sequence. Not shown are the requirements for AC and DC loads, including a short initial Current Wetting Pulse, to be applied to the line 20ms after the end of the Tone Alert signal and to be maintained during reception of the FSK signal. Note that, for simplicity of presentation, the Data Retiming function is not used in Figure 8a (RXCK is kept high).



[1] Sum of these two periods does not exceed 5 sec
[2] IRQN may go low at end of DET high period, but this is not guaranteed.

Figure 8a : BT On-hook System Signals

Bellcore System

Figure 8b illustrates the line signalling and CMX602A I/O signals for the Bellcore on-hook Caller ID system as defined in Bellcore documents GR-30-CORE and SR-TSV-002476 and also in ETS 300 659-1 section 6.1.1.

As for the BT system, the 'Chan Seize' signal is a '1010..' FSK bit sequence. The Bellcore specifications do not require AC or DC line terminations while the FSK data is being received, however ETS 300 659-1 allows for the possibility of an AC termination being applied. Note that, for simplicity of presentation, the Data Retiming function is not used in Figure 8b (RXCK is kept high).

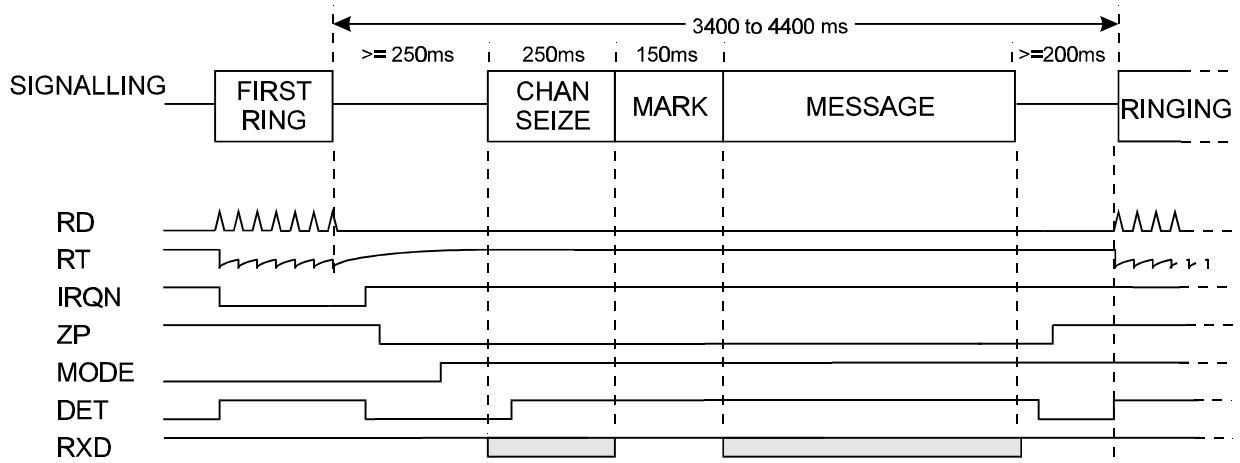


Figure 8b : Bellcore On-hook System Signals

Other On-hook Systems

ETS 300 659-1 also allows for systems where the FSK transmission is preceded by a Dual Tone Alerting signal similar to that used by BT but without a line reversal (section 6.1.2a) or by a Ringing Pulse Alerting Signal (section 6.1.2b).

The U.K. CCA (Cable Communications Association) specification TW/P&E/312 precedes the FSK signals by a 200 to 450ms ring burst. AC and DC line terminations during FSK reception are optional.

Mercury Communications Ltd. specification MNR 19 allows for either the BT system or that specified by CCA.

As these are all slight variants on the BT and Bellcore systems, they can also be handled by the CMX602A.

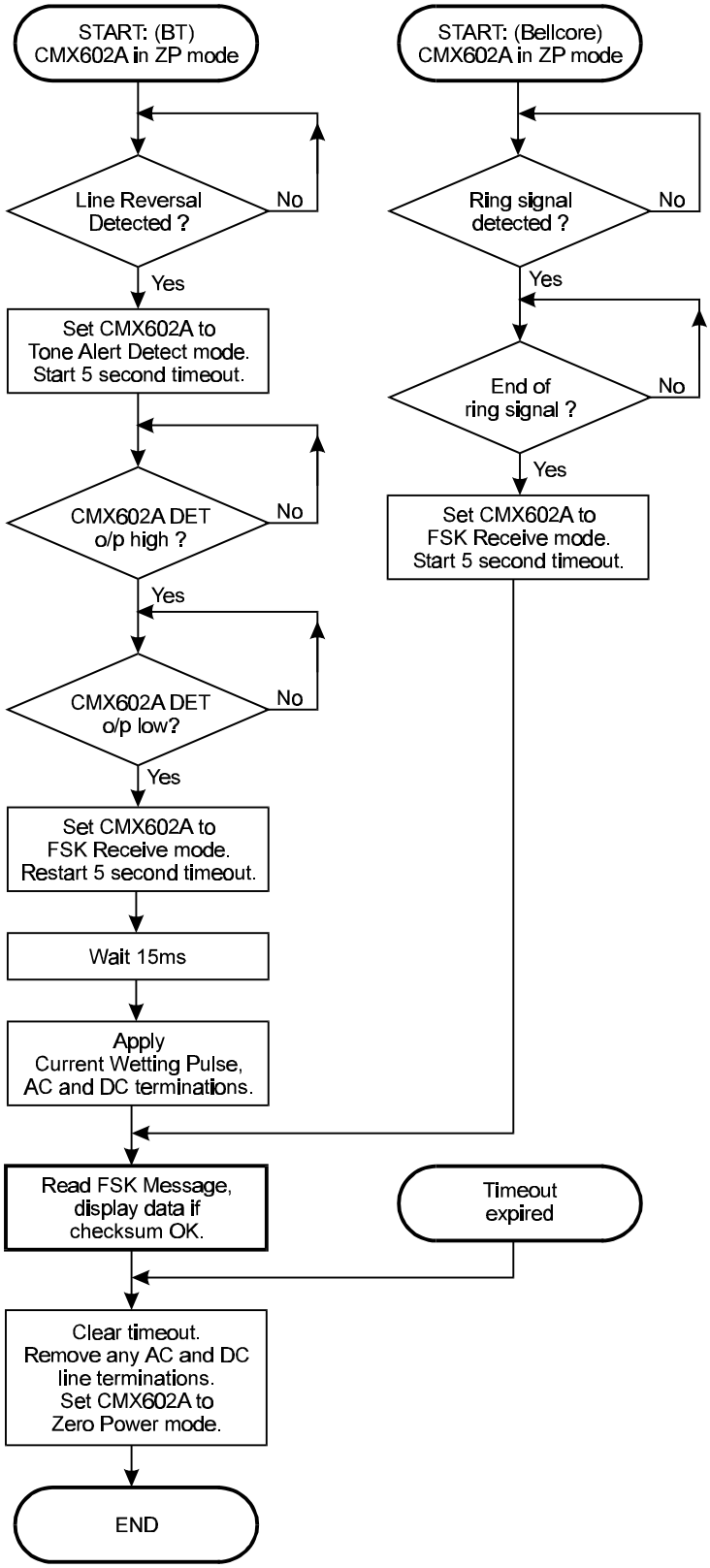
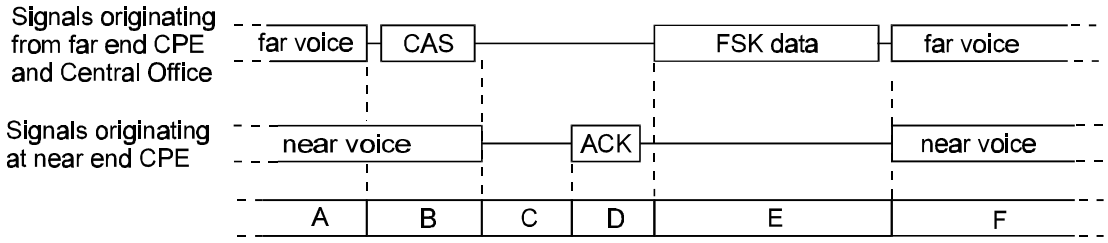


Figure 8c : Flow Chart for On-hook Operation of CMX602A

1.6.2 'Off-Hook' Operation

The CIDCW (Calling Identity on Call Waiting) system described in this section operates when the telephone set is in use (off-hook) to display the number of a waiting caller without interrupting the current call.

Bellcore documents GR-30-CORE and SR-TSV-002476, BT specifications SIN227 and SIN242 Part 2 and ETS 300-659-2 all describe similar systems in which a successful CIDCW transaction consists of a sequence of actions between the CPE (Customer Premises Equipment - e.g. a telephone) and the Central Office as indicated in Figure 9a.



A. Normal conversation with both near and far end voice present.
B. Central Office mutes far end voice, sends CAS and becomes silent.
C. CPE recognises CIDCW initiation and mutes near end voice and keypad.
D. CPE sends dtmf ACK to Central Office to signal its readiness to receive FSK data.
E. Central Office recognises ACK and sends FSK Caller ID data to CPE.
F. CIDCW transaction is complete. CPE unmutes near end voice and the Central Office unmutes far end voice, returning to normal conversation.

Figure 9a : CIDCW Transaction from Near End CPE Perspective

The CAS signal is transmitted by the Central Office to initiate a CIDCW transaction and consists of a 80ms burst of simultaneous 2130Hz and 2750Hz tones.

CAS detection is very important because a “missed” signal causes Caller ID information to be lost and a false signal detection produces a disruptive tone which is heard by the far end caller. Because the CAS signals must be detected in the presence of conversations which both mask and masquerade as the tone signals, this function is difficult to accomplish correctly.

Because the numbers of false responses (Talk-offs) and missed signals (Talk-downs) are related to the speech levels at the CMX602A input, and because the level of near end speech from the local handset is normally greater than that of far end speech coming from the Central Office, a further improvement in overall performance can be obtained by taking the CMX602A’s audio input from the receive side of the telephone set hybrid where this is possible.

The internal algorithms used by the CMX602A to drive the DET and IRQN outputs in Tone Alert Detect mode have been optimised for the detection of off-hook CAS signals in the presence of speech when used according to the following principles:

1. If it is possible to mute the local speech from the microphone rapidly (within 0.5ms) without introducing noise (i.e. where the CIDCW equipment is built into the telephone set) then this should be done whenever the CMX602A is in Tone Detect mode and the DET output is high. Doing this will markedly reduce the number of false responses generated by local (near end) speech. Note that the DET output is not used for any other purpose in an off-hook application when the CMX602A is set to Tone Alert Detect mode.

2. The IRQN output going low when in Tone Alert Detect mode indicates that a CAS has been detected. The local handset and keypad should then be muted as required by the Bellcore specification and the CMX602A switched to FSK Receive mode to be ready to receive the FSK data, doing this will also clear the IRQN output.

3. The CMX602A's DET output should be monitored for a period of 50ms after changing to FSK Receive mode, before sending the ACK signal, and the transaction abandoned if the DET output goes high during this time, which would be the case if a false CAS detect had been caused by far end speech.

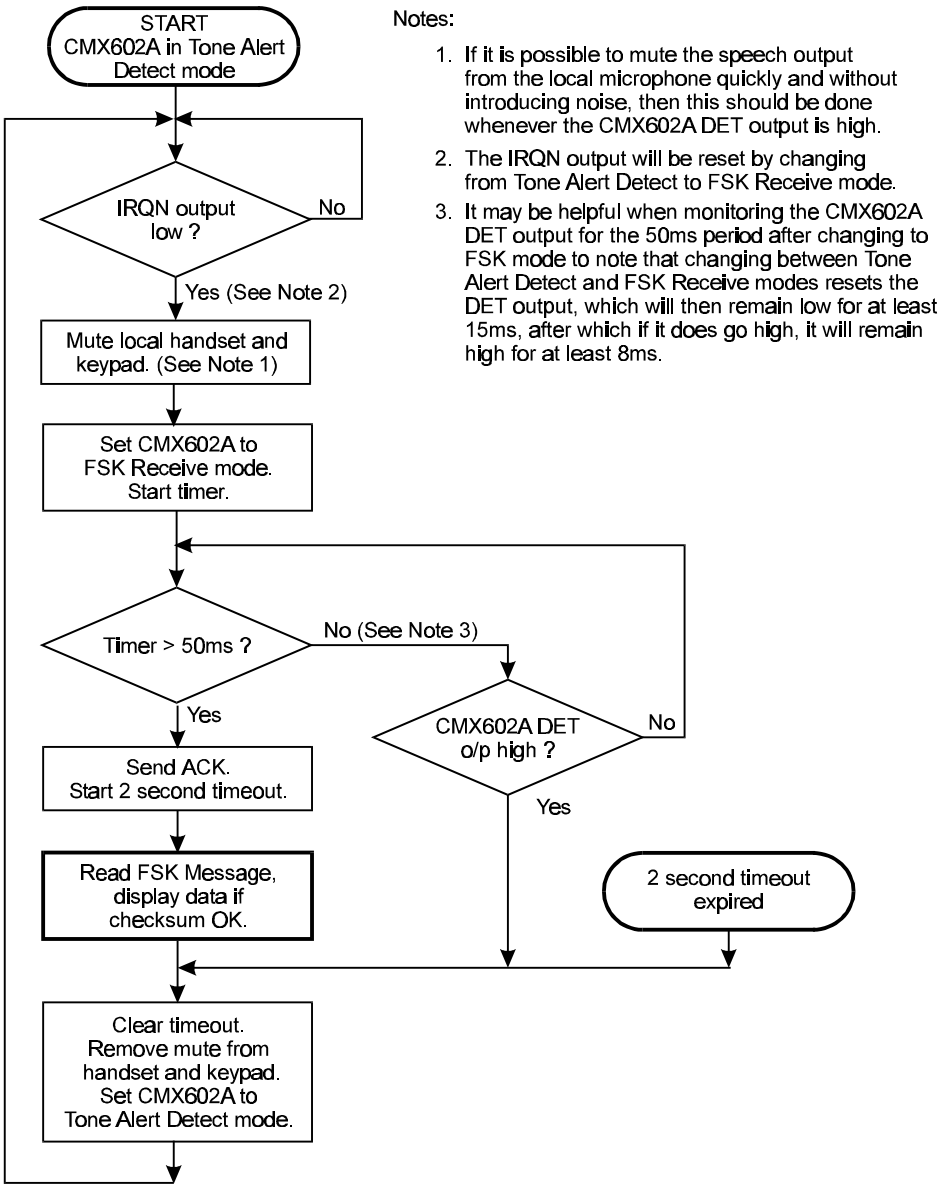


Figure 9b : Flow Chart for Off-hook Operation of CMX602A

1.7 Performance Specification

1.7.1 Electrical Performance

Absolute Maximum Ratings
Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current into or out of V_{DD} and V_{SS} pins	-30	+30	mA
Current into or out of any other pin	-20	+20	mA

D4 / P3 Packages	Min.	Max.	Units
Total Allowable Power Dissipation at Tamb = 25°C		800	mW
... Derating		13	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

Operating Limits
Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		2.7	5.5	V
Operating Temperature	2	-40	+85	°C
Xtal frequency	1	3.575965	3.583125	MHz

Notes: 1. An Xtal frequency of 3.579545MHz ±0.1% is required for correct Tone Alert and FSK detection.
2. Operating temperature range -10°C to +60°C at V_{DD} < 3.0V.

Operating Characteristics

For the following conditions unless otherwise specified:

V_{DD} = 2.7V at Tamb = -10 to +60°C and V_{DD} = 3.3V to 5.5V at Tamb = -40 to +85°C,
Xtal Frequency = 3.579545MHz ± 0.1%
0dBV corresponds to 1.0Vrms

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD} (ZP input high) at V_{DD} = 5.0V	1,2		0.02	1.0	µA
I_{DD} (ZP input low) at V_{DD} = 3.0V	1		0.5	1.0	mA
I_{DD} (ZP input low) at V_{DD} = 5.0V	1		1.0	2.0	mA
Logic '1' input level (RXCK and XTAL inputs)		70%			V_{DD}
Logic '0' input level (RXCK and XTAL inputs)				30%	V_{DD}
Logic input leakage current (Vin = 0 to V_{DD}) excluding XTAL input		-1.0		+1.0	µA
Output logic '1' level (I_{OH} = 360µA)		V_{DD} - 0.4			V
Output logic '0' level (I_{OL} = 360µA)				0.4	V
IRQN o/p 'off' state current (Vout = V_{DD})				1.0	µA
Schmitt Trigger input thresholds, see fig 10					
High going (Vthi)		$0.56V_{DD}$		$0.56V_{DD}$ + 0.6V	V
Low going (Vtlo)		$0.44V_{DD}$ - 0.6V		$0.44V_{DD}$	V
Tone Alert Detector					
'Low' tone nominal frequency			2130		Hz
'High' tone nominal frequency			2750		Hz
Start of Tone Alert signal to DET high time (Fig. 6 Tton)			55.0		ms
End of Tone Alert signal to DET and IRQN low time (Fig 6 Ttoff)		0.5		10.0	ms
DET high time to ensure IRQN goes low (Fig 6 TqCAS)		8.0		45.0	ms
To ensure detection:	3				
'Low' tone frequency tolerance				±20	Hz
'High' tone frequency tolerance				±30	Hz
Level (per tone)	4	-40.0		-2.2	dBV
2750Hz tone level wrt 2130Hz tone level		-7.0		+7.0	dB
Signal to Noise ratio	5	20.0			dB
Dual tone burst duration for DET output		75			ms
Dual tone burst duration to ensure IRQN goes low		75		85	ms
To ensure non-detection:	6				
'Low' tone frequency tolerance		±75			Hz
'High' tone frequency tolerance		±95			Hz
Level (total)	4			-46.0	dBV
Dual tone burst duration				45.0	ms

	Notes	Min.	Typ.	Max.	Units
FSK Receiver					
Transmission rate		1188	1200	1212	Baud
V23 Mark (logical 1) frequency		1280	1300	1320	Hz
V23 Space (logical 0) frequency		2068	2100	2132	Hz
Bell202 Mark (logical 1) frequency		1188	1200	1212	Hz
Bell202 Space (logical 0) frequency		2178	2200	2222	Hz
Valid input level range	4	-40.0		-8.0	dBV
Acceptable twist (mark level wrt space level)					
V23		-7.0		+7.0	dB
Bell202		-10.0		+10.0	dB
Acceptable Signal to Noise ratio					
V23	5	20.0			dB
Bell202	5	30.0			dB
Level Detector 'on' threshold level	4			-40.0	dBV
Level Detector 'off' to 'on' time (Fig 4 Teon)				25.0	ms
Level Detector 'on' to 'off' time (Fig 4 Teoff)		8.0			ms
Input Signal Amplifier					
Input impedance	7	10.0			MΩ
Voltage gain			500		V/V
XTAL Input					
'High' pulse width	8	100			ns
'Low' pulse width	8	100			ns

Notes:

1. At 25°C, not including any current drawn from the CMX602A pins by external circuitry other than X1, C1 and C2.
2. RD, MODE, RXCK inputs at V_{SS}, ZP input at V_{DD}. See also Figure 11.
3. All conditions must be met to ensure detection.
4. For V_{DD} = 5.0V with equal level tones and with the input signal amplifier external components as section 1.4. The internal threshold levels are proportional to V_{DD}. To cater for other supply voltages or different signal level ranges the voltage gain of the input signal amplifier should be adjusted by selecting the appropriate external components as described in section 1.5
5. Flat noise in 300 - 3400Hz band for V23, 200 - 3200Hz for Bell202.
6. Meeting any of these conditions will ensure non-detection.
7. Open loop, small signal low frequency measurements.
8. Timing for an external input to the CLOCK/XTAL pin.

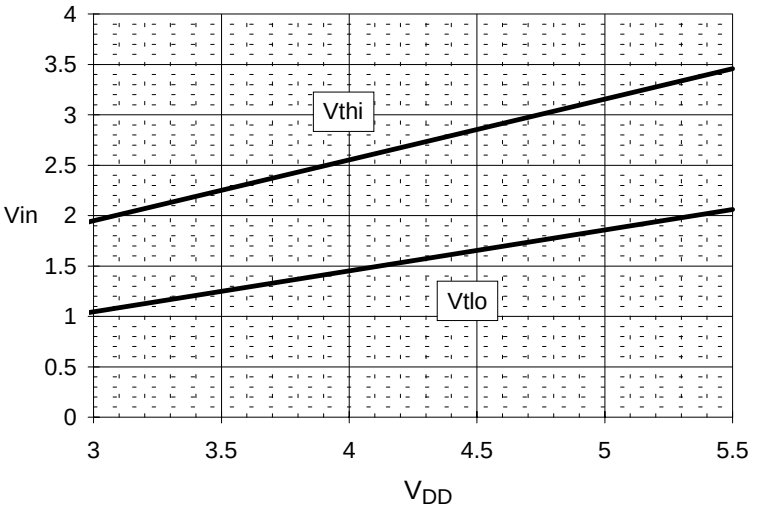


Figure 10 : Schmitt Trigger typical input voltage thresholds vs. V_{DD}

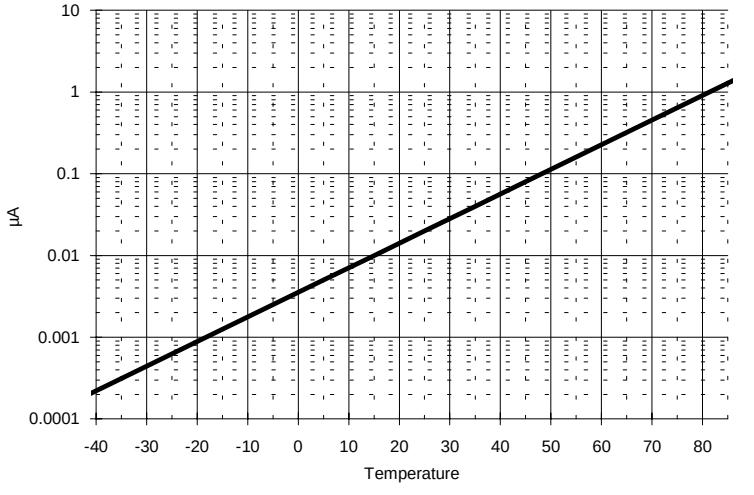
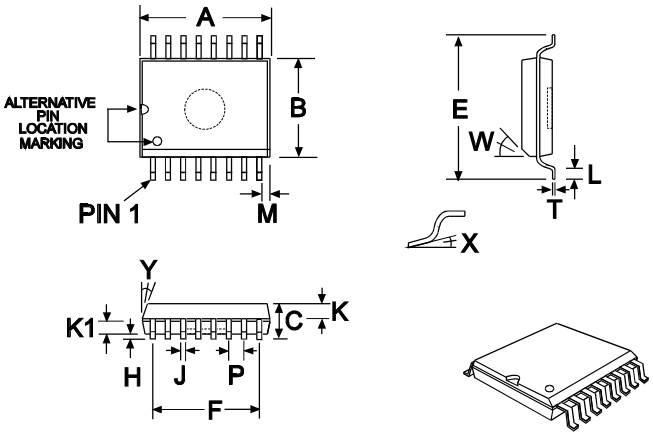


Figure 11 : Typical 'Zero Power' I_{DD} vs. Temperature (V_{DD} = 5.0V)

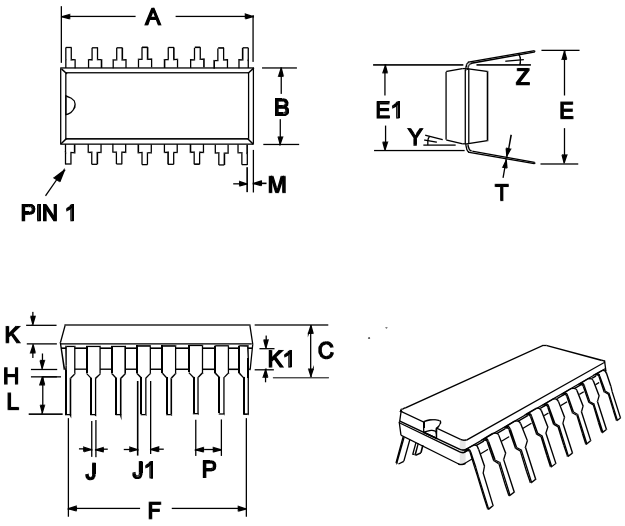
1.7.2 Packaging



DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.291 (7.39)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.394 (10.01)		0.419 (10.64)
F		0.366 (9.29)	
H	0.004 (0.10)		0.012 (0.30)
J	0.013 (0.33)		0.019 (0.48)
K		0.041 (1.04)	
K1		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
M	0.021 (0.53)		0.031 (0.79)
P		0.050 (1.27)	
T	0.009 (0.23)		0.012 (0.30)
W		45°	
X	0°		8°
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles in degrees

Figure 12 : 16-pin SOIC (D4) Mechanical Outline: ***Order as part no. CMX602AD4***



DIM.	MIN.	TYP.	MAX.
A	0.740 (18.80)		0.810 (20.57)
B	0.240 (6.10)		0.260 (6.60)
C	0.135 (3.43)		0.175 (4.45)
E	0.300 (7.62)		0.390 (9.91).
E1	0.290 (7.37)		0.325 (8.26)
F		0.70 (17.78)	
H	0.015 (0.38)		0.035 (0.89)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.056 (1.42)		0.064 (1.63)
K1	0.056 (1.42)		0.064 (1.63)
L	0.121 (3.07)		0.150 (3.81)
M		0.028 (0.72)	
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles in degrees

Figure 13 : 16-pin DIL (P3) Mechanical Outline: ***Order as part no. CMX602AP3***

CONSUMER MICROCIRCUITS LIMITED
1 WHEATON ROAD
WITHAM - ESSEX
CM8 3TD - ENGLAND
Telephone: +44 1376 513833
Telefax: +44 1376 518247
e-mail: sales@cmlmicro.co.uk
http://www.cmlmicro.co.uk

CML Microcircuits

COMMUNICATION SEMICONDUCTORS

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In the process of creating a more global image, the three standard product semiconductor companies of CML Microsystems Plc *(Consumer Microcircuits Limited (UK), MX-COM, Inc (USA) and CML Microcircuits (Singapore) Pte Ltd)* have undergone name changes and, whilst maintaining their separate new names *(CML Microcircuits (UK) Ltd, CML Microcircuits (USA) Inc and CML Microcircuits (Singapore) Pte Ltd*), now operate under the single title **CML Microcircuits**.
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This notification is relevant product information to which it is attached.

Company contact information is as below:

CML Microcircuits (UK) Ltd
COMMUNICATION SEMICONDUCTORS

Oval Park, Langford, Maldon,
Essex, CM9 6WG, England
Tel: +44 (0)1621 875500
Fax: +44 (0)1621 875600
uk.sales@cmlmicro.com
www.cmlmicro.com

CML Microcircuits (USA) Inc.
COMMUNICATION SEMICONDUCTORS

4800 Bethania Station Road,
Winston-Salem, NC 27105, USA
Tel: +1 336 744 5050,
0800 638 5577
Fax: +1 336 744 5054
us.sales@cmlmicro.com
www.cmlmicro.com

CML Microcircuits (Singapore) Pte Ltd
COMMUNICATION SEMICONDUCTORS

No 2 Kallang Pudding Road, 09-05/
06 Mactech Industrial Building,
Singapore 349307
Tel: +65 7450426
Fax: +65 7452917
sg.sales@cmlmicro.com
www.cmlmicro.com

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Fax: +44 (0)1621 875600
uk.sales@cmlmicro.com
www.cmlmicro.com

CML Microcircuits (USA) Inc.
COMMUNICATION SEMICONDUCTORS

4800 Bethania Station Road,
Winston-Salem, NC 27105, USA
Tel: +1 336 744 5050,
0800 638 5577
Fax: +1 336 744 5054
us.sales@cmlmicro.com
www.cmlmicro.com

CML Microcircuits (Singapore) Pte Ltd
COMMUNICATION SEMICONDUCTORS

No 2 Kallang Pudding Road, 09-05/
06 Mactech Industrial Building,
Singapore 349307
Tel: +65 7450426
Fax: +65 7452917
sg.sales@cmlmicro.com
www.cmlmicro.com

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