Consumer Microcircuits Limited
COMMUNICATION SEMICONDUCTORS

CMX635
ISDN Subscriber Processor

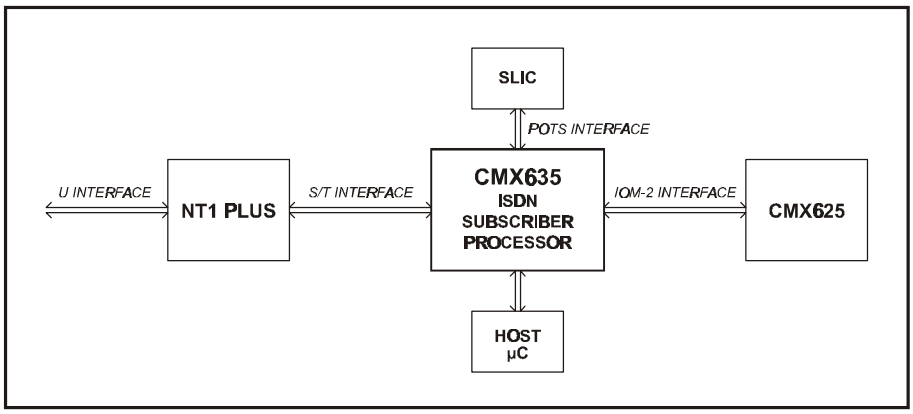
D/635/2 December 2001 Advance Information

Features

- S/T Interface to ITU-T I.430 (TE & NT1)
- 2B + 1D-channel HDLC Controllers
- IOM™-2 / GCI Interface
- Selectable A-Law/µ-Law PCM Codec
- 100mW Speaker-Phone Output
- 2 Independent Analogue Inputs
- Pre-Programmed Tone Generators
- V.23/Bell 202 FSK Generator
- Ringing Signal and SPM Generators
- DTMF Encoder/Decoder

Applications

- ISDN Terminal Equipment
- ISDN Intelligent NT's
- ISDN Phones and Feature Phones
- Digital & Analogue Answer-Phones
- Data Adaptors
- Active and Passive Terminal Adaptors
- Alarm Systems
- Point-Of-Sale Terminals
- 'Group 4' Fax Equipment
- Video Phones



2.7V
LOW POWER OPERATION

IOM is a trademark of Siemens AG.

1.1 Brief Description

The CMX635 is an integrated Subscriber Processor designed for low chip-count ISDN voice/data terminals and POTS terminal adaptors. Its functions facilitate operation in an ISDN feature phone with speakerphone capability or in a POTS terminal adapter with Subscriber Pulse Metering (SPM), DTMF encoder/decoder, Caller Line ID (CLID) and Caller ID on Call Waiting (CIDCW) capabilities. It also implements many functions needed in an intelligent NT or NT1Plus system.

The CMX635 incorporates a 4-wire ST interface conforming to ITU-T I.430 and ETS 300 012-1 specifications. HDLC Controllers and associated FIFOs are provided for B1, B2 and D-channels, which can be configured to automatically process the bit stuffing, flag generation/recognition, address matching and CRC generation/checking required to support the ITU Q.921 protocol. An IOM-2™ /GCI interface is provided to enable operation with other IOM compliant devices.

The µController interface is compatible with multiplexed and non-multiplexed address/data busses and generic Motorola and Intel style control. The CMX635 will automatically detect which style of interface is being used and configure itself accordingly. The device is available in a 48-pin TQFP package and has progressive powersave modes to aid low power operation.

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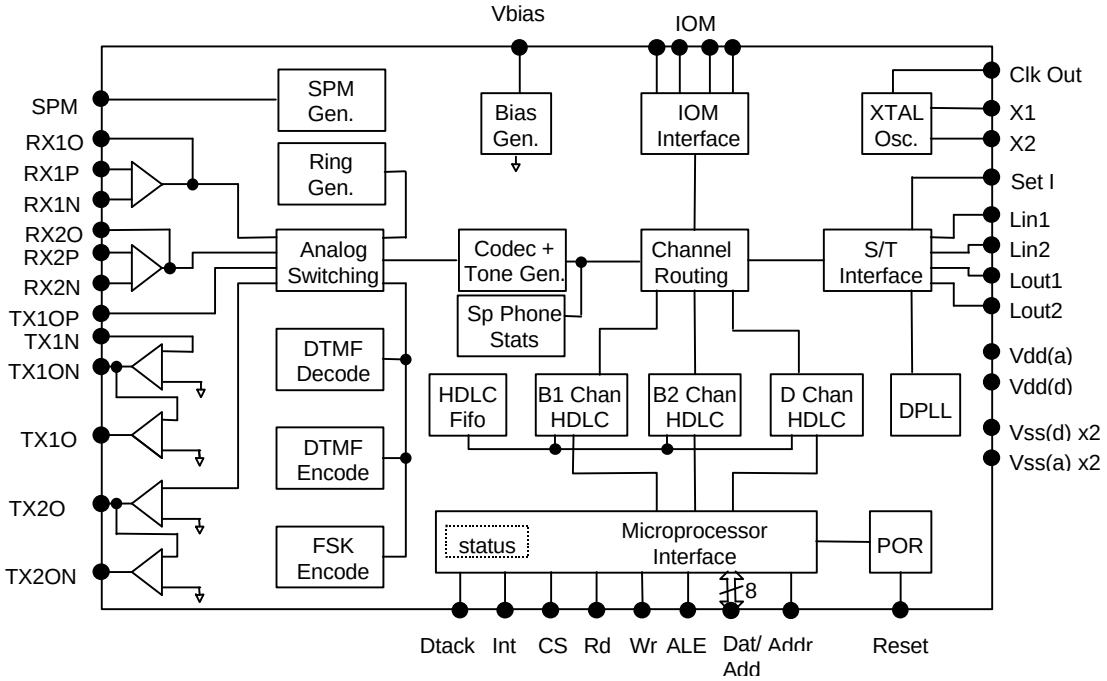
1.2 CMX635 Block Diagrams

1.2.1 Functional Block Diagram

The diagram below shows the main elements of the CMX635.

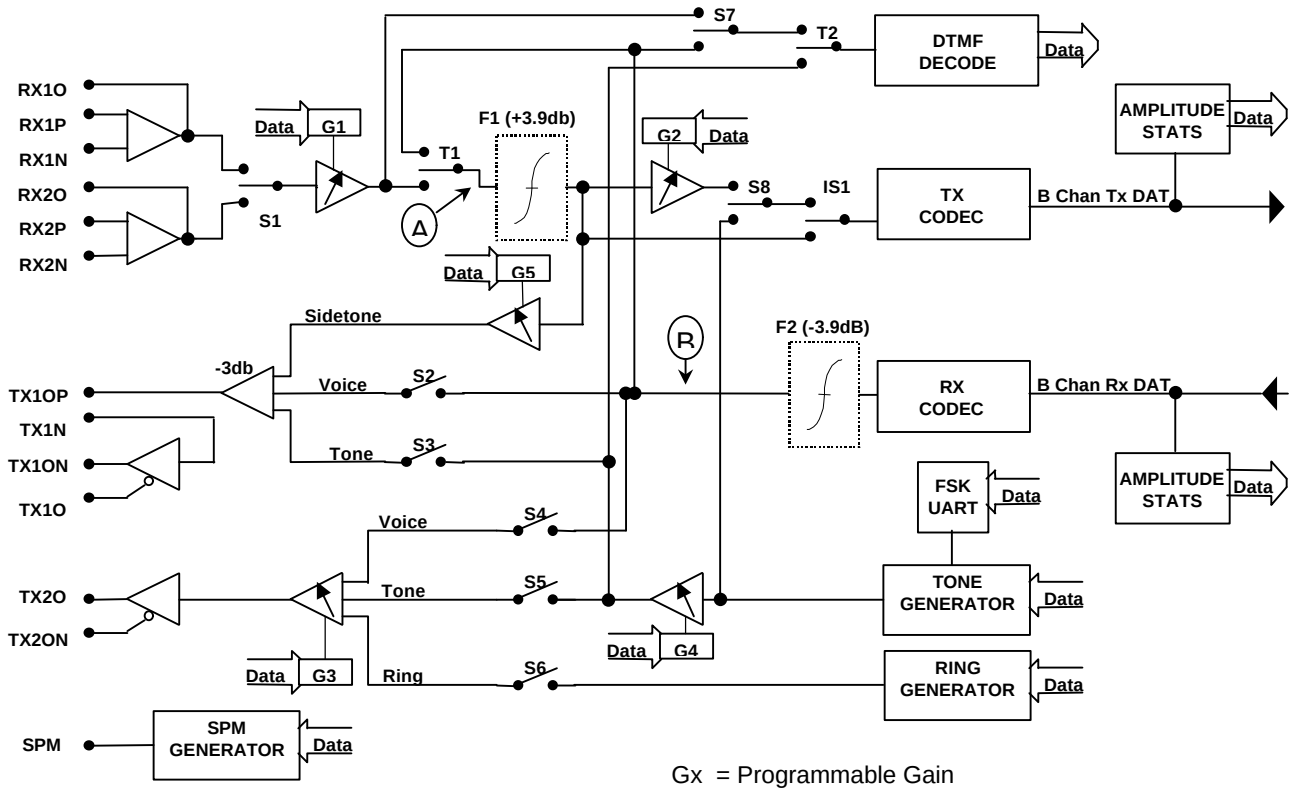


RX1 and RX2 channels used for Mic or POTS input.
TX1 channel used for Earpiece or POTS output.
TX2 channel used for loudspeaker or POTS Ring output.

For clarity, internal Processor bus not shown.

Figure 1. CMX635 BLOCK DIAGRAM

1.2.2 Analogue Block Diagram



Gx = Programmable Gain
Sx = User Switch
ISx = Internal Switch
Fx = Filter
Tx = Test Switch

Notes:

G1 = 0dB to 22.5dB (in 1.5db steps) - Level set/AGC gain.
G2 = 0dB to –42dB (in 3dB steps + mute) - Speakerphone attenuation.
G3 = +6dB to –42dB (in 0.5dB steps + mute) - Speaker/ring output gain.
G4 = 0dB to –42dB (in 3dB steps + mute) - Tone gain
G5 = -6dB to –36dB (in 2dB steps) - Sidetone gain.

S1 – S8 = User selectable switches.

IS1 = Internally operated switches (shown for information only).

T1 - T2 = Test Switches (shown for information only).

At reference points “A” and “B” the nominal signal level scaling as defined in ITU-T G714 is:
0dbm0 ≡ 0dBm = 775 mV r.m.s. at 5V power supply.

The maximum unclipped sine wave possible on reference points “A” and “B” is:
3.14dbm0 ≡ 3.14dBm = 1.11 V r.m.s. for A law companding at 5 V supply.

Peak to peak full scale input signal to Rx Codec is 0.986 x V_{DD} for A-law companding,
And 0.989 x V_{DD} for µ-law companding.

Figure 2. ANALOGUE BLOCK DIAGRAM

1.3 Signal List

1.3.1 Pin numbers

The following table lists the complete pin description of the CMX635 48-pin TFQP (L4) package.

Pin #	Name	Type	Function
30	STTXp	Ana	ST interface transmit output - positive
31	STTXn	Ana	ST interface transmit output - negative
27	STRXp	Ana	ST interface receive input - positive
28	STRXn	Ana	ST interface receive input - negative
42	DCL	I_t/O_c	IOM-2 interface Data Clock
41	FSC	I_t/O_c	IOM-2 interface Frame Sync
43	IOMTx	O/D, I_t	IOM transmit output - DD when upstream device –Note 1
44	IOMRx	I_t, O/D	IOM receive input - DU when upstream device – Note 1
7	AD0	I_c/O_c	Processor Address/Data Bus bit 0 (lsb)
6	AD1	I_c/O_c	Processor Address/Data Bus bit 1
5	AD2	I_c/O_c	Processor Address/Data Bus bit 2
4	AD3	I_c/O_c	Processor Address/Data Bus bit 3
3	AD4	I_c/O_c	Processor Address/Data Bus bit 4
2	AD5	I_c/O_c	Processor Address/Data Bus bit 5
1	AD6	I_c/O_c	Processor Address/Data Bus bit 6
48	AD7	I_c/O_c	Processor Address/Data Bus bit 7 (msb)
14	ASel	I_c	Address Select
9	Dtack	O/D	Data Acknowledge
15	ALE	I_c	Address Latch Enable (AS in Motorola style applications)
12	nWR	I_c	Write Strobe (RD/nWR or E in Motorola style applications)
11	nRD	I_c	Read Strobe (DS in Motorola style applications)
13	nCS	I_c	Chip Select
8	nIRQ	O/D	Interrupt request
16	RESET	I_c	Chip Reset
46	X1	Ana	Crystal (or oscillator) input
45	X2	Ana	Crystal input 2
47	CLKOUT	O_c	Clock Out - Buffered master clock
18	VBIAS	Ana	Internal Bias.
23	RX1O	Ana	Analogue input amplifier #1 output
24	RX1P	Ana	Analogue input amplifier #1 positive input
25	RX1N	Ana	Analogue input amplifier #1 negative input
20	RX2O	Ana	Analogue input amplifier #2 output
21	RX2P	Ana	Analogue input amplifier #2 positive input
22	RX2N	Ana	Analogue input amplifier #2 negative input
38	TX1OP	Ana	Output #1 raw output
36	TX1O	Ana	Output Amplifier #1 positive output - earpiece/POTS
35	TX1ON	Ana	Output Amplifier #1 negative output - earpiece/POTS
37	TX1N	Ana	Output Amplifier #1 negative input
34	TX2O	Ana	Output Amplifier #2 positive output - Loudspeaker/Ring
33	TX2ON	Ana	Output Amplifier #2 negative output - Loudspeaker/Ring
17	SPM	Ana	Subscriber Pulse Metering Output
29	STISet	Ana	ST Tx Current Limit Set
39	VDDa	S	Positive Analogue Supply, 2.7 - 5 V
26	VDDa	S	Positive Analogue Supply, 2.7 - 5 V
32	VSSa	S	Analogue Gnd
19	VSSa	S	Analogue Gnd
40	VDDd	S	Positive Digital Supply, 2.7 - 5 V
10	VSSd	S	Digital Gnd

Pin Type Legend:

I - Digital Input
O - Digital Output
I/O - Digital Bi-directional
O/D - Open Drain
Ana - Analogue Input or Output

Subscript denotes input/output levels
C - CMOS
T - TTL

Note 1: IOMRx normally TTL input but can become open drain output during bus reversal.
IOMTx normally open drain output but can become TTL input during bus reversal.

1.3.2 Pin description

STTxp, STTxn
ST bus differential transmit outputs. Upstream data in TE configuration and Downstream data in NT configuration. The nominal amplitude is ±2.1V differential with 280Ù load which equates to ±750mV at the ST interface when the recommended line transformer is used. STTxp is positive with respect to STTxn for transmission of the Frame Pulse bit.
Note: Particular care should be taken to avoid electro-static discharge damage to these pins as the unpowered impedance requirements result in reduced internal protection.

STRxp, STRxn
ST bus differential receive inputs. Downstream data in TE configuration and Upstream data in NT configuration. The nominal expected differential pulse amplitude is ±1.2V which equates to ±750mV at the ST interface with recommended components. Amplitudes down to 255mV at the ST interface can be accommodated while signal activity above 100mV will generate a “Wake-up” interrupt if required. Polarity need only be maintained for point to multipoint configurations.

DCL
IOM-2 interface “terminal” mode data clock operating at a nominal frequency 1.536MHz. The DCL can be configured as an output (cmos levels) in timing master mode or as an input (ttl levels) in timing slave mode. DCL operates at twice the IOM bit rate and is used to sample the data on the IOM receive input.

FSC
IOM-2 interface Frame Sync operating at a nominal frequency of 8kHz. The FSC can be configured as an output (cmos levels) in timing master mode or as an input (ttl levels) in timing slave mode. The rising edge of FSC defines the start of an IOM frame and is nominally synchronous with the rising edge of DCL.

IOMTx, IOMRx
IOM-2 interface transmit and receive data pins operating at a nominal bit rate of 768kbps. The IOMTx pin equates to the IOM DD (Data Downstream) signal when the CMX635 is the upstream device (TE configuration) and to the IOM DU (Data Upstream) signal when the CMX635 is the downstream device (NT configuration). The IOMTx pin can be configured as open drain or active cmos level output. The direction of the IOMTx and IOMRx pins can be reversed for certain channels in the IOM frame.

AD[7:0]
Processor interface Address/Data bus. Bi-directional cmos level input/output bus that carries multiplexed address and data when multiplexed mode is automatically detected by the CMX635 and data only when non-multiplexed mode is detected.

ASel
Address Select. Asel, when asserted, selects the internal indirect address register as the destination for non-multiplexed processor read/writes, or the data register when de-asserted. Asel may be connected to A[0] of the non-multiplexed processor address bus. Connect to Vss for multiplexed interface operation.

Dtack
Data Acknowledge. Active only when the Motorola style multiplexed mode processor interface is detected. It is an open drain output that is pulled low at the start of a processor read or write cycle and remains low until the CMX635 internal cycle is complete. The Dtack signal can be used to implement a hardware handshake cycle timing mechanism.

ALE
Address Latch Enable. The multiplexed address from the AD bus is latched on the falling edge of ALE. Connect ALE to Vcc if an Intel style non-multiplexed interface is being used and to Vss for a Motorola style non-multiplexed interface.

nWR
Write Strobe, active low. Latches the data from the AD bus on the rising edge in Intel style mode. Acts as a R/nW strobe in Motorola mode. See the timing diagrams in section 1.8.1 for more details on the nWR pin function.

nRD
Read Strobe, active low. Initiates a CMX635 read cycle and enables read data to be driven onto the AD bus in Intel style mode. Acts as a DS or E strobe in Motorola style mode. See the timing diagrams in section 1.8.1 for more details on the nWR pin function.

nCS
Chip Select, active low. Must be low for duration of read or write cycle in all interface modes. Processor interface is inactive and will not respond to read/write strobe activity when nCS is high.

nIRQ
Interrupt Request, open drain. Pulled to Vss when the CMX635 internal Status Registers generate an unmasked interrupt request. It remains in its high impedance state when no interrupts are pending. An external pull-up resistor is required.

RESET
Global Chip Reset. Active high reset input resets CMX635 internal state and restores default configuration. The RESET input should be asserted at power-up before any configuration is written or modes activated. The RESET must be asserted until the oscillator input has stabilised (either from a crystal or external clock source) to ensure full internal reset.

X1, X2
Oscillator input pins. A 12.288Mhz or 15.36MHz crystal may be connected between these pins (see External Components section 1.4) or an external clock source may be connected to X1 with X2 connected to Vss.

CLOCKOUT
Buffered Clock. A buffered version of the input clock on X1 is available on CLOCKOUT and may be used for driving the clock inputs of other devices. Optionally the internal phase locked 1.536MHz clock may be routed to CLOCKOUT, which can be utilised by external circuitry to lock together multiple CMX635 devices if required.

VBias
The internal analogue reference voltage. An external capacitor must be connected between Vbias and analogue ground to ensure noise free operation.

RX1O, RX1P, RX1N, RX2O, RX2P, RX2N
Output, positive and negative inputs of the differential microphone input amplifiers. See section 1.4.2 for details of the equivalent analogue input circuits.

TX1O, TX1ON, TX1N, TXOP
Differential Outputs, negative input and internal preamplifier output of the earpiece/POTS output amplifier. See section 1.4.2 for details of the equivalent analogue output circuits. The required external gain components are inserted between the TX1ON and TX1N pins, which form the input impedance to the inverting earpiece amplifier.

TX2O, TX2ON
Loudspeaker/Ring amplifier differential outputs.

SPM
Subscriber Pulse Metering sine wave output for emulating POTS style call cost information.

STISet
ST transmitter current set pin. A fixed resistor must be connected between this pin and analogue Vss to ensure accurate current limit on the ST transmitter.

VSSd, VDDd, VSSa, VDDa
Analogue and Digital supply pins. Ensure adequate high and low frequency decoupling between positive and negative supplies. It is recommended that the analogue and digital supplies are locally separated.

1.4 External Components

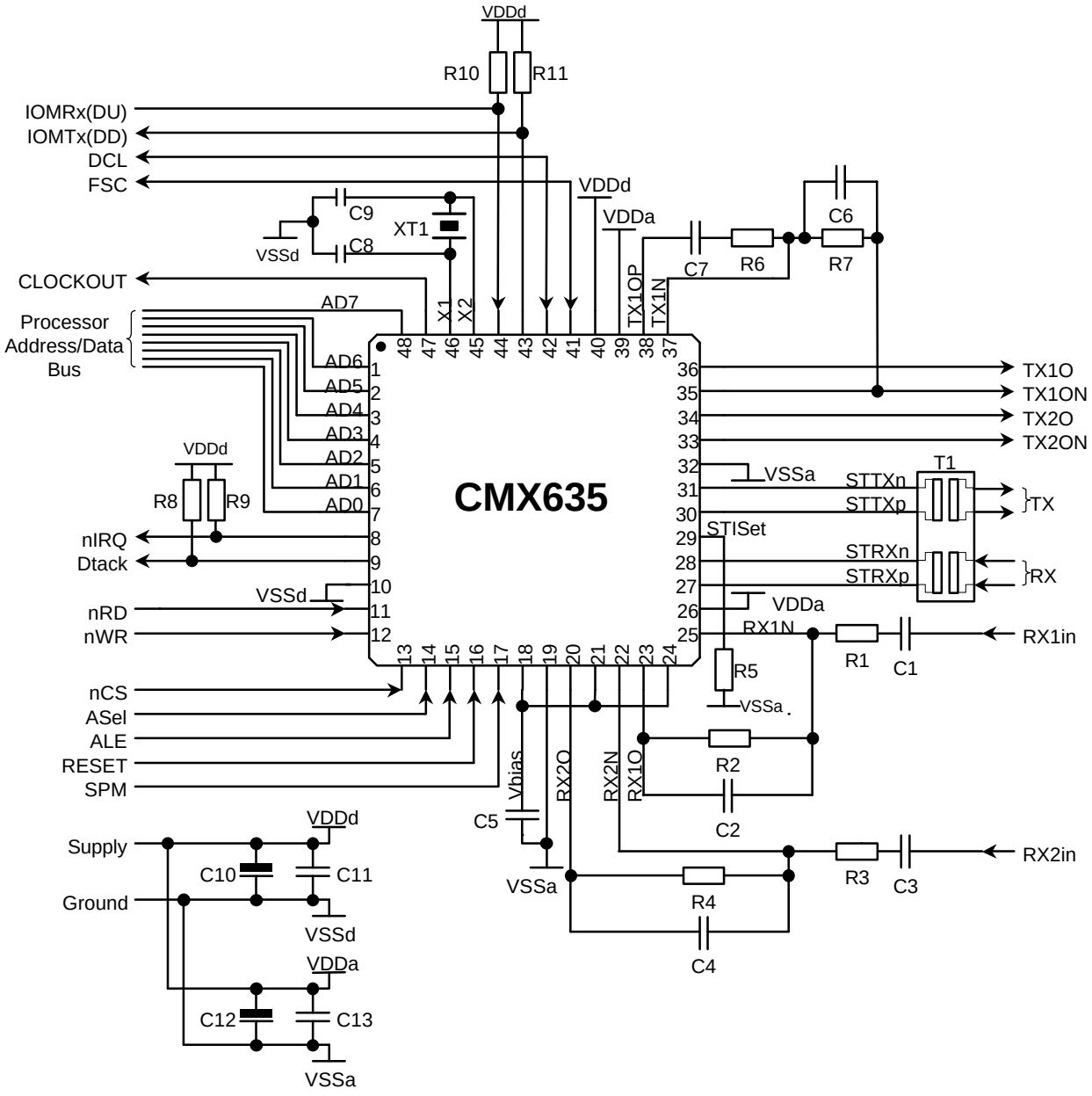


Figure 3. Recommended External Components

1.4.1 Component Values

XT1	12.288MHz or 15.36MHz	
T1	Line Transformer, 2:1 Turns Ratio i.e. ETAL P3024 – Note 1.	
R1, R3	Note 2.	
R2, R4	110kΩ	1%
R5	15 kΩ	2%
R6	Note 3.	
R7	39kΩ	1%
R8, R9	10kΩ	5%
R10, R11	750R (5V supply),	5%
	470R (3.3V supply)	5%
C1, C3, C5	1.0µF	5%
C2, C4	220pF	5%
C6	150pF	5%
C7	27nF	5%
C8, C9	33pF	20%
C10, C12	1.0µF	10%
C11, C13	10nF	10% - Note 4.

Notes:

1. If a suitable transformer module is not used, protection components should be added around the line transformers, including 33R series resistors in the STTX lines and 10kΩ series resistors in the STRX lines.

2. R1, R2, C1 and C2 form the gain components of input amplifier RX1. R3, R4, C3 and C4 form the gain components of input amplifier RX2. R1 and R3 should be chosen as required by the input signal level according to the following formula:

Gain = -R2/R1 or -R4/R3

C1, R1 and C3, R3 should be chosen so as not to compromise the low frequency performance.

3. R6, R7, C6 and C7 form the gain components of output amplifier TX1. R6 should be chosen to give the required output signal level according to the following formula:

Gain = -R7/R6

4. Ensure that high frequency filter capacitors are placed physically close to appropriate power pins.

1.4.2 Equivalent Analogue Input/Output Circuits

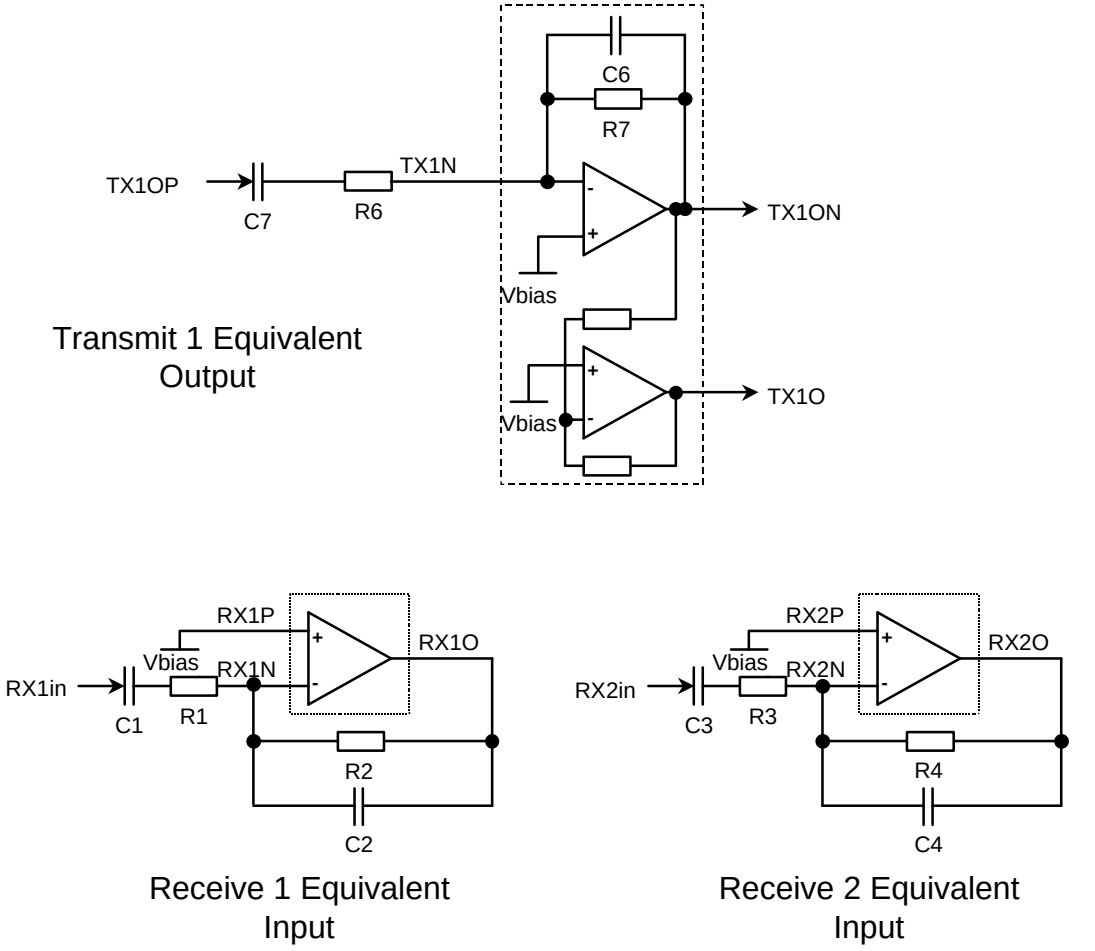


Figure 4. Equivalent Input/Output Circuits

1.5 Functional Description

The CMX635 is a highly integrated ISDN Subscriber Processor that allows low chip count systems to be designed for a wide variety of ISDN voice/data terminals and POTS terminal adaptors. It can also provide the majority of functions required to implement an intelligent NT or NT1Plus system.

The CMX635 incorporates a 4-wire ST interface, which conforms fully to the ITU-T I.430 and ETS 300 012-1 specifications. It provides the necessary layer-1 control to implement both the TE and NT ends of the ST reference point and the layer-2 controls to implement the D-channel signalling layer.

HDLC Controllers and associated FIFOs are provided for the B1, B2 and D-channels. The Controllers can be configured to automatically process the bit stuffing, flag generation/recognition, address matching and CRC generation/checking required to support the ITU Q.921 protocol reducing the software overhead on the host processor. The automatic processing can be progressively disabled until fully transparent operation is achieved with corresponding increased processor load. The data FIFOs are implemented as a 1024 byte RAM that can be flexibly partitioned to form the 6 required FIFOs (2B+D, Receive and Transmit), enabling optimum FIFO size to be selected for the application.

An IOM-2™ /GCI interface is provided to enable operation with other IOM compliant devices. This facility can be used to connect to a 'U' Interface device in NT mode of operation or to expand the number of POTS ports in TE mode by connection to devices such as the CMX625 – ISDN TA POTS Interface. The IOM interface can be configured as a timing master or slave for TE or NT applications respectively and has full Mult-Framing capabilities.

The CMX635 has the functions necessary for operation as an ISDN feature phone with speakerphone capability or as a POTS terminal adapter. There are 2 independent uncommitted differential input amplifiers suitable for connection to 2 microphones for feature-phone applications or to a SLIC/POTS hybrid for POTS operation. A 100mW power amplifier is provided to drive a speaker for feature-phones or the ring input to a SLIC for POTS. An additional output is provided to drive a handset earpiece or the SLIC/Hybrid input for POTS.

Sophisticated speakerphone operation can be implemented using the digital noise and voice filters available in the CMX635 in conjunction with user supplied software algorithms.

For POTS operation a DTMF decoder enables interpretation of dialling information and can also be configured to detect far end DTMF tones. A tone generator supplies all of the necessary tone frequencies for call progress tones. Other tone standards supported are: Fax and Modem 'answer' and 'originate', ITU (CCITT) 'R1' and 'R2' signals, and sufficient tones for simple melody generation.

Caller Line ID (CLID) and Caller ID on Call Waiting (CIDCW) functionality can be emulated using the tone generator and the FSK UART facility.

A Subscriber Pulse Metering (SPM) output is provided to enable operation with POTS legacy payphone equipment. The frequency standard can be set to either 12kHz or 16kHz.

A DTMF generator is available to allow feature-phone equipment to generate comfort dial tones and to enable control of remote DTMF signalling and Menuing systems.

The µController interface is compatible with multiplexed and non-multiplexed address/data busses and generic Motorola and Intel style control. The CMX635 will automatically detect which style of interface is being used and configure itself accordingly.

The CMX635 is highly configurable, via internal software accessible registers, to operate in a wide variety of applications. The details of every configuration and Status Register are described in the Programming Guide section 1.6.

The main functions of the CMX635 are shown in the block diagrams and are conceptually:

- The ST interface and Digital Phase Locked Loop
- The HDLC Controllers and FIFOs
- The IOM Interface
- The G.711 Codec and Analogue Gain Path
- The Tone Generator and Tone Decoder
- The Channel Routing Block
- Speaker Phone Functions
- The Processor Interface, Top Level Status and Power Control

1.5.1 The ST interface and Digital Phase Locked Loop

The ST Interface performs the following functions:

- S/T Bus Activation/Deactivation Control
- Clock and Data Recovery
- Frame Synchronisation
- D-channel Access
- Multi-Frame Generation/Reception

The Activation/Deactivation control when configured in TE mode follows closely the ITU-T I.430 requirements and is mainly autonomous (Timer T3 requiring implementation in software). The activation states are advanced through automatic detection of the INFO0, INFO2 and INFO4 signals on the receive bus and are initiated by software writes of the Activate and Deactivate request primitives and the Power Up/Down status. Note that although the ITU specification provides no facility for the ST bus to be deactivated directly by the TE, the Deactivate Request control is provided to allow implementation of timer T3 in software. The ST activation state can be read by software and the detection of the various INFO signals can be configured to generate an interrupt if required. The activation status indicators 'Connect Indication', 'Activate Indication' and 'Error Indication' are available to the software and may also be configured to generate an interrupt request if required.

The ST interface autonomously outputs the 'INFO0', 'INFO1' and 'INFO3' signals at the appropriate states of activation/deactivation.

For NT mode of operation, the next state is under software control and is written directly to the ST interface. The detection of 'INFO0', 'INFO1' and 'INFO3' is available to the software to enable next state calculation.

The Data Recovery function consists of an analogue section and a digital section. The analogue ST receiver continuously tracks the amplitude of the incoming signal and uses an adaptive slicing level to recover digital data from the 3 level receiver input. The data is coded into positive pulse, negative pulse or no pulse. The digital section over-samples the recovered data and performs a majority decision algorithm to determine the correct recovered bit stream.

The Clock Recovery function consists of a digital phase-locked loop that tracks the raw sampled data in TE mode to produce a filtered and frequency locked master sample clock at a nominal 192kHz. This clock is used to sample the recovered receive bit stream and to generate a phase locked ST transmit clock. In NT mode the ST bit clock tracks the received IOM FSC signal thus maintaining network synchronisation.

The Frame Synchronisation function detects the correct occurrence of Framing and Auxiliary Framing pulses and in TE mode adjusts the receive and transmit frames accordingly. Two consecutive correctly received frames are required before the interface is designated as Frame Locked.

D-channel access in TE mode is initiated by writing the 'Data Request' primitive to the CMX635 along with the required primary priority level. The primary priority can be set to 8 for signalling frames and to 10 for data frames. The D-channel Access function will then ensure that the D-channel is available by monitoring the number of consecutive D-channel Echo bits that are set to binary 1. If the count reaches the level defined by the priority, the D-channel HDLC block is allowed to transmit. If an echo bit is received that does not match the transmitted D bit, the D-channel is released and a 'Collision' status flag is set. A 'Data Indication' primitive can be configured to generate an interrupt when the D-channel has been successfully acquired. After transmission of an HDLC frame, and if another frame is pending, the priority is automatically decreased (8 to 9 and 10 to 11) to allow other TE devices access to the D-channel. If multiple D-channel transmission frames are set up in the HDLC FIFO (see section 1.5.2) the access mechanism will automatically allow other TE's access to the D-channel between frames but will remain active until all frames are sent.

D-channel access in intelligent NT mode uses a similar access mechanism to TE mode but the D bits from the downstream TE's are used to determine D-channel activity instead of the echo bits. When an NT has successfully acquired the D-channel it sets the echo bits to the downstream TE's to binary 0, thus inhibiting TE D-channel access.

The CMX635 supports full ST Multi-framing capability and in TE mode will synchronise to incoming multi-frame markers. In NT mode formatted multi-frames are generated. The CMX635 is capable of processing 1 'Q' channel and '5' S channels as defined in ITU-T I.430. Full sets of interruptible status flags are available to indicate when the transmit/receive data buffers require servicing.

1.5.2 The HDLC Controllers and FIFOs

The CMX635 contains flexible Controllers and FIFOs for both B-channels and the D-channel that can be individually selected and enabled.

The main functions of the HDLC Controllers and FIFOs are:

- Flag generation/recognition
- Bit Stuffing/Destuffing and Octet Alignment
- Address Field Matching
- CRC generation/checking
- Re-configurable FIFO data buffers on all transmit and receive channels
- Multiple HDLC frame generation and Reception

The CMX635 will automatically generate the 01111110b sequence defined as an HDLC flag at the beginning of each new frame. Reception of an HDLC frame will initiate the frame receive sequence and the reception of a second flag will be interpreted as the end of an HDLC frame. 'Shared' flags (1 flag between the end of a frame and the start of a new frame) will be processed correctly in the receive channel. In the B transmit channels a 'shared' flag can optionally be used between multiple frames.
The bit stuffing and de-stuffing requirements of the HDLC protocol are automatically implemented unless the fully transparent modes of operation are selected. If transparent receive mode for a B-channel is selected, the serial bit stream is formed directly into octets and written to the receive FIFO. Transparent receive mode is not available in the D-channel. If transparent transmit mode is selected, the data from the FIFO is read in octets and transmitted directly as a serial bit stream octet aligned with the ST frame B-channel octets.

The address field matching function can be used in the D-channel to match incoming SAPI and TEI identifiers automatically. When address matching is turned on, incoming data frames are ignored unless the required address fields match the pre-programmed values. 4 independent match addresses can be programmed for each of the 1st and 2nd address fields as well as the broadcast addresses for both fields. The extent of address matching required can be selected to be zero, one or both fields. The combination of the pre-programmed match registers to be used is also programmable. A successful address match will set an interruptible status bit. If address matching is turned off, all incoming frames are routed to the receive FIFO irrespective of address values and the software must determine if the frame is relevant.

For transmit frames, either 1 or 2 address registers may be prepended to the transmit FIFO data automatically unless User Address mode is selected, in which case the address fields must be written to the FIFO as part of the data frame by software.

The CMX635 can automatically generate and decode the16 bit CRC fields appended to the end of HDLC frames and for received frames will generate an interruptable Good Packet or CRC Error status as appropriate. If automatic CRC handling is not required, the transmit CRC value can be supplied by the user and written as the last data octet(s) to the FIFO. For received frames the CRC value available as the last octet(s) in the receive FIFO can be decoded in software. If automatic CRC generation is enabled, a facility is provided to force a CRC error for purposes of system test/checks.

Status flags are provided to indicate a number of abnormal conditions, which can be configured to generate interrupt requests. The conditions indicated are:

- Received CRC error
- Received octet mis-alignment (frame not an integer number of octets)
- Received packet aborted (7 consecutive binary 1's received)
- Received short packet (frame length less that pre-programmed minimum)
- Transmit aborted (collision detected In the D-channel)

The CMX635 contains a FIFO, for each of the B receive and transmit channels and the D receive and transmit channel (6 total). The FIFOs are implemented as part of a 1024 byte RAM and the FIFO depths can be independently configured for each channel, in 4 byte increments, up to the 1024 byte RAM size. The sum of FIFO sizes must not exceed the 1024 byte limit. A full set of FIFO status indicators are available for each channel including 'Full', 'Empty', 'Near Full', 'Near Empty', 'Over-Write' and 'Under-Read'. The 'Near Full' and 'Near Empty' status indicate when the FIFO is 8 bytes from being full and 8 bytes from being empty respectively. The 'Full' and 'Empty' status have programmable polarity to allow for alternative interrupt generation on 'Not Full' and 'Not Empty'. Each FIFO can be individually cleared which obviates the need to read the entire FIFO if an error or abort is detected.

When a valid frame is detected the receive FIFOs are always written with all data between opening and closing flags, irrespective of the address matching and CRC checking selected.

The CMX635 HDLC controllers have extensive functionality to allow transmission and reception of multiple frames of data without processor intervention, subject to the FIFO depths set. Two methods are available for multiple frame transmission.

The first method allows multiple frames of the same length to be transmitted by writing an Octet Count register with the frame length and a Frame Count register with the required number of frames. The data to be transmitted is then written contiguously to the FIFO. When HDLC transmission is enabled, the Octet Counter (which can be read asynchronously by software) defines the FIFO data frame boundaries and decrements as each octet is transmitted. After each frame the Frame Counter is decremented to a minimum count of 1. After each frame has been

transmitted an interruptable 'Frame Complete' flag is raised and after all of the frames have been transmitted an interruptable 'All Frames Complete' flag is raised.

The second method allows for multiple frames of differing lengths to be transmitted. The number of octets in the following frame is written to the FIFO prepending the frame data. This is repeated for each frame in the multiple frame. During transmission the Octet Count is read from the FIFO and used as in method 1 above along with the pre-programmed Frame Count. After each frame the next Octet Count is loaded from the FIFO until all frames have been transmitted.

A Received Octet Counter is available to facilitate multiple frame reception. When a frame has been successfully received the software is required to respond to a Good Packet interrupt by reading and storing the Received Octet counter value. This value can then be used for reconstructing the received frame when the FIFO is eventually read. As the counter is only modulo 256, a rollover indication is provided to enable handling of long frames.

1.5.3 The IOM Interface

The CMX635 contains an industry standard IOM-2 interface to facilitate data transfer and programming of other IOM-2 compliant devices such as the CMX625 ISDN TA POTS Interface. A summary of the IOM-2 standard may be found in section 1.7.2 of this document.

The interface operates in Terminal Mode where 3 channels of 4 octets are transmitted per frame. The IOM-2 standard defines octets in each frame for:

- 8 bits of B1 and B2 data and 2 bits of D data.
- 8 bits of Monitor 0 data + 2 handshake bits, used for layer-1 device control functions.
- 8 bits of Monitor 1 data + 2 handshake bits, used for programming and interrogation of other IOM devices.
- 4 bits of Control/Indicate (CI) 0 data used for passing layer-1 primitives.
- 6 bits of Control/Indicate (CI) 1 data used for real time status indication between IOM devices.
- 2 8-bit channels of Inter-Communication data (IC0 & IC1) used as alternative 64kb/s data channels.
- An 8-bit TIC (Terminal IC) bus used for D-channel access from other layer-2 devices.

The IOM interface can be configured as a timing master, where the IOM clock (DCL) and the IOM frame sync. (FSC) are generated by the device, or as a timing slave where an external device provides the clock and sync. signals. Typically the CMX635 will be configured as a timing master when used in a TE system and a timing slave (taking the clock and sync signals from a U interface transceiver) in an NT system. The CMX635 always operates as a control master device.

The IOM-2 clock in terminal mode is nominally 1.536MHz giving 192 clocks per 8kHz frame, or 2 clocks per data bit. The FSC and DCL are derived from the recovered 192kHz S/T sample clock, which maintains PCM octet synchronisation. In NT mode, as a timing slave, the incoming FSC is used to synchronise the generated 192kHz S/T data.

The monitor channels (0 and 1) provide a mechanism for passing programming and information octets between the master and slave IOM devices. Only 1 channel can be active at a time, the active channel being selectable from the 'IOM Monitor Channel Control' register. The monitor handshake protocol in the IOM specification is generated automatically within the CMX635 and any errors in the handshaking or received data will abort the transmit/receive sequence and raise interruptable abort flags in the 'IOM Status' register.
The operation of the B, D and IC channels is fully autonomous and they are activated by routing data to and from the appropriate channels using the 'Data Routing' registers (section 1.5.6).

Data is transmitted in the selected monitor channel by writing to the 'Monitor Channel Transmit' register when the Tx channel is idle. The 'Monitor Tx Buffer Empty' status flag will indicate when

another transmit octet is required. The original data octet will be retransmitted continuously until the transmit buffer is refreshed. Setting the 'Tx EOF' bit in the 'Monitor Channel Control' register when the 'Tx Buffer Empty' status flag is asserted terminates the monitor frame.

Data is received in the selected monitor channel by reading from the 'Monitor Channel Receive' register when the 'Rx Data Available' flag is asserted. The 'Rx EOF' flag indicates the end of a received IOM frame and the 'Rx Abort' flag indicates an error in reception.

The Command/Indicate channels provide a mechanism for passing "real time" layer-1 primitives (CI0) and status flags (CI1) between IOM devices. Data written to the 'CI Transmit' registers will be immediately reflected in the appropriate CI channel and will persist until the register data is changed. The received CI channel is read from the 'CI Receive' registers and 'New CI Data' flags indicate when two consecutive frames contain new and identical CI data.

The 'CI0 Transmit' register contains extra locations to enable an IOM Timing Request (TIM) to be generated and to control the Bus Activation Request (BAC) bit in the TIC channel. The TIM is used to request activation of the upstream IOM device and pulls the DU pin low from its deactivated open-drain state.

When the CMX635 is configured as a timing master, the IOM bus can be deactivated by turning off the DCL and FSC and placing the IOMTx pin in the open drain state. An IOM deactivation sequence can be optionally invoked that ensures deactivation is not completed until 4 frames of the primitive DC (Deactivate confirmation - 1111b) has been received in the CI0 channel from all downstream devices.

The CMX635 implements a sub-set of the TIC bus control functions. The TIC bus allows layer-1 control of the D-channel from other IOM devices. The CMX635 enables control of the transmitted BAC bit in NT applications when required by the U transceiver device but does not generate or monitor TIC bus addresses. In TE mode the D-channel access function will automatically operate the Stop/Go (S/G) bit to prevent other layer-1 devices from accessing the D-channel when occupied by the CMX635. The received BAC bit is monitored to establish when other layer-1 devices require access to the D-channel.

The CMX635 can be configured to reverse its Tx and Rx pin directions in the IC channels and/or the MON1 and CI1 channels. This feature is known as "bus reversal" and enables the CMX635, when configured as a downstream IOM device, to communicate with other downstream IOM devices.

1.5.4 The G.711 Codec and Analogue Gain Path

The PCM Codec-Filter performs voice digitisation and reconstruction and incorporates encoder bandpass and decoder lowpass filters with pre and post-filtering and with selectable A-law and μ-law companding. In each case the coder and decoder process a companded 8-bit PCM word following CCITT recommendation G.711 for A-law and μ-law conversion. The encoder bandpass filter and decoder lowpass filter provides passband flatness and stopband rejection according to CCITT recommendation G.712. The lowpass filter contains the required (Sin X)/X compensation.

Flexible receive and transmit digital gain control and analogue routing controls are provided to enable configuration into POTS or ISDN feature-phone applications.

Examples of the possible configurations for POTS are:

- Sine, Square or Trapezoid ring frequency routed to speaker output with programmable amplitude. Cadence controlled within CMX635 or externally.
- Received analogue Codec signal routed to earpiece output (SLIC/Hybrid input).
- Call progress or DTMF tones summed with or replacing Codec signal to earpiece at programmable amplitude.
- Call Waiting Tone (SAS), Caller Line ID on Call Waiting alert signal (CAS) and FSK caller ID data replacing signal to earpiece at programmable amplitude.
- Received DTMF tones from receive Codec routed to DTMF decoder for remote signalling detection.
- DTMF tones from POTS interface routed to DTMF decoder for dialled number detection.

Examples of the possible configurations for ISDN phones are:

- Input from 1 of 2 microphone inputs switchable through programmable gain to transmit Codec. Allows transducer matching and A.G.C. function for speakerphone operation.
- Independent programmable microphone channel attenuation for speakerphone algorithms.
- Received analogue Codec signal routed to earpiece and/or loudspeaker output. Loudspeaker amplifier has programmable gain for volume control and speakerphone attenuation.
- Programmable proportion of microphone channel can be added to earpiece output as “sidetone”.
- DTMF tones can be routed to earpiece/speaker for dialling feedback or to transmit Codec for remote DTMF signalling.
- Full range of pre-programmed tones can be routed to speaker at programmable amplitude for ringing.

The Programming Guide, section 1.6, details the full range of routing and gain control functions available.

1.5.5 The Tone Generator and Tone Decoder

The Tone Generator can be used to generate tones for either DTMF tones, call progress tones, ringing signals for ISDN phones and FSK data tones for POTS caller ID functions.

The tones available are pre-programmed and grouped into 4 tone fields of up to 256 tones each. To select a particular tone or tone pair the ‘Tone/Codec Control’ register is first written with the required tone field and the ‘Tone’ register is then written with the selection from that field. The Tone Enable register allows independent power save control for the various tone types.

The Ring signal can be configured as a sine, square or trapezoidal output at a number of frequencies between 17Hz and 51Hz.

The FSK tones are automatically generated when the FSK function is enabled and FSK data is written to the transmit uart. The tone frequencies for FSK transmission can be selected to be compliant with either Bell 202 or V.23 standards.

The FSK UART can be programmed to convert the transmit data from octets to serial asynchronous data characters by adding Start and Stop bits or to transmit the octets synchronously with no start or stop bits. The baud rate is fixed at 1200 baud. Status flags indicate when the transmit buffer requires more data and whether the buffer data has underflowed (the UART has started a new FSK character before the buffer has been refreshed).

The DTMF decoder can accept a wide range of signal input amplitudes and produces a 4 bit DTMF character code that can be read from the 'DTMF Receive Data' register. Status flags indicate when a valid tone is being detected and when it ceases.

A Subscriber Pulse Metering (SPM) tone is available at a separate pin and can be programmed to 12kHz or 16kHz. When turned on, the output ramps from zero to full amplitude in approximately 4mS and ramps down again when turned off. This output allows emulation of the exchange call charging information for POTS style payphones.

1.5.6 The Channel Routing Block

The Channel Routing block enables the active data channels (B1, B2, D, IC1, IC2) to be flexibly routed between the ST interface, the IOM interface, the HDLC controllers and the Codec.

The available routing resources allow implementation of a full suite of loopback paths in either the transparent (the incoming data continues to be passed to the original destination as well as looping back) or the non-transparent (original source/destination for data is disabled) modes.

For B data routing, 4 prioritised routing registers are available. Each register contains a required 4-bit source and 4-bit destination port code. If there are conflicts between routing register data sources, the highest priority register routing will be implemented and the lower priority routing will be used as a destination only.

D-channel routing is contained within a single register, which is divided into high and low priority routing 4-bit nibbles. Within each nibble 2-bit source and destination port codes can be programmed. The priority mechanism works in a similar fashion to the B data routing above.

1.5.7 Speaker Phone Functions

The CMX635 contains comprehensive hardware filters, voice-above-noise detectors and signal path attenuators to allow a sophisticated implementation of software controlled speakerphone algorithms. The data processing is carried out on the 8kHz 8-bit wide PCM data in both the receive and transmit paths. Status bits are available to indicate the presence of voice above the background noise in both the receive and transmit channels and the amplitude of the detected voice can be read by software. The software algorithm can then decide which is the dominant channel and distribute the loop gain between receive and transmit channels.

The following data processing functions on both the receive and transmit digital data paths are provided. Note that all data processing is done on companded data in both channels.

- Full wave rectification conversion of input data
- Noise filtering of converted data with long time constant (~ 10 s)
- Speech filtering of converted data with fast attack time constant (~ 1 ms) and selectable slow decay time constant (128, 256, 500 ms).
- Auto Gated Noise Filter i.e. the statistics integration is suspended when speech is detected in the channel.
- Interrupt control system based upon filter output comparators, which provides three interrupt sources for each channel. The interrupt sources are: -

1) Speech filter output > noise filter output
2) Speech filter output > noise filter output + programmable threshold
3) Speech filer output > noise filter output + programmable threshold +/- hysteresis value.

- Interrupt generation when a change in any of the above conditions takes place. The user can poll the indicator flag bits to determine the exact condition that exists within the channel.
- A hysteresis register to prevent rapid and spurious interrupts when a slow noisy signal moves close to the integrated background level.

1.5.8 The Processor Interface, Top Level Status and Power Control

The processor interface will automatically configure itself to operate with either multiplexed or non-multiplexed address/data architectures and with generic Motorola or Intel control signals.

The processor interface type is configured after power-up by making a dummy write to the CMX635, which will monitor activity on the bus control lines and decode the appropriate interface type.

When the non-multiplexed interface is detected it is mapped as 2 addresses on the processor bus that are distinguishable by the state of the Asel pin during the read/write cycle. The first address (Asel set to binary 1) is the “indirect” address register for the following data access and must be written first. The second address (Asel = binary 0) accesses the register defined by the indirect address. Typically the single address pin (Asel) will be connected to the LSB of the processor address bus. The indirect address is persistent and, once written, can be used for further data accesses to the same address (i.e. block reads/writes to the Fifo data registers).

When the multiplexed interface is detected the internal register address is automatically demultiplexed from the AD bus and thus only single read/write cycles are required.

The Top Level Status register accumulates interrupt requests from the lower level blocks (as shown in Figure 5) and can be programmed to generate a selective device level interrupt request dependent on the state of the top level interrupt mask. Each lower level Status Register can be programmed to generate the interrupt requests to the top level Status Register via their own status masks. The Status Register/interrupt structure is hierarchical at 3 levels. The top level Status Register accumulates the interrupt requests from a number of level-2 Status Registers. Some of the level-2 Status Registers accumulate interrupt requests from level-3 Status Registers. To respond to an interrupt originating from a level-3 Status Register, both the top level status and the level-2 Status Registers must be read to determine the source of the interrupt.

The Power Control function includes a Clock Control register, and 3 Enable registers. The Clock Control register selects the master crystal frequency (12.288MHz or 15.36MHz), the signal routed to the CLKOUT pin (Clock In or 1.536MHz) and allows the master crystal oscillator to be disabled for complete power down applications. A hardware reset must be issued to re-enable the oscillator. The Clock Enable register can disable the system clock to individual blocks when not required thus saving power. The Tone and Audio Enable registers allow selective control of the analogue functions, Codec and tone generator/decoder, progressively reducing power consumption as un-used functions are disabled.

A Power Control Status register is available which indicates external “wake-up” events on the ST and IOM busses. Any activity on the ST bus will trigger an ST wake-up interrupt (if the interrupt is enabled with the appropriate masks), while the IOMRx pin (DU in TE applications) being pulled low will trigger an IOM wake-up interrupt. These interrupts will be generated even if the IOM and ST master clocks have been disabled.

The ‘Power Control Status’ register also contains 2 flags, ‘CI0 Channel Idle’ and ‘IOM Deactivated’ that indicate when the IOM bus can be safely deactivated. The ‘CI0 Channel Idle’

status indicates that there has been 2 consecutive IOM frames received with the bus access bit set inactive (binary 1). In this condition there is no activity or pending activity in the CI0 channel. The ‘IOM Deactivated’ flag is valid when the IOM Deactivate sequence is in use. The flag is asserted when all downstream devices have signalled complete deactivation.

1.6 Programming Guide.

1.6.1 Interrupt Structure

The CMX635 interrupt structure is hierarchical in nature with the interrupts from the various functional blocks converging in a top level Status Register to create a single chip level interrupt. The majority of interrupts can be interrogated from the next level of block Status Registers and a few require access to a third level of Status Registers. Each Status Register at each level can be individually masked on a bit by bit basis with its own Mask Register. Each level of Status Register is persistent, i.e. the status flags are latched and can only be cleared by reading the appropriate register. To prevent continuous interrupts from being generated the software interrupt handler should either read the interrupting Status Register or temporarily mask the appropriate bit.

The top level (level 1) Status Register comprises level-2 interrupt sources as follows.

Bit	Interrupt Source	Section No.
[0]	HDLC D-channel Status	1.6.2.8.2
[1]	HDLC B1-channel Status	1.6.2.8.2
[2]	HDLC B2-channel Status	1.6.2.8.2
[3]	ST Interface Status Register	1.6.2.1.4
[4]	IOM Interface Status Register	1.6.2.10.5
[5]	Tone Generator Status Register	1.6.2.14.5
[6]	Clock & Power Control Status Register	1.6.2.11.4
[7]	Speakerphone Interrupt Status	1.6.2.12.6

The HDLC D, B1, B2 Status Registers and the ST Interface Status Register each have a level-3 interrupt source as detailed in the relevant sections.

The interrupt structure is shown diagrammatically in Figure 5.

Note that the reset value of the top level Status Register is the fully masked condition. For valid interrupts to be generated the top level Mask Register must be initialised early in the initialisation sequence.

Top Level Status Register Addr = $E1 Reset = $00
TopLevel Status Mask Register Addr = $E0 Reset = $00

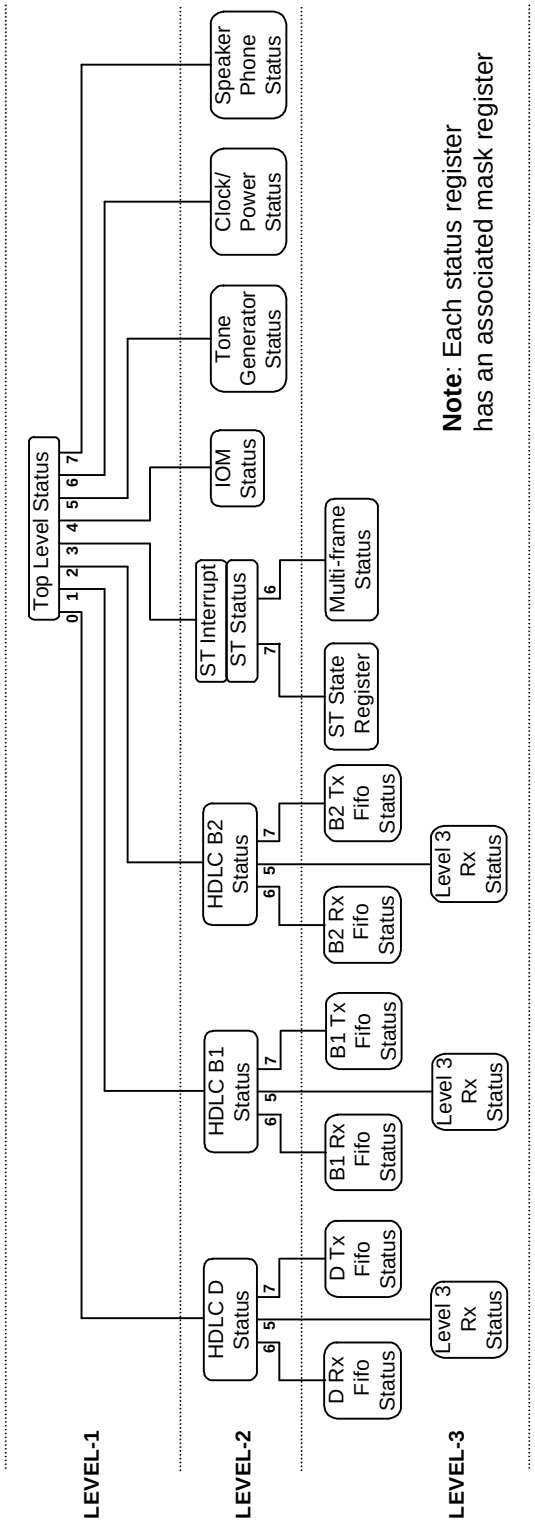


Figure 5. Interrupt Structure

1.6.2 CMX635 Register Definition and Description

The control registers of the CMX635 fall into the following broad categories:

- ST Interface Block
- Data Routing Block
- HDLC Fifo Control
- HDLC B1-channel Control
- HDLC B2-channel Control
- HDLC D-channel Control
- IOM Interface Control
- Clock and Power Control
- Speaker Phone Statistics
- Audio/Tone Block
- Top Level Status Register

These registers relate to the main functional blocks as defined in the functional block diagram.

Note that the clock for each block being written or read must be activated using the Clock Enable register as detailed in section 1.6.2.11.1

1.6.2.1 ST Interface Block

The ST Interface block registers provide the necessary primitive control for activating and reporting the status of the ST bus. They also provide the means to configure the CMX635 into its various operating modes and to control the multiframing capabilities.

The registers available in this block are:

- ST Control Register
- ST Set-Up Register
- ST Interrupt Register
- ST Status Register
- Interrupt Mask Register
- ST State Machine Register
- ST State Machine Mask Register
- MultiFrame S Register
- MultiFrame Q Register
- MultiFrame Status/Control Register
- MultiFrame Status Mask Register
- MultiFrame S Bit Counter

1.6.2.1.1 ST Control Register

Addr = $80 Reset = $00 (write/read)

The following table lists the bit functions of the ST Control Register.

Bit	Function
[0]	Activate Request (PH-AR)
[1]	Deactivate Request (MPH-DR)
[2]	Power Up
[3]	Unused
[4]	Data Request (PH-DATA)
[5]	Priority (PH-DATA Request parameter)
[6]	Force Echo 0
[7]	Unused

Unused bits in the Control register will read back as binary 0.

The Activate Request bit equates to the PH-AR primitive and initiates ST bus activation when the CMX635 is configured in TE mode. This bit is a transient signal that advances the ST activation state machine to F4 when written with a binary 1 and reads back as binary 0.

The Deactivate Request bit equates to the MPH-DR primitive. It is a transient signal that returns the ST activation state machine to F3 when written with a binary 1 and reads back as binary 0. This control is provided to allow implementation of timer T3 in software.

The Power Up bit advances the ST activation state machine to F2 when written with a binary 1 and returns it to F1 when written with a binary 0. The status of the external power supply is expected to be indicated to the controlling processor by an external power supply monitor device.

The Data Request bit equates to the PH-DATA request primitive and is used in conjunction with the priority bit to initiate the D-channel access procedure. The access procedure is initiated when written with a binary 1 and will be maintained until the required D-channel HDLC frame(s) has been transmitted. Multiple HDLC frame transmission is possible if the D-channel frame count is set to > 1 and the required data is written to the FIFOs (see section 1.6.2.3). The current status of the Data Request bit can be read at any time. Note that for a successful D-channel frame transmission the HDLC D-channel must be correctly initialised and enabled and data routing must be established between the HDLC block and the ST interface.

The Priority bit sets the primary priority level required for a pending D-channel access. A priority of binary 0 will require 8/9 D-channel echo bits at binary 1 before access is allowed. A priority of binary 1 will require 10/11 echo bits at binary 1 before access is allowed. The secondary priority (i.e. 9 instead of 8 and 11 instead of 10) is automatically selected each time a successful access is made in accordance with ITU-T I.430.

The Force Echo0 bit may be used in NT mode to force the Echo bits transmitted downstream to binary 0. This may be required in certain loopback configurations to prevent partial D-channel access by downstream devices.

1.6.2.1.2 ST Set-Up Register

Addr = $82 Reset = $01 (write/read)

Currently only bit 0 is utilised in the Setup register.

Bit 0 is designated “TE Mode”. A binary 1 written to this bit will configure the CMX635 as a TE device. A binary 0 will configure the CMX635 as an NT device. When configured as a TE device the in-built ITU-T I.430 TE activation state machine will be utilised, the reference clock timing is taken from the incoming ST bit rate, the NT-TE frame structure will be recognised and TE Multi-Framing functionality will be invoked. When configured as an NT device the activation states are under software control, the reference clock timing is taken from the IOM interface, the TE-NT generated/ recognised and NT Multi-Framing functionality will be invoked.

Bits 1 - 7 will read back as binary 0.

1.6.2.1.3 ST Interrupt Register/Interrupt Mask Register

Addr = $85 Reset = $00 (read only) - Interrupt
Addr = $84 Reset = $00 (write/read) - Mask

The ST Interrupt Register and its associated Mask Register form part of the hierarchical interrupt structure (see section 1.6.1) and provides a level-2 interrupt source to the top level Status Register. It represents an edge sensitive version of the associated ST Status Register.

Bits 0-3 of the Interrupt Register are set to binary 1 whenever the corresponding Status Register bits change (0 to 1 or 1 to 0). Bits 4 -7 are set to binary 1 only when the corresponding status bits change from binary 0 to binary 1.

All bits are reset to binary 0 when the Interrupt Register is read by software.

The Mask register will prevent the corresponding bit of the Interrupt Register from generating an ST block interrupt when set to binary 0.

1.6.2.1.4 ST Status Register

Addr = $83 Reset = $00 (read only)

The ST Status register indicates the status of the ST interface according to the definitions in the following table.

Bit	Function
[0]	Connect Indication (MPH-II(c))
[1]	Activate Indication (PH-AI)
[2]	Activate Error (MPH-EI1)
[3]	Data Indication (PH-DATA Ind)
[4]	Collision
[5]	Unused
[6]	Multi-frame Interrupt
[7]	State Machine Interrupt

These status bits represent a real time indication of ST interface Status. The edge-detected version is available in the ST Interrupt Register, which is used along with the Mask Register to generate ST status interrupts.
The Connect Indication bit will be set to binary 1 when the device is connected, i.e. state F3 and above. It will be reset to binary 0 when the device is in state F1 or F2.

The Activate Indication bit will be set to binary 1 when the device is activated i.e. when in state F7 or F8.

The Data Indication bit will be set to binary 1 when a pending D-channel access request has been granted and will be reset to binary 0 on completion of the frame.

The Collision bit will be set to binary 1 when a collision is detected during the D-channel access procedure. It is provided for monitoring purposes only.

The Multi-frame interrupt bit indicates a change in status of the Multi-frame block, which represents a level-3 interrupt source.

The State Machine Interrupt block indicates a change in status of the State Machine Register, which represents a level-3 interrupt source.

1.6.2.1.5 ST State Machine Register/ State Machine Mask Register

State Machine Addr = $87 Reset = $00
Mask Reset Addr = $88 Reset = $00 (write/read)

The ST State Machine register forms a level-3 interrupt source (see section 1.6.1) for the level-2 ST Status register (section 1.6.2.1.4).

The ST State Machine Register provides visibility of the state of the Activate/Deactivate state machine in the ST interface and the ability to write the required state for NT mode operation. It also provides an indication of the detected INFO signals. The register bits are defined in the following table.

Bit	Function
[0]	State Variable [0]
[1]	State Variable [1]
[2]	State Variable [2]
[3]	Synced
[4]	INFO0 detected
[5]	INFO1 detected
[6]	INFO2 detected
[7]	INFO3 or 4 detected

The 3 bit state variable register can be configured to interrupt at each change of state via the SM Mask Register. In TE mode the activation/deactivation control is automatic (with the exception of expiry of T3) whilst in NT mode state transition is controlled in software by writing the appropriate code to the state variable bits. The state decoding is as follows.

Encoding	NT State	TE State
000b	G1	F1
001b	G2	F2
010b	G3	F3
011b	G4	F4
100b	Unused, Set to 0	F5
101b	Unused, Set to 0	F6
110b	Unused, Set to 0	F7
111b	Unused, Set to 0	F8

The Synced bit will be set to binary 1 when the ST interface has achieved frame synchronisation.

The INFO0/1/2 bits will be set to binary 1 when the appropriate INFO signal has been detected.

The INFO3 or 4 bit will be set to binary 1 when INFO3 is detected in NT mode and INFO4 is detected in TE mode.

The SM Mask register will allow any change of state of the State Machine Register to generate an interrupt when the equivalent bit in the Mask Register is set to binary 1.

1.6.2.1.6 Multi-Frame S Register

Addr = $89 Reset = $00 (Write/Read)

All 5 defined channels of S data can be generated/received by the CMX635. The S register represents a single bit from each channel and must be written every 5 ST frames in NT Mode and read every 5 frames in TE mode. There will therefore be 4 write/reads required in 1 multi-frame (5ms) to build up the 5 channels of 4 bit S data.

The MF Status register (see section 1.6.2.1.8) indicates the start of a multi-frame and thus when the data for bit[0] of each S channel must be written/read. It also indicates when new S data is required or available and a number of other status flags.

The register bits are defined as follows.

Bit	Function
[0]	SC1x
[1]	SC2x
[2]	SC3x
[3]	SC4x
[4]	SC5x
[5]	Unused
[6]	Unused
[7]	Unused

1.6.2.1.7 Multi-Frame Q Register

Addr = $8A Reset = $0F (Write/Read)

The Multi-Frame Q register represents the complete 4 bits of the Q channel and is written every 20 ST frames in TE Mode and read every 20 frames in NT mode. The MF Status register (see section 1.6.2.1.8) indicates when new Q data is required or available. The Q register bits are allocated as follows

Bit	Function
[0] (lsb)	Q1
[1]	Q2
[2]	Q3
[3]	Q4
[4]	Unused
[5]	Unused
[6]	Unused
[7] (msb)	Unused

1.6.2.1.8 Multi-Frame Status Register/ Mask Register

Addr = $8B Reset = $00 (Read/Write) Status
Addr = $8C Reset = $00 (Write/Read) Mask

The Multi-Frame Status register forms a level-3 interrupt source (see section 1.6.1) for the level-2 ST Status register (section 1.6.2.1.4).

The status bits are defined in the following table.

Bit	Function	
[0] (lsb)	Tx Data Under-run	read only
[1]	Rx Data Over-run	read only
[2]	Tx Buffer Empty	read only
[3]	Rx Buffer Full	read only
[4]	Start of Multi-Frame	read only
[5]	Multi-Frame Synced	read only
[6]	Unused	
[7] (msb)	Multi-Frame Enable	read/write

NOTE: Tx data and Tx buffer refer to the Q data and register in TE mode and the S data and register in NT mode. Rx data and Rx buffer refer to the S data and register in TE mode and the Q data and register in NT mode.

The status bits are cleared by reading from the Status Register and, in the case of Rx buffer full and Tx buffer empty, by reading or writing the appropriate Rx/Tx register.

The least significant 6 bits of the Multi-Frame Status register are read only status bits. The most significant bit – Multi-Frame Enable – is can be written and when set to a binary 1 will enable multi-frame operation.

The Tx data under-run bit will be set to binary 1 if the Tx buffer has not been refreshed with data before new frame data is required.

The Rx data over-run bit will be set to binary 1 if new data is received before the previous data has been read from the receive buffer. The receive buffer will be overwritten with the new data.

The Tx buffer empty bit will be set to binary 1 when the data from the Tx buffer has been transferred to the multi-frame transmitter. This bit indicates the earliest that new Tx data can be loaded into the Tx buffer. In NT mode, new data must be loaded before the Tx data under-run indication (approx. 5 ST frames or 625 μS from Tx buffer empty) or the S bit data sequence will be corrupted. In TE mode the Tx under-run indication will occur approx. 20 ST frames (2.5 mS) after the Tx buffer empty indication and the Q register will be retransmitted if the Q register is not updated.

The Rx buffer full bit will be set to binary 1 when new Rx data is available for reading. The Rx buffer must be read before the Rx over-run indication or Rx data could be lost. This will occur approx. 5 ST frames (625 μS) after Rx buffer full in TE mode and 20 ST frames (2.5mS) in NT mode.

The start of multi-frame bit will be set to binary 1 at the earliest point that bit 1 of the 5 S data channels can be written to the S register in NT mode.

The multi-frame synced bit is set to binary 1 when the correct sequence of Fa and M bits have been detected, indicating that the multi-frame is synchronised.

1.6.2.1.9 Multi-Frame S Bit Counter

Addr = $8D Reset = $00 (read only)

The S Bit Counter indicates which of the 4 bits of the 5 SC registers is currently being received in TE mode. The counter will start at decimal 0 at the beginning of a multi-frame and count up 1 every 5 ST frames to a maximum of decimal 3. The counter aids reconstruction of the 5 SC registers.

The following table defines the bits.

Bit	Function
[1:0]	Binary encoded S bit count
[7:2]	Unused, reads back as binary 0

1.6.2.2 Data Routing Block

The data routing block controls the source and destination ports for the B1, B2 and D-channel data.

The available ports for B-channel data are:

- ST B1-channel
- ST B2-channel
- HDLC B1-channel
- HDLC B2-channel
- IOM B1-channel
- IOM B2-channel
- IOM IC1 channel
- IOM IC2 channel
- Codec

The available ports for D-channel data are:

- ST D-channel
- HDLC D-channel
- IOM D-channel

The B and D-channel routing is controlled by a prioritised set of 5 routing registers as follows:

B Route Control 1 (highest priority)	Addr = $B0	Reset = $00
B Route Control 2	Addr = $B1	Reset = $00
B Route Control 3	Addr = $B2	Reset = $00
B Route Control 4 (lowest priority)	Addr = $B3	Reset = $00
D Route Control	Addr = $B4	Reset = $00

The 4 B and 1 D registers can all written and read.

The bit definition for all 4 B routing registers is identical and is shown in the following table.

Bit	Function
[3:0]	Source/Destination Code A
[7:4]	Source/Destination Code B

Each B-channel source/destination port is allocated a 4-bit code and the B-channel data is routed between code A and code B ports. Each route control register can have an independent pair of ports specified, but where a conflict arises with a higher priority register the lower priority port can only receive data. Specifying the same code for A and B within a single routing register will set up a loop-back.

The B-channel port codes are as follows:

Code (hex)	Port
0	Off - no routing connection
1	ST B1-channel
2	ST B2-channel
3	IOM B1-channel
4	IOM B2-channel
5	IOM IC1 channel
6	IOM IC2 channel
7	HDLC B1-channel
8	HDLC B2-channel
9	Codec
A to F	Unused – selects no routing

Example 1:
Route ST B1 to HDLC B2, ST B2 to Codec.

B Route Control 1 = 18h
B Route Control 2 = 29h
B Route Control 3 = 00h
B Route Control 4 = 00h

Example 2:
Route ST B1 to ST B1, ST B2 to ST B2, ST B1 to Codec, ST B2 to IOM IC1

B Route Control 1 = 11h
B Route Control 2 = 22h
B Route Control 3 = 19h
B Route Control 4 = 25h

In this case a loopback has been implemented in both B-channels, whilst the downstream data is being passed through to the Codec and IOM IC1 channels. Data generated by the Codec and IOM bus is lost.

The bit definition for the D routing register is shown in the following table.

Bit	Function
[1:0]	Source/Destination Code B (low priority)
[3:2]	Source/Destination Code A (low priority)
[5:4]	Source/Destination Code B (high priority)
[7:6]	Source/Destination Code A (high priority)

The operation of the D routing register is similar to the B routing registers but the routing priority is defined in 2 halves of a single register. The source/destination codes are 2 bits wide as follows:

Code (bin)	Port
00	Off - no routing connection
01	ST D-channel
10	HDLC D-channel
11	IOM D-channel

Example 3:
Loop back ST D-channel while passing D-channel through to IOM D-channel.

D Route Control = 01010110b

1.6.2.3 HDLC FIFO Control

The CMX635 HDLC FIFOs are constructed from a single 1024 x 8 RAM, which can be flexibly subdivided into the 6 required channels (B1 Rx and Tx, B2 Rx and Tx, D Rx and TX) under software control. Each FIFO has its own Status Register and associated Mask Register to enable efficient block transfer between CMX635 and processor.

The FIFO registers available are:

- 6 base address registers, one for each channel, defining the RAM base address for each FIFO.
- 3 read ports for the Rx FIFOs and 3 write ports for the Tx FIFOs.
- A FIFO clear register for resetting each FIFO individually.
- 6 status and 6 associated Mask Registers, 1 of each for each channel.

1.6.2.3.1 Base Address Registers

The 6 base address registers used to partition the internal RAM into the 6 required Fifos are:

D Tx Base Address	Addr = $60	Reset = $00	(Write/Read)
D Rx Base Address	Addr = $61	Reset = $10	(Write/Read)
B1 Tx Base Address	Addr = $62	Reset = $20	(Write/Read)
B1 Rx Base Address	Addr = $63	Reset = $58	(Write/Read)
B2 Tx Base Address	Addr = $64	Reset = $90	(Write/Read)
B2 Rx Base Address	Addr = $65	Reset = $C8	(Write/Read)

The order of partitioning of the RAM is always as shown above with the D Tx FIFO being nearest the bottom (address 0) and the B2 Rx FIFO nearest the top. The base addresses can be set on 4 byte boundaries and are derived internally as a concatenation of the base address register (as the most significant 8 bits of the address) and binary 00 (as the least significant 2 bits). The base address of the next highest FIFO must always be greater than that of the previous FIFO base address. The reset values of the FIFO base address registers give FIFO depths of 64 bytes for the D Rx and Tx channels, 224 bytes for the B1/B2 Rx and Tx channels.

1.6.2.3.2 Read/Write Ports

The data for HDLC transmission/reception is written/read from these ports as raw unencoded octets (if autonomous mode of operation is selected). The appropriate Tx enable must be asserted before the transmit FIFOs can be written to.

The 6 FIFO ports are:

D Tx Channel	Addr = $68	(Write)
D Rx Channel	Addr = $6B	(Read)
B1Tx Channel	Addr = $69	(Write)
B1 Rx Channel	Addr = $6C	(Read)
B2Tx Channel	Addr = $6A	(Write)
B2 Rx Channel	Addr = $6D	(Read)

1.6.2.3.3 Fifo Clear Register

Addr = $6E (Write)

Each Fifo channel can be individually cleared by writing a binary 1 to the appropriate bit position. The data is not actually written, but is used to generate a transient clear strobe. The read and write pointers will be set equal to each other and the base address. This gives a convenient method to re-initialise the FIFO if required.

The bit definition is shown in the following table.

Bit	Function
[0]	D-channel Tx FIFO clear
[1]	D-channel Rx FIFO clear
[2]	B1-channel Tx FIFO clear
[3]	B1-channel Rx FIFO clear
[4]	B2-channel Tx FIFO clear
[5]	B2-channel Rx FIFO clear
[6]	Unused
[7]	Unused

1.6.2.3.4 Status and Mask Registers

Each FIFO channel has an associated status (Read) and mask (Write/Read) register as follows:

D Tx Status	Addr = $70	Reset = $00
D Tx Mask Register	Addr = $72	Reset = $00
D Rx Status	Addr = $71	Reset = $00
D Rx Mask Register	Addr = $73	Reset = $00
B1 Tx Status	Addr = $74	Reset = $00
B1 Tx Mask Register	Addr = $76	Reset = $00
B1 Rx Status	Addr = $75	Reset = $00
B1 Rx Mask Register	Addr = $77	Reset = $00
B2 Tx Status	Addr = $78	Reset = $00
B2 Tx Mask Register	Addr = $7A	Reset = $00
B2 Rx Status	Addr = $79	Reset = $00
B2 Rx Mask Register	Addr = $7B	Reset = $00

These registers form a level-3 interrupt source to the level-2 HDLC B1, B2 and D HDLC Status registers (section 1.6.2.8.2).

The Status Registers all have the same bit allocations as shown in the following table.

Bit	Function
[0]	FIFO Over write - clears on stats reg read
[1]	FIFO Under read - clears on stats reg read
[2]	FIFO Empty flag - clears on FIFO status change
[3]	FIFO Full flag - clears on FIFO status change
[4]	FIFO Near Empty (Tx FIFO only) - clears on FIFO status change
[5]	FIFO Near Full (Rx FIFO only) - clears on FIFO status change
[6]	Unused
[7]	Unused

The FIFO overwrite bit is set to binary 1 if a write to the FIFO is made when full. A write to the FIFO can be via the data port for a Tx FIFO or an internal write for an Rx FIFO.

The FIFO under-read bit is set to binary 1 if a read from the FIFO is made when empty. A read from the FIFO can be via the data port for an Rx FIFO or an internal read for a Tx FIFO.

The FIFO empty bit has a programmable polarity. When the Mask Register bit 6 is binary 0, the empty flag will be set to binary 1 when the last available location in the RAM is read. It will only clear to binary 0 when the FIFO is written. When the Mask Register bit 6 is binary 1 the sense of the flag is reversed - i.e. it becomes FIFO not-empty.

The FIFO full bit has a programmable polarity. When the Mask Register bit 7 is binary 0, the FIFO full bit will be set to binary 1 when the last remaining location in the RAM is written. It will only clear to binary 0 when the FIFO is read. When the Mask Register bit 7 is binary 1 the sense of the flag is reversed – i.e. it becomes FIFO not-full.

The FIFO near empty bit is only applicable to the Tx FIFOs and will be set to binary 1 when only 8 octets remain in the FIFO. It will only clear to binary 0 when the FIFO contains more than 8 octets of data. For the Rx FIFOs this bit is permanently set to binary 0.

The FIFO near full bit is only applicable to the Rx FIFOs and will be set to binary 1 when only the FIFO is 8 octets short of being full. It will only clear to binary 0 when the FIFO is read and more

than 8 octets of space is available in the FIFO. For the Tx FIFOs this bit is permanently set to binary 0.

The Mask Register bits 0 to 5, when set to binary 0, will prevent a binary 1 in the corresponding Status Register bit position from generating a level-3 interrupt request (see section 1.6.1) to the level-2 HDLC Status Register (see 1.6.2.8.2). The function of mask bits 6 and 7 is as previously explained.

1.6.2.4 HDLC Rx Channel Control

Each of the 3 Rx Channels (B1, B2 and D) has a similar set of control registers as follows.

- Rx Mode register
- 9 address matching control registers
- Level-2 HDLC Status register and Mask Register
- Level-3 Rx Status register and Mask Register
- Rx Octet Counter

Rx Mode Register

D-channel	Addr = $00	Reset = $00	(Write/Read)
B1-channel	Addr = $20	Reset = $00	(Write/Read)
B2-channel	Addr = $40	Reset = $00	(Write/Read)

The Rx Mode register controls the receive channel operation as follows:

1.6.2.5 D Channel Rx Mode Register	
Bit	**1.6.2.6 Function**
[2:0]	Minimum expected receive octet count
[3]	Receive Enable
[4]	Reserved
[5]	Unused
[6]	Unused
[7]	Unused

1.6.2.7 B Channel Rx Mode Register	
Bit	**1.6.2.8 Function**
[2:0]	Minimum expected receive octet count
[3]	Receive Enable
[4]	Receive Channel Transparent Mode
[5]	Reserved
[6]	Unused
[7]	Unused

The minimum receive octet count (all received octets between opening and closing flags) sets the limit below which an error status is generated for short received frames.

The receive enable bit when set to binary 1 is the master enable for the Rx channel and must be enabled to read the Fifo. When disabled, any data remaining in the fifo will be lost and the fifo reset.

The receive channel transparent mode bit when set to binary 1 enables the transparent receive mode in the B-channels which does not process flags, bit stuffing, addresses or CRC. All received

data is written to the FIFO and the processing of framing and protocols becomes the responsibility of the controlling software.

1.6.2.8.1 Address Matching Control registers

The user can initialise up to 4 1st (A1-A4) and 4 2nd (B1-B4) address-matching registers for comparing incoming SAPI and TEI address fields. The combination of matching performed with these registers is set by the Match Request Register. Only the most significant 7 bits are compared as the lsb of each address field acts as an address extension bit and does not form part of the address. The registers can all be read or written to.

The address matching registers are designated as follow:

Address Match Register A1, A2, A3 and A4 (Reset = $00):

A1 D-channel	Addr = $01	A1 B1-channel	Addr = $21	A1 B2-channel	Addr = $41
A2 D-channel	Addr = $02	A2 B1-channel	Addr = $22	A2 B2-channel	Addr = $42
A3 D-channel	Addr = $03	A3 B1-channel	Addr = $23	A3 B2-channel	Addr = $43
A4 D-channel	Addr = $04	A4 B1-channel	Addr = $24	A4 B2-channel	Addr = $44

Address Match Register B1, B2, B3 and B4 (Reset = $00):

B1 D-channel	Addr = $05	B1 B1-channel	Addr = $25	B1 B2-channel	Addr = $45
B2 D-channel	Addr = $06	B2 B1-channel	Addr = $26	B2 B2-channel	Addr = $46
B3 D-channel	Addr = $07	B3 B1-channel	Addr = $27	B3 B2-channel	Addr = $47
B4 D-channel	Addr = $08	B4 B1-channel	Addr = $28	B4 B2-channel	Addr = $48

Match Request Register (Reset = $00)

D-channel	Addr = $09
B1-channel	Addr = $29
B2-channel	Addr = $49

The Match Request Register for each channel defines the extent of address matching according to the table below:

Bit	Function
[0]	Match 1st address byte to selected A match registers
[1]	Match 2st address byte to selected B match registers
[2]	Match broadcast addresses, 1st address to FFh, 2nd address to FEh
[3]	Use match registers A1 and/or B1
[4]	Use match registers A2 and/or B2
[5]	Use match registers A3 and/or B3
[6]	Use match registers A4 and/or B4
[7]	Unused

Bit 0, when set to binary 1, enables address matching on the 1st received address octet and can be used in isolation for single address octet HDLC frames.

Bit 1, when set to binary 1, enables address matching on the 2nd received address octet and must be used in conjunction with bit 0 set to binary 1.

If both bit 0 and bit 1 are set to binary 0, address matching is turned off and all addresses will “match” i.e. all received frames will be written to the FIFO and can generate receive interrupts.

Bits 3 to 6 define how many and which addresses are compared to the incoming address fields. A binary 1 will enable the relevant match register, which will be compared, along with other selected match registers, against the incoming address fields.

1.6.2.8.2 Level-2 HDLC Status and Mask Registers

The layer-2 HDLC Status Register (Read Only) indicates the status of the receive and transmit channels and accepts level-3 interrupt requests from the Rx and Tx FIFOs. There is a Status Register and a Mask Register (Write/Read) for each channel as follows:

Status Registers:

D-channel	Addr = $0B	Reset = $00
B1-channel	Addr = $2B	Reset = $00
B2-channel	Addr = $4B	Reset = $00

Mask Registers:

D-channel	Addr = $0D	Reset = $00
B1-channel	Addr = $2D	Reset = $00
B2-channel	Addr = $4D	Reset = $00

The bit definition is as follows:

Bit	Function
[0] (lsb)	Received good frame
[1]	Address match
[2]	Tx abort
[3]	Tx frame completed
[4]	Tx all frames completed
[5]	Layer-3 Status Register interrupt
[6]	Rx FIFO status interrupt
[7] (msb)	Tx FIFO status interrupt

The received good frame bit is set to binary 1 when all of the conditions for a successful frame reception have been met (above minimum length, address matched, aligned flags, correct CRC).

The address match bit is set to binary 1 when a successful match has been found with the specified addresses (see section 1.6.2.8.1). Note that if both 1st and 2nd address matching is specified, the status will not change until the 2nd address field successfully matches.

The Tx abort bit is set to binary 1 if the transmission is aborted. This can occur if the Tx FIFO runs out of data (fifo empty) or in the D-channel, if the D-channel access is removed possibly due to a detected collision.

The Tx frame completed bit is set to binary 1 when a frame has been successfully transmitted.

The Tx all frames completed bit is set to binary 1 when all frames in a multi-frame HDLC transmission have been completed.

Bits 5, 6 and 7 indicate an interrupt request from level-3 Status Registers.

The Mask Register bits, when set to binary 0, will prevent a binary 1 in the corresponding Status Register bit position from generating a level-2 interrupt request (see section 1.6.1) to the level-1 top level Status Register.

1.6.2.8.3 Level-3 Receive Status and Mask Registers

There is a level-3 Status Register (Read Only) and a Mask Register (Read/Write) for each channel as follows:

Status Registers:

D-channel	Addr = $0C	Reset = $00
B1-channel	Addr = $2C	Reset = $00
B2-channel	Addr = $4C	Reset = $00

Mask Registers:

D-channel	Addr = $0E	Reset = $00
B1-channel	Addr = $2E	Reset = $00
B2-channel	Addr = $4E	Reset = $00

The level-3 receive Status Register provides further information on aborted receive frames as follows:

Bit	Function
[0]	CRC error
[1]	Rx octet mis-aligned error
[2]	Rx packet aborted
[3]	Rx short packet
[4]	Rx Octet Counter roll over
[5]	Unused
[6]	Unused
[7]	Unused

An Rx octet mis-aligned flag is generated when a non-integer number of octets have been received between an opening and closing flag.

An Rx packet aborted flag is generated when 7 consecutive binary 1s are received during a frame.

An Rx short packet flag is generated when the received packet length is less than the pre-programmed minimum.

The Rx Octet Counter roll over bit is set to binary 1 when the Rx Octet counter rolls over (see section 1.6.2.8.4).

The Mask Register bits, when set to binary 0, will prevent a binary 1 in the corresponding Status Register bit position from generating a level-3 interrupt request (see section 1.6.1) to the level-2 HDLC Status Register.

1.6.2.8.4 Rx Octet Counter

D-channel	Addr = $0F	Reset = $00	(Read Only)
B1-channel	Addr = $2F	Reset = $00	(Read Only)
B2-channel	Addr = $4F	Reset = $00	(Read Only)

The Rx octet counter counts the number of octets received into the Rx FIFO - note modulus of 256 means that rollover could occur on large FIFOs. Level-3 receive Status Register bit 5 warns of this condition (see section 1.6.2.8.3).

NOTE: When flags are used as the receive interframe idle mode (Flag Idle) the Rx Octet counter must be read within 900uS (D channel), or 250uS (B Channel), of receipt of a Received Good Frame interrupt for reliable operation.

1.6.2.9 HDLC Tx Channel Control

Each of the 3 Tx Channels (B1, B2 and D) has a similar set of control registers as follows.

- Tx Mode register
- 2 Tx Address Registers
- Tx Frame Count Register
- Tx Octet Count Register

1.6.2.9.1 Tx Mode Register

D-channel	Addr = $10	Reset = $00	(Write/Read)
B1-channel	Addr = $30	Reset = $00	(Write/Read)
B2-channel	Addr = $50	Reset = $00	(Write/Read)

The Tx mode register controls the HDLC transmit functions. The bit definition is given in the following table:

Bit	Function
[0]	Link List Mode
[1]	User CRC Mode
[2]	Transparent Mode
[3]	Tx enable
[4]	Single Address Mode
[5]	User Address Mode
[6]	Force error
[7]	Back to back mode

A binary 1 in the appropriate bit position selects the described function.

Link list mode is a mode of operation intended for multi-frame HDLC transmissions. It enables the FIFOs to autonomously transmit multiple frames of varying lengths and is used in conjunction with the Tx frame count register (see 1.6.2.9.3). To use link list mode, the FIFOs are written with multiple frames of data, the first octet of which is the number of data octets in the following frame. During transmission at the start of each new frame the octet count is automatically read from the FIFO and loaded into the Tx octet counter (section 0). This process is repeated for the number iterations specified in the Tx Frame Count register.

User CRC mode when selected requires the CRC octets to be written to the Tx FIFO and included in the Tx octet count. The software must calculate the correct CRC value. When this mode is not selected the CRC values are automatically calculated and appended to the frame and are not included in the octet count.

Transparent mode when selected will cause only the FIFO data to be transmitted with no HDLC formatting at all (i.e. no flags, bit stuffing, address octets or CRC octets).

Tx Enable is the master enable for the Tx channel. This bit must be set to binary 1 before the relevant fifo can be written. In addition any data remaining in the fifo when this bit is set to binary 0 will be lost i.e. the fifo will be reset.

Single address mode when selected, causes only a single address octet to be prepended to the data octets (Tx address high register and only if user address mode is not selected).

User address mode when selected will prevent either Tx address high or Tx address low from being prepended to the data octets. The required address octet(s) must be written to the FIFO along with the data octets.

Force error when selected will cause an erroneous CRC value to be generated. This is used for system test purposes only.

Back to back mode when selected will cause a single flag to be generated between consecutive frames of a multi-frame transmission i.e. a shared start/end flag.

1.6.2.9.2 Tx Address Registers

2 Tx address registers for each channel define the address to be transmitted in the first and second octet of a frame when the user address mode is not selected. The registers are:

Tx Address High (1st octet address):

D-channel	Addr = $15	Reset = $00	(Write/Read)
B1-channel	Addr = $35	Reset = $00	(Write/Read)
B2-channel	Addr = $55	Reset = $00	(Write/Read)

Tx Address Low (2nd octet address):

D-channel	Addr = $14	Reset = $00	(Write/Read)
B1-channel	Addr = $34	Reset = $00	(Write/Read)
B2-channel	Addr = $54	Reset = $00	(Write/Read)

1.6.2.9.3 Tx Frame Count Register

D-channel	Addr = $16	Reset = $00	(Write/Read)
B1-channel	Addr = $36	Reset = $00	(Write/Read)
B2-channel	Addr = $56	Reset = $00	(Write/Read)

The Tx frame count register sets the required number of frames to be transmitted in a multi-frame transmission and, in the B channel, allows an interframe fill of HDLC flags (Flag Idle). The bit definition for B channel operation is given in the following table:

Bit	Function
[6:0]	Transmit Frame Count
[7]	Set Flag Idle Mode

Bits [6:0] ([7:0] in the D channel) allow a maximum frame count of 127 (255 for D channel) to be set for multi-frame transmissions. As the end of each frame is transmitted, the register value is decremented. This allows multiframe transmission progress to be monitored. The HDLC channel returns to idle mode when the counter reaches zero. The count should be set to 1 for single frame transmissions.

NOTE: Setting the frame count to a non-zero value is the “normal” method of initiating a transmission in the B channels, however transmission will not begin until valid routing has been set up. Transmission in the D channel also requires the ST interface Data Request primitive to be written.

Bit [7] in the B channel, when set to binary 1, enables Flag Idle mode of transmission whereby interframe time is filled with continuous HDLC flags. Delays between frames may occur in single frame transmission mode, when the frame counter decrements to zero or when the fifo becomes empty in multiframe transmission mode. If bit [7] is set to binary 0, Mark Idle mode is selected whereby interframe fill is HDLC marks (binary 1, no signal).

Tx Octet Count Register

D-channel	Addr = $17	Reset = $00	(Write/Read)
B1-channel	Addr = $37	Reset = $00	(Write/Read)
B2-channel	Addr = $57	Reset = $00	(Write/Read)

The Tx octet count register sets the number of octets to be transmitted in any frame. This must be set for single frames and non-linked list mode of multi-frame transmission in which the frame lengths must be constant. The maximum frame length for multi-frame operation is 256 FIFO octets. To transmit single frames greater than 256 octets, the Tx octet counter must be re-written before it decrements to 0.

For non-linked list multi-frames the Tx octet count is used to delimit the FIFO data into individual constant length frames.

In linked list mode multi-frames the octet count is written to the FIFO as the first octet of each frame and is automatically loaded into the octet count register to establish the length of the current frame. The frame length can therefore be variable.

1.6.2.10 IOM Interface Control

The IOM interface allows export and import of B and D-channel data as well as programming control of other IOM compliant devices such as the CMX625 POTS Codec.

The registers available to control the interface are:

- IOM Control Register
- Monitor Channel Control Register
- Monitor Channel Tx Register
- Monitor Channel Rx Register
- IOM Status Register, Mask Register and Real Time Status
- CI0 and CI1 Channel Transmit and Receive Registers

1.6.2.10.1 IOM Control Register

Addr = $90 Reset = $00 (Write/Read)

The IOM control register provides the control of the IOM operating modes.

The bits are defined according to the following table:

Bit	Function
[0]	Timing Master
[1]	IC Channel Bus Reversal
[2]	Reserved – set to binary 0
[3]	IOM Enable
[4]	Use Deactivate State Machine
[5]	Active Outputs
[6]	Monitor Channel Bus Reversal
[7]	Unused

The Timing Master bit when set to binary 1 will set the CMX635 as the IOM timing master. In this mode the IOM frame sync (FSC) and clock (DCL) are generated by and exported from the CMX635. When set to binary 0 these signals are imported from an external timing master device

(i.e. when configured into an NT system). The CMX635 will always operate as the IOM control master.

The IC Channel Bus Reversal bit when set to binary 1 enables bus reversal in the IC1 and IC2, channels. Similarly, the Monitor Channel Bus Reversal bit when set to binary 1 enables bus reversal in the Monitor1 and CI1 channels. This means that data is transmitted on the IOM Rx pins and received on the Tx pins (c.f. normal operation - transmit on Tx, receive on Rx). Note that the Tx pin is designated DD when the CMX635 is an upstream device to other IOM devices (TE) and DU when configured as a downstream device (NT). Similarly the Rx pin is DU for a TE and DD for an NT. A possible application of this function is when the CMX635 is configured in an intelligent NT system, where it is the downstream device to a U interface transceiver. To expand the POTS capability to 2 ports, a CMX625 could be added as another downstream device. The Rx and Tx pins of the CMX635 and CMX625 would be connected together and bus reversal in the monitor channel would be selected to allow the CMX625 to be programmed from the CMX635 whilst still being capable of receiving B-channel data directly from the U interface.

The Use Deactivate State Machine bit when set to binary 1 will delay IOM deactivation after a deactivate command has been issued, until 4 frames of the primitive DC (Deactivate confirmation - 1111b) has been received from all downstream devices.

The Active Outputs bit when set to binary 1 will cause the Tx pin to change from an open drain output, requiring an external pull-up resistor, to a fully driven output. This mode enables lower power and faster drive of the DD line in TE mode as an external pull-up resistor is not required. To avoid contention on the DD line, Active Output mode should not be selected when bus reversal mode is also selected.

1.6.2.10.2 Monitor Channel Control Register

Addr = $92 Reset = $02 (Write/Read)

The Monitor Channel Control Register selects the active monitor channel and provides for control of the monitor channel transmit sequence. The bits are defined according to the following table:

Bit	Function
[0]	Transmit EOF code
[1]	Monitor Channel #1 select
[2]	Tx Abort Request
[7:3]	Unused

The Transmit EOF bit must be set to binary 1 when all of the required data octets have been transmitted. This causes an EOF code to be transmitted (MX high for 2 consecutive frames).

The Monitor Channel Select bit should be set to binary 1 to select transmission (and reception) in the MON1 channel. Set to binary 0 to select MON0 as the active channel.

The Tx Abort bit when set to binary 1 will cause an abort code to be transmitted (MX high for 2 consecutive frames) and return the IOM monitor channel interface to the idle state.

1.6.2.10.3 Monitor Channel Tx Register

Addr = $91 Reset = $FF (Write Only)

This register should be written with the desired monitor channel transmit data when the Tx Buffer Empty bit in the Status Register is set to binary 1 (see section 1.6.2.10.5). Note that there is no maximum response time requirement to the Tx Buffer Empty flag as the transmission speed is controlled by a hardware handshake mechanism (section 1.7.2).

1.6.2.10.4 Monitor Channel Rx Register

Addr = $93 (Read Only)

This register contains the latest monitor channel receive data and should be read when the Monitor Rx Data available bit in the Status Register is set to binary 1 (see section 1.6.2.10.5). Note that there is no maximum response time requirement to the Rx Data Available flag as the transmission speed is controlled by a hardware handshake mechanism (section 1.7.2).

1.6.2.10.5 IOM Status Register/Mask Register/Real Time Status

Status Register	Addr = $94		(Read Only)
Mask Register	Addr = $96	Reset = $00	(Write/Read)
Real Time Status	Addr = $95		(Read Only)

The bits of the IOM Status Register are defined according to the following table:

Bit	Function
[0]	New CI0 Data Available
[1]	New CI1 Data Available
[2]	Monitor Rx Data Available
[3]	Monitor Tx Buffer Empty
[4]	Monitor Rx EOF Detected
[5]	Monitor Rx Abort Detected
[6]	Monitor Tx Abort Detected
[7]	Monitor Tx Idle

The New CI0/CI1 Data Available bits are set to binary 1 when a change is detected in the CI bus data. The data is read from the appropriate CI receive register (see section 1.6.2.10.6).

The Monitor Rx Data Available bit is set to binary 1 when a new Rx data octet is received in the active monitor channel.

The Monitor Tx Buffer Empty bit when set to binary 1, indicates that a new octet can be written to the monitor Tx register.

The Monitor Rx EOF bit is set to binary 1 when an end of file code is detected in the monitor Rx channel.

The Monitor Rx Abort bit is set to binary 1 when a premature end of File code is detected in the monitor Rx channel. This can occur if an incorrect handshake sequence is detected or the received data is corrupted.

The Monitor Tx Abort bit is set to binary 1 when an incorrect handshake sequence is detected or a Tx Abort command is issued.

The Monitor Tx Idle bit, when set to binary 1, indicates when the monitor transmit channel has reached its idle state. The software should wait for the Tx Idle status before beginning transmission of another monitor channel message.

1.6.2.10.6 CI Channel Transmit/Receive Registers

Transmit:

CI0 Tx	Addr = $97	(Write/Read)
CI1 Tx	Addr = $98	(Write/Read)

Receive:

CI0 Rx	Addr = $99	(Read Only)
CI1 Rx	Addr = $9A	(Read Only)

The CI0 Transmit Register is used to set the required 4 bit CI0 data, to control the BAC (Bus Access) bit in the TIC channel and to issue an IOM timing request (TIM) to an upstream device. The bits are defined in the following table:

Bit	Function	Reset
[3:0]	CI0 Data	1111b
[4]	BAC	0
[6:5]	Unused	-
[7]	TIM	0

The CI0 Data is used to transmit 4 bit layer-1 primitive codes to external layer-1 devices.

The BAC bit is used when the CMX635 is configured as a downstream device. It is transmitted as bit 4 of the TIC bus (Bit 5 of the last octet of channel 2 in a terminal mode frame). The BAC bit is provided to support upstream devices that require BAC control. The CMX635 does not support full TIC bus access protocol and cannot be used with other downstream layer-1 devices on the same IOM bus. See section 1.7.2.5 for more details on TIC bus operation.

The TIM bit when set to binary 1, issues a hardware timing request (IOM Tx or DU pulled low) and is intended for use when the CMX635 is configured as a downstream device. The TIM request will persist until either a hardware reset or activity is detected on the IOM DCL signal.

The CI1 Transmit Register is used to set the required 6 bit CI1 data and only the 6 LSBs are used.

The CI0 Receive Register contains the latest 4-bit CI0 value in the 4 LSBs. The msb is set to binary 1 when the same CI0 data has been received in at least 2 consecutive frames.

The CI1 Receive Register contains the latest 6 bit CI1 value in the 6 LSBs. The msb is set to binary 1 when the same CI1 data has been received in at least 2 consecutive frames.

1.6.2.11 Clock and Power Control

The Clock and Power Control block provides the means to limit power consumption by disabling functions not required for particular applications (or particular modes in the same application). It also provides the necessary status signals to allow “wake up” from a powered down state.

The Clock and Power block consists of the following registers:

- Clock Enable Register
- Audio Power Save Register
- Tone Power Save Register
- Status Register and Mask

1.6.2.11.1 Clock Enable Register

Addr = $D0 Reset = $3F (Write/Read)

The clock enable register allows the master clock to the individual functional blocks to be turned off in order to reduce power consumption. The bits are defined according to the following table:

Bit	Function	Reset
[0]	IOM Clk Enable	1
[1]	ST Interface Clock Enable	1
[2]	DPLL Clock Enable	1
[3]	Data Routing Clock Enable	1
[4]	HDLC Block Clock Enable	1
[5]	Speaker Phone Clock Enable	1
[6]	Unused	0
[7]	Unused	0

The clocks to the functional blocks are enabled by setting the relevant bit position to binary 1.

1.6.2.11.2 Audio Enable Register

Addr = $D5 Reset = $00 (Write/Read)

The analogue functions of the audio input/output path can be individually enabled or set to a low power state with the audio enable register. The bits are defined according to the following table:

Bit	Function	Reset
[0]	ST Transceiver Enable	0
[1]	Input Amp Rx1 Enable	0
[2]	Input Amp Rx2 Enable	0
[3]	Earpiece Amp Tx1 Enable	0
[4]	Speaker Amp Tx2 Enable	0
[5]	Sidetone Amp Enable	0
[6]	Codec Enable	0
[7]	Power Save All	0

When set to binary 1 the relevant analogue functional blocks are enabled. When set to binary 0 they are set to their low power mode.

When bit 7 is set to binary 1 all of the remaining analogue functions are set to their zero power mode. This bit should **not** be asserted unless **all** of the other analogue functions are disabled. Note that even when all of the analogue functions are disabled, a small power drain still exists due to the “wake up” function remaining enabled. Setting bit 7 to binary 1 will cause all analogue power drain to be removed, including that due to the wake-up function. In this mode, activity on the ST bus will not generate a wake-up status signal.

1.6.2.11.3 Tone Enable Register

Addr = $D6 Reset = $00 (Write/Read)

The analogue functions of the tone generator/decoder function can be individually enabled or set to a low power state with the tone enable register. The bits are defined according to the following table:

Bit	Function	Reset
[0]	DTMF Decoder Enable	0
[1]	Tone Generator Enable	0
[2]	FSK Tone Enable	0
[3]	Ring Generator Enable	0
[4]	SPM Generator Enable	0
[5]	Tone/FSK/Ring On/Off	0
[6]	SPM On/Off	0
[7]	Unused	0

When set to binary 1 the relevant analogue functional blocks are enabled. When set to binary 0 they are set to their low power mode. Note that the tone and FSK outputs cannot be enabled simultaneously. The FSK output has highest priority and will be unconditionally enabled when set to binary 1. The tone output will only be enabled when set to binary 1 and the FSK output is disabled.

The Ring, Tone and FSK signals are turned on when bit 5 is set to binary 1 and off when set to binary 0. The active signal type is selected by the Tone or FSK enable bits and, in the case of the Ring signal, by selecting the appropriate ring frequency from the tone tables. When controlled from bit 5, the Tone signal starts from $V_{BIAS,}$ and returns to V_{BIAS} before ending. When FSK mode is enabled, bit 5 initiates FSK transmission.

The SPM output tone is ramped up to its maximum amplitude when bit 6 is set to binary 1 and ramped down again when set to binary 0 (see section 1.6.2.14.1). Note that when setting the SPM generator to its power save mode after outputting an SPM tone, the tone must first be turned off and then sufficient time allowed for the tone to ramp down to zero amplitude (approx. 4.5mS) before the generator is power saved.

1.6.2.11.4 Status/Mask Registers

Status Addr = $D2 Reset = $00 (Read Only)
Mask Addr = $D1 Reset = $00 (Write/Read)

The Clock and Power Status Register indicates the presence of IOM or ST wake-up signals on the respective busses and reports progress of the IOM deactivation sequence. The bits are defined according to the following table:

Bit	Function
[0]	IOM Wakeup (TIM)
[1]	ST Wakeup
[2]	IOM Deactivated
[3]	CI0 Channel Idle
[7:4]	Unused

The IOM Wakeup bit when set to binary 1 indicates activity on the IOM bus. When the TIM interrupt is detected, the software should enable the IOM interface by enabling the IOM master clock (see section 1.6.2.11.1) and enabling the IOM block (see section 1.6.2.10.1). This will start

the IOM DCL and FSC outputs (timing master mode) and allow CI0 primitives to be exchanged if required.

The ST Wakeup bit when set to binary 1 indicates activity on the ST bus. It is only required when the ST bus and transceiver circuitry is in the power save mode and is used by the software to initiate reactivation of the ST bus.

The IOM Deactivated bit when set to binary 1 indicates that the IOM bus has been completely deactivated functionally and that the master clock to the IOM block can be safely disabled. It is intended for use with the IOM deactivate state machine (see section 1.6.2.10.1) and allows time for all downstream IOM devices to deactivate properly before the IOM clocks are stopped. If the deactivate state machine is not used this bit will be set to binary 1 as soon as the IOM disable command is issued.

The CI0 Channel Idle bit is set to binary 1 when the deactivate state machine is used, when the BAC bit of the TIC bus is high for 2 consecutive frames and when the CI0 code DI (1111b) is being received.

The Mask Register bits, when set to binary 0, will prevent a binary 1 in the corresponding Status Register bit position from generating a level-2 interrupt request (see section 1.6.1) to the level-1 top level Status Register.

1.6.2.11.5 Clock Control Register

Addr = $D7 Reset = $00

The Clock Control register enables

- 12.288MHz or 15.36MHz master crystal mode
- Buffered Master Clock or 1.536MHz Phase Locked clock output
- Stopping of master crystal oscillator

The bit definition of the Clock Control register is as follows:

Bit	Function
[0]	Stop Xtal
[1]	Select Master Xtal
[2]	Select Output Clock
[7:3]	Unused

When the Stop Xtal bit is set to binary 1 the master crystal oscillator is disabled. This will set the CMX635 into its lowest power state. The Xtal can only be restarted by asserting a hardware reset on the device Reset pin.

When a 15.36MHz master crystal is to be used (possibly for NT configurations) the Select Master Xtal bit should be set to binary 1. When a 12.288MHz crystal is to be used it should be set to binary 0 (default).

A buffered version of the master clock is output on the CLKOUT pin (47) when the Select Output Clock bit is set to binary 0. When set to binary 1, the 1.536MHz IOM clock is output.

1.6.2.12 Speaker Phone Statistics

The speakerphone functions are provided to enable an efficient hands free speakerphone design to be implemented using the CMX635. The design of speakerphone systems breaks down into two critical functions.

The first function gathers statistical data on the transmit and receive data streams in which sufficient data processing must be done to separate and identify speech data from background noise on each channel. The CMX635 provides the hardware within the device to carry out these tasks.

The second function is an algorithm to decide which channel is dominant (if any) and partition the overall loop gain between the receive and transmit path so that acoustic feedback is prevented. The software running on the system controller provides this task. The transmit and receive gains are adjusted by writing to the Speakerphone attenuation register and the Loudspeaker Gain Register respectively. This approach provides a high degree of latitude to system level designers to create inventive strategies in speakerphone functions whilst relieving the core processor from computational tasks at high data rates. All internal digital signal processing is carried out with 24-bit precision with the most significant 8 bits available to the user.

The CMX635 provides the following data processing functions on both the receive and transmit data paths. Note that all data processing is done on companded data in both channels.

- Full wave rectification conversion of input data
- Noise filtering of converted data with long time constant (~ 10 s)
- Speech filtering of converted data with fast attack time constant (~ 1 ms) and selectable slow decay time constant (128, 256, 500 ms).
- Auto Gated Noise Filter i.e. the statistics integration is suspended when speech is detected in the channel.
- Interrupt control system based upon filter output comparators, which provides three interrupt sources for each channel. The interrupt sources are:
    1) Speech filter output > noise filter output
    2) Speech filter output > noise filter output + programmable threshold
    3) Speech filer output > noise filter output + programmable threshold +/- hysteresis value.
- Interrupt generation when a change in any of the above conditions takes place. The user can poll the indicator flag bits to determine the exact condition that exists within the channel.
- A hysteresis register to prevent rapid and spurious interrupts when a slow noisy signal moves close to the integrated background level.

The transmit path operates independently on two transmit data streams. One is provided after the attenuation block (see analogue block diagram, section 1.2.2) and the other before the attenuator. The pre-attenuated statistics allow the input to be fully characterised when the transmit channel is deemed to be the non-dominant channel, and thus attenuated (or even muted).

The value of the filtered data in both the noise and speech filter is available to the user, however the filter is updated at the 8kHz sample rate and to allow the processor to synchronise to the sample rate an 8kHz interrupt is provided.

All interrupts are maskable.

The registers provided for speakerphone control are:

- Mode Register
- A Receive Channel and Transmit Channel Threshold Register
- A Receive Channel and Transmit Channel Hysteresis Register
- A Receive Channel and Transmit Channel Speech Filter Output Register
- A Receive Channel and Transmit Channel Noise Filter Output Register
- Status, Interrupt Status and Mask Registers

1.6.2.12.1 Speakerphone Mode Register

Addr = $C0 (Write/Read)

The Speakerphone Mode Register bit allocations are defined in the following table:

Bit	Function
[1:0]	Transmit Channel Speech Filter Coefficient
[2]	Transmit Channel Auto Integrate Mode
[4:3]	Receive Channel Speech Filter Coefficient
[5]	Receive Channel Auto Integrate Mode
[7:6]	Attenuated Channel Speech Filter Coefficient

The Co-efficient codes for bits [1:0], [4:3] and [7:6] are identical and are defined below:

Code	Function
00b	127ms discharge time constant
01b	256ms discharge time constant
10b	512ms discharge time constant
11b	1ms charge and discharge time constant

Bits 2 and 5 control the auto-integrate mode of the respective channels. A binary 1 turns auto-integrate mode on. The auto-integrate function turns off the noise filter integration when speech is detected giving a more accurate noise level.

1.6.2.12.2 Receive/Transmit Channel Threshold Registers

Receive Addr = $C2 (Write/Read)
Transmit Addr = $C1 (Write/Read)

The receive and transmit threshold registers contain the absolute level above the average noise value that will generate a Status1 interrupt (speech level > noise + threshold).

The threshold level has a magnitude of 6 bits and is contained in register bits [5:0]. Bits [7:6] are unused.

1.6.2.12.3 Receive/Transmit Channel Hysteresis Registers

Receive Addr = $C4 (Write/Read)
Transmit Addr = $C3 (Write/Read)

The receive and transmit hysteresis registers contain the value of the hysteresis level applied to the threshold value (section 1.6.2.12.2) before a Status 2 interrupt (speech level > noise + threshold ± hysteresis) is generated.

The hysteresis level has a magnitude of 5 bits and is contained in register bits [4:0]. Bits [7:5] are unused.

1.6.2.12.4 Receive/Transmit/Attenuated Channel Speech Filter Outputs

Receive	Addr = $C6	(Read Only)
Transmit	Addr = $C5	(Read Only)
Attenuated	Addr = $C7	(Read Only)

The speech filter registers contain the most significant 8 bits of the 24-bit speech filter output.

The registers can be read asynchronously at any time to obtain the latest value of the speech filter output, or they can be read synchronously with the 8kHz sample clock to enable every speech filter output change to be read. This is achieved through the use of an 8kHz sample interrupt (section 1.6.2.12.6). The synchronous read facility may be used where the internal speech detectors are not used and software algorithms are implemented instead.

1.6.2.12.5 Receive/Transmit Channel Noise Filter Outputs

Receive	Addr = $C9	(Read Only)
Transmit	Addr = $C8	(Read Only)

The noise filter registers contain the most significant 8 bits of the 24-bit noise filter output. Like the speech filter output they can be read synchronously or asynchronously.

The noise filter has a fixed symmetrical attack and decay time constant of approximately 10 seconds and is used to determine the background noise level such that speech can be differentiated from it. It can be frozen during detected speech using the auto-integrate function.

1.6.2.12.6 Status/Interrupt/Mask Registers

Status	Addr = $CC	Reset = $00	(Read Ony)
Interrupt	Addr = $CB	Reset = $00	(Read Only)
Mask	Addr = $CA	Reset = $00	(Write/Read)

The speakerphone interrupt request forms a level-2 interrupt to the top level Status Register (section 1.6.1) and is derived from the SP Interrupt Status Register. This register indicates whenever a change in state has occurred in the corresponding Status register bits (which give a real time indication of the various status inputs). The Mask Register bits, when set to binary 0, will prevent a binary 1 in the corresponding interrupt Status Register bit position from generating a layer-2 interrupt request.

The interrupt Status Register is cleared to all binary 0s when read by software.

The interrupt Status Register bits are defined in the following table:

Bit	Function
[0]	Tx Status 0 changed state
[1]	Tx Status 1changed state
[2]	Tx Status 2 changed state
[3]	Rx Status 0 changed state
[4]	Rx Status 1changed state
[5]	Rx Status 2 changed state
[6]	8kHz sample interrupt
[7]	Unused

Bits [5:0] indicate that there has been a change in state in the corresponding Status Register bit positions when set to binary 1. Change of state refers to either binary 0 to 1 or binary 1 to 0 transitions.
Bit 6 will be set to binary 1 at each reference 8kHz sample clock and may be used for synchronous reads of the filter output registers.

The speakerphone Status Register continuously indicates the current status of the speakerphone functions. The bits are defined as follows:

Bit	Function
[0]	Tx Status 0 (speech level > noise)
[1]	Tx Status 1 (speech level > noise + threshold)
[2]	Tx Status 2 (speech level > noise + threshold ± hysteresis)
[3]	Rx Status 0 (speech level > noise)
[4]	Rx Status 1 (speech level > noise + threshold)
[5]	Rx Status 2 (speech level > noise + threshold ± hysteresis)
[7:6]	Unused

Bits 0 and 3 indicate that the speech filter output is greater than the noise filter output when set to binary 1. This is an indication of detected speech as the speech filter responds to changes in input much faster than the noise filter.

Bits 1 and 4 indicate that the speech filter output is greater than the noise filter output plus a programmable threshold value when set to binary 1. This is an alternative indication of speech where small relative amplitude changes can be ignored. It provides better noise immunity of the speech output.

Bits 2 and 5 are set to binary 1 when an increasing speech filter output exceeds the noise level by the threshold plus the programmable hysteresis level. They are set to binary 0 when a decreasing speech filter output falls below the threshold less the hysteresis level. This ensures that rapid change of status does not occur for marginal speech signals (when the speech level approaches the noise level).

1.6.2.12.7 Filter Reset Register

Addr = $CD (Write)

A write to this location with the value $01 (lsb = binary 1) will clear and hold clear the 3 voice filter and 2 noise filter registers. The filter registers are released when the reset register is written with $00 (lsb = binary 0). Note that only this function and a chip reset will clear the filter register.

1.6.2.13 Audio Block

Refer to the analogue block diagram (section 1.2.2) for an overview of the Audio/Tone/Codec Block.

The Audio Block contains 3 registers to control the audio path gain and 1 register to control the required routing.

The registers available to control the Audio Path gain and routing functions are:

- Audio Rx Gain and Speakerphone Rx Attenuation Register
- Speaker Output Amplifier Gain Register
- Tone Injection Attenuation and Sidetone Attenuation Register
- Audio Routing Register

1.6.2.13.1 Audio Rx Gain (G1) and Speakerphone Attenuation (G2) Register

Addr = $F7 Reset = $00 (Write/Read)

These two 4 bit gain controls are combined into a single register as follows:

Bits[7:4]	G2 Gain	Bits[3:0]	G1 Gain
0000b	0 dB	0000b	0 dB
0001b	-3 dB	0001b	1.5 dB
0010b	-6 dB	0010b	3.0 dB
0011b	-9 dB	0011b	4.5 dB
0100b	-12 dB	0100b	6.0 dB
0101b	-15 dB	0101b	7.5 dB
0110b	-18 dB	0110b	9.0 dB
0111b	-21 dB	0111b	10.5 dB
1000b	-24 dB	1000b	12.0 dB
1001b	-27 dB	1001b	13.5 dB
1010b	-30 dB	1010b	15.0 dB
1011b	-33 dB	1011b	16.5 dB
1100b	-36 dB	1100b	18.0 dB
1101b	-39 dB	1101b	19.5 dB
1110b	-42 dB	1110b	21.0 dB
1111b	Mute	1111b	22.5 dB

The Audio Rx Gain register (G1) is used to control the second stage of gain required to match the dynamic range of the codec input to the transducer being used. The gain required will vary widely dependent on the configuration (POTS or ISDN phone) and both the type of microphone being used and the distance from the microphone of the voice source (handset, desk speakerphone, conference speakerphone, etc.). The first stage of gain is provided by the input amplifiers and associated external feedback components.

The Rx gain register also enables implementation of a software controlled Automatic Gain Control algorithm in conjunction with the data derived from the speakerphone statistics registers.

The Speakerphone Rx Attenuation register (G2) provides for programmable attenuation of the input voice signal applied to the codec and is used for speakerphone operation. It includes a complete mute function.

1.6.2.13.2 Speaker Output Amplifier Gain Register (G3)

Addr = $F6 Reset = $00 (Write/Read)

The speaker amplifier gain register consists of a 3 bit coarse control and a 4 bit fine control plus a mute function as follows:

Bits[6:4]	$G3_{course}$ Gain	Bits[3:0]	$G3_{fine}$ Gain
000b	+6 dB	0000b	0 dB
001b	0 dB	0001b	-0.5 dB
010b	-6 dB	0010b	-1.0 dB
011b	-12 dB	0011b	-1.5 dB
100b	-18 dB	0100b	-2.0 dB
101b	-24 dB	0101b	-2.5 dB
110b	-30 dB	0110b	-3.0 dB
111b	-36 dB	0111b	-3.5 dB
		1000b	-4.0 dB
		1001b	-4.5 dB
		1010b	-5.0 dB
		1011b	-5.5 dB
		1100b	Mute
		1101b	Mute
		1110b	Mute
		1111b	Mute

Bit 7 is unused and should be set to binary 0.

The total gain is the addition in dBs of the $G3_{course}$ and the $G3_{fine}$ settings. The binary code 01111111b may be used to completely mute the loudspeaker output.

The Speaker Output Amplifier Gain register adjusts the power output from the speaker amplifier. It can be used as a volume control and as a means of attenuating the speaker output for speakerphone operation. For POTS configurations, the speaker output is intended for use as the ring input to a SLIC.

1.6.2.13.3 Tone Injection Attenuation (G4) and Sidetone Attenuation (G5) Register

Addr = $F8 Reset = $00 (Write/Read)

These two 4 bit gain controls are combined into a single register as follows:

Bits[7:4]	G5 Gain	Bits[3:0]	G4 Gain
0000b	-6 dB	0000b	0 dB
0001b	-8 dB	0001b	-3 dB
0010b	-10 dB	0010b	-6 dB
0011b	-12 dB	0011b	-9 dB
0100b	-14 dB	0100b	-12 dB
0101b	-16 dB	0101b	-15 dB
0110b	-18 dB	0110b	-18 dB
0111b	-20 dB	0111b	-21 dB
1000b	-22 dB	1000b	-24 dB
1001b	-24 dB	1001b	-27 dB
1010b	-26 dB	1010b	-30 dB
1011b	-28 dB	1011b	-33 dB
1100b	-30 dB	1100b	-36 dB
1101b	-32 dB	1101b	-39 dB
1110b	-34 dB	1110b	-42 dB
1111b	-36 dB	1111b	Mute

The Tone Injection Attenuation register (G4) controls the relative amplitude of the call progress and DTMF comfort tones injected into the earpiece/speaker outputs. It includes a complete mute function.

The Sidetone Attenuation register (G5) allows a programmable level of voice Rx data to be injected into the earpiece amplifier path. This emulates the monitor function intrinsic in a POTS system. If the sidetone function is not required (i.e. POTS configuration), the sidetone amplifier should be disabled (see section 1.6.2.11.2).

1.6.2.13.4 Audio Routing Register

Addr = $F9 Reset = $00 (Write/Read)

The Audio Routing register controls the switch functions S1 to S8. The bits are defined in the following table:

Bit	Function
[0]	S1 - Microphone Input 1 Select
[1]	S2 - Rx Codec to Earpiece Output
[2]	S3 - Tone to Earpiece Output
[3]	S4 - Rx Codec to Loudspeaker Output
[4]	S5 - Tone to Loudspeaker Output
[5]	S6 - Ring output to Loudspeaker Output
[6]	S7 - Rx Codec to DTMF Decoder
[7]	S8 - Tone (DTMF) to Tx Codec

Only 1 microphone input at a time may be active. Microphone input RX2 is selected when bit 0 is set to binary 1 and RX1 selected when set to binary 0.

The receive codec output is routed to the earpiece summing amplifier, TX1, when bit 1 is set to binary 1.

The tone output is routed to the earpiece summing amplifier, TX1, when bit 2 is set to binary 1. The relative amplitude of codec and tone signals can be adjusted with G4.

The receive codec output is routed to the loudspeaker summing amplifier, TX2, when bit 3 is set to binary 1.

The tone output is routed to the loudspeaker summing amplifier, TX2, when bit 4 is set to binary 1. The relative amplitude of codec and tone signals can be adjusted with G4.

The ring generator output is routed to the loudspeaker summing amplifier, TX2, when bit 5 is set to binary 1. This function should only be used for POTS configurations, the ring output frequency and waveform being programmed via the Tone/Codec Control register and the Tone Data register.

The input to the DTMF decoder is routed from the receive codec output when bit 6 is set to binary 1 and from the selected microphone input when set to binary 0. In POTS configuration the DTMF input should be routed from the microphone input (SLIC/Hybrid output in POTS mode) to allow detection of DTMF dialling information from the POTS phone. In ISDN phone applications the DTMF decoder may be routed from the receive codec output to allow implementation of remote control functions using in band DTMF signalling.

The input to the transmit codec is switched to the tone generator when bit 7 is set to binary 1. This allows the ISDN phone to transmit in band DTMF tones for remote access systems (menuing systems, answer-phone access etc.).

1.6.2.14 Tone/Codec Block

Refer to the analogue block diagram (section 1.2.2) for an overview of the Audio/Tone/Codec Block.

The Tone/Codec Block contains the following functions:

- Tone generation (call progress and DTMF)
- PCM Codec
- Ring Tone Generation
- SPM Generation
- FSK UART for caller ID emulation
- DTMF decoder

The registers available to control the Tone functions are:

- Control Register
- Mode Register
- FSK Transmit Data
- Tone Data Register
- DTMF Receive Data
- Status and Mask Registers

1.6.2.14.1 Tone/Codec Control Register

Addr = $F0 Reset = $00 (Write/Read)

The Control Register in the Tone/Codec block controls the codec enable, the companding law, and the ring waveform select. The bits are defined according to the following table:

Bit	Function
[0]	Select Bell FSK Mode
[1]	Select Asynchronous FSK Mode
[2]	Select SPM Frequency
[4:3]	Ring Waveform Select
[5]	Codec Companding Law
[7:6]	Tone Field Select

The FSK standard is selected with bit 0. Bell 202 mode is selected (1200 bps, mark = 1200Hz, space = 2200Hz) when set to binary 1. V.23 mode is selected (1200 bps, mark = 1300Hz, space = 2100Hz) when set to binary 0.

Synchronous or Asynchronous mode of FSK operation is set with bit 1. Asynchronous mode is selected when set to binary 1, synchronous mode when set to binary 0. In asynchronous mode the 8 bits from the FSK transmit data register will be transmitted as asynchronous data characters at 1200 bps according to the following format and shown in Figure 6:

One Start bit (Space)
Eight Data bits (D0-D7) with the lsb (D0) transmitted first
One Stop bit (Mark)

In synchronous mode, shown in Figure 7, the data bits are transmitted with no start or stop bits. The FSK UART status is indicated in bits 0 (FSK UART data underflow) and bit 1 (FSK UART buffer empty) of the Tone Status Register. Data for transmission should be loaded when the buffer empty status is asserted. This status bit indicates when the data in the FSK Transmit Data register is transferred to the UART for transmission and the data register can be safely reloaded. Reloading must occur within approximately 10 bit periods (8.3mS) for asynchronous mode and 8 bit periods (6.7mS) for synchronous mode if an underflow is to be avoided. If the UART runs out of data, the data underflow status is asserted and the UART will transmit continuous binary 1's in asynchronous mode or retransmit the last data in synchronous mode until new data is loaded. FSK transmission is initiated with the 'Tone Enable' register (see section 1.6.2.11.3).

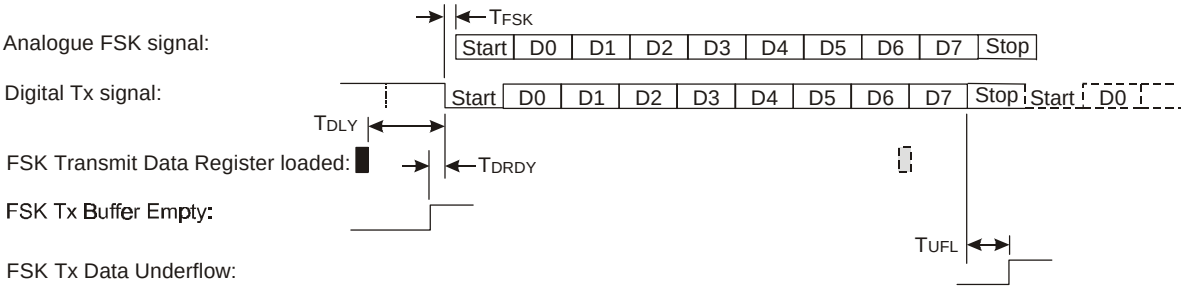


Figure 6. Asynchronous FSK UART Operation

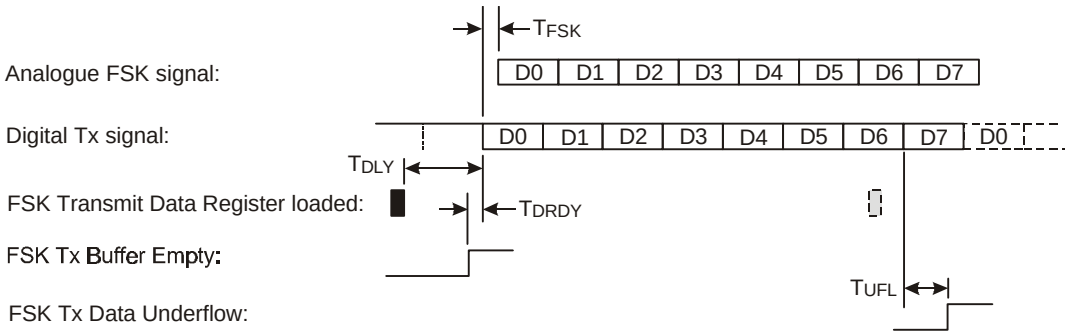


Figure 7. Synchronous FSK UART Operation

The SPM frequency is set with bit 2 of the Control Register. A binary 1 selects 16kHz and a binary 0 selects 12kHz. The SPM tone is turned on and off with the Tone Enable Register (see section 1.6.2.11.3). The SPM tone has a rise and fall time each of approximately 4ms. It rises from the bias level to 0dBm in 16 steps of 2dB magnitude, and falls from 0dBm to bias level in 16 steps of 2dB magnitude.

The RING signal is a square, trapezoidal or sinusoidal wave that can be routed to the speaker output through the variable gain of G3. The square and trapezoidal waves are approximately twice the amplitude of the sinusoidal wave and the gain of the tone injection attenuator (see section 1.6.2.13.3) must be adjusted accordingly. The trapezoidal ringing waveform has a crest factor (CF) of 1.35. The ring frequency is set by selecting tone field 0 (bits 6 and 7) and writing the required tone data, in bit field 3 to 0, to the Tone Data Register (see section 1.6.2.14.3).

The ring waveform is selected by bits 4 and 3 according to the following table:

Code	Ring Waveform
00b	Square Wave
01b	Trapezoidal
10b	Sinusoidal
11b	Unused

Bit 5 when set to binary 1 selects µ-law companding. When set to binary 0, A-law companding is selected.

The tone selection is accomplished by selecting 1 of 256 tone pair combinations (using the Tone Data Register, section 1.6.2.14.3) from 1 of 4 tone fields, giving a choice of 1024 pre-programmed tone combinations. The tone field is selected by bits 6 and 7 according to the following table:

Code	Tone Field
00b	Tone Field 0
01b	Tone Field 1
10b	Tone Field 2
11b	Tone Field 3

1.6.2.14.2 FSK Transmit Data

Addr = $F1 Reset = $00 (Write/Read)

The FSK Transmit Data Register should be written with the required 8 bit FSK data when the FSK buffer empty status is set (see section 1.6.2.14.5). The data will then be transmitted lsb first according to the format set in the Tone/Codec Control Register defined in section 1.6.2.14.1.

1.6.2.14.3 Tone Data Register

Addr = $F2 Reset = $00 (Write/Read)

The Tone Data Register selects the tone pairs, single tone or ring frequency required from 1 of 4 tone fields. The selection codes for each of the tone fields are defined in the following 4 tables:

Tone Field 0, Tone/Codec Control Register [7:6] = 00b									
TX TONES Register Bits 4-7				Frequency	TX TONES Register Bits 0-3				Frequency
D7	D6	D5	D4	(Hz)	D3	D2	D1	D0	(Hz)
0	0	0	0	0 = OFF	0	0	0	0	0 = OFF
0	0	0	1	252.4	0	0	0	1	* 17.1
0	0	1	0	268.7	0	0	1	0	* 20.5
0	0	1	1	285.3	0	0	1	1	* 24.9
0	1	0	0	315.5	0	1	0	0	* 34.1
0	1	0	1	330.5	0	1	0	1	* 41.0
0	1	1	0	375.2	0	1	1	0	* 51.2
0	1	1	1	404.3	0	1	1	1	-
1	0	0	0	468.0	1	0	0	0	262.9
1	0	0	1	495.8	1	0	0	1	293.6
1	0	1	0	520.6	1	0	1	0	348.2
1	0	1	1	548.0	1	0	1	1	392.6
1	1	0	0	562.8	1	1	0	0	1600
1	1	0	1	578.4	1	1	0	1	1633
1	1	1	0	595.0	1	1	1	0	1827
1	1	1	1	612.5	1	1	1	1	587.2

NOTE: * These outputs are utilised for the ring frequency only.

Tone Field 1, Tone/Codec Control Register [7:6] = 01b									
TX TONES Register Bits 4-7				Frequency	TX TONES Register Bits 0-3				Frequency
D7	D6	D5	D4	(Hz)	D3	D2	D1	D0	(Hz)
0	0	0	0	0 = OFF	0	0	0	0	0 = OFF
0	0	0	1	120	0	0	0	1	330
0	0	1	0	150	0	0	1	0	416
0	0	1	1	154	0	0	1	1	420
0	1	0	0	250	0	1	0	0	425
0	1	0	1	300	0	1	0	1	433
0	1	1	0	350	0	1	1	0	440
0	1	1	1	360	0	1	1	1	450
1	0	0	0	367	1	0	0	0	460
1	0	0	1	375	1	0	0	1	480
1	0	1	0	380	1	0	1	0	500
1	0	1	1	383	1	0	1	1	600
1	1	0	0	400	1	1	0	0	620
1	1	0	1	450	1	1	0	1	720
1	1	1	0	475	1	1	1	0	930
1	1	1	1	480	1	1	1	1	-

Tone Field 2, Tone/Codec Control Register [7:6] = 10b									
TX TONES Register Bits 4-7				Frequency	TX TONES Register Bits 0-3				Frequency
D7	D6	D5	D4	(Hz)	D3	D2	D1	D0	(Hz)
0	0	0	0	0 = OFF	0	0	0	0	0 = OFF
0	0	0	1	700	0	0	0	1	700
0	0	1	0	900	0	0	1	0	900
0	0	1	1	1100	0	0	1	1	1100
0	1	0	0	1300	0	1	0	0	1300
0	1	0	1	1500	0	1	0	1	1500
0	1	1	0	1700	0	1	1	0	1700
0	1	1	1	-	0	1	1	1	-
1	0	0	0	950	1	0	0	0	2100
1	0	0	1	1400	1	0	0	1	2225
1	0	1	0	1800	1	0	1	0	-
1	0	1	1	2130	1	0	1	1	2750
1	1	0	0	697	1	1	0	0	1209
1	1	0	1	770	1	1	0	1	1336
1	1	1	0	852	1	1	1	0	1477
1	1	1	1	941	1	1	1	1	1633

Tone Field 3, Tone/Codec Control Register [7:6] = 11b									
TX TONES Register Bits 4-7				Frequency	TX TONES Register Bits 0-3				Frequency
D7	D6	D5	D4	(Hz)	D3	D2	D1	D0	(Hz)
0	0	0	0	0 = OFF	0	0	0	0	0 = OFF
0	0	0	1	540	0	0	0	1	540
0	0	1	0	660	0	0	1	0	660
0	0	1	1	780	0	0	1	1	780
0	1	0	0	900	0	1	0	0	900
0	1	0	1	1020	0	1	0	1	1020
0	1	1	0	1140	0	1	1	0	1140
0	1	1	1	-	0	1	1	1	-
1	0	0	0	1380	1	0	0	0	1380
1	0	0	1	1500	1	0	0	1	1500
1	0	1	0	1620	1	0	1	0	1620
1	0	1	1	1740	1	0	1	1	1740
1	1	0	0	1860	1	1	0	0	1860
1	1	0	1	1980	1	1	0	1	1980
1	1	1	0	-	1	1	1	0	-
1	1	1	1	-	1	1	1	1	-

1.6.2.14.4 DTMF Receive Data

Addr = $F5 (Read Only)

The DTMF Receive Data Register will contain new decoded DTMF data when the DTMF detected status is set (see 1.6.2.14.5). The DTMF state change status will be set whenever a change in state of the DTMF decoder is detected. This can occur when a DTMF tone is detected and also when the DTMF tone ceases. The DTMF detected status will indicate which.

The 4 bit DTMF receive data is encoded as follows:

DTMF Receive Data Register Bits 0 - 3				DTMF Tone Pairs		
Bit 3 (D3)	Bit 2 (D2)	Bit 1 (D1)	Bit 0 (D0)	Lower Frequency (Hz)	Upper Frequency (Hz)	Keypad Legend
0	0	0	0	941	1633	D
0	0	0	1	697	1209	1
0	0	1	0	697	1336	2
0	0	1	1	697	1477	3
0	1	0	0	770	1209	4
0	1	0	1	770	1336	5
0	1	1	0	770	1477	6
0	1	1	1	852	1209	7
1	0	0	0	852	1336	8
1	0	0	1	852	1477	9
1	0	1	0	941	1336	0
1	0	1	1	941	1209	*
1	1	0	0	941	1477	#
1	1	0	1	697	1633	A
1	1	1	0	770	1633	B
1	1	1	1	852	1633	C

1.6.2.14.5 Tone Status/Mask Registers

Status	Addr = $F4	Reset = $00	(Read Only)
Mask	Addr = $F3	Reset = $00	(Write/Read)

The Tone Status Register combined with its associated Mask Register generates a level-2 interrupt request that forms bit 5 of the top level-1 Status Register.

The tone Status Register bits are defined according to the following table:

Bit	Function
[3:0]	Unused
[4]	DTMF Rx Tone Detected
[5]	DTMF Rx State Change
[6]	FSK Tx Buffer Empty
[7]	FSK Tx Data Underflow

Bit 4 will be set to binary 1 when an acceptable quality DTMF tone has been detected. It will be reset to binary 0 when the tone ceases.

Bit 5 will be set to binary 1 whenever the DTMF state changes (i.e. Bit 4 changes from 0 to 1 or from 1 to 0). This can be used to generate an interrupt to indicate the beginning or the end of a detected tone. It is cleared to binary 0 whenever the Status Register is read.

Bit 6, when set to binary 1, indicates that the FSK transmit buffer is ready to accept another data byte.

Bit 7 will be set to binary 1 if the FSK Tx buffer is not refreshed before new data is required for transmission.

The Mask Register bits, when set to binary 0, will prevent a binary 1 in the corresponding Status Register bit position from generating a level-2 interrupt request (see section 1.6.1) to the level-1 Status Register.

Bits 7, 6 and 4 are only cleared to binary 0 when the relevant status changes (i.e. a write to the FSK buffer clears bit 6 and 7, cessation of a DTMF tone clears bit 4).

1.6.3 Register Address Definition Summary

Address	Name	Block
$00	D-channel Rx Mode Register	HDLC D RX
$01	D-channel Rx Address Match Register A1	HDLC D RX
$02	D-channel Rx Address Match Register A2	HDLC D RX
$03	D-channel Rx Address Match Register A3	HDLC D RX
$04	D-channel Rx Address Match Register A4	HDLC D RX
$05	D-channel Rx Address Match Register B1	HDLC D RX
$06	D-channel Rx Address Match Register B2	HDLC D RX
$07	D-channel Rx Address Match Register B3	HDLC D RX
$08	D-channel Rx Address Match Register B4	HDLC D RX
$09	D-channel Rx Match Request Register	HDLC D RX
$0A	Reserved	HDLC D RX
$0B	D-channel Layer-2 HDLC Status Register	HDLC D RX
$0C	D-channel Layer-3 HDLC Status Register	HDLC D RX
$0D	D-channel Layer-2 HDLC Status Mask Register	HDLC D RX
$0E	D-channel Layer-3 HDLC Status Mask Register	HDLC D RX
$0F	D-channel Rx Octet Counter	HDLC D RX
$10	D-channel Tx Mode Register	HDLC D TX
$11	Reserved	HDLC D TX
$12-$13	Unused	
$14	D-channel Tx Address Low Register	HDLC D TX
$15	D-channel Tx Address High Register	HDLC D TX
$16	D-channel Tx Frame Count Register	HDLC D TX
$17	D-channel Tx Octet Count Register	HDLC D TX
$18-$1F	Unused	
$20	B1-channel Rx Mode Register	HDLC B1 RX
$21	B1-channel Rx Address Match Register A1	HDLC B1 RX
$22	B1-channel Rx Address Match Register A2	HDLC B1 RX
$23	B1-channel Rx Address Match Register A3	HDLC B1 RX
$24	B1-channel Rx Address Match Register A4	HDLC B1 RX
$25	B1-channel Rx Address Match Register B1	HDLC B1 RX
$26	B1-channel Rx Address Match Register B2	HDLC B1 RX
$27	B1-channel Rx Address Match Register B3	HDLC B1 RX
$28	B1-channel Rx Address Match Register B4	HDLC B1 RX
$29	B1-channel Rx Match Request Register	HDLC B1 RX
$2A	Reserved	HDLC B1 RX
$2B	B1-channel Layer-2 HDLC Status Register	HDLC B1 RX
$2C	B1-channel Layer-3 HDLC Status Register	HDLC B1 RX
$2D	B1-channel Layer-2 HDLC Status Mask Register	HDLC B1 RX
$2E	B1-channel Layer-3 HDLC Status Mask Register	HDLC B1 RX
$2F	B1-channel Rx Octet Counter	HDLC B1 RX
$30	B1-channel Tx Mode Register	HDLC B1 TX
$31	Reserved	HDLC B1 TX
$32-$33	Unused	
$34	B1-channel Tx Address Low Register	HDLC B1 TX
$35	B1-channel Tx Address High Register	HDLC B1 TX
$36	B1-channel Tx Frame Count Register	HDLC B1 TX
$37	B1-channel Tx Octet Count Register	HDLC B1 TX
$38-$3F	Unused	
$40	B2-channel Rx Mode Register	HDLC B2 RX
$41	B2-channel Rx Address Match Register A1	HDLC B2 RX
$42	B2-channel Rx Address Match Register A2	HDLC B2 RX

Address	Name	Block
$43	B2-channel Rx Address Match Register A3	HDLC B2 RX
$44	B2-channel Rx Address Match Register A4	HDLC B2 RX
$45	B2-channel Rx Address Match Register B1	HDLC B2 RX
$46	B2-channel Rx Address Match Register B2	HDLC B2 RX
$47	B2-channel Rx Address Match Register B3	HDLC B2 RX
$48	B2-channel Rx Address Match Register B4	HDLC B2 RX
$49	B2-channel Rx Match Request Register	HDLC B2 RX
$4A	Reserved	HDLC B2 RX
$4B	B2-channel Layer-2 HDLC Status Register	HDLC B2 RX
$4C	B2-channel Layer-3 HDLC Status Register	HDLC B2 RX
$4D	B2-channel Layer-2 HDLC Status Mask Register	HDLC B2 RX
$4E	B2-channel Layer-3 HDLC Status Mask Register	HDLC B2 RX
$4F	B2-channel Rx Octet Counter	HDLC B2 RX
$50	B2-channel Tx Mode Register	HDLC B2 TX
$51	Reserved	HDLC B2 TX
$52-$53	Unused	
$54	B2-channel Tx Address Low Register	HDLC B2 TX
$55	B2-channel Tx Address High Register	HDLC B2 TX
$56	B2-channel Tx Frame Count Register	HDLC B2 TX
$57	B2-channel Tx Octet Count Register	HDLC B2 TX
$58-$5F	Unused	
$60	Fifo D Tx Base Address	HDLC FIFO
$61	Fifo D Rx Base Address	HDLC FIFO
$62	Fifo B1 Tx Base Address	HDLC FIFO
$63	Fifo B1 Rx Base Address	HDLC FIFO
$64	Fifo B2 Tx Base Address	HDLC FIFO
$65	Fifo B2 Rx Base Address	HDLC FIFO
$66-$67	Unused	
$68	Fifo D Tx Channel Write Port	HDLC FIFO
$69	Fifo B1 Tx Channel Write Port	HDLC FIFO
$6A	Fifo B2 Tx Channel Write Port	HDLC FIFO
$6B	Fifo D Rx Channel Read Port	HDLC FIFO
$6C	Fifo B1 Rx Channel Read Port	HDLC FIFO
$6D	Fifo B2 Rx Channel Read Port	HDLC FIFO
$6E	Fifo Clear Register	HDLC FIFO
$6F	Reserved	HDLC FIFO
$70	D Tx Status Register	HDLC FIFO
$71	D Rx Status Register	HDLC FIFO
$72	D Tx Status Mask Register	HDLC FIFO
$73	D Rx Status Mask Register	HDLC FIFO
$74	B1 Tx Status Register	HDLC FIFO
$75	B1 Rx Status Register	HDLC FIFO
$76	B1 Tx Status Mask Register	HDLC FIFO
$77	B1 Rx Status Mask Register	HDLC FIFO
$78	B2 Tx Status Register	HDLC FIFO
$79	B2 Rx Status Register	HDLC FIFO
$7A	B2 Tx Status Mask Register	HDLC FIFO
$7B	B2 Rx Status Mask Register	HDLC FIFO
$7C-$7D	Reserved	HDLC FIFO
$7E-$7F	Unused	
$80	ST Control Register	ST INTERFACE
$81	Unused	ST INTERFACE
$82	ST Set-Up Register	ST INTERFACE

Address	Name	Block
$83	ST Status Register	ST INTERFACE
$84	Interrupt Mask Register	ST INTERFACE
$85	ST Interrupt Register	ST INTERFACE
$86	Reserved	ST INTERFACE
$87	ST State Machine Register	ST INTERFACE
$88	State Machine Mask Register	ST INTERFACE
$89	Multi-Frame S Register	ST INTERFACE
$8A	Multi-Frame Q Register	ST INTERFACE
$8B	Multi-Frame Status Register	ST INTERFACE
$8C	Multi-Frame Status Mask Register	ST INTERFACE
$8D	Multi-Frame S Bit Counter	ST INTERFACE
$8E	Reserved	ST INTERFACE
$8F	Unused	
$90	IOM Control Register	IOM INTERFACE
$91	IOM Monitor Channel Tx Register	IOM INTERFACE
$92	IOM Monitor Channel Control Register	IOM INTERFACE
$93	IOM Monitor Channel Rx Register	IOM INTERFACE
$94	IOM Status Register	IOM INTERFACE
$95	IOM Real Time Status	IOM INTERFACE
$96	IOM Status Mask Register	IOM INTERFACE
$97	IOM CI0 Transmit Register	IOM INTERFACE
$98	IOM CI1 Transmit Register	IOM INTERFACE
$99	IOM CI0 Receive Register	IOM INTERFACE
$9A	IOM CI1 Receive Register	IOM INTERFACE
$9B-$9D	Reserved	IOM INTERFACE
$9E-$9F	Unused	
$A0-$A1	Reserved	DPLL
$A2-$AF	Unused	
$B0	B Route Control 1	DATA ROUTING
$B1	B Route Control 2	DATA ROUTING
$B2	B Route Control 3	DATA ROUTING
$B3	B Route Control 4	DATA ROUTING
$B4	D Route Control	DATA ROUTING
$B5	Reserved	DATA ROUTING
$B6-$BF	Unused	
$C0	Speakerphone Mode Register	SPEAKER-PHONE
$C1	Speakerphone Transmit Channel Threshold Register	SPEAKER-PHONE
$C2	Speakerphone Receive Channel Threshold Register	SPEAKER-PHONE
$C3	Speakerphone Transmit Channel Hysteresis Register	SPEAKER-PHONE
$C4	Speakerphone Receive Channel Hysteresis Register	SPEAKER-PHONE
$C5	Speakerphone Transmit Channel Speech Filter Output	SPEAKER-PHONE
$C6	Speakerphone Receive Channel Speech Filter Output	SPEAKER-PHONE
$C7	Speakerphone Attenuated Channel Speech Filter Output	SPEAKER-PHONE
$C8	Speakerphone Transmit Channel Noise Filter Output	SPEAKER-PHONE
$C9	Speakerphone Receive Channel Noise Filter Output	SPEAKER-PHONE
$CA	Speakerphone Interrupt Mask Register	SPEAKER-PHONE
$CB	Speakerphone Interrupt Status Register	SPEAKER-PHONE
$CC	Speakerphone Status Register	SPEAKER-PHONE
$CD	Speakerphone Filter Reset	SPEAKER-PHONE
$CE-$CF	Unused	
$D0	Clock Enable Register	CLOCK/POWER
$D1	Clock /Power Status Mask Register	CLOCK/POWER
$D2	Clock /Power Status Register	CLOCK/POWER

Address	Name	Block
$D3-$D4	Reserved	CLOCK/POWER
$D5	Audio Enable Register	CLOCK/POWER
$D6	Tone Enable Register	CLOCK/POWER
$D7	Clock Control Register	CLOCK/POWER
$D8-$DF	Unused	
$E0	Top Level Status Mask Register	TOP
$E1	Top Level Status Register	TOP
$E2-$EF	Unused	
$F0	Tone/Codec Control Register	TONE-GEN
$F1	FSK Transmit Data	TONE-GEN
$F2	Tone Data Register	TONE-GEN
$F3	Tone Status Mask Register	TONE-GEN
$F4	Tone Status Register	TONE-GEN
$F5	DTMF Receive Data	TONE-GEN
$F6	Speaker Output Amplifier Gain Register	AUDIO BLOCK
$F7	Audio Rx Gain and Speakerphone Attenuation Register	AUDIO BLOCK
$F8	Tone Injection Attenuation and Sidetone Attenuation Register	AUDIO BLOCK
$F9	Audio Routing Register	AUDIO BLOCK
$FA-$FD	Reserved	AUDIO BLOCK
$FE-$FF	Unused	

1.7 Application Notes

1.7.1 Example CMX635 Configurations

The following sections give a brief summary of potential applications for the CMX635.

1.7.1.1 Dual Short Loop POTS System

The following diagram shows how a dual POTS system might be implemented. The CMX635 provides all of the required functions to emulate the exchange in a conventional POTS system. The SLIC provides the 4 to 2 wire conversion, ring voltage amplifier, the off-hook detection and the ring trip detection. A CMX625 provides a second fully functional POTS port, which is programmed, from the CMX635 via the IOM interface.

A power supply/control device is required which will generate the high voltage required by the SLIC (50 - 80 VDC) and the Vdd/Vss supplies required by the CMX635 and processor. In addition, the power controller may be required to extract power from the S/T bus (Power Source 1 or "Phantom Power") or utilise the auxiliary Power Source 2 input. The power controller must also signal impending power loss to the processor to allow controlled shutdown of both the processor and the data link itself (via an exchange of messages). The power supply must therefore be maintained for a defined period after power loss.

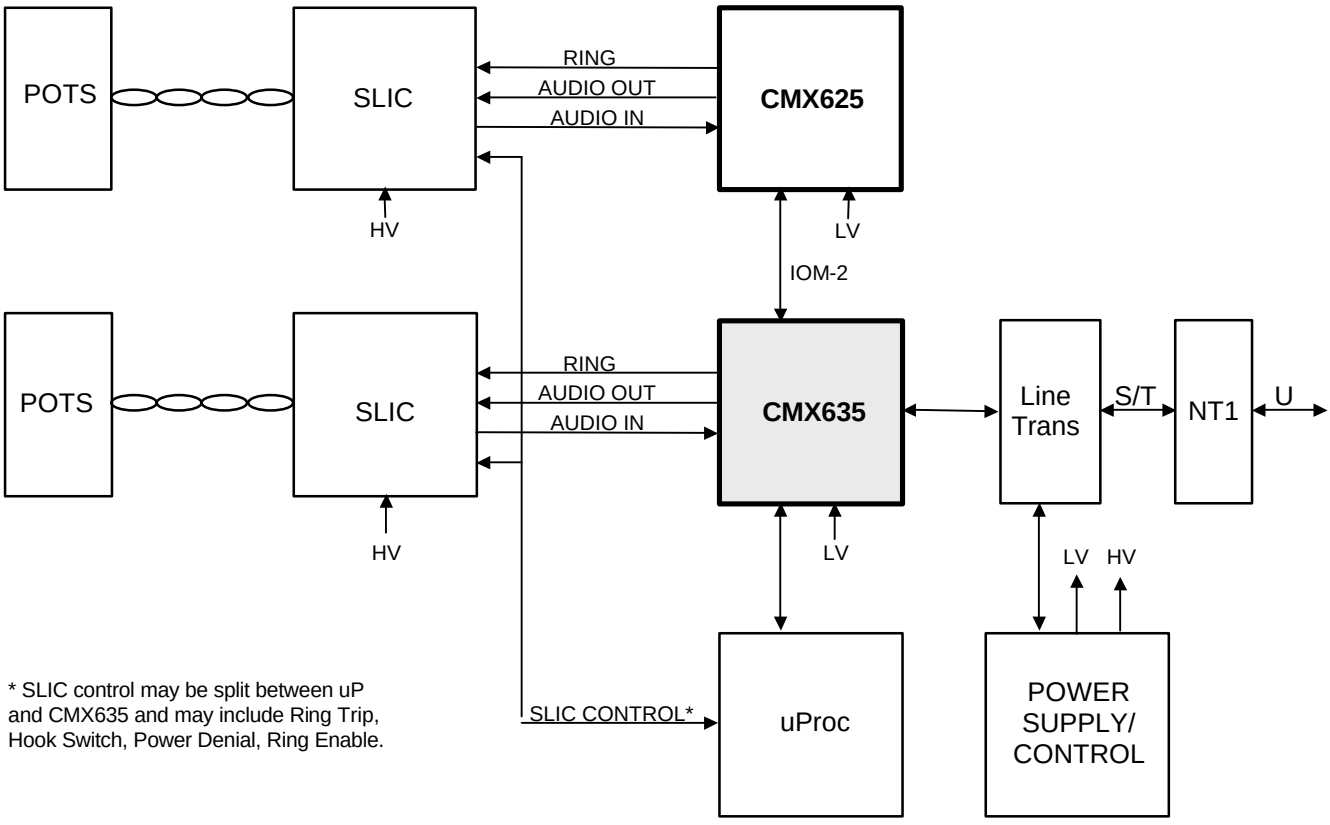


Figure 8. Dual POTS Configuration

1.7.1.2 ISDN Telephone/Feature/Speaker Phone.

In this configuration the transducers are interfaced directly to the CMX635. The processor will control the display and keypad and will programme the required tones and amplitudes. In a speakerphone system the processor may also implement the algorithms necessary to control the attenuation of the transmit and receive voice channels to prevent feedback or "howling". To assist in this task, the CMX635 provides statistics about the amplitude of the voice channels and the background noise.

A data port is shown operating through a UART, which may be a simple RS232 device or a more complex USB driver.

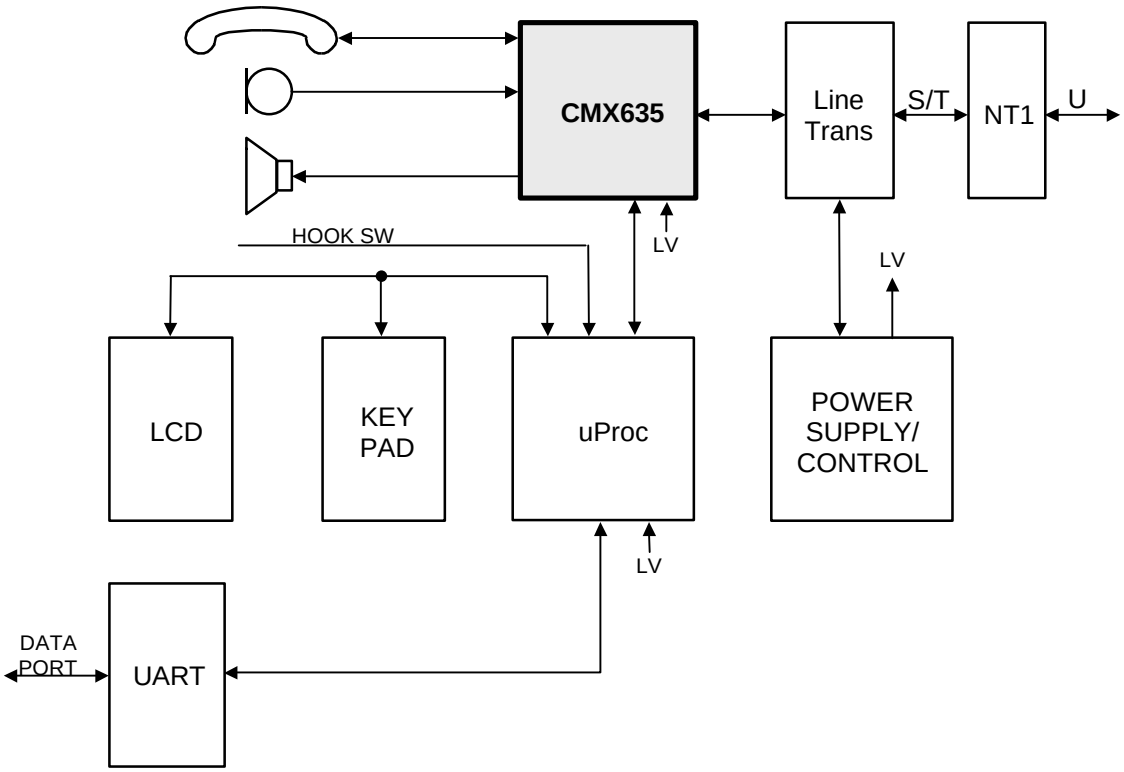


Figure 9. ISDN Telephone Configuration

1.7.1.3 ISDN PC Card (Active Data Adaptor)

The CMX635 is suited for use in an active, or intelligent data adaptor with a local controlling micro-controller hosting the layer-3 ISDN protocol stack and the low-level device drivers for the CMX635 and the data compression algorithms. The CMX635 provides the HDLC layer-1 and partial layer-2 interfaces and also provides a voice channel interface.

Bus interface circuitry is required to interface to the PCI bus and would typically include dual-port RAM, buffering, address control logic etc.

This configuration provides high performance data transfer that is not subject to the data “drop-outs” that can occur with passive data adaptors.

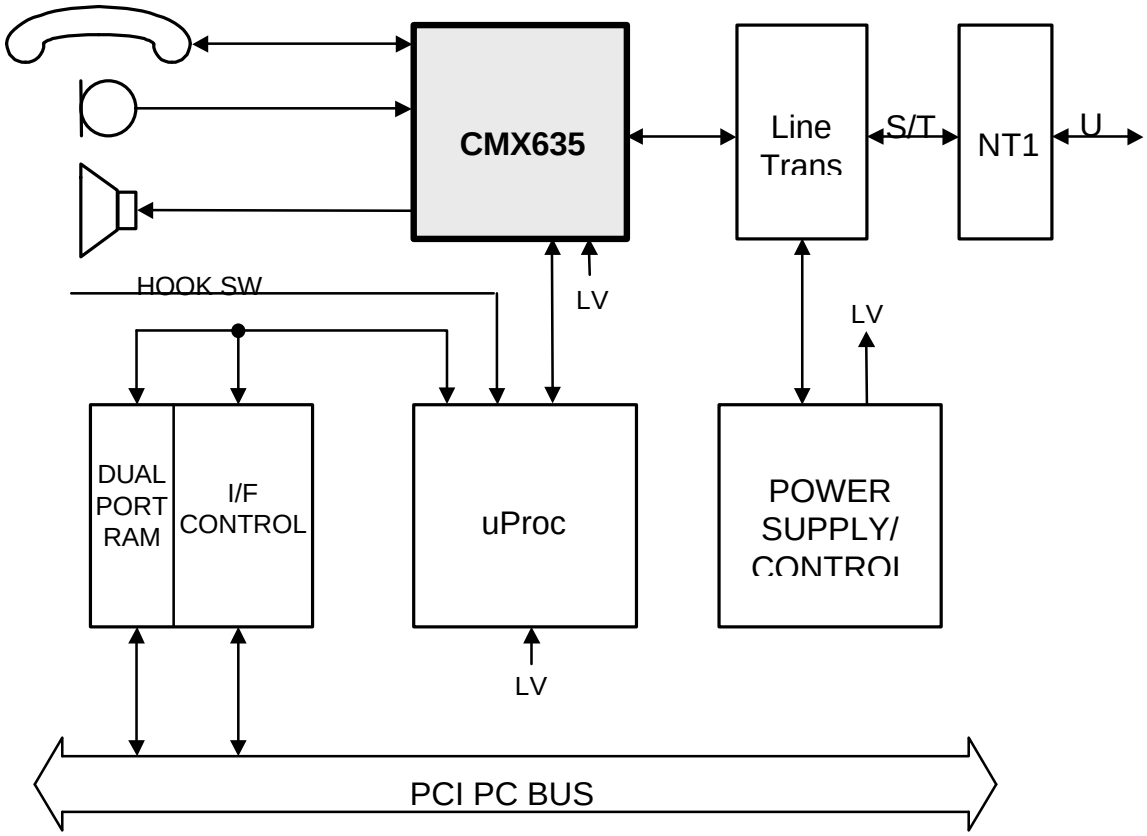


Figure 10. PCI Card Configuration

1.7.1.4 Video Phone

The scheme shown below allows compressed video data to be passed to the CMX635 via the IOM-2 peripheral port. The audio channel is connected to the CMX635 and the digitised data is exported to the audio compressor over the IOM-2 bus. The incoming video is digitised and compressed using a video codec. The compressed audio is routed directly to the video codec where it is combined with the video for transmission over a single B-channel or both B-channels simultaneously. The combined compressed Video/Audio data is re-imported into the CMX635 via the IOM interface for transmission over the ST bus.

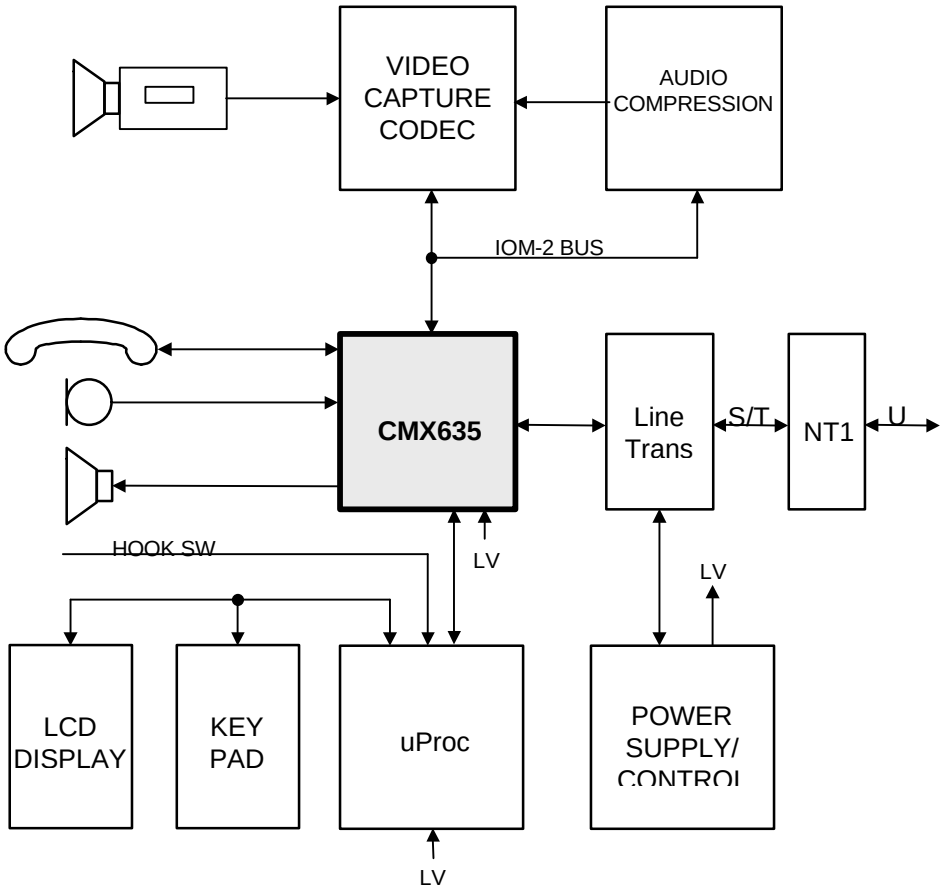


Figure 11. Video Phone Configuration

1.7.1.5 Intelligent NT or NT1Plus

The CMX635 can be used in a cost effective NT1Plus configuration with the addition of a U interface transceiver and a CMX625 connected via the IOM-2 bus. This system provides 2 fully functional POTS lines and an ST bus for digital expansion to any TE configured ISDN equipment.

The local processor contains the layer-3 signalling protocol stack and the CMX635 has the capability to share the D-channel with downstream layer-2 devices.

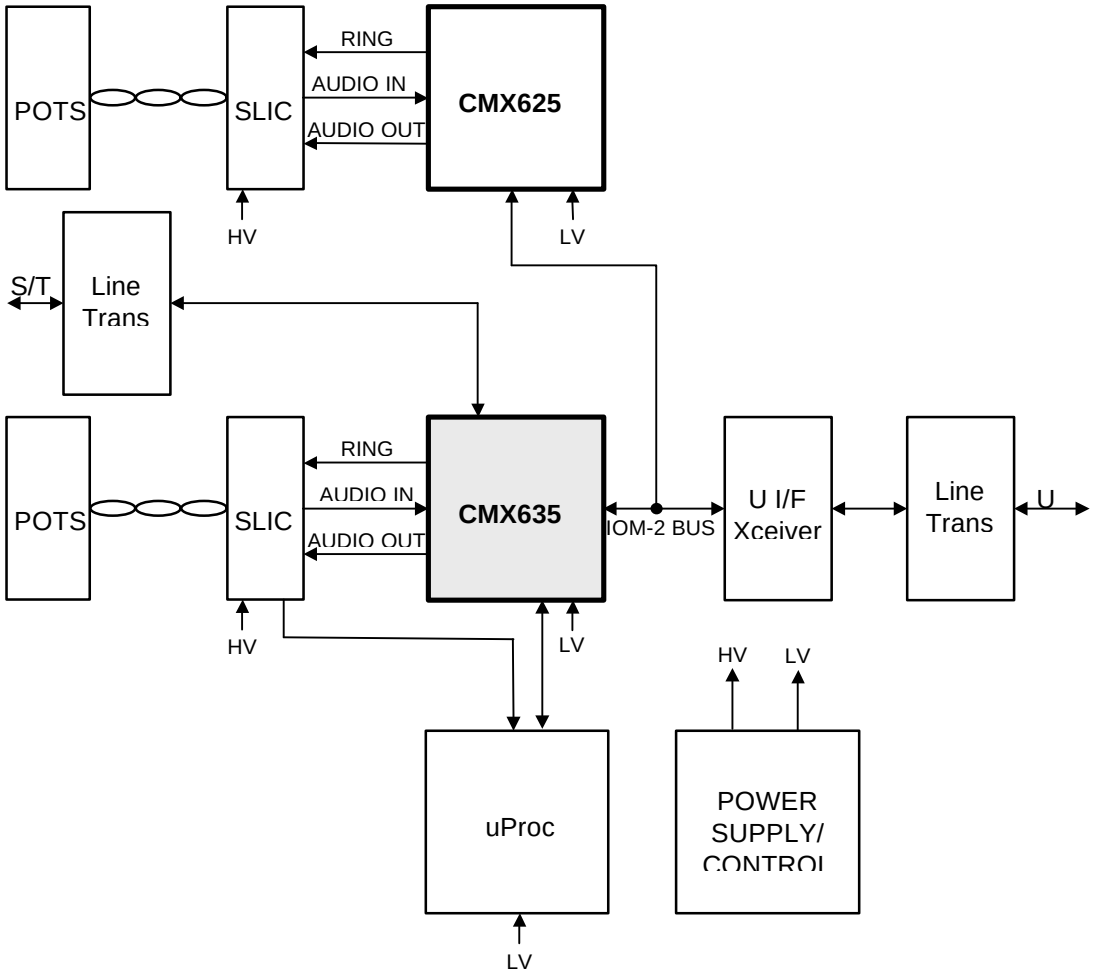


Figure 12. NT1-Plus Configuration

1.7.2 IOM-2 Interface Summary

1.7.2.1 General

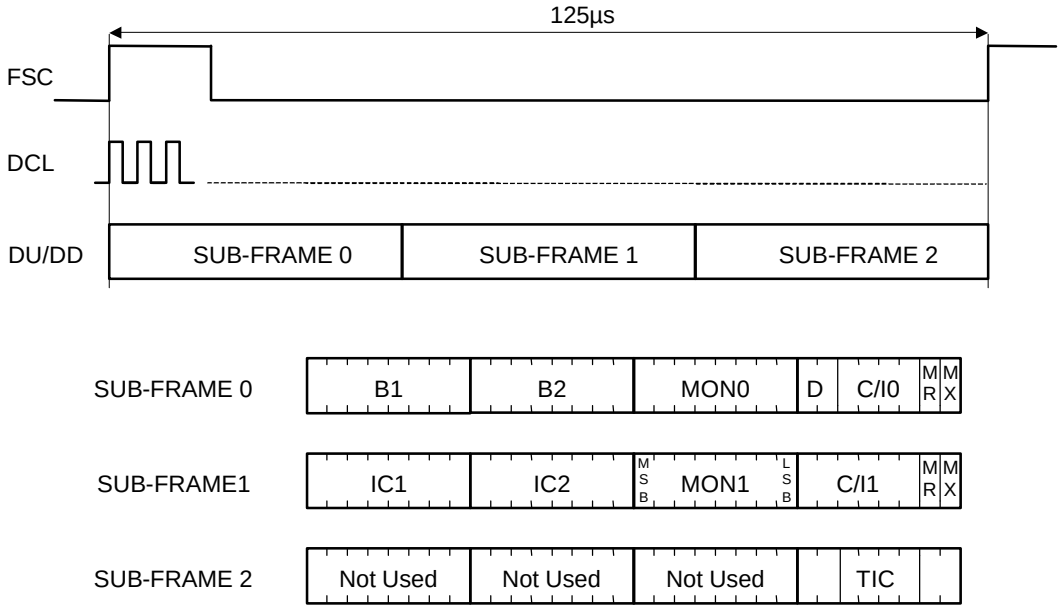
The IOM®-2 (ISDN Oriented Modular revision 2) is an industry standard serial bus for interconnecting telecommunications IC's. The bus is an evolution of the IOM® interface and is also known as the GCI (General Circuit Interface).

The IOM-2 bus provides a symmetrical full duplex communication link, containing user data, control/programming and status channels. There are two basic modes of operation known as Terminal mode (TE mode) and non-Terminal mode (non-TE or Line Card mode). The CMX635 operates in TE mode and the following description refers to TE mode only.

The various channels are time multiplexed over a basic four wire serial interface, namely FSC, DCL, DD and DU. Frames are delimited by an 8kHz Frame Synchronisation Clock (FSC), which is generated by the upstream device. The Data Clock (DCL) clocks data on and off of the data bus (DU and DD) and runs at 1.536MHz, which is twice the bit rate. It is always generated by the upstream device. Data Downstream (DD) receives data from the network. Data Upstream (DU) transmits data to the network. When the bus is deactivated or when data is not being transmitted, DD and DU are held in a high impedance state unless the Active Output feature of the CMX635 is programmed. This allows many downstream IOM devices to be connected to the same DD/DU bus.

1.7.2.2 Frame Structure

The TE mode frame structure consists of 3 sub-frames of 4 bytes each repeated at 8kHz, i.e. 96 bits in 125µs or a data rate of 768kbps. Figure 13 shows the TE mode frame structure.



FSC = 8kHz
DCL = 1.536MHz
DD, DU = 768kbps

Figure 13. Terminal Mode Frame Structure

'Sub-frame 0' is used for passing the 2 ISDN PCM data channels (B1 and B2), the ISDN signalling channel (D) and Layer-1 transceiver control (MON0 and C/I0).

'Sub-frame 1' is used for passing 2 auxiliary PCM Inter-Connect channels (IC1 and IC2), an asynchronous programming channel (MON1) and a status indication channel (C/I1).

'Sub-frame 2' contains the Terminal Integrated Circuit (TIC) bus channel used for arbitrating between multiple layer-2 D-channel controllers connected on the IOM bus.

The 'Monitor' channels, MON0 and MON1, are identical and have two associated pairs of handshake bits, MX and MR (monitor transmit and receive) that control data flow located in the fourth byte of sub-frames 0 and 1. The handshake procedure utilising the MX and MR bits is described in section 1.7.2.3. The MON1 byte is used for programming and controlling devices attached to the IOM-2 interface such as the CMX625, ISDN TA POTS Interface. The MON0 byte is used for configuring other layer-1 devices such a U interface transceiver when the CMX635 is used in NT mode.

MON1 channel contention is avoided by a "speak when spoken to" system whereby the IOM slave devices are given a unique address and only respond when that address is broadcast by the IOM master device. The IOM slave devices cannot initiate MON1 communication directly in a multi-slave application. Each slave must monitor the MON1 channel for its unique address in the first byte before processing the following command. Each slave can therefore only drive the DU MON1 channel when specifically requested to by the master.

The 'D' channel consists of two bits located in the fourth byte of sub-frame 0. They provide a 16kbps D-channel data rate for layer-2 IOM devices.

The 'Command/Indicate' channels, C/I0 and C/I1, provide real time status information between devices connected via the IOM-2 bus. The data in these channels is continuously transmitted, reflecting changes as they occur. The C/I0 channel in sub-frame 0 consists of 4 bits (the other bits being the MX, MR and D-channel) and the C/I1 channel in sub-frame 1 is 6 bits wide (the other bits being the MR and MX). The C/I0 channel is used to communicate layer-1 control primitives and is described in more detail in section 1.7.2.4. The C/I1 channel is shared by all devices on the IOM-2 bus with no mechanism for determining and resolving contention. If multiple slave devices are expected to drive the C/I1 channel then care must be taken to allocate different bits to each device. An example of C/I1 channel usage would be 6 slave devices each allocated one of the 6 C/I1 bits. When a slave requires attention it asserts its own bit, which is detected by the master as a C/I1 value change (generating a processor interrupt). The processor would then initiate MON1 communications with the appropriate slave and service its request. This is an example of one usage, but the C/I1 bits may be used for any real time command/indicate purpose dependent on system design and number of slaves on the IOM-2 bus.

The 'Inter-Chip communication Channels' consists of two 64kbps data channels, IC1 and IC2, and provide additional communications paths between IOM devices. These channels can be used to route intermediate data between devices. An example is a voice scrambler system where the unscrambled data is passed from an IOM Codec to an IOM scrambler in one of the IC channels and the scrambled data is output into a B-channel for transmission by a layer-1 device.

The 'TIC' bus is used for connecting more than one layer-2 device to the D and C/I0 channels in sub-frame 0 and is described in more detail in section 1.7.2.5.

1.7.2.3 Monitor Channel Handshake Protocol

The Monitor channel operates on an event driven basis. While data transfers on the bus take place synchronised to the frame sync, the flow of data is controlled by a handshake procedure using the outgoing MX (monitor transmit) and incoming MR (monitor receive) bits. Data is placed onto the monitor channel and the MX bit is activated. This data will be transmitted repeatedly (once per 8kHz frame) until the transfer is acknowledged (ACK) via the MR bit. The actual data rate is not fixed but is dependent upon the response speed of the transmitter and receiver.

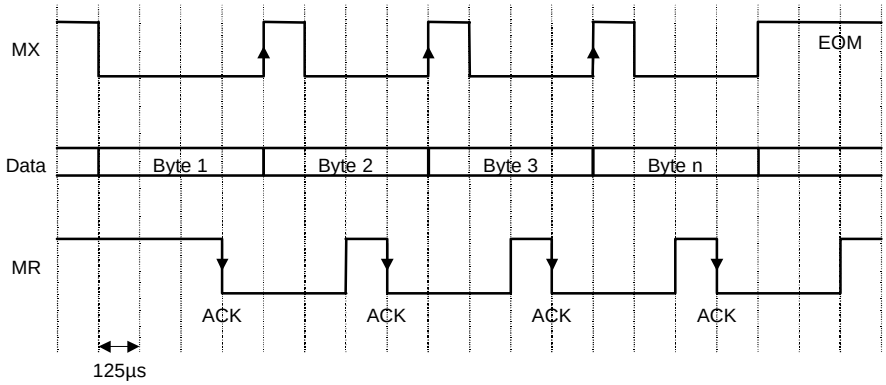
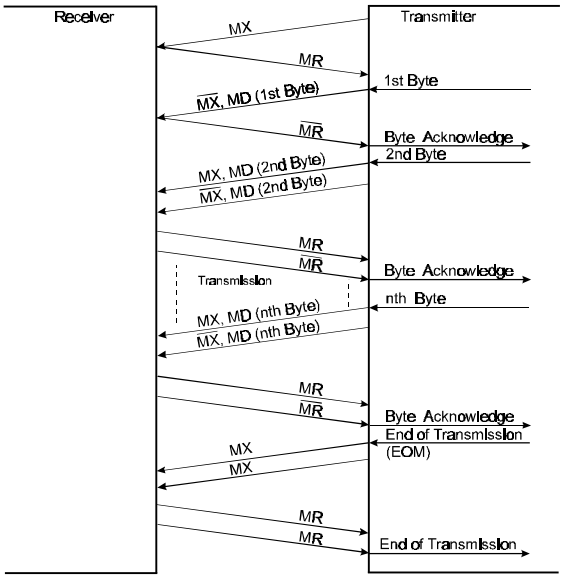


Figure 14. Monitor Handshake Timing (general case)

Figure 14 shows the general case for monitor handshake timing. The first byte of data is placed on the bus and MX is activated (low). MX remains active and the data remains valid until an inactive-to-active transition of MR is received, indicating that the receiver has read the data off of the bus. The next byte is placed on the bus after the inactive-to-active transmission of MR, as early as the next frame (there is no limit to the maximum number of frames). At the time that the second byte is transmitted, MX is returned inactive (high) for one frame (MX inactive for more than one frame indicates an End of Message). In response to MX going active (low), MR will be deactivated (high) for one frame (the MX inactive to MR inactive delay can be any number of frames). This procedure is repeated for each additional byte. The transmitter sends an End of Message (EOM), after the last byte of data has been transmitted, by not reactivating MX after deactivating it.

The receiver can hold off the transmitter by keeping MR active until the receiver is ready for the next byte. The transmitter will not start the next transmission cycle until MR goes inactive. The transmitter is able to abort a transmission by holding MX inactive (high) for two or more frames.

Figure 15 shows the monitor channel handshake procedure.



MX = Monitor Transmit Bit, active low.
MR = Monitor Receive Bit, active high.
MD = Monitor Data

Figure 15. Monitor Channel Handshake Procedure

Figure 16 shows the maximum speed case for monitor handshake timing. The transmitter can be designed for a higher data throughput than is provided by the general case. The transmitter can deactivate (high) MX and transmit new data one frame after MR is deactivated. In this way, the transmitter is anticipating that MR will be reactivated one frame after it is deactivated, minimising the delay between bytes. MR being held inactive (high) for two or more frames indicates an abort is being signalled by the receiver.

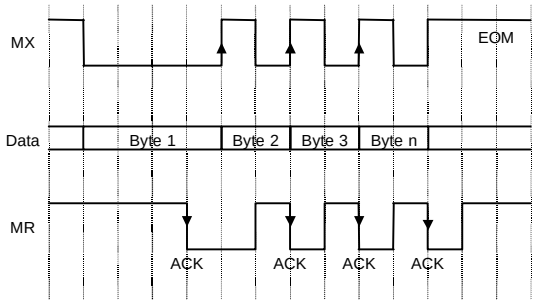


Figure 16. Monitor Handshake Timing (maximum speed case)

The abort is a signal from the receiver to the transmitter indicating that data has been missed. The receiver is able to abort a transmission by holding MR inactive (high) for two or more frames in response to MX going active. Figure 17 shows a monitor abort request from the receiver.

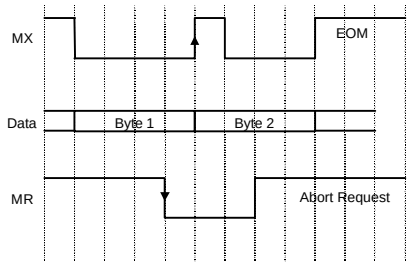


Figure 17. Abort Request from the Receiver

1.7.2.4 C/I0 Channel Description

The C/I0 channel in sub-frame 0 is used to pass predefined 4-bit layer-1 control primitives between layer-1 devices. The CMX635 in an NT configuration might use the C/I0 channel to communicate with a U interface transceiver.

The predefined codes for NT operation are listed in the following table.

C/I0 Code	DD	DU
0000	DR	TIM
0001	RES	RES
0010	TM2	TM2
0011	TM1	TM1
0100	RSY	RSY
0101	-	-
0110	-	-
0111	PU	-
1000	AR	AR
1001	-	-
1010	ARL	ARL
1011	-	-
1100	AI	AI
1101	-	-
1110	AIL	-
1111	DC	DI

The abbreviations used in the previous table are:

AI - Activate Indication
AIL - Activate Indication Local test loop
AR - Activation Request
ARL - Activation Request Local test loop
DC - Deactivation Confirmation
DI - Deactivation Indication
DR - Deactivation Request
PU - Power Up
RES - Reset
RSY - Resynchronisation
TIM - Timing Request
TM1 - Test Mode 1
TM2 - Test Mode 2

1.7.2.5 TIC Bus Description

The TIC bus allows multiple layer-2 devices on the same IOM bus to access the D and C/I0 channels.

The TIC bus is defined as bits[5:2] of the last byte of sub-frame 0. The format for the TIC channel in the downstream direction is as follows:

7	6	5	4	3	2	1	0
1	1	S/G	1	1	1	1	1

The Stop/Go bit S/G when set to binary 1 indicates to downstream layer-2 devices that the D and/or C/I0 channels are occupied. These devices would then be required to wait until the S/G bit changed to binary 0 before attempting to request D-channel access via the BAC/TAD mechanism.

The S/G bit in the CMX635 when configured as an upstream device is controlled by the D-channel routing and the D-channel access mechanism. If the D-channel is routed from the IOM bus to the ST bus and the ST D-channel is free, the S/G bit will be set to binary 0.

When the CMX635 is configured as a downstream device the S/G bit input is ignored, thus the CMX635 can be the only downstream layer-2 device in an NT configuration.

The format for the TIC channel in the upstream direction is as follows:

7	6	5	4	3	2	1	0
1	1	BAC	T.A.D.			1	1

BAC - Bus Access Bit
TAD - TIC Bus Address

The TIC bus in the upstream direction provides a contention resolution mechanism for multiple downstream layer-2 controllers. The downstream controllers must monitor BAC and when it is set to binary 1, the D-channel is available. A downstream controller requiring access to the D-channel will then start to transmit its unique TAD, monitoring each bit as it is transmitted. If a contention is detected (TAD bit is binary 0 when binary 1 was transmitted) the controller immediately ceases transmission. If the complete TAD is transmitted without contention the controller 'occupies' the D-channel by setting its BAC to binary 0. This will hold off other controllers until the D-channel is released (BAC set to binary 1). At the end of a transmission, the controller will not attempt to occupy the D-channel until the BAC has been at binary 1 for at least 2 consecutive frames, allowing other lower priority controllers access to the channel.

The CMX635 does not monitor the TAD bits, as this is purely a mechanism for downstream layer-2 controllers to resolve contention between themselves.

The CMX635 can set the BAC to binary 0 when configured as a downstream device to allow for upstream devices that require BAC activation, however the CMX635 itself has no TIC bus arbitration mechanism. The TAD bits are not driven and default to binary 1.

When the CMX635 is configured as an upstream device with multiple downstream layer-2 controllers, it can successfully arbitrate D-channel access between itself and the external controllers.

When the CMX635 requires access to the D-channel the processor will set up the routing between the HDLC block and the ST interface. This will automatically set the S/G bit to binary 1 and prevent access from the external controllers. The Data Request primitive is then written to the ST

control register (section 1.6.2.1.1) and the D-channel access mechanism will arbitrate access with other ST layer-1 devices as normal.

If a downstream IOM controller requires D-channel access it will issue the AR primitive with the required priority to the CMX635 via the C/I0 channel (see section 1.7.2.4). The processor will then route the IOM D-channel to the ST interface and issue the Activate Request primitive to the ST control register. When the D-channel access mechanism determines that the ST D-channel is free, the S/G bit will automatically be set to binary 0 allowing the external controller to complete its TIC bus procedure and transmit in the IOM D-channel. Note that the 4-bit CI AR codes override most of the other codes and can be potentially issued by multiple downstream controllers. The CMX635 simply grants access to the IOM D-channel. The TIC procedure determines which controller has priority.

1.7.3 Tone Switching

When using the Tone/FSK On/Off bit (bit 5) of the Tone Enable register (section 1.6.2.11.3), each tone starts from $V_{BIAS,}$ and returns to V_{BIAS} before ending:

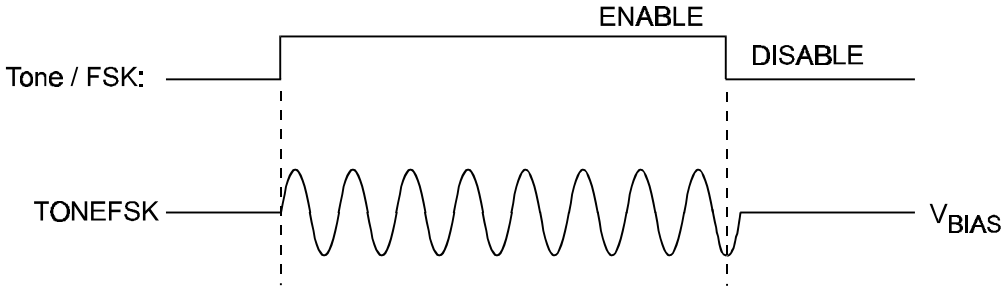


Figure 18. Tone Starting and Stopping

When switching between tones in the same column (bits 7 - 4 or bits 3 - 0) of the Tone Data register, section 1.6.2.14.3), the transition will be phase continuous. However, switching to the 'OFF' state will immediately take the output of that tone generator to V_{BIAS}.

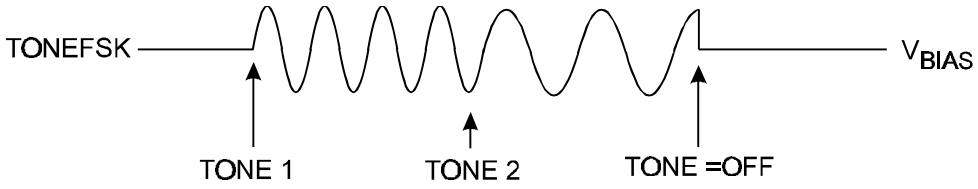


Figure 19. Tone Changing

The Tone Data register values that do not have a frequency allocated are indicated by '-' in the Tone Field tables. These values should not be used.

1.7.4 Telecom Tones

The following tables give the hex codes to be programmed into the particular tone field location for various telecommunications systems applications. The tables are not exhaustive, but list the more commonly used tones.

Ringing Signals

(f ±2.5%) (Hz)	Field 0 (Hex)
Off	$00
16.7	$01
20	$02
25	$03
35	$04
40	$05
50	$06

On Hook 'CPE Alert Tones

Single Tone (Hz)	Field 0 (Hex)
375.2	$60
404.3	$70
468	$80
495.8	$90
520.6	$A0
548	$B0
562.8	$C0
578.4	$D0
1633	$0D

Dual Tone (Hz)	Field 0 (Hex)
375.2+1827	$6E
404.3+1827	$7E
468+1827	$8E
495.8+1827	$9E
520.6+1827	$AE
548+1827	$BE
562.8+1827	$CE
578.4+1827	$DE

NYNEX (MRAA) - AMR Alert Tones (Single Tone)

Group A (Hz)	Field 0 (Hex)
252.4	$10
268.7	$20
285.3	$30
315.5	$40
330.5	$50
375.2	$60

Group B (Hz)	Field 0 (Hex)
468	$80
495.8	$90
520.6	$A0
562.8	$C0
595	$E0
612.5	$F0

Single Frequency Call Progress Tones

(Hz)	Field 1 (Hex)
Off	$00
120	$10
150	$20
154	$30
250	$40
300	$50
350	$60
400	$C0
425	$04
440	$06
450	$07
480	$09
500	$0A
600	$0B
620	$0C

Dual Frequency Call Progress Tones

Additive Mixing (Hz)	Field 1 (Hex)
Off	$00
350+440	$66
440+480	$F6
480+620	$FC
400+425	$C4
400+450	$C7
425+450	$D4
425+480	$F4
120+620	$1C
150+450	$27

Multiplicative Mixing (Hz)	Field 1 (Hex)
400*16.2	$B2
400*20	$A3
400*25	$94
400*33	$85
400*40	$76
400*50	$67
450*25	$E4
600*120	$FD

Dual Tone Multi Frequency Generation

(Hz)	Field 2 (Hex)
Off	$00
941+1633	$FF
697+1209	$CC
697+1336	$CD
697+1477	$CE
770+1209	$DC
770+1336	$DD
770+1477	$DE
852+1209	$EC
852+1336	$ED
852+1477	$EE
941+1336	$FD
941+1209	$FC
941+1477	$FE
697+1633	$CF
770+1633	$DF
852+1633	$EF

Special Information Tones, Fax and Modem Tones and Customer Premises Alert Tones

(Hz)	Field 2 (Hex)
Off	$00
950	$80
1100	$30
1300	$40
1400	$90
1800	$A0
2100	$08
2225	$09
2130+2750	$BB

CCITT 'R1' Signalling Tones

(Hz)	Field 2 (Hex)
700+900	$12
700+1100	$13
900+1100	$23
700+1300	$14
900+1300	$24
1100+1300	$34
700+1500	$15
900+1500	$25
1100+1500	$35
1300+1500	$45
700+1700	$16
900+1700	$26
1100+1700	$36
1300+1700	$46
1500+1700	$56

CCITT 'R2' Signalling Tones

Forward mode (Hz)	Field 3 (Hex)
Off	$00
1380+1500	$89
1380+1620	$8A
1500+1620	$9A
1380+1740	$8B
1500+1740	$9B
1620+1740	$AB
1380+1860	$8C
1500+1860	$9C
1620+1860	$AC
1740+1860	$BC
1380+1980	$8D
1500+1980	$9D
1620+1980	$AD
1740+1980	$BD
1860+1980	$CD

Backward mode (Hz)	Field 3 (Hex)
Off	$00
1140+1020	$65
1140+900	$64
1020+900	$54
1140+780	$63
1020+780	$53
900+780	$43
1140+660	$62
1020+660	$52
900+660	$42
780+660	$32
1140+540	$61
1020+540	$51
900+540	$41
780+540	$31
660+540	$21

1.8 Performance Specification

1.8.1 Electrical Performance

1.8.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Unit
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current into or out of V_{DD} and V_{SS} pins	-50	+50	mA
Current into or out of any other pin	-20	+20	mA

L4 Package	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at Tamb = 25°C	-	550	mW
... Derating	-	9.0	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

1.8.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	**Min.**	**Max.**	**Unit**
Supply (V_{DD} - V_{SS})		3.0	5.5	V
Operating Temperature		-40	+85	°C

1.8.1.3 Operating Characteristics

For the following conditions unless otherwise specified:
V_{DD} = 3.0V to 5.5V at Tamb = -40 to +85°C,
0dBm = 775mVrms = 0dBm0. Xtal frequency at nominal 12.288MHz or 15.36MHz.

Details in this section represent design target values and are not currently guaranteed.

DC Parameters		Symbol	Notes	Min.	Typ.	Max.	Unit
I_{DD}	All Enabled, V_{DD} = 5.0V	I_{DD5a}	1, 2	-	43.0	-	mA
	All Disabled, V_{DD} = 5.0V	I_{DD5b}	1, 3	-	20.0	-	ìA
	ST bus and HDLC only activated, V_{DD} = 5.0V	I_{DD5c}	1, 4	-	28.0	-	mA
	+ Rx1, Tx1 and Codec, V_{DD} = 5.0V	I_{DD5d}	1	-	32.0	-	mA
	+ Tx2, DTMF Rx and Tone Gen V_{DD} = 5.0V	I_{DD5e}	1, 5	-	37.0	-	mA
	All Enabled, V_{DD} = 3.3V	I_{DD3a}	1, 2	-	24.0	-	mA
	All Disabled, V_{DD} = 3.3V	I_{DD3b}	1, 3	-	20.0	-	ìA
	ST bus and HDLC only activated, V_{DD} = 3.3V	I_{DD3c}	1, 4	-	16.0	-	mA
	+ Rx1, Tx1 and Codec, V_{DD} = 3.3V	I_{DD3d}	1	-	18.0	-	mA
	+ Tx2, DTMF Rx and Tone Gen V_{DD} = 3.3V	I_{DD3e}	1, 5	-	22.0	-	mA
Logic Input Leakage Current (Vin = 0 to V_{DD}),		I_I		-1.0	-	+1.0	µA
Logic '1' Input Level (CMOS inputs)		V_{IH}	6	70%	-	-	V_{DD}
Logic '0' Input Level (CMOS inputs)		V_{IL}	6	-	-	30%	V_{DD}
Logic '1' Input Level (TTL inputs)		V_{IH}	6	2.0	-	-	V
Logic '0' Input Level (TTL inputs), Vdd = 3.3 – 5.5 V		V_{IL}	6, 7	-	-	0.8	V
Output Logic '1' Level DCL,FSC (I_{OH} = 2mA)		V_{OH}	8	0.8	-	-	V_{DD}
Output Logic '0' Level DCL,FSC (I_{OL} = 3mA)		V_{OL}	8	-	-	0.4	V
Output Logic '1' Level IOMTx, IOMRx (I_{OH} = 4mA)		V_{OH}	8	0.8	-	-	V_{DD}
Output Logic '0' Level IOMTx, IOMRx (I_{OL} = 6mA)		V_{OL}	8	-	-	0.4	V
Output Logic '1' Level AD, CLKOUT (I_{OH} = 3mA)		V_{OH}	8	0.8	-	-	V_{DD}
Output Logic '0' Level AD, CLKOUT (I_{OL} = 4.5mA)		V_{OL}	8	-	-	0.4	V
Output Logic '0' Level nIRQ, Dtack (I_{OL} = 4.5mA)		V_{OL}	8	-	-	0.4	V
Open Drain O/Ps Off State Current (V_{OUT} = V_{DD})		I_{ODOH}		-	-	1.0	µA

Notes:

1. At 25°C, not including any current drawn from the CMX635 pins by external circuitry.
2. All clocks running, all analogue blocks enabled.
3. Master oscillator stopped, all analogue blocks in power save mode.
4. No load on Tx2, generating and receiving DTMF tones.
5. Driving recommended external components with continuous binary 0 (mark).
6. All inputs CMOS except IOM FSC, DCL, IOMRx and IOMTx, see Signal List.
7. Derate linearly minimum TTL Logic '0' level from 0.8V at Vdd = 3.3V to 0.5V at Vdd = 2.7V.
8. All outputs CMOS levels.

FSK Output	Notes	Min.	Typ.	Max.	Unit
Output of Tone Generator block (for FSK tones)	9,11	-1.0	0	1.0	dBm
Twist (Mark level w.r.t. Space level)		-2.0	0	+2.0	dB
Tx 1200bits/sec (V.23 mode)					
Baud Rate		1194	1200	1206	Baud
Mark (Logical 1) Frequency		1297	1300	1303	Hz
Space (Logical 0) Frequency		2097	2100	2103	Hz
Tx 1200bits/sec (Bell 202 mode)					
Baud Rate		1194	1200	1206	Baud
Mark (Logical 1) Frequency		1197	1200	1203	Hz
Space (Logical 0) Frequency		2197	2200	2203	Hz

Tone Outputs	Notes	Min.	Typ.	Max.	Unit
Output of Tone Generator block for:	11				
Single tone	9	-1.0	0	1.0	dBm
Dual tone (per tone)	9	-4.0	-3.0	-2.0	dBm
DTMF High Frequency Group	9	-4.0	-3.0	-2.0	dBm
DTMF Low Frequency Group	9	-6.0	-5.0	-4.0	dBm
Tone frequency resolution		-2.5	-	2.5	Hz
Tone output distortion	10	-	0.8	-	%

Notes:

9. At V_{DD} = 5.0V, signal levels are proportional to V_{DD}.
10. Frequency above 300Hz.
11. See Analogue Block Diagram (section 1.2.2) for internal block definition.

DTMF Decoder	Notes	Min.	Typ.	Max.	Unit
Valid input signal levels (input to DTMF Decode block) (each tone of composite signal)	9, 11	-29.0	-	-2	dBm
Not decode level (either tone of composite signal)	9	-	-	-40.0	dBm
Twist = High Tone/Low Tone		-9.0	-	10.0	dB
Frequency Detect Bandwidth		±1.8	-	±4.5	%
Dial Tone Tolerance	12	-	-	0	dB
Noise Tolerance	12, 13	-	-14.0	-	dB
Tone Response time	14	-	-	40.0	ms
Tone De-response time	14	-	-	45.0	ms
Tone burst detected	14	40.0	-	-	ms
Tone burst ignored	14	-	20.0	-	ms
Pause length detected	14	40.0	-	-	ms
Pause length ignored	14	-	-	20.0	ms

Notes:

12. Referenced to DTMF tone of lower amplitude.
13. Bandwidth limited: 0 to 3.4kHz Gaussian Noise.
14. At nominal signal frequencies and without skew.

SPM Signal Level	Notes	Min.	Typ.	Max.	Unit
Level at SPM pin	9, 15	-1.5	0	1.0	dBm
Tone frequency accuracy		-14.0	-	14.0	Hz
Tone output distortion		-	1.2	-	%
Output Impedance		-	10.0	-	kΩ

Notes:

15. SPM has a soft rise and fall time of about 4ms. The level changes between V_{BIAS} and 0dBm in 2dB steps, 16 steps per rise and fall. When SPM is disabled, an extra 4ms falling tail end of signal should be taken into consideration.

PCM Codec-Filter	Notes	Min.	Typ.	Max.	Unit
PCM Codec-Filter (F1)	11				
Passband	16	300	-	3400	Hz
Passband Gain (at 1.02kHz)	16	-	3.9	-	dB
Passband Ripple (w.r.t. gain at 1.02kHz)	16	-0.25	-	+0.25	dB
Stopband Attenuation (w.r.t. gain at 1.02kHz)	16	30.0	-	-	dB
Group delay					
Absolute		-	-	600	µs
Relative to 1kHz:					
500Hz		-	-	1.5	ms
600Hz		-	-	0.75	ms
2600Hz		-	-	0.25	ms
2800Hz		-	-	1.5	ms
Signal-to-total distortion ratio as a function of input level (1kHz input level):					
-45dBm	17	22.0	-	-	dBp
-40dBm	17	27.0	-	-	dBp
-30dBm	17	33.0	-	-	dBp
0dBm	17	33.0	-	-	dBp
Variation of gain with input level (1kHz input signal)					
-55dBm0		-3.0	-	+3.0	dB
-50dBm0		-1.0	-	+1.0	dB
-40dBm0		-0.5	-	+0.5	dB
+3dBm0		-0.5	-	+0.5	dB
Idle channel noise	17	-	-	-65.0	dBm0p

Notes:

16. Meets G.712 specification for analogue-digital attenuation characteristics (Figure 20).
17. Represents a psophometrically weighted measurement.

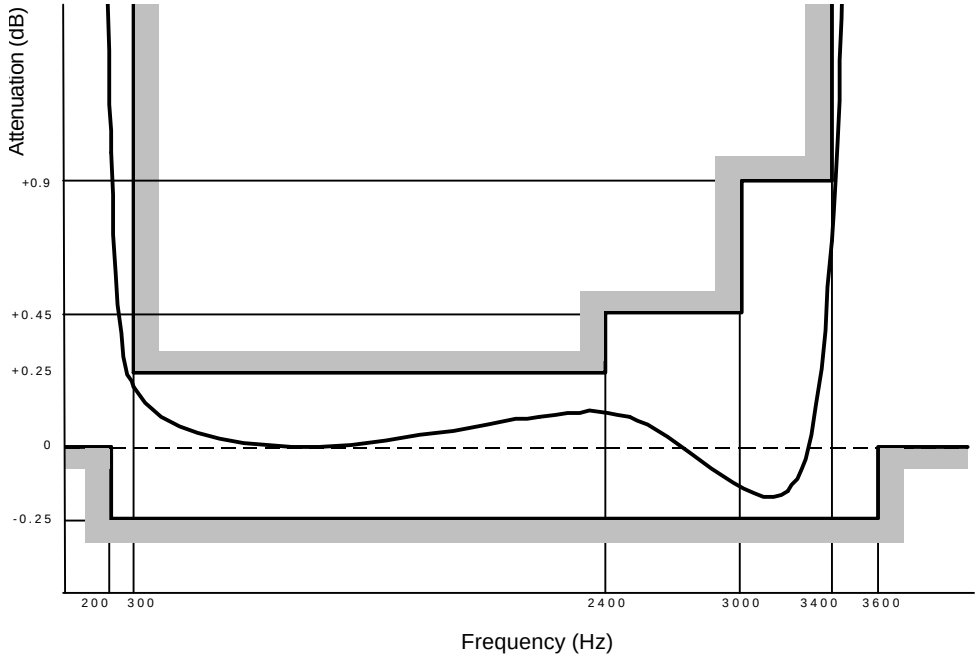


Figure 20. Codec Filter Attenuation Characteristics and Limits

Input Amplifiers RX1 and RX2		Notes	Min.	Typ.	Max.	Unit
Open Loop Gain	(I/P – 1mV at 100Hz)		-	60.0	-	dB
Unity Gain Bandwidth			-	1.0	-	MHz
Input Impedance	(at 100Hz)		10	-	-	MΩ
Minimum Impedance on RX1O and RX2O pins			100	-	-	kΩ

Output Amplifiers TX1		Notes	Min.	Typ.	Max.	Unit
Open Loop Gain	(I/P – 1mV at 100Hz)		-	40.0	-	dB
Unity Gain Bandwidth			-	1.0	-	MHz
Input Impedance	(at 100Hz)		10	-	-	MΩ
Output Voltage Swing	(150Ω load at V_{DD} = 5.0V)		-	4.2	-	Vpp
Output Voltage Swing	(150Ω load at V_{DD} = 3.3V)		-	2.7	-	Vpp
Capacitive Load Limit			-	-	100	pF
Minimum Impedance on TX1OP pin			100	-	-	kΩ

Output Amplifiers TX2		Notes	Min.	Typ.	Max.	Unit
Output Voltage Swing	(50Ω load at V_{DD} = 5.0V)		-	3.2	-	Vpp
Output Voltage Swing	(50Ω load at V_{DD} = 3.3V)		-	2.1	-	Vpp
Capacitive Load Limit			-	-	100	pF

Power-Up Timing	Notes	Min.	Typ.	Max.	Unit
Device reset to reliable Tone signals at TX1 and SPM outputs		-	50.0	-	ms

Typical UART Timings (See Figure 6 and Figure 7)		Notes	Min.	Typ.	Max.	Unit
T_{FSK}	(delay through the modulator)		-	106	-	µs
T_{DLY}	(1 bit period)		-	833	-	µs
T_{DRDY}	(¼ bit-period)		-	208	-	µs
T_{UFL}	(¾ bit-period)		-	625	-	µs

IOM-2 Bus Timing (See Figure 21)		Notes	Min.	Typ.	Max.	Unit
t_{DCL}	DCL clock period in TE Mode		-	651	-	ns
t_R / t_F	DCL clock rise time / fall time	18	-	-	20	ns
FSC	FSC period		-	125	-	µs
t_{FSCS}	FSC set-up time		70	-	-	ns
t_{FSCH}	FSC hold time		40	-	-	ns
t_{DUDC}	DU delay clock (data out)	18	-	-	100	ns
t_{DUDF}	DU delay frame (data out)	18	-	-	150	ns

Notes:

18. Condition C_L = 150pF

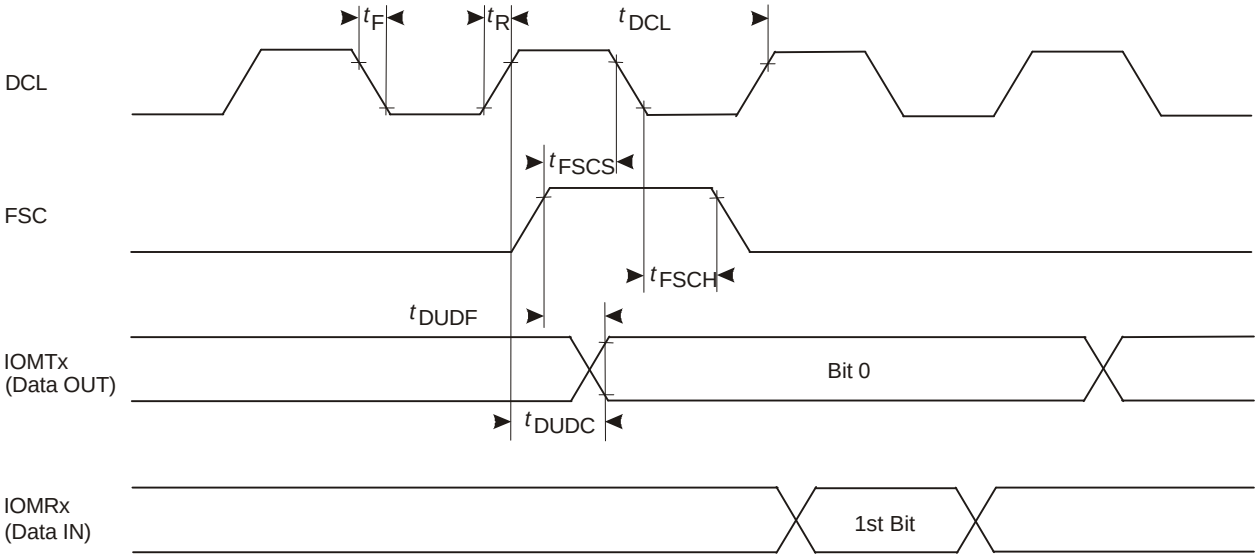


Figure 21. IOM-2 Bus Timing Diagram

		Intel Multiplexed Style Processor Bus Timing (See Figure 22)	**Notes**	**Min.**	**Typ.**	**Max.**	**Unit**
1a	t_{RL}	Read strobe pulse width low	18	170	-	-	ns
1b	t_{RL}	Read strobe pulse width low	19	270	-	-	ns
2	t_{WL}	Write strobe pulse width low		100	-	-	ns
3	t_{RCS}	nCS from read strobe hold		10	-	-	ns
4	t_{WCS}	nCS from write strobe hold		10	-	-	ns
5	t_{AW}	Address strobe to write strobe set		10	-	-	ns
6	t_{AR}	Address strobe to read strobe set		10	-	-	ns
7	t_{AS}	Address Latch Enable pulse width		20	-	-	ns
8	t_{AAS}	Address set up time to address strobe		10	-	-	ns
9	t_{AAH}	Address hold time from address strobe		10	-	-	ns
10a	t_{RAC}	Read access time from read strobe	18, 20	15	-	220 (250)	ns
10b	t_{RAC}	Read access time from read strobe	19	15	-	310	ns
11	t_{RH}	Read data hold time from read strobe		10	-	-	ns
12	t_{WS}	Write data setup time to write strobe		10	-	-	ns
13	t_{WH}	Write data hold time from write strobe		10	-	-	ns
14	t_{CSA}	nCS to address strobe		10	-	-	ns

Notes:

19. Register access operations in 12.288MHz and 15.36MHz.
20. Fifo access operations in 15.36MHz mode only.
21. Default values in following table are for 12.288MHz operation. Where different, values for 15.36MHz operation are shown in brackets.

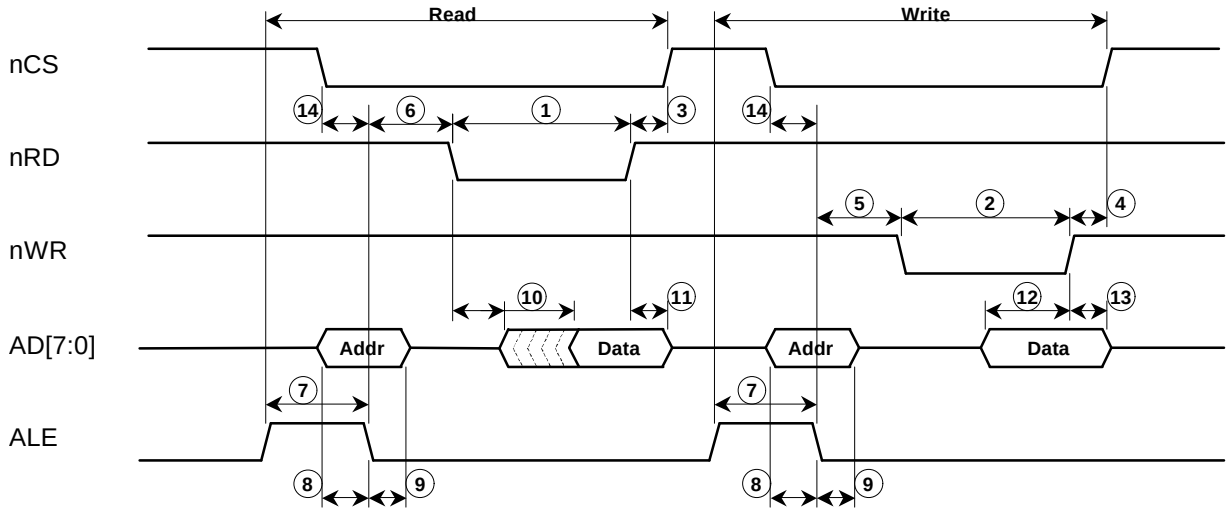


Figure 22. Processor Bus Timing – Intel Multiplexed

		Motorola Multiplexed Style Processor Bus Timing (See Figure 23)	**Notes**	**Min.**	**Typ.**	**Max.**	**Unit**
1a	t_{EHW}	E high time for read cycle	18	170	-	-	ns
1b	t_{EHW}	E high time for read cycle	19	270	-	-	ns
2	t_{EHR}	E high time for write cycle		100	-	-	ns
3	t_{ECS}	nCS from E hold		0	-	-	ns
4	t_{CSE}	nCS to E set up		10	-	-	ns
5	t_{ASE}	Address strobe to E set up		10	-	-	ns
6	t_{AS}	Address strobe Width		20	-	-	ns
7	t_{AAS}	Address set up time to AS		10	-	-	ns
8	t_{AAH}	Address hold time from AS		10	-	-	ns
9a	t_{RAC}	Read access time from E		15	-	220 (250)	ns
9b	t_{RAC}	Read access time from E		15	-	310	ns
10	t_{RH}	Read data hold time from E		10	-	-	ns
11	t_{WS}	Write data setup time to E		10	-	-	ns
12	t_{WH}	Write data hold time from E		10	-	-	ns
13	t_{RWE}	R/nW transition to E set up		10	-	-	ns
14	t_{CSAS}	nCS to address strobe		10	-	-	ns
15	t_{RWAS}	R/nW to address strobe		10	-	-	ns

Notes:

The processor control pins are redefined as follows for a Motorola multiplexed style interface:

nRD	E	(pin #11)
nWR	R/nW	(pin #12)
ALE	AS	(pin #15)

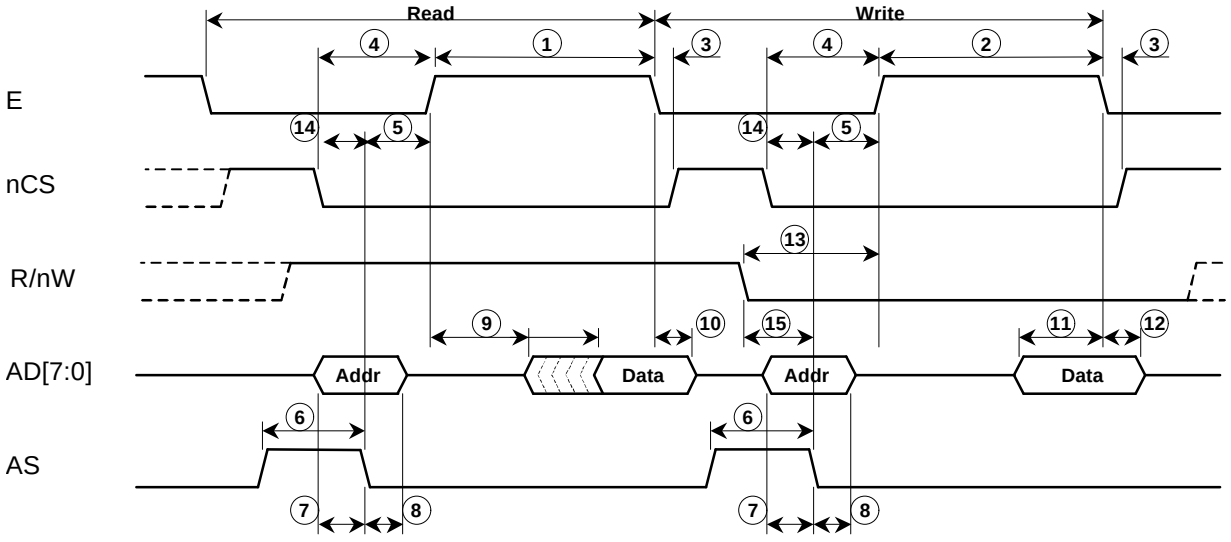


Figure 23. Processor Bus Timing – Motorola Multiplexed

	Intel Non-multiplexed Style Processor Bus Timing (See Figure 24)		**Notes**	**Min.**	**Typ.**	**Max.**	**Unit**
1	t_{CSWS}	nCS to nWR setup	21	10	-	-	ns
2	t_{CSWH}	nCS from nWR hold	21	10	-	-	ns
3	t_{ASS}	ASel to nWR setup		10	-	-	ns
4	t_{ASH}	ASel from nWR hold		10	-	-	ns
5	t_W	nWR pulse width		100	-	-	ns
6a	t_R	nRD pulse width	18	170	-	-	ns
6a	t_R	nRD pulse width	19	270	-	-	ns
7	t_{CSRS}	nCS to nRD setup	21	10	-	-	ns
8	t_{CSRH}	nCS from nRD hold	21	10	-	-	ns
9	t_{ADS}	Indirect address/data set up time to nWR		10	-	-	ns
10	t_{ADH}	Indirect address/data hold time from nWR		10	-	-	ns
11a	t_{RAC}	Read access time from nRD	18	15	-	220 (250)	ns
11b	t_{RAC}	Read access time from nRD	19	15	-	310	ns
12	t_{RH}	Read data hold time from nRD↑	22	10	-	-	ns
13	t_{CTWR}	Cycle time nWR to nRD for addr Wr/Rd	23	90 (110)	-	-	ns
14	t_{CTW}	Cycle time nWR to nWR for addr Wr/Wr	23	90 (110)	-	-	ns
Consecutive Reads/Writes (See Figure 25)							
15a	t_{CWW}	Cycle time nWR to nWR for write-write	18, 24	260	-	-	ns
15b	t_{CWW}	Cycle time nWR to nWR for write-write	19, 24	330	-	-	ns
16a	t_{CRR}	Cycle time nRD to nRD for read-read	18, 24	260	-	-	ns
16b	t_{CRR}	Cycle time nRD to nRD for read-read	19, 24	330	-	-	ns

Notes:

22. nCS may be kept low for consecutive writes/reads.
23. Time to high impedance.
24. Indirect address write followed by a data read or write cycle.
25. Consecutive data read/writes using persistent indirect address.

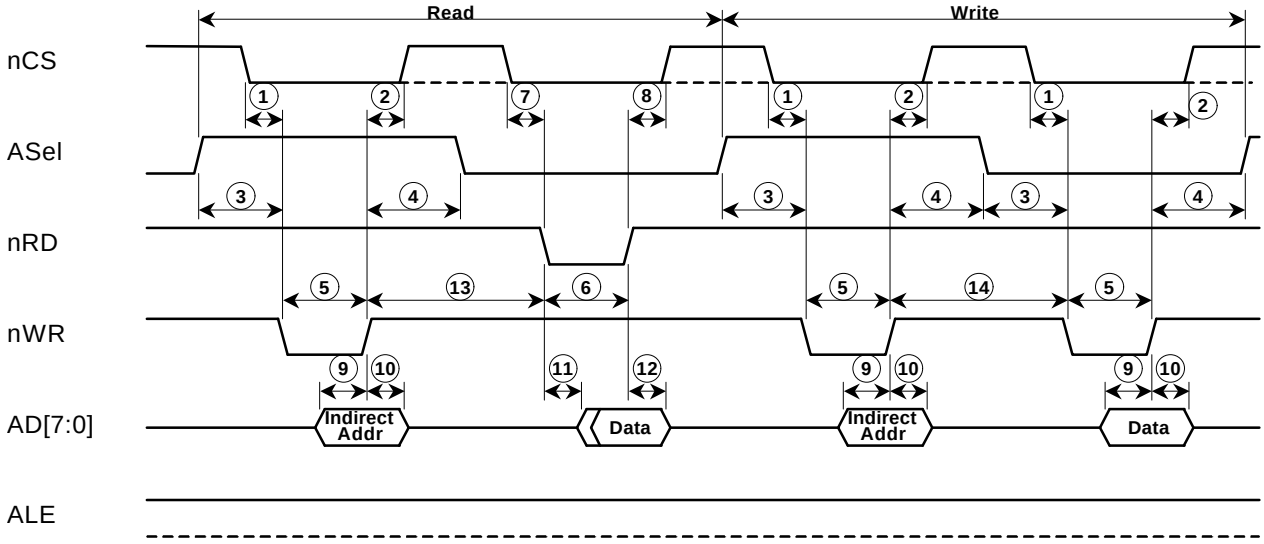


Figure 24. Processor Bus Timing – Intel Non-multiplexed

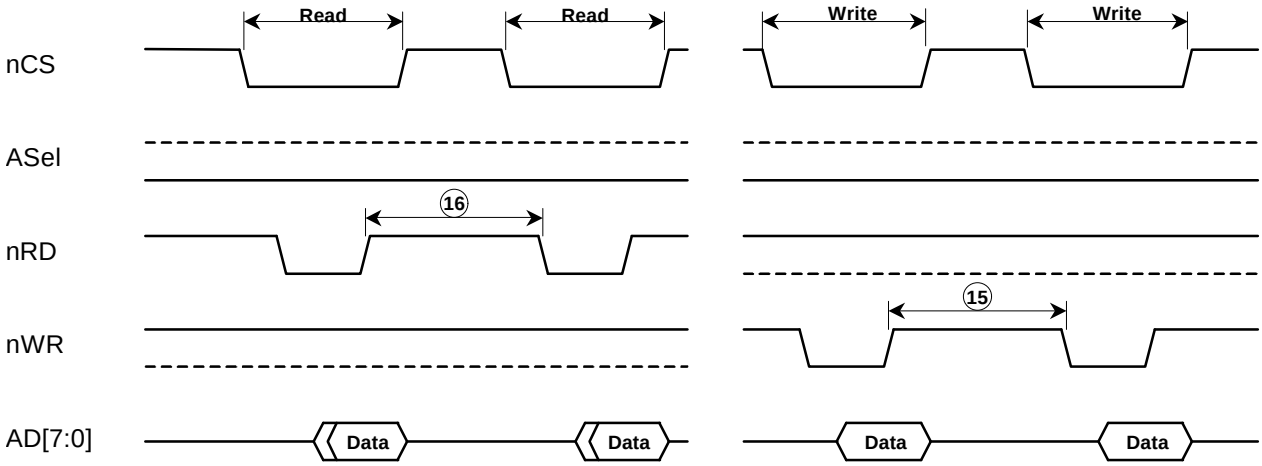


Figure 25. Processor Bus Timing – Consecutive Read/Writes

		Motorola Non-multiplexed Style Processor Bus Timing (See Figure 26 below)	**Notes**	**Min.**	**Typ.**	**Max.**	**Unit**
1	t_{CSS}	nCS to nDS setup		10	-	-	ns
2	t_{CSAWH}	nCS from nDS hold		10	-	-	ns
3	t_{AAS}	ASel to nDS setup		10	-	-	ns
4	t_{AAH}	ASel from nDS hold		10	-	-	ns
5	t_{DSWA}	nDS pulse width for address write		20	-	-	ns
6	t_{DSWD}	nDS pulse width for data write		100	-	-	ns
7a	t_{DSR}	nDS pulse width for read	18	170	-	-	ns
7b	t_{DSR}	nDS pulse width for read	19	270	-	-	ns
8	t_{AS}	Indirect address set up time to nDS		10	-	-	ns
9	t_{AH}	Indirect address hold time from nDS		10	-	-	ns
10a	t_{RAC}	Read access time from nDS (reg.	18	15	-	220 (250)	ns
10b	t_{RAC}	Read access time from nDS (fifo read)	19	15	-	310	ns
11	t_{RH}	Read data hold time from nCS	22	10	-	-	ns
12	t_{RWS}	R/nW transition to nDS setup		0	-	-	ns
13	t_{RWH}	R/nW transition from nDS hold		0	-	-	ns
14	t_{CTWR}	Cycle time nDS to nDS for addr	23	90 (110)	-	-	ns
15	t_{CTWW}	Cycle time nDS to nDS for addr	23	90 (110)	-	-	ns
16	t_{DDLA}	Dtack delay from nDS , address write		-	-	45	ns
17	t_{DDHA}	Dtack delay from nDS , address write		-	-	45	ns
18	t_{DDLD}	Dtack delay from nDS , data		-	-	170	ns
19	t_{DCSD}	Dtack delay from nCS , data		-	-	20	ns
Consecutive Reads/Writes (See Figure 27 below)							
20a	t_{CWW}	Cycle time nCS to nDS for write-	18, 24	170	-	-	ns
20b	t_{CWW}	Cycle time nCS to nDS for write-	19, 24	270	-	-	ns
21a	t_{CRR}	Cycle time nDS to nDS for read-read	18, 24	270	-	-	ns
21b	t_{CRR}	Cycle time nDS to nDS for read-read	19, 24	330	-	-	ns

Notes:

The processor control pins are redefined as follows for a Motorola multiplexed style interface:

nRD nDS (pin #11)
nWR R/nW (pin #12)

The CMX635 ALE pin (#15) should be connected to Vss for this mode of operation.

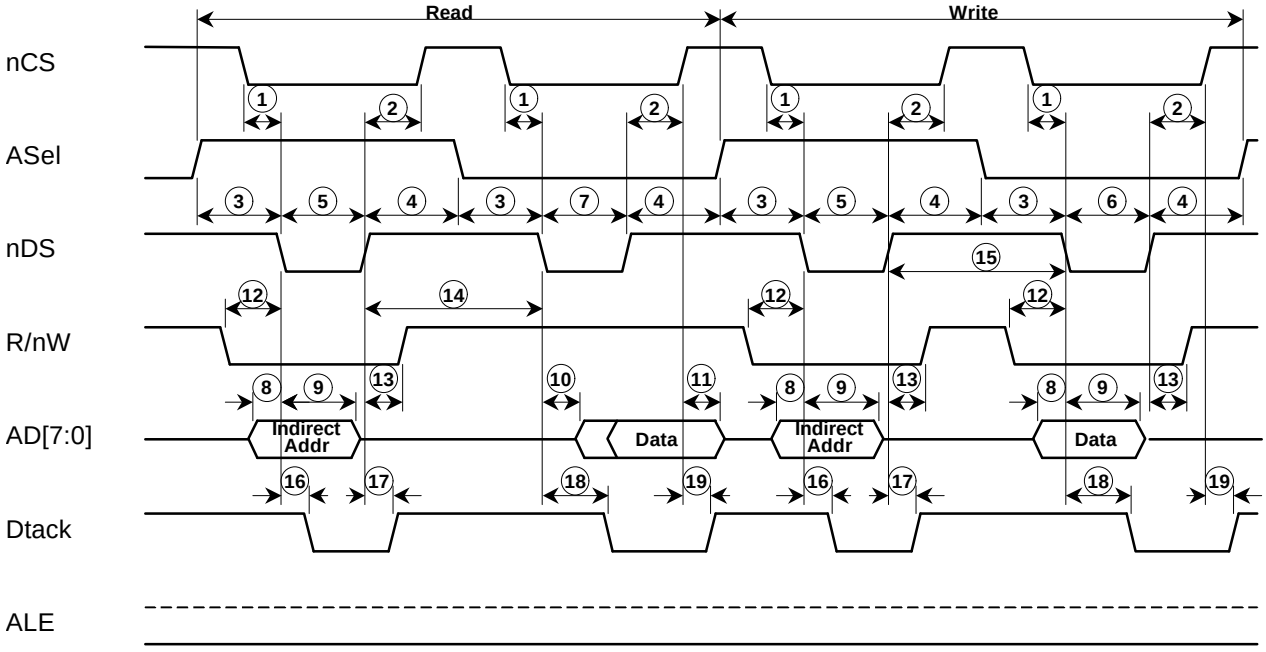


Figure 26. Processor Bus Timing – Motorola Non-multiplexed

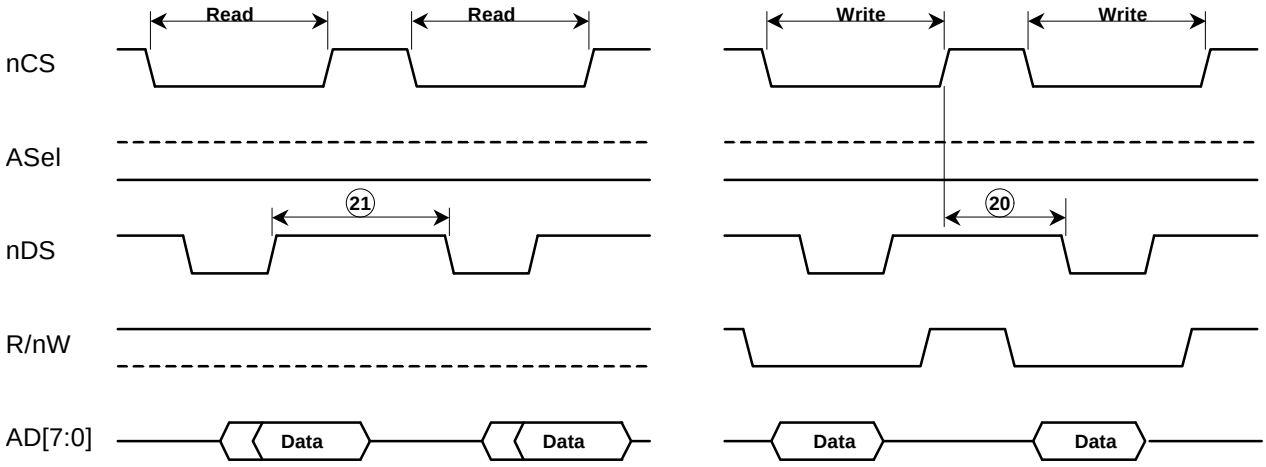
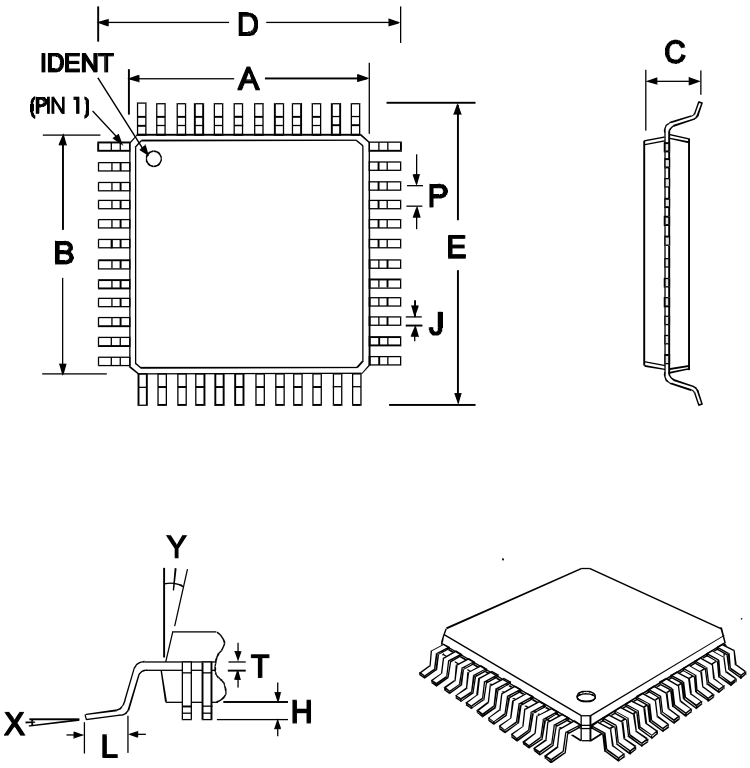


Figure 27. Processor Bus Timing – Consecutive Reads/Writes

1.8.2 Packaging



DIM.	MIN.	TYP.	MAX.
A	0.272 (6.90)		0.280 (7.10)
B	0.272 (6.90)		0.280 (7.10)
C			0.063 (1.60)
D	0.344 (8.75)		0.364 (9.25)
E	0.344 (8.75)		0.364 (9.25)
H	0.002 (0.05)		0.006 (0.15)
J	0.004 (0.11)		0.011 (0.27)
L	0.014 (0.35)		0.026 (0.66)
P		0.020 (0.50)	
T		0.005 (0.13)	
X	0°		7°
Y	11°		13°

NOTE : All dimensions in inches (mm.)
Angles in degrees

Lead coplanarity to be
0 to 0.003 (0.08) Max

Figure 28. 48-Pin TQFP (L4) Mechanical Outline

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CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CML Product Data

In the process of creating a more global image, the three standard product semiconductor companies of CML Microsystems Plc *(Consumer Microcircuits Limited (UK), MX-COM, Inc (USA) and CML Microcircuits (Singapore) Pte Ltd)* have undergone name changes and, whilst maintaining their separate new names *(CML Microcircuits (UK) Ltd, CML Microcircuits (USA) Inc and CML Microcircuits (Singapore) Pte Ltd*), now operate under the single title **CML Microcircuits**.
These companies are all 100% owned operating companies of the CML Microsystems Plc Group and these changes are purely changes of name and do not change any underlying legal entities and hence will have no effect on any agreements or contacts currently in force.

CML Microcircuits Product Prefix Codes

Until the latter part of 1996, the differentiator between products manufactured and sold from MXCOM, Inc. and Consumer Microcircuits Limited were denoted by the prefixes MX and FX respectively. These products use the same silicon etc. and today still carry the same prefixes. In the latter part of 1996, both companies adopted the common prefix: CMX.

This notification is relevant product information to which it is attached.

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