CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CMX7011
Digital Voice Processor

D/7011_FI1.x/6 April 2013

DATASHEET

Provisional Issue

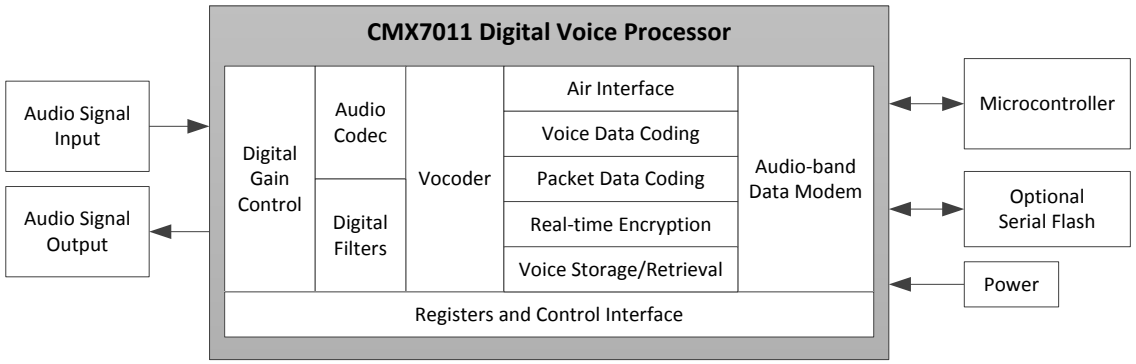
7011FI-1.x: Digital Voice Encryption for Analogue Radio Systems

Features

- Digital voice security on analogue PMR channels (12.5kHz/25kHz)
- Simple interfacing, via audio connections, to existing PMR radio
- Ultimate in high-level analogue radio security
- Embedded RALCWI Vocoder (supplied under licence and royalty free)
- Embedded audio-band modem
- Built in robust over-air data protocol with good tolerance to bit errors
- Ultimate in high-level analogue radio security
- Real-time digital voice encryption with user-programmable 16-bit encryption keys
- External voice data routing option
- Programmable instant voice capture – eliminating 'PTT' clipping
- Voice storage and retrieval with 'step back' feature
- Packet data with user-programmable packet data size
- Flexible 256 address programming
- Late entry operation, provides optimum performance in fading conditions
- Small 48-pin LQFP/VQFN package options

Applications

- Real-time voice security
- Voice encryption on analogue PMR radios
- Secure wireless door access and gate entry systems
- Providing the digital advantage on analogue radio systems
- A Plug and Play device (the CMX188) can be made available for high quantity applications



1 Brief Description

The CMX7011 is a flexible, half duplex, digital voice processor specifically designed for digital voice encryption applications that transmits and receives secure voice via an embedded robust data modem for use within an analogue PMR. The device allows simple implementation and configuration within existing designs and is intended to be added to a radio via an accessory module or “feature socket”. The device is simple to control via a small, low-power microcontroller. The CMX7011 offers better quality speech than that of traditional analogue radios at the fringes of reception and, using the internal digital encryption algorithm, significantly higher levels of security are achieved.

Built in to the CMX7011 is CML's proven and reliable RALCWI (Robust Advanced Low Complexity Waveform Interpolation) vocoder providing near toll quality speech at a low bit rate. One of the most significant features in the CMX7011's design is the programmable push-to-talk (PTT) buffer which offers instant voice capture in transmit mode. The PTT buffer temporarily stores the initial part of the speech and can therefore eliminate clipping that can be caused by the time taken to decode sub audio signals like CTCSS and system delays caused by repeaters. Within the CMX7011's header frame is a user-programmable 8-bit address field which allows up to 256 individual user addresses to be defined.

The device includes programmable voice storage and retrieval with step-back feature which permits storage of a minimum of 20 seconds of vocoded speech in receive mode.

Packet data enables secure data transfer with CRC and optional interleaving of data bits with user-programmable packet data size.

Late entry allows a receiving radio to re-join a call after recovering from fading conditions

Note that text shown in pale grey indicates features that will be supported in future versions of the device.

This Data Sheet is the first part of a two-part document.

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It is always recommended that you check for the latest product datasheet version from the Datasheets page of the CML website: [www.cmlmicro.com].

History

Version	Changes	Date
6	• EDS status changed to Provisional • Late entry functionality added • Fine output gain control added • App Notes added - 'Setting Encoder Noise Gate Parameters' and 'Setting Decoder Noise Gate Parameters' • Minor editorial changes	15th April 2013
5	• Voice store and retrieve functionality added • Packet data functionality added	18th Feb 2013
4	• Correction of VDD to DVDD • Correction of streaming C-BUS description and timing constraints • Correction of I/O to GPIO, also references to GPIO1 and GPIO2 • Minor typographical improvements	24th Oct 2012
3	• New system diagram added to front of datasheet • New block diagram added to Section 2 • Information on external data routing added to Section 7.7 • Information on external data routing registers added to Section 9	3rd September 2012
2	• Information on noise gate registers added to Section 9.1 • Modification to IOCTRL register in Section 9.1 • Application note added for basic device operation in Section 10. • Various typographical and editorial changes	28th May 2012
1	• First release, Advance Information	5th Apr 2012

This is Provisional Information; changes and additions may be made to this specification. Parameters marked TBD or left blank will be included in later issues. Items that are highlighted or greyed out should be ignored. These will be clarified in later issues of this document. Information in this provisional document should not be relied upon for final product design.

2 Block Diagram

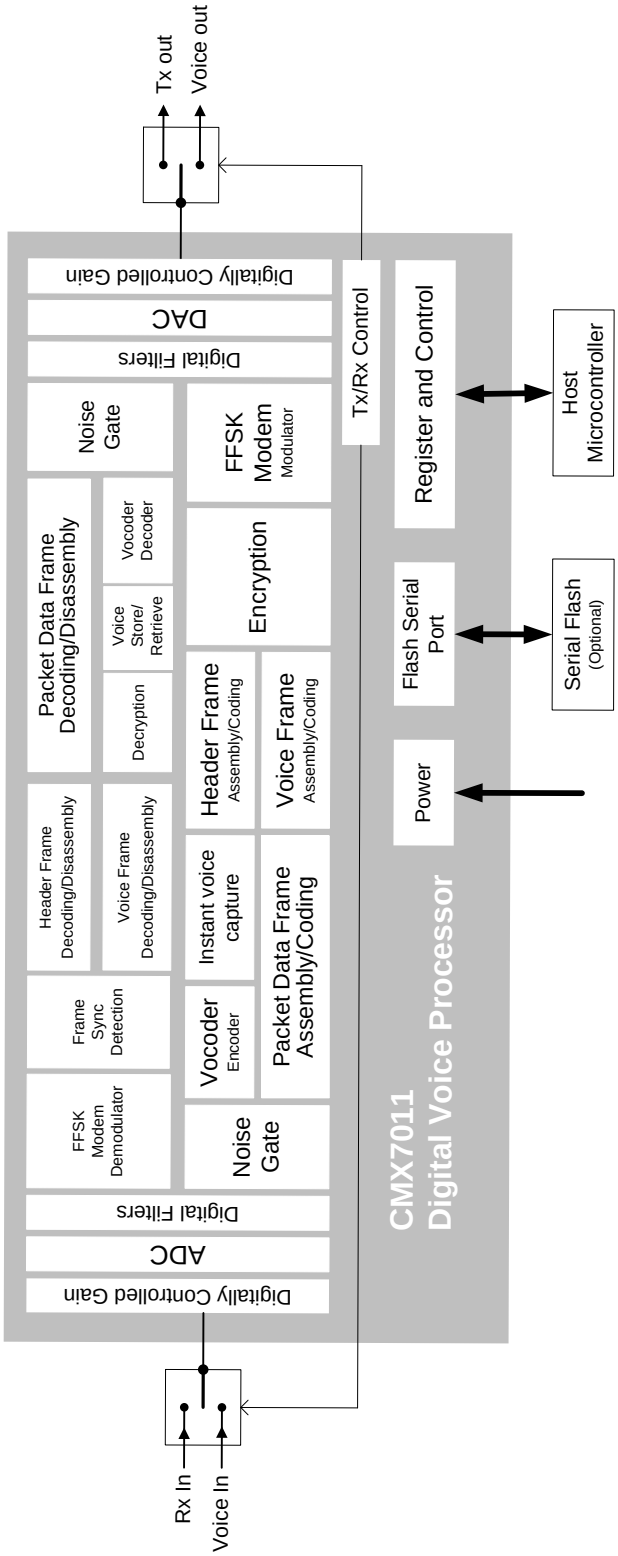


Figure 1 Block Diagram

3 Pin and Signal List

CMX7011 L4/Q3	Pin		Signal Description	
Pin No.	**Name**	**Type**		
1	AVDD	Power	Analogue Positive Power Supply 3.3V	
2	AVSS	Power	Analogue Negative Power Supply 0V	
3	VBIAS	Analogue Output	Analogue Bias (approximately 1.65 Volts)	
4	VSSREF	Power	Analogue Negative Reference	
5	INPUTP	Analogue Input	Audio CODEC Positive Input (self biased)	
6	INPUTN	Analogue Input	Audio CODEC Negative Input (self biased)	
7	AVDD	Power	Analogue Positive Power Supply 3.3V	
8	AVSS	Power	Analogue Negative Power Supply 0V	
9	VSSPA	Power	Output Amplifier Negative Power Supply 0V	
10	OUTP	Analogue Output	Audio CODEC – Amplifier Positive Output	
11	OUTN	Analogue Output	Audio CODEC – Amplifier Negative Output	
12	VDDPA	Power	Output Amplifier Positive Power Supply 3.3V	
13	DVDD	Power	Digital Positive Power Supply 1.8V	
14	~	NC	Reserved for future use. Do not connect to this pin.	
15	SDI	Digital Input	SSP port serial data input	FLASH PORT
16	SDO	Digital Output	SSP port serial data output	
17	SCLK	Digital Input	SSP port serial clock input	
18	~	NC	Reserved for future use. Do not connect to this pin.	
19	GPIO1	Digital Input/Output	General Purpose Input/Output	
20	GPIO2	Digital Input/Output	General Purpose Input/Output	
21	SSOUT	Digital Output	SSP Slave Select	
22	DVSS	Power	Negative Power Supply 0V	
23	~	NC	Reserved for future use. Do not connect to this pin.	
24	IOVDD	Power	Digital I/O Positive Power Supply 3.3V	
25	TEST	TEST	Must be connected to DV_{SS} via external 100kΩ resistor.	

CMX7011 L4/Q3	Pin		Signal Description	
Pin No.	**Name**	**Type**		
26	DVSS	Power	Negative Power Supply 0V	
27	XTAL/CLK	Input	Crystal Input	
28	XTALN	Output	Crystal Output	
29	IOVDD	Power	Digital I/O Positive Power Supply 3.3V	
30	RESETN	Digital Input	General Reset (active low)	
31	XTALSEL1	Digital Input	These bits select the crystal/clock frequency, according to Table 3.	
32	XTALSEL2	Digital Input		
33	XTALSEL3	Digital Input		
34	ENABXTAL	Digital Input	Enable Crystal Oscillator/External Clock Input	
35	IOVDD	Power	Digital I/O Positive Power Supply 3.3V	
36	~	NC	Reserved for future use. Do not connect to this pin.	
37	~	NC	Reserved for future use. Do not connect to this pin.	
38	~	NC	Reserved for future use. Do not connect to this pin.	
39	~	NC	Reserved for future use. Do not connect to this pin.	
40	~	NC	Reserved for future use. Do not connect to this pin.	
41	VSS	Power	Negative Power Supply 0V	
42	CLK	Digital Input	C-BUS Serial Clock	C-BUS
43	CDATA	Digital Input	C-BUS Command Data	
44	RDATA	Tri-state output	C-BUS Reply Data	
45	CSN	Digital Input	C-BUS Chip Select (bar)	
46	IRQN	Open Drain Digital Output	C-BUS Interrupt Request (bar)	
47	IOVDD	Power	Digital I/O Positive Power Supply 3.3V	
48	DVDD	Power	Digital Positive Power Supply 1.8V	
EXPOSED METAL PAD	SUB	NC	On the Q3 package only, the central metal pad may be connected to Analogue Ground (Avss) or left unconnected. **No other electrical connection is permitted.**	

Note: If the GPIO1 and GPIO2 lines on pins 19 and 20 respectively are to be used as inputs, they must be pulled up to VDD or down to VSS, so that they are not left in a floating state.

Table 1 Pin List and Functions

4 External Components

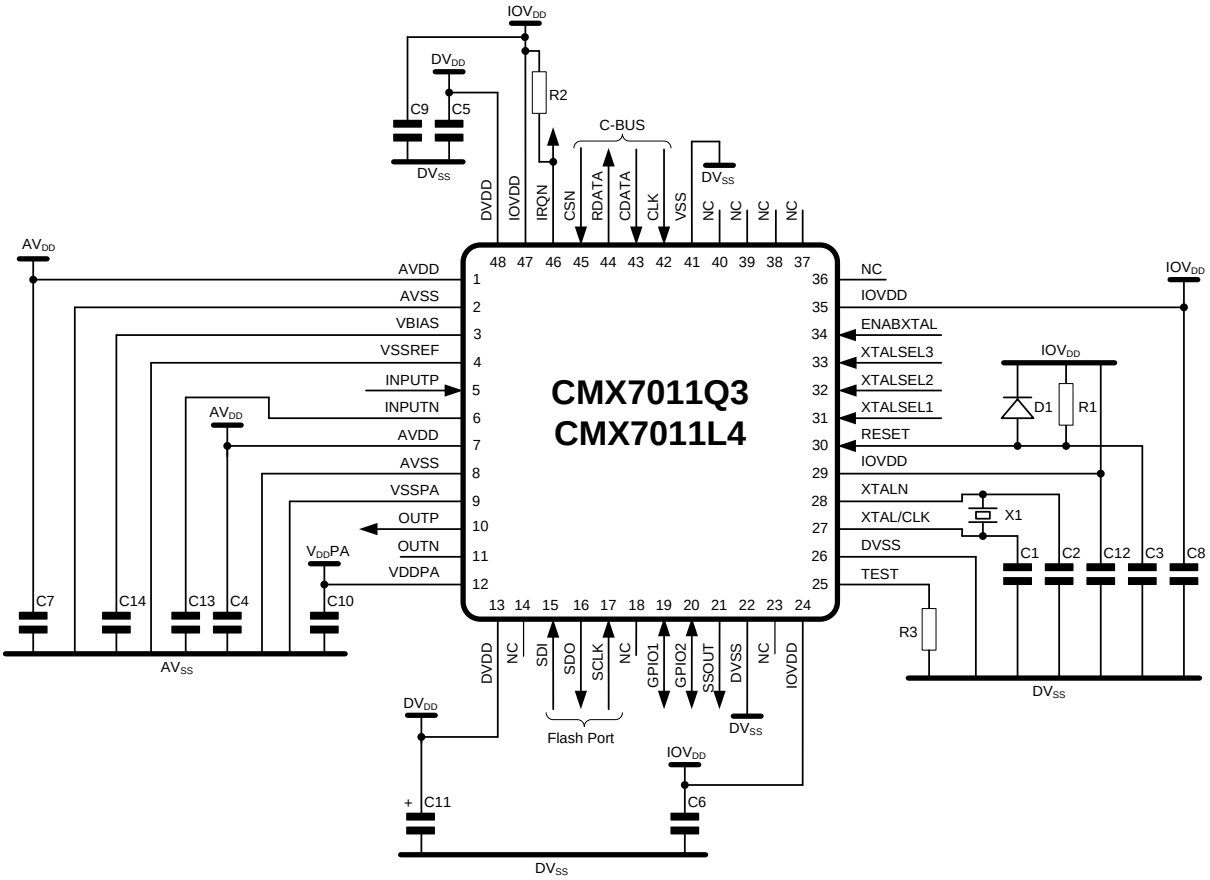


Figure 2 Recommended External Components

C1	22pF	C7	100nF	C13	100nF
C2	22pF	C8	100nF	C14	100nF
C3	1.0µF	C9	100nF	R1	470kΩ
C4	100nF	C10	100nF	R2	100kΩ
C5	1.0µF	C11	1.0µF	R3	100kΩ
C6	100nF	C12	100nF	D1	small signal diode

Table 2 Recommended Component Values

Notes: 1. On the CMX7011, the crystal selection pins (XTALSEL1, XTALSEL2 and XTALSEL3) must be permanently tied to either IOVDD or VSS and not driven from a logic level output of the host microcontroller (see Table 3 for a list of crystal frequencies). For 9.6MHz and 12.0MHz operation, either a crystal or a clock can be used. For all other frequencies, a clock must be injected into the XTALIN pin and the XTALOUT pin must be left unconnected.

2. To use the CMX7011, tie the ENABXTAL pin to IOV_{DD}. If the ENABXTAL pin is connected to VSS it will force the device into a deep powersave mode, where the C-BUS interface and clock input (XTALIN) are disabled and the crystal oscillator is powered down.

3. A single 10µF electrolytic capacitor may be fitted in place of C5 and C11, providing the two V_{DD} pins are connected together on the pcb with an adequate width power supply trace.

4. If the GPIO1 and GPIO2 lines on pins 19 and 20 respectively are to be used as inputs, they must be pulled up to V_{DD} or down to V_{SS}, so that they are not left in a floating state.

Crystal Select Input Pins:			Clock/Crystal Frequency	Clock/Crystal Choice
XTALSEL3	XTALSEL2	XTALSEL1		
0	0	1	9.6MHz	crystal or clock
0	1	0	12.0MHz	crystal or clock
0	1	1	14.4MHz	external clock only
1	0	0	16.8MHz	external clock only
1	0	1	19.2MHz	external clock only
1	1	0	21.6MHz	external clock only
1	1	1	24.0MHz	external clock only

Table 3 Clock/Crystal Selection

5 PCB Layout Guidelines and Power Supply Decoupling

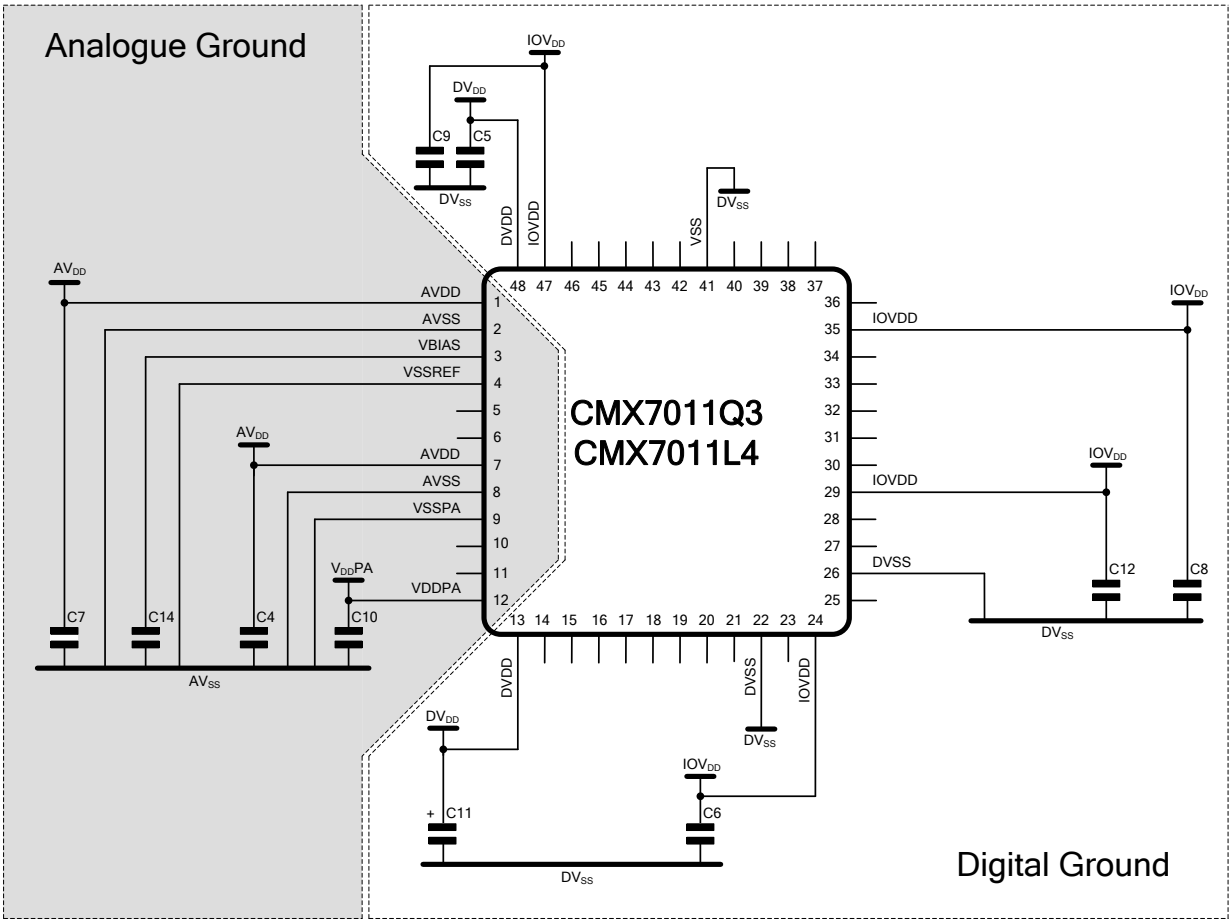


Figure 3 CMX7011 Power Supply and De-coupling

Component values as per Figure 3.

Notes:

It is important to protect the analogue pins from extraneous inband noise and to minimise the impedance between the CMX7011 and the power supply and bias de-coupling capacitors. The de-coupling capacitors C4, C5, C6, C7, C8, C9, C10, C11, C12 and C14 should be as close as possible to the CMX7011. It is therefore recommended that the printed circuit board is laid out with separate ground planes for the AV_{SS} and (digital) V_{SS} supplies in the area of the CMX7011, with provision to make links between them close to the CMX7011. The use of a multi-layer printed circuit board will facilitate the provision of ground planes on separate layers, e.g. for use with VQFN packages.

On the CMX7011, V_{BIAS} is used as an internal reference for detecting and generating the various analogue signals. It must be carefully decoupled, to ensure its integrity, so apart from the decoupling capacitor shown, no other loads should be connected. If V_{BIAS} needs to be used to set an external mid-point reference, it must be buffered with a high input impedance buffer.

6 General Description

The CMX7011, when loaded with Function Image™ 7011FI-1.x, is a half-duplex, secure digital voice processor for use in analogue PMR or wireless secure door access and gate entry systems.

The device can be interfaced directly to the radio's audio path. Programmable input and output gain stages assist with signal level setting for optimum performance. The output gain stage can be adjusted in both coarse and fine increments. The device has one signal input and one signal output and therefore, external switching is required to switch between receive and transmit.

The device uses an embedded RALCWI vocoder and audio-band 2400bps FFSK modem to digitise voice and apply it to an air interface protocol for use in 12.5kHz/25kHz channel analogue PMR radios. The embedded coding scheme provides good tolerance to transmission bit errors and provides real-time voice encryption with programmable 16-bit encryption keys/scramble seeds. An external voice data routing option is also provided to allow voice data to be passed to and from the external host microcontroller.

Instant voice capture is provided to eliminate annoying voice 'clipping' that can occur at the beginning of a voice transmission caused by repeater delays and sub-audio signal decoding in the receiver. Digital voice is buffered in the transmit side and released after a user-programmable period.

Noise gating is included in the Vocoder function, in both transmit and receive operations, to minimise the effects of background noise and improve the overall voice quality.

Voice store and retrieve (VSR) offers storage of a minimum of 20 seconds of vocoded speech in receive mode. The recorded speech can be played back, paused, resumed, or erased so that memory can be reused. VSR also includes a step-back feature which allows the device to step back in discrete steps during playback mode.

Packet data operation allows the device to send packetised data with CRC, FEC and interleaving, as a complete transaction. The only host intervention required is to specify the length of the data packet, transfer it into the device's buffer, and instruct the device to transmit. The CMX7011 performs CRC calculation, FEC coding and interleaving prior to transmission. In receive mode, the device will perform all the de-interleaving, error correction and CRC checking without any host intervention.

Late entry allows a radio receiver to (a) join a call when the synchronisation frame transmitted at the start of a burst was missed and (b) rejoin an ongoing call that temporarily dropped out due to an Rx signal fade. Successful receiver synchronisation must be achieved to recover the audio portion of a call and the synchronisation process must be performed on transmitted sync frames. The Late Entry function retransmits sync frame multiple times during a call to enable a receiver to resynchronise. Each transmitted Late Entry sync frame replaces a voice frame that carries either audible voice (during active speech) or silence (during speech pauses). A Late Entry sync frame that replaces a silent voice frame has minimal impact on received audio. The CMX7011 automatically mitigates the impact of active speech frames replaced by Late Entry sync frames providing this does not occur too frequently. If a suitable pause in active speech does not occur within a maximum time limit a Late Entry sync frame will replace an active speech voice frame so resynchronisation is not delayed too much. Configurable parameters control the late entry process and permit the user to optimise Late Entry operation.

The device utilises CML's proprietary *FirmASIC*® component technology. On-chip sub-systems are configured by a Function Image™ data file that is uploaded during device initialisation and defines the device's function and feature set. New features and enhancements to existing functions may be provided from time to time, expanding the capabilities of the device.

Please refer to the CMX7011 product page on the CML Website for up-to-date product data and currently available Function Images.

7 Detailed Descriptions

7.1 Host Interface

A serial data interface (C-BUS) is used for command, status and data transfers between the CMX7011 and the host microcontroller; this interface is compatible with Microwire/SPI. Interrupt signals notify the host microcontroller when a change in status has occurred and the microcontroller should read the status register across the C-BUS and respond accordingly. Interrupts only occur if the appropriate mask bit has been set.

To minimise activity on the C-BUS interface, optimise response times and ensure reliable data transfers, it is advised that the IRQ facility be used (using the IRQ enable register, $1F). It is permissible for the host to poll the IRQ pin if the host does not support a fully interrupt-driven architecture. This removes the need to continually poll the C-BUS status register ($40) for status changes.

7.1.1 C-BUS Operation

This block provides for the transfer of data and control or status information between the internal registers of the CMX7011 and the host microcontroller, by using the C-BUS serial bus. Each transaction consists of a single Register Address byte sent from the microcontroller, which may be followed by a data word sent from the microcontroller (written into one of the Write-Only Registers), or a data word sent to the microcontroller (read out from one of the Read-Only Registers). All C-BUS data words are a multiple of 8 bits wide, the width depending on the source or destination register. Note that certain C-BUS transactions require only an address byte to be sent from the microcontroller, no data transfer being required. The operation of the C-BUS is illustrated in Figure 4.

Data sent from the microcontroller on the CDATA (command data) line is clocked into the CMX7011 on the rising edge of the CLK input. Data sent from the CMX7011 to the microcontroller on the RDATA (reply data) line is valid when CLK is high. The CSN line must be held low during a data transfer and kept high between transfers. The C-BUS interface is compatible with most common microcontroller serial interfaces and may also be easily implemented with general purpose microcontroller I/O pins controlled by a simple software routine. Figure 4 and Figure 5 give detailed C-BUS timing requirements. Note that, due to internal timing constraints, there may be a delay of up to 60µs between the end of a C-BUS write operation and the device reading the data from its internal register.

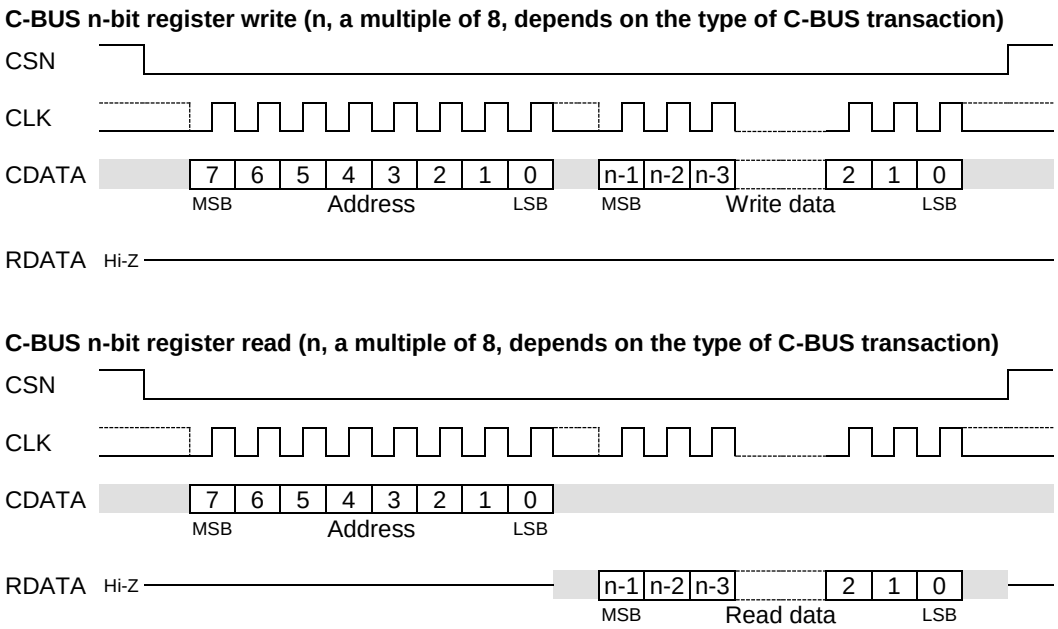


Figure 4 Basic C-BUS Transactions

To increase the data bandwidth between the microcontroller and the CMX7011, certain of the C-BUS read and write registers are capable of data-streaming operation. This allows a single address byte to be followed by the transfer of multiple read or write data words via a FIFO, all within the same C-BUS transaction. This can significantly increase the transfer rate of large data blocks, as shown in Figure 5.

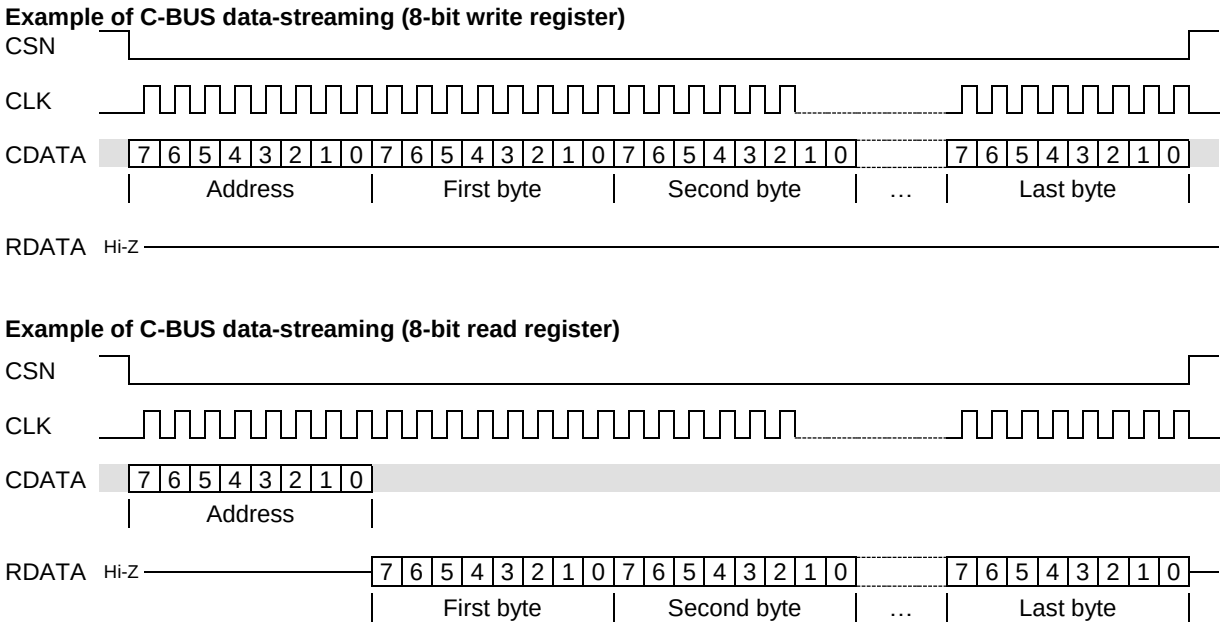


Figure 5 C-BUS Data-Streaming Operation

Notes:

1. For Command byte transfers only the first 8 bits are transferred ($01 = Reset)
2. For single byte data transfers only the first 8 bits of the data are transferred
3. The CDATA and RDATA lines are never active at the same time. The address byte determines the data direction for each C-BUS transfer.
4. The CLK can be high or low at the start and end of each C-BUS transaction.
5. The gaps shown between each byte on the CDATA and RDATA lines in the above diagram are optional, the host may insert gaps or concatenate the data as required.

7.2 Input Stage

Voice is fed in to the CMX7011 via the audio inputs at pins 5 and 6 via a variable analogue input gain stage. This input stage includes up to 22.5dB of switchable gain in 1.5dB steps. The input gain blocks are provided to allow for inputs from different audio sources. Depending on the type of audio source used, users may wish to consider an external low-noise preamplifier prior to the input stage. The gain is controlled by the register $05 - AIG (analogue input gain). In addition to the variable gain there is also 20dB of gain available (microphone amplifier gain) in a single step (also controlled by the analogue input gain register). If the user requires an input gain in the order of 20dB or above, the use of this single gain stage is advised to provide the bulk of the gain. Any additional smaller increments can then be added using the variable gain. Using this approach means that the best noise performance will be achieved.

7.3 Output Stage

The output stage is fed from the outputs of the DAC and consists of a single analogue gain block which is controlled by two registers: The AOG (analogue output gain) $A06 register provides up to 14dB of attenuation and up to 16dB of gain, in 2dB steps. There is also an additional 6dB of loudspeaker gain available in a single step. An alternative method of gain adjustment is available via the FCAOG (fine control analogue output gain) $1B register. FCAOG provides both coarse and fine gain adjustment within a single register. Coarse gain control is similar to AOG with 2dB increments and fine gain control of up to -3dB is provided in 0.2dB increments.

7.4 Peak Level Function

The audio samples may be passed through a peak level measurement function which may be used to determine when the input signal is approaching the threshold at which clipping occurs. The peak level function monitors each 20ms block of speech (160 discrete samples) and will select the sample with the highest value and write the value to the PLEVEL register. This information is useful for setting the value of the input gain stage to obtain the best possible performance of the CMX7011. The function is switched on and off via the PLV register and is controlled by the one of the bits in the CTRL register.

7.5 Noise gate

The programmable noise gate stage that follows peak level detection removes the background noise between speech pauses and can be used to remove noise generated in front-end analogue circuitry or the effects of ambient noise.

Three parameters control the noise gate. An upper threshold level value controls the point at which the gate opens and allows audio to pass. A lower threshold value controls the point at which the gate closes thereby preventing audio to pass. These two parameters together control the hysteresis and prevent 'chattering'. A third parameter controls how many consecutive frames of audio must be below the lower threshold before the gate closes. This 'gate shut delay' prevents the tail end of words (like a trailing 's') from being clipped.

Once the gate shut delay has expired, the gate does not shut abruptly, but closes over a period of 16 frames. Each frame has progressively more attenuation applied, until the frames are silent. This happens in approximately 6dB steps. The diagram below illustrates the difference between a gated and non-gated

signal and clearly shows the improvement in background noise level which is a benefit that this stage brings.

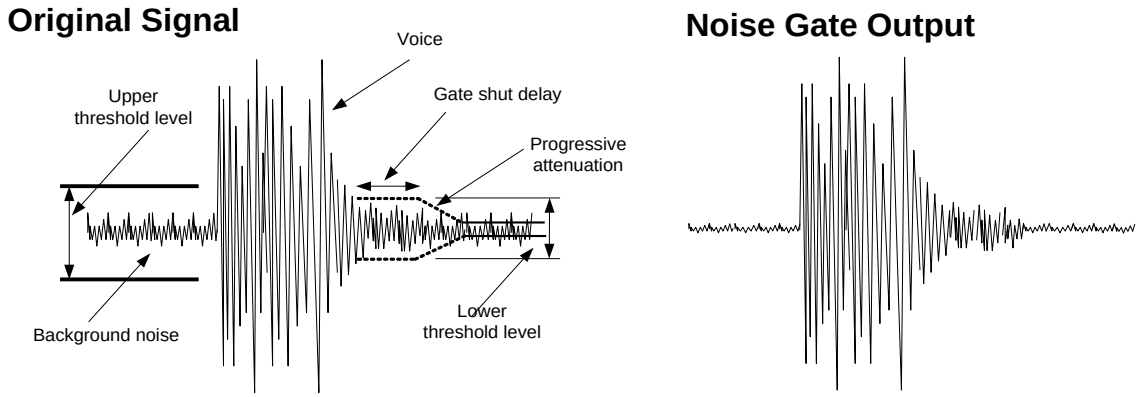


Figure 6 Noise Gate Behaviour

The various parameters of the noise gate such as upper threshold, lower threshold, mute, and gate shut delay are controlled by dedicated C-BUS registers described later.

7.6 Vocoder

The voice encoding/decoding is performed by a low data rate vocoder algorithm which is based on Robust Advanced Low Complexity Waveform Interpolation (RALCWI) technology.

RALCWI technology uses unique proprietary signal decomposition and parameter encoding methods, ensuring high voice quality at high compression ratios. The voice quality of RALCWI-class Vocoders, as estimated by independent listeners, is similar to that provided by standard Vocoders running at bit rates above 4000 bps. The Mean Opinion Score (MOS) of voice quality for this Vocoder is about 3.5-3.6. This value was determined by a paired comparison method, performing listening tests of developed and standard voice Vocoders.

Both input and output stages include a high-order digital channel filter, to constrain the input and output signals to an audio bandwidth of 4kHz. This avoids the necessity of adding external third (or higher) order filters, thus saving external components.

7.7 Voice Store and Retrieve

Following the Vocoder section is the voice store and retrieve sub system, which has the ability to store and play back previously-vocoded speech. Speech is stored, in encoded form, in on-chip RAM. Once stored, it is available for playback until it is either deleted or the device is reset. The maximum amount of memory available will depend on the amount of RAM being used by other operations being carried out by the device. However there will always be a minimum of 20 seconds available specifically for VSR.

Up to eight storage buffers are used to store eight discrete periods of speech and the memory for these buffers is allocated dynamically in 0.8 second (40 frames) blocks as the speech is being stored. The device will indicate when all available memory has been used up by setting a dedicated bit in one of the registers.

All operations within VSR are controlled by one 16-bit write register, one 16-bit read register, the Mode bits of the CTRL register, an interrupt request, and one of the bits in the STATUS register. Commands within the write register are provided for resetting and erasing of the buffers, start, stop and resume for playback mode, start and stop for record mode, and a stepback command which moves the current playback position back, by a specified amount, to a new location. The position of playback at any time is indicated by a playback pointer. This position is saved when playback is stopped so that play can resume from that position. The pointer is moved to a new location when the stepback command is executed.

Other commands are provided to interrogate the amount of free memory space available, the amount of speech stored in a specific buffer, and the current status of the VSR, i.e. record, playback or idle. More detailed information covering the operation of the registers is given in the Configuration Guide.

7.8 Real Time Encryption

Note: throughout the following description, and in the register descriptions in the configuration guide (Section 9), the terms ‘scrambling’ and ‘encryption’ are both used and refer to the same functionality. Similarly, ‘scramble seeds’ and ‘encryption keys’ are used in the same manner.

Real time encryption is implemented with a 16-bit pseudo-random sequence which operates on all data bits after the header frame. The encryption uses start codes (‘seeding’) which means that the sequence will be seeded to start from any value other than zero. System security is improved because only receivers with the same seed can decrypt and decode the transmitted data.

There are 16 possible encryption keys (scramble seeds) and these values are held in an internal table - two of the values cannot be modified (scramble “whitening” or scramble disabled). It is also possible to program new scramble seed values into the table. This is covered in more detail in the C-BUS register descriptions.

7.9 External Data Routing

7.9.1 Transmit

If external data routing is used the vocoder output must be redirected to the host microcontroller. One of the bits in the SCRAMBLE register functions as a switch and this must be first set to external data routing (described in detail in the Configuration Guide section of this document). The seed index can be set to any chosen value. When the device is commanded to transmit, and after each 20ms frame of voice has been encoded, it will supply data, a frame at a time, to the host microcontroller via the C-BUS ODATA (out data) register and its associated FIFO. The host is notified when a frame head is available via the VFA (vocoder frame available) bit of the STATUS register. If IRQ (interrupt request) has been enabled in the IRQENAB register, a C-BUS interrupt will be generated and the host will then read the data. The host will subsequently process the data and, when it has completed processing, will return the frame to the device via the IDATA (in data) register, and its associated FIFO, for onward transmission.

7.9.2 Receive

When the device is set to receive, it will receive a valid frame head from the transmitting device and if the transmitter is using external data routing, the receiving device will automatically switch to external data routing mode. The host can establish that the device is in external data routing mode by reading the bit that functions as an external scrambling switch in the DESCRAMBLE register after having received a valid frame head. If this switch is set to external data routing it indicates that the receiver is expecting the host to read, process and return the frames before they are supplied to the device's vocoder for decoding. Processing of the frames is similar to that described for transmit mode. The device will indicate that a frame is ready to be read when the VFA bit in the STATUS register is set.

The host should return as many frames as it is sent – no more, no less. There are registers provided to indicate data flow problems during development and debugging, for example the FSTAT (frame flow status) register can indicate problems such as input or output FIFO full status or the oversupply/underflow of data to the host. These facilities are described in detail in the User Manual section of this document.

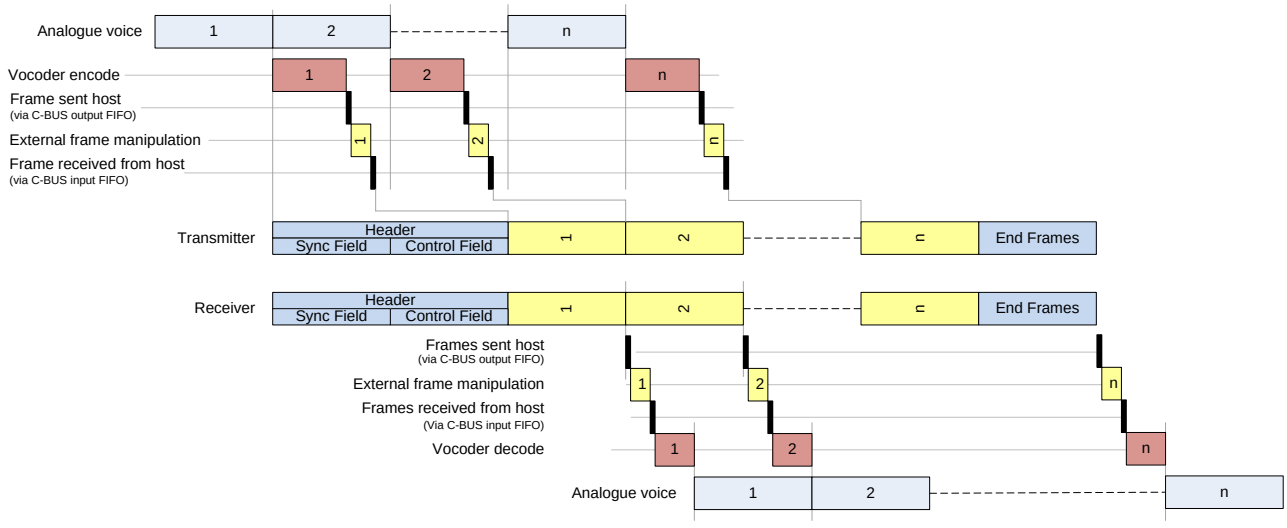


Figure 7 External Data Routing

7.10 Instant Voice Capture

The CMX7011 features instant voice capture which adds a delay between the time when the device starts to encode voice for transmission to the time when it actually transmits the encoded voice. This is useful because in an analogue PMR radio network there are various inherent system delays which can all contribute to an overall time lag before a receiving device starts to respond to a transmission. Examples of such delays are: time taken to decode a CTCSS sub-audio signal, and system delays introduced by repeaters. The PTT buffer allows a user to programme delay times between 0 and 600ms. The delay times are specified in frames, and the function is controlled by the PTTDELAY register described in the C-BUS register section.

The following diagram illustrates how the PTT delay buffer is implemented.

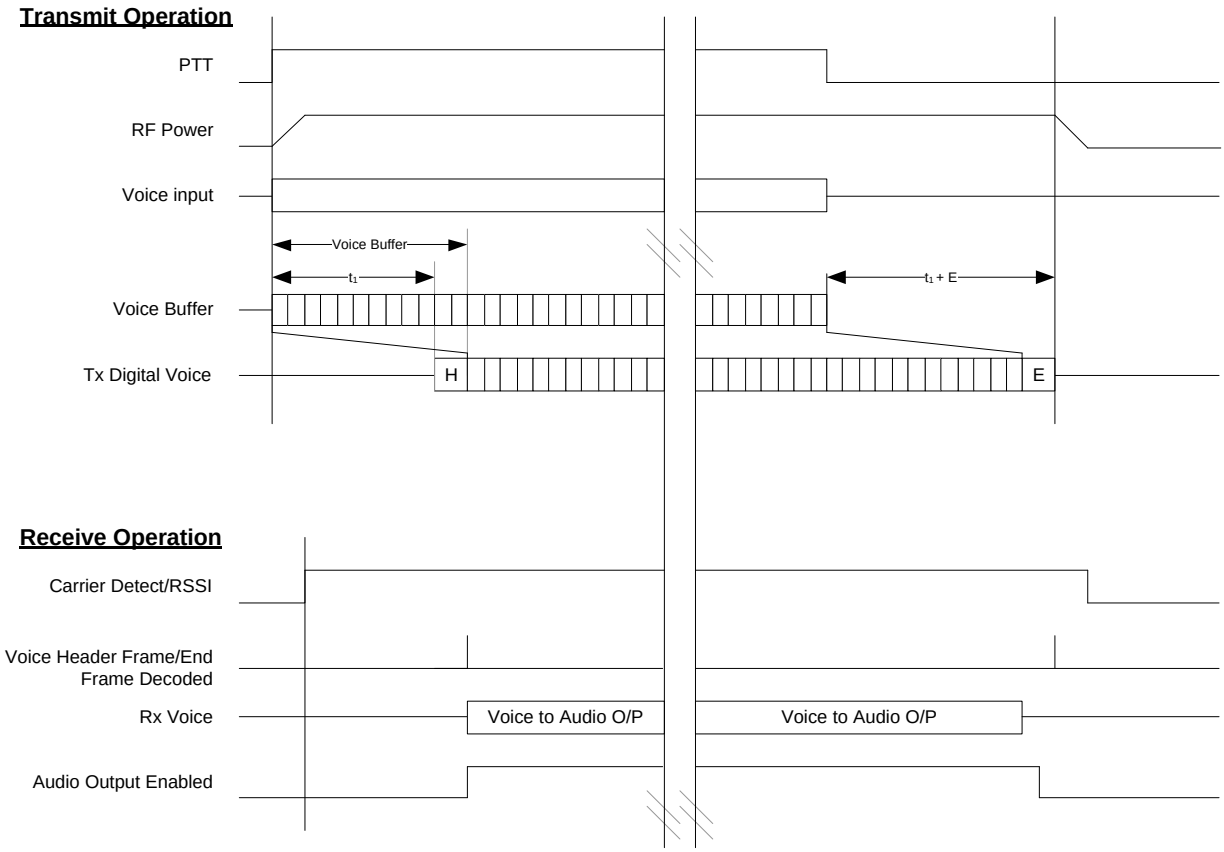


Figure 8 Typical Timing for PTT Delay

In Figure 8 it can be seen that from the time that the PTT button is engaged, there will be a small finite time taken for the RF power to ramp up from zero to full operating power. However, voice input will be captured immediately and vocoded voice data will be buffered in RAM on a frame-by-frame basis. In the example, 12 frames are buffered and this includes the header frame time. Therefore the actual transmission of digital voice is delayed by a period equal to t_1 plus the header frame time. At the end of the transmit operation, following the last frame of buffered voice frames, the actual transmission will continue for a period equal to t_1 plus the end-of-voice (EOV) frames time. The host will then be notified when digital voice transmission has finished.

In receive mode, carrier detect/RSSI may be present, but the audio output will not be enabled until the header frame has been correctly detected. Audio output will continue and will be only be disabled once the final end-of-voice frame has been detected.

7.11 Packet Data Operation

The CMX7011 can send data packets of 0 to a maximum length of 255 bytes, together with a CRC, as one complete transaction. All the host needs to do is to transfer the data into the device, specify its length and then instruct the device to transmit the data. The device will calculate a CRC for the data, split the data up into 4-byte chunks, calculate an FEC for them and interleave the resultant bits for transmission. Each 4 bytes of data is sent as 6 bytes (4 bits of FEC per byte of data).

The receiver will receive a complete packet, de-interleaving the 4-byte chunks, performing any error correction required and then checking the overall CRC without any host intervention. The device will indicate that it has received a complete packet and also report whether or not the CRC is correct. Once the host has been informed, it can read the data from the device, and, optionally, the received CRC.

The device has an internal 260-byte buffer that is used for both transmit and receive. When transmitting, the host must put the required data in the buffer prior to instructing the device to transmit. This is done using the PDATA register ($1D) in conjunction with the streaming input register IDATA ($10). The IDATA register has a 128-byte FIFO behind it, so, up to 128 bytes of message can be sent into the device in one go. Messages of greater than 128 bytes must therefore be written to the device in two parts.

Once the data to be sent has been transferred into the device, the host must indicate how much of it is to be sent by writing the packet length into the TXPL register ($0C) and then command the device to transmit the data by writing the appropriate value to the mode bits of the CTRL register ($11). Before the device transmits the packet, it will calculate a CRC value for the data. If the data length is less that 17 bytes, the CRC will be a 16-bit one otherwise a 32-bit CRC is calculated. The device places the CRC value in the buffer at the end of the data.

The device will indicate that the whole packet has been transmitted by setting the EOT bit in the STATUS register and, if enabled, pull IRQN low.

The receiving device must be placed in the receive mode prior to the data being transmitted. The receiver will first look for the sync word and once found will accept the frame head packet. If this packet is received intact, it will indicate to the receiving device whether the data being transmitted is digital voice data, or packet data. If it is digital voice that is being transmitted, the receiver will start decoding voice. If the transmission is packet data, the receiving device will collect the FEC-protected packets, de-interleave them, apply any error correction required and then place the data in its internal buffer. This will be done until the whole of the data has been received. Once the required amount of data has been collected, the device will calculate the CRC and check it agrees with the CRC that was transmitted. The receiving device will then set the EOT/RSR flag in the status register and set the RSTAT register to indicate that data with a good, or a bad, CRC has been received.

Once the device has indicated that it has received data, the length of the data in bytes may be read from the RXPL register ($2C). The host may then read the data from the buffer using the PDATA register ($1D) in conjunction with the streaming output register ODATA ($30). Like the IDATA register, the ODATA register has a FIFO behind it which allows up to 127 bytes to be read from the buffer in one streaming transaction.

7.12 Late entry

The CMX7011, when used for digital voice, has two modes of operation:

- Digital Voice
- Digital Voice with Late Entry

7.12.1 Digital Voice

In standard digital voice mode it will be impossible for a receiver to start receiving part way through a transmission. This is because the synchronisation frame is sent only once, at the start of the transmission. Thus while in standard digital voice mode a receiver that starts receiving after the start of the transmission will not be able to acquire synchronisation and receive any audio.

7.12.2 Digital Voice with Late Entry

In digital voice with late entry it is possible for a receiver to join a transmission already in progress. In this mode additional re-synchronisation frames are sent during the transmission, allowing the receiver to acquire synchronisation.

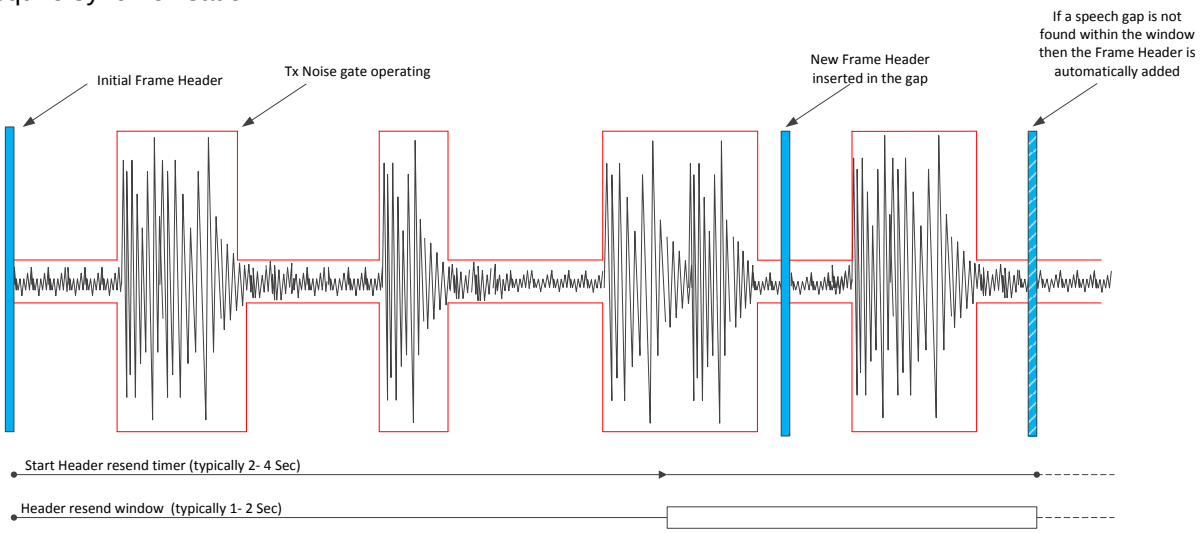


Figure 9 Late Entry Operation

To minimise how often Late Entry synch frames replace active speech voice frames, the device works in conjunction with the noise gate to look for silence that falls below a programmable threshold level and within a programmable time window. The device will then insert additional sync frames within those periods. These are controlled by the LETH ($19) and LEWIN ($18) registers.

To minimise the reduction in digital security the device may be programmed to randomly choose a different scramble index in the scramble seed table each time resynchronisation is performed. This is controlled by bit 4 in the SCRAMBLE ($04) register.

When receiving digital voice with late entry the receiver will know (based on the LEWIN settings) when to expect a new frame sync and will be prepared to accept it, thereby reducing the chance of falsing.

Note: External scrambling is not currently supported when the device operates with late entry.

Control of late entry is via the following registers:

- CTRL ($11) – the switch to turn late entry on or off
- LEWIN ($18) – the late entry time window for resynch frames to be sent
- LETH ($19) – the late entry silence threshold level for generating resynch frames
- DVETH ($1A) – the digital voice error thresholds
- SCRAMBLE ($04) – late entry scramble seed randomising

7.13 Initialisation

On first applying power, three actions have to be performed: the crystal oscillator has to start up (if used), the bias chain has to be powered up, so that the decoupling capacitor (C14) has charged to AV_{DD} / 2, and on-chip digital circuits have to be reset into a known state. The crystal oscillator typically takes much less than 20ms to start up, but the actual time will depend on the ESR of the crystal used. With the components shown in Figure 3, the BIAS pin will take 100ms typically to reach its steady-state value of AV_{DD} / 2. There are two sources of reset:

- pulling the RESETN signal (pin 30) to '0' for at least 200ns, then returning it to '1' (the pin does not have an internal pullup resistor). Note that the device does not have an automatic power-up reset.
- writing to the C-BUS RESET register ($01). This is a 1-byte command which has no data.

A hard reset (taking RESETN low) will also force the ENABXTAL signal low, which disables the clock and powersaves the crystal oscillator. On first applying power, the RESETN pin should be held low until all the power supplies have stabilised, to ensure correct operation of the device. When coming out of a hard reset, the device needs the crystal oscillator to be working, then counts 65,536 clock cycles (= 5.4ms delay with a 12.0MHz clock), then automatically performs a soft reset by writing to the C-BUS RESET register.

A soft reset (writing to the RESET register) will clear all registers to '0', unless noted otherwise – in which case the default settings are restored. The device will be ready to accept C-BUS commands approximately 1.5ms after completion of the soft reset action and will indicate that it is ready by setting bit 15 of the STATUS register ($40) to '1' and also by indicating a C-BUS interrupt request by pulling the IRQN pin low. Note that on reset, the IRQENAB register ($1F) bit 15 will automatically be set to '1', thus enabling the RDY interrupt to activate the IRQN pin.

Connecting the ENABXTAL pin to V_{SS} when the device is operational will force the device into a power-save mode where the C-BUS interface and clock input (XTALIN) are disabled and the crystal oscillator is powered down. However, the BIAS pin and C-BUS registers are not disturbed, so normal operation can be resumed by re-connecting the ENABXTAL pin to IOV_{DD} and waiting for the crystal oscillator to re-start.

The device is now ready to accept the loading of the Function Image™. Please refer to the Application Note in Section 10.1.

7.14 C-BUS register Summary

C-BUS Register Name	C-BUS Address	CMX7011 R/W/CMD	CMX7011 Size (bits)
RESET	$01	CMD	-
SCRAMBLE	$04	W	8
AIG	$05	W	8
AOG	$06	W	8
RADDR	$07	W	8
LADDR	$08	W	8
POWERSAVE	$09	W	8
PTTDELAY	$0A	W	8
EOVCOUNT	$0B	W	8
TXPL	$0C	W	8
SVSREQ	$0E	W	8
IOCTRL	$0F	W	8
IDATA	$10	W	8
CTRL	$11	W	16
LSEED	$12	W	16
FSYNC	$13	W	16
ENGUTH	$14	W	16
ENGLTH	$15	W	16
ENGSDY	$16	W	16
DNGTH	$17	W	16
LEWIN	$18	W	16
LETH	$19	W	16
DVETH	$1A	W	16
FCAOG	$1B	W	16
VSRW	$1C	W	16
PDATA	$1D	W	16
IRQENAB	$1F	W	16
FSTAT	$21	R	8
FTYPE	$22	R	8
FHEADV	$23	R	8
DESCRAMBLE	$24	R	8
ADDRESS	$25	R	8
RSTAT	$26	R	8
RXPL	$2C	R	8
SVCACK	$2E	R	8
IORD	$2F	R	8
ODATA	$30	R	8
PLEVEL	$31	R	16
VSRR	$32	R	16
STATUS	$40	R	16

Table 4 C-BUS Registers

All other C-BUS addresses (including those not listed above) are either reserved for future use or allocated for production testing and must not be accessed in normal operation.

8 Performance Specification

8.1 Electrical Performance

8.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Power Supplies			
IOV_{DD} - V_{SS}	-0.3	4.0	V
DV_{DD} - DV_{SS}	-0.3	2.16	V
AV_{DD} - AV_{SS}	-0.3	4.0	V
$V_{DD}PA$ - $V_{SS}PA$	-0.3	4.0	V
Voltage on any pin to V_{SS}	-0.3	IOV_{DD} + 0.3	V
Current into or out of any pin, except power supply pins, OUTP and OUTN.	-20	+20	mA
Current into or out of power supply pins, OUTP and OUTN.	-120	+120	mA

L4 Package (48-pin LQFP)	**Min.**	**Max.**	**Units**
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	1600	mW
... Derating	–	16.0	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

Q3 Package (48-pin VQFN)	**Min.**	**Max.**	**Units**
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	1750	mW
... Derating	–	17.5	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

8.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Min	Typ	Max.	Units
IOV_{DD} - V_{ss}	3.0	3.3	3.6	V
DV_{DD} - DV_{SS}	1.7	1.8	1.9	V
AV_{DD} - AV_{SS}	3.0	3.3	3.6	V
$V_{DD}PA$ - $V_{SS}PA$	3.0	3.3	3.6	V
Operating Temperature	-40	–	+85	°C
Xtal Frequency	9.6	–	12	MHz
External Clock Frequency (injected into XTALin pin)	9.6	–	24	MHz

8.1.3 Operating Characteristics

Using the recommended components in Figure 2 and for the following conditions unless otherwise specified:

Xtal Freq. = 12.0MHz ±100ppm, $V_{DD}PA = AV_{DD} = IOV_{DD}$ = 3.0V to 3.6V; DV_{DD} = 1.7V to 1.9V; T_{AMB} = 25°C;
all gain settings are 0dB. Figures apply to CMX7011, unless otherwise stated.
Note: Parametric measurements in this section are subject to further characterisation.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD} Total powersaved (ENABXTAL pin connected to VSS)	1	–	50	–	µA
I_{DD} Digital (after Reset, Xtal enabled)	1, 8, 18	–	14.0	–	mA
I_{DD} IODigital (after Reset, Xtal enabled)	1, 9, 18	–	0.5	–	mA
I_{DD} Digital	1, 8, 19	–	17.5	–	mA
Operational Modes					
I_{DD} IODigital	1, 9, 20	–	0.6	–	mA
I_{DD} Analogue PA	1, 9, 20	–	0.7	–	mA
I_{DD} Analogue Vocoder encoding	1, 9, 20	–	6.5	–	mA
I_{DD} Analogue Vocoder decoding	1, 9, 20	–	2.8	–	mA
I_{DD} Digital Vocoder encoding	1, 8	–	33	–	mA
I_{DD} Digital Vocoder decoding	1, 8	–	20.0	–	mA
I_{DD} Analogue	1, 9, 20	–	10	–	mA
Logic Inputs and Outputs					
Input logic '1' level		80%	–	–	IOV_{DD}
Input logic '0' level		–	–	20%	IOV_{DD}
Input leakage current (Vin = 0 to IOV_{DD})	1	–	–	±5	µA
Input capacitance		–	3	–	pF
Output logic '1' level (I_{OH} = 2mA)		90%	–	–	IOV_{DD}
Output logic '0' level (I_{OL} = -5mA)		–	–	10%	IOV_{DD}
"Off" state leakage current (IRQN or RDATA)	1	–	–	±5	µA
Analogue Inputs					
Minimum input sensitivity	21		1		V
Analogue Outputs					
Differential output dc offset (OUT P – OUT N)	3	–	–	±40	mV
XTALin					
Input logic '1' level		70%	–	–	IOV_{DD}
Input logic '0' level		–	–	30%	IOV_{DD}
Input current (Vin = 0 to IOV_{DD})		–	–	±40	µA
XTALout					
Output logic '1' level (I_{OH} = 0.5mA)		90%	–	–	IOV_{DD}
Output logic '0' level (I_{OL} = -1.2mA)		–	–	10%	IOV_{DD}

	Notes	Min.	Typ.	Max.	Units
AC Parameters					
XTALin					
'High' pulse width	4	15	–	–	ns
'Low' pulse width	4	15	–	–	ns
Input impedance (at 12.0MHz)					
Powered-up Resistance		–	150	–	kΩ
Capacitance		–	20	–	pF
Powered-down Resistance		–	300	–	kΩ
Capacitance		–	20	–	pF
Xtal start up time (from powersave)		–	20	–	ms
BIAS					
Start up time (from powersave)		–	100	–	ms
CODEC					
Input Impedance (INPUT P or INPUT N)		–	10	–	kΩ
Input Voltage Range (INPUT P or INPUT N)	10, 17	–	–	20 to 80	%AV_{DD}
Differential Input Voltage (pk to pk)	11, 12, 17	–	–	100	%AV_{DD}
Output Load Impedance (OUT P or OUT N)	6	32	–	–	Ω
Output Voltage Range (OUT P or OUT N)	3, 13, 17	–	–	10 to 90	% V_{DD}PA
Differential Output Voltage (pk to pk)	3, 11, 17	–	–	160	% V_{DD}PA
Differential Output Power	3	–	120	–	mW
Input Gain Setting Accuracy		–	±0.5	–	dB
Output Gain Setting Accuracy		–	±0.5	–	dB
ADC SINAD	5, 14	–	86	–	dB
DAC SINAD	7, 15	–	80	–	dB
Vocoder Performance					
Sample Rate		–	8	–	ks/s
Data Rate		–	2400	–	bps
Lower Frequency Limit (internally bandlimited)		60	–	–	Hz
Upper Frequency Limit (internally bandlimited)		–	–	3900	Hz
Encoder Algorithmic Delay	16	–	–	20	ms
Decoder Algorithmic Delay	16	–	–	12	ms

		Notes	Min.	Typ.	Max.	Units
C-BUS Timings		2				
t_{CSE}	CSN-Enable to Clock-High time		100	–	–	ns
t_{CSH}	Last Clock-High to CSN-High time		100	–	–	ns
t_{LOZ}	Clock-Low to Reply Output enable time		0.0	–	–	ns
t_{HIZ}	CSN-High to Reply Output 3-state time		–	–	1.0	µs
t_{CSOFF}	CSN-High time between transactions		1.0	–	–	µs
t_{NXT}	Inter-Byte time		200	–	–	ns
t_{CK}	Clock-Cycle time		200	–	–	ns
t_{CH}	Serial Clock-High time		100	–	–	ns
t_{CL}	Serial Clock-Low time		100	–	–	ns
t_{CDS}	Command Data Set-Up time		75	–	–	ns
t_{CDH}	Command Data Hold time		25	–	–	ns
t_{RDS}	Reply Data Set-Up time		50	–	–	ns
t_{RDH}	Reply Data Hold time		0	–	–	ns

Notes:

1. T_{AMB} = 25°C, not including any current drawn from the device pins by external circuitry.
2. Maximum 30pF load on each C-BUS or CODEC (SSP) interface line.
3. Measured whilst driving a 32Ω resistive load between OUTP and OUTN pins.
4. Timing for an external input to the XTALin pin.
5. Differential measurement, 10Hz to 4kHz bandwidth.
6. Care should be taken to avoid shorting the OUTP and OUTN pins together, or to any V_{DD} or V_{SS}.
7. Differential measurement, 300Hz to 4kHz bandwidth, no load.
8. 1.8V nominal supply.
9. 3.3V nominal supply.
10. This is the maximum signal range on each pin of the differential input. The common mode voltage can be any voltage within this range but, for optimum dynamic range, it should be set to about AV_{DD} /2. If the inputs are ac coupled, on-chip resistors will set the dc bias of each input to this voltage automatically.
11. This is the maximum differential peak to peak signal amplitude, which corresponds to a signal on each input of (AV_{DD} /2 ± 25% AV_{DD}). Exceeding this can result in increased distortion products.
12. Because the amplitude of speech fluctuates, it is important to set the average speech level such that the level of distortion that results from the occasional overdriving of the inputs is at an acceptable level.
13. This is the maximum voltage on each pin of the differential output, such that the device does not start to introduce significant harmonic distortion.
14. The internal ADC is a sigma-delta type which samples at 2.4MHz. It is important that there is no significant energy close to this frequency or at any of its harmonics, thus avoiding the need for an external low-pass anti-alias filter.
15. The internal DAC is a sigma-delta type which samples at 2.4MHz. It will output energy at this frequency and its harmonics. Should this present a problem, it is suggested that some external filtering be used at the audio outputs.
16. Excludes the 20/40/60/80 ms sample collection period.
17. Internal gain settings are 0dB on input gain for the optimum vocoded level and +6dB on output gain for the optimum vocoded level, subject to further characterisation.
18. ADC or DAC disabled, Vocoder is disabled.
19. ADC or DAC enabled, Vocoder is disabled.
20. ADC or DAC enabled, Vocoder is enabled.
21. Minimum input sensitivity is quoted as peak-to-peak for an Analogue Input Gain value of 0dB.

8.1.3 Operating Characteristics (continued)

Timing Diagrams

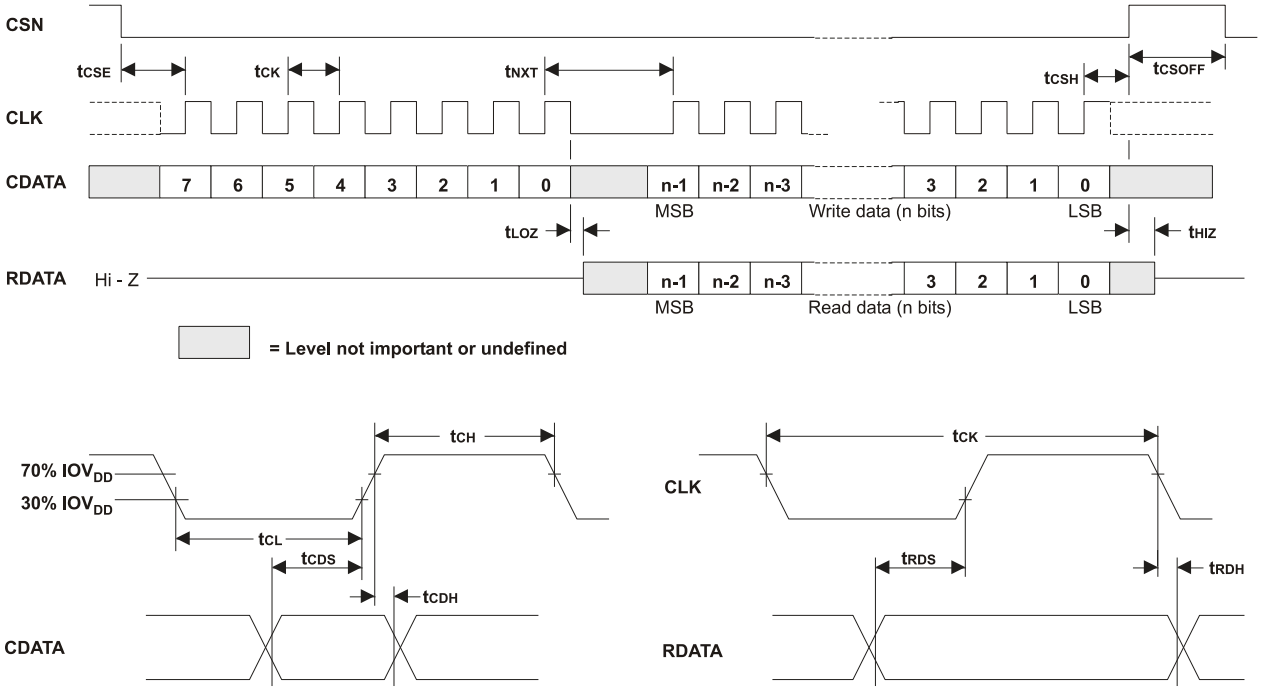
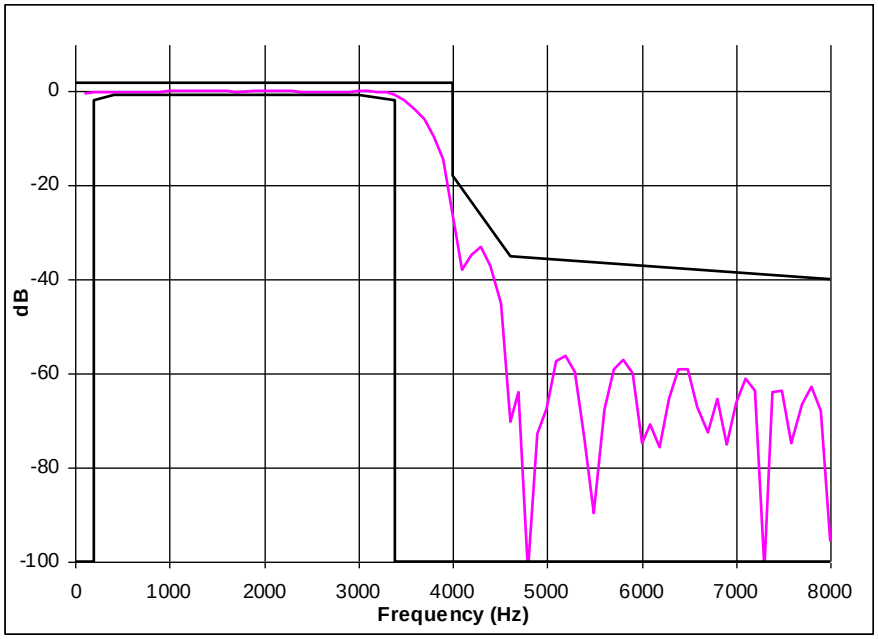


Figure 10 C-BUS Timing



(ADC Input Frequency Vs Fundamental tone power for 750mVrms differential input, normalised to 1kHz)

Figure 11 ADC Input Filter - Typical Response

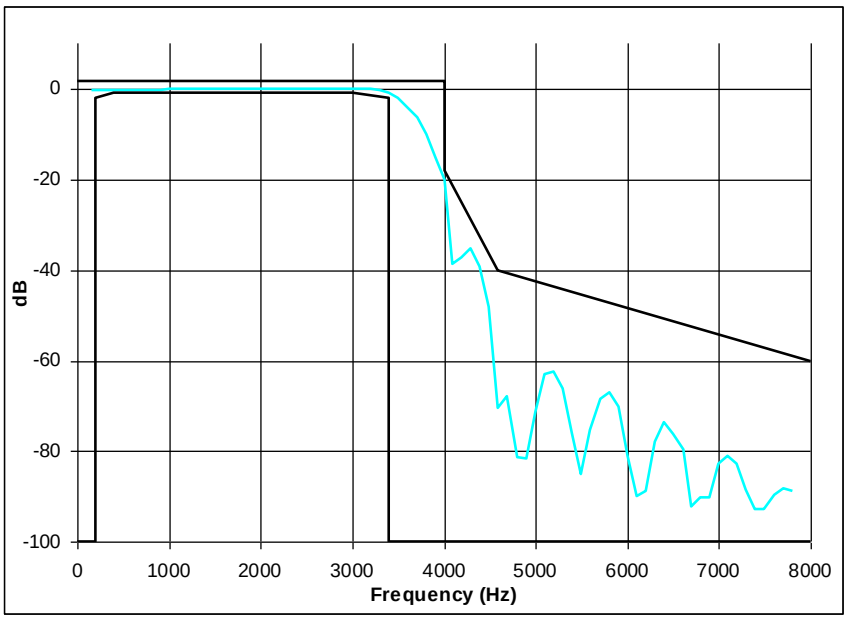
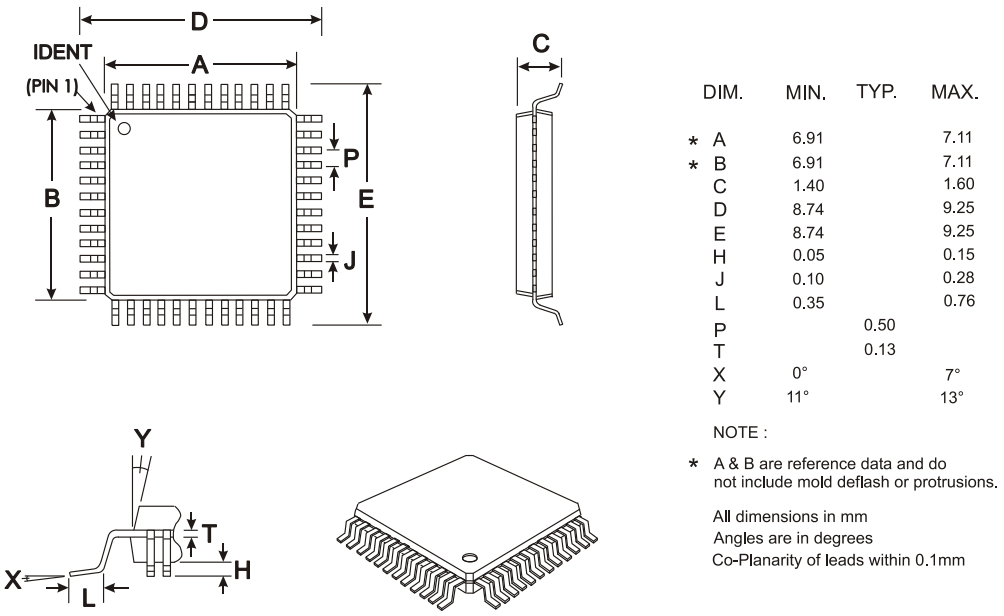


Figure 12 DAC Output Filter - Typical Response

(DAC Output Frequency Vs Measured tone power for 32000 peak sample level differential output, normalised to 1kHz)

8.2 Packaging



DIM.	MIN.	TYP.	MAX.
* A	6.91		7.11
* B	6.91		7.11
C	1.40		1.60
D	8.74		9.25
E	8.74		9.25
H	0.05		0.15
J	0.10		0.28
L	0.35		0.76
P		0.50	
T		0.13	
X	0°		7°
Y	11°		13°

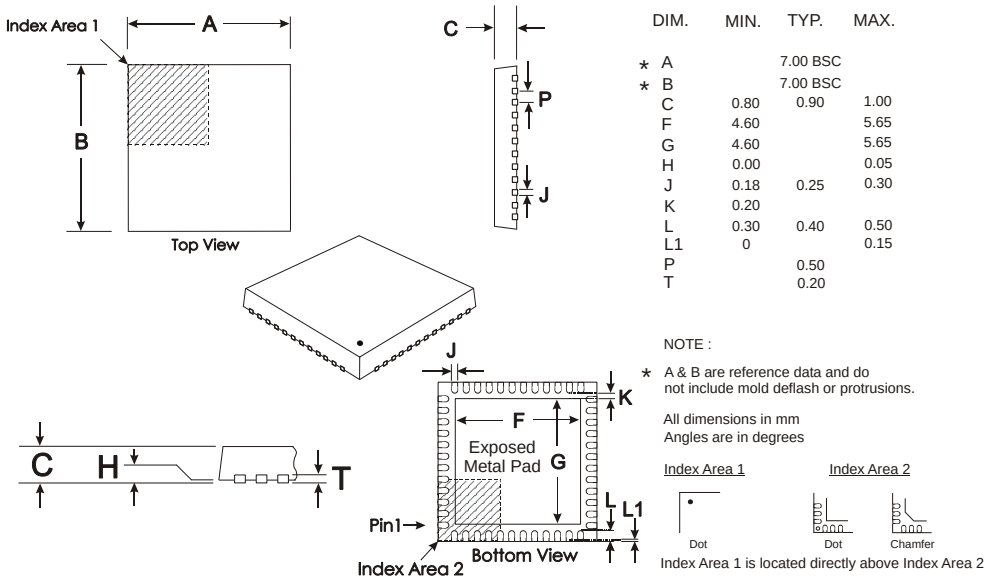
NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees
Co-Planarity of leads within 0.1mm

Figure 13 48-pin LQFP Mechanical Outline (L4)

Order as part no. CMX7011L4



DIM.	MIN.	TYP.	MAX.
* A		7.00 BSC	
* B		7.00 BSC	
C	0.80	0.90	1.00
F	4.60		5.65
G	4.60		5.65
H	0.00		0.05
J	0.18	0.25	0.30
K	0.20		
L	0.30	0.40	0.50
L1	0		0.15
P		0.50	
T		0.20	

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Index Area 1 Index Area 2

Index Area 1 is located directly above Index Area 2

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 14 48-pin VQFN Mechanical Outline (Q3)

Order as part no. CMX7011Q3

As package dimensions may change after publication of this datasheet, it is recommended that you check for the latest Packaging Information from the Datasheets page of the CML website: [http://www.cmlmicro.com/].

Infinite Capabilities . . .
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CML's proprietary *FirmASIC*® component technology reduces cost, time to market and development risk, with increased flexibility for the designer and end application. *FirmASIC*® combines Analogue, Digital, Firmware and Memory technologies in a single silicon platform that can be focused to deliver the right feature mix, performance and price for a target application family. Specific functions of a *FirmASIC*® device are determined by uploading its Function Image™ during device initialization. New Function Images™ may be later provided to supplement and enhance device functions, expanding or modifying end-product features without the need for expensive and time-consuming design changes. *FirmASIC*® devices provide significant time to market and commercial benefits over Custom ASIC, Structured ASIC, FPGA and DSP solutions. They may also be exclusively customised where security or intellectual property issues prevent the use of Application Specific Standard Products (ASSP's).

RALCWI™ Vocoder

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