CML Microcircuits
COMMUNICATION SEMICONDUCTORS

CMX7261
Voice Multi-transcoder

7261FI-2.x – G.723.1 Full Duplex Codec

D/7261_FI-2.x/4 June 2016

DATASHEET

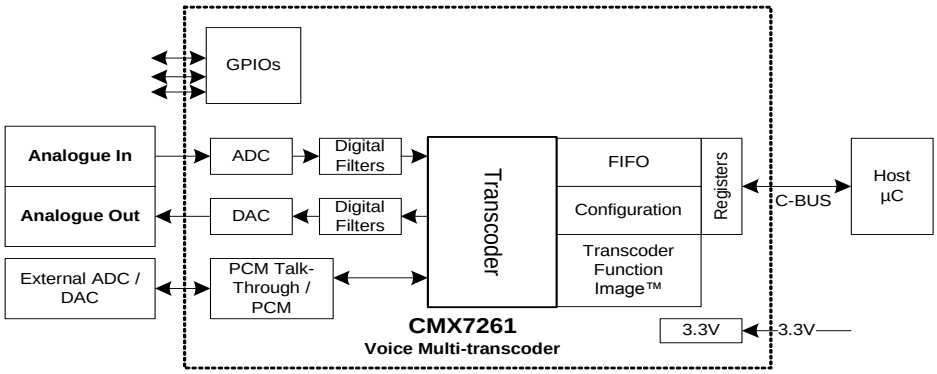
Advance Information

Features

- Half-duplex operation
- Full-duplex operation
- Codec support:
  - G.723.1 codec (5.3kbps / 6.3kbps rates) with Annex A
  - PCM (linear, µ-law, A-law),
- Transcoding support:
  - PCM to G.723.1 and reverse
  - PCM µ/A/linear to PCM µ/A/linear transcoder
- No external DSP or codecs required: simply upload Function Image™ (FI)
- Transcoder routing:
  - Choice of input sources – C-BUS transfer to host, external PCM device/codec, analogue audio input
  - Choice of output sources – C-BUS transfer to host, external PCM device/codec, analogue audio output
- C-BUS host serial interface
  - SPI-like with register addressing
  - Read/Write 128-word FIFOs and data buffers to streamline transfers and relax host service latency
- Auxiliary functions
  - Three GPIOs
  - Analogue input/output gain adjustment
  - Analogue input multiplexer
  - Analogue output multiplexer
- Master/Slave PCM serial interface
  - For external audio CODEC
- Low power 3.3V operation with powersave functions
- Small 64-pin VQFN or LQFP package

Applications

- Half duplex digital radio systems
- Full duplex digital radio systems
- Personal area network voice links
- Privacy-type digital voice communications
- Wireless PBX
- VoIP applications
- Digital Software Defined Radio (SDR)



This document contains:

Datasheet | User Manual

1 Brief Description

The CMX7261 Multi-transcoder IC is a device supporting multiple speech codecs in a single chip. When loaded with FI-2.x the CMX7261 is capable of encoding analogue voice into PCM (linear, µ-law or A-law) or G.723.1 data formats at either 5.3kbps or 6.3kbps. It is capable of decoding PCM or G.723.1 (both rates) back to analogue voice. It can also transcode data between PCM formats and G.723.1.

Input and output signals may be passed through the C-BUS interface, the PCM port or the on-chip converters (ADC/DAC).

The device utilises CML's proprietary FirmASIC® component technology. On-chip sub-systems are configured by a Function Image™ data file that is uploaded during device initialisation and defines the device's function and feature set. The Function Image™ can be loaded automatically from a host µC over the C-BUS serial interface or from an external memory device. The device's functions and features can be enhanced by subsequent Function Image™ releases, facilitating in-the-field upgrades.

The CMX7261 operates from a 3.3V supply and includes selectable powersaving modes. It is available in a 64-VQFN (Q1) or a 64-LQFP (L9) package.

Note that text shown in pale grey indicates features that will be supported in future versions of the device. This Data Sheet is the first part of a two-part document.

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2 History

Version	Changes	Date
4	• Section 8.5.1: Added new Table 5 – G723.1 typical Process Times • Section 9.1.3: Processing delays added to performance characteristics • Section 10.1.33: 'New frame Format' and 'New Frame Data' bits added to IRQ Status register $7E	07/06/16
3	Full public release, minor typographical corrections	14/03/16
2	First public release	01/03/16
1	Advance Draft for first alpha release	21/12/15

Information in this data sheet should not be relied upon for final product design. It is recommended that you check for the latest product datasheet version from the CML website: [www.cmlmicro.com].

3 Block Diagrams

3.1 Half Duplex Transcoder

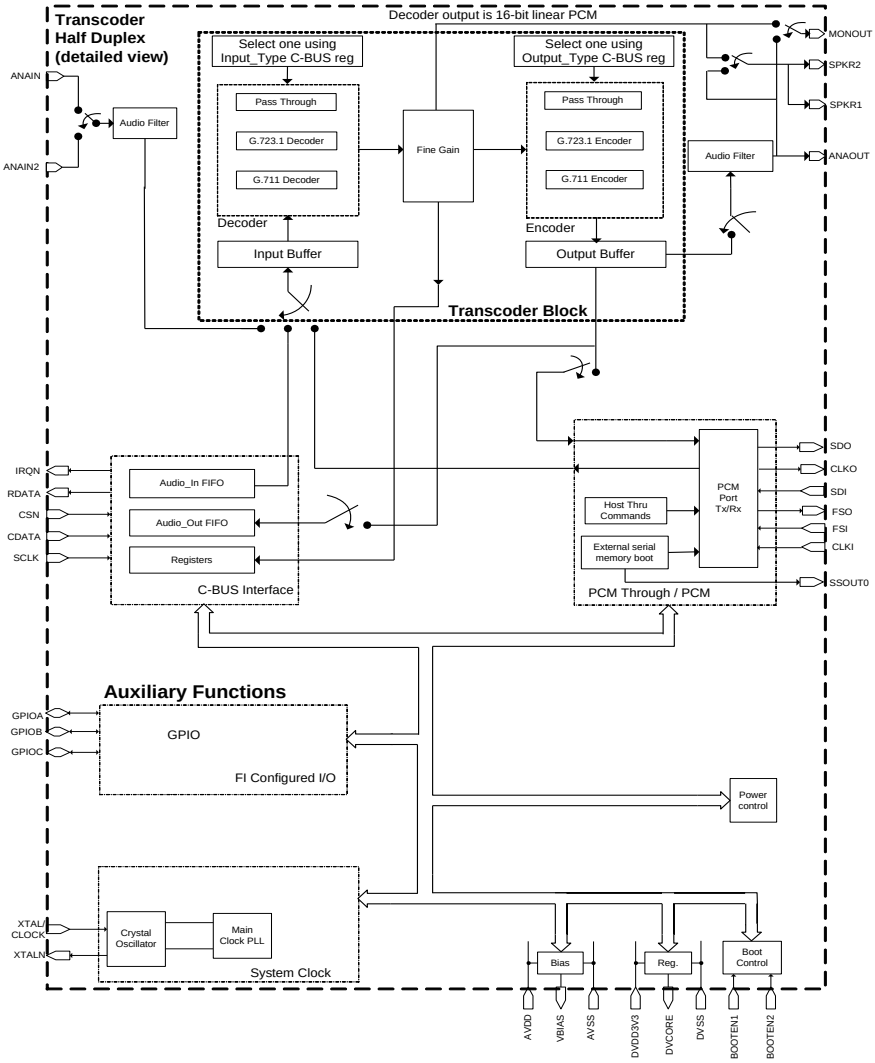


Figure 1 Block Diagram

Figure 1 presents a detailed view of the CMX7261, as used in half duplex mode. In Figure 1, the Decoder and the Encoder together form a 'Transcoder Block'. The CMX7261 contains two such 'Transcoder Blocks' (Figure 1 shows only one of them). In full duplex mode both Transcoder Blocks are used, whereas in half duplex mode only one Transcoder Block is used.

3.2 Full Duplex Transcoder

Figure 2 depicts a block level overview of full duplex transcoding operation. Full duplex operation means that a type of transcoding may be specified on one channel, and the opposite transcoding will then be implemented on a second audio stream. For example, if channel-1 is set to transcode from linear PCM to G.723.1, channel-2 will transcode from G.723.1 to linear PCM.

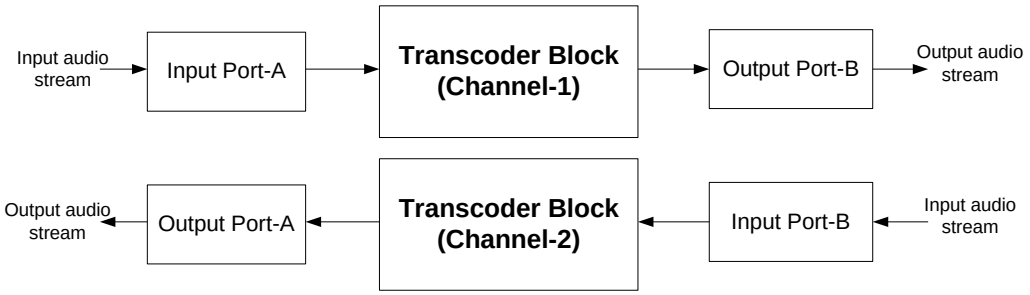


Figure 2 Full Duplex Block Diagram

In full duplex operation, the input and output ports may be specified on one channel and the opposite input and output ports will be used for the second channel.
Table 1 shows the mapping between Input Ports and Output Ports.

Table 1 Input and Output Ports – Full Duplex Mapping

Input Port-A / B	← *maps to* →	Output Port-A / B
Analogue In		Analogue Out
Audio In FIFO (C-BUS In)		Audio Out FIFO (C-BUS Out)
PCM Port In		PCM Port Out

For example, if channel-1 input port is set to Analogue In and its output port set to Audio Out FIFO, then channel-2 input port will be Audio In FIFO and its output port will be Analogue Out.

4 Pin and Signal List

64-pin Q1/L9	Pin		Signal Description
Pin No.	Name	Type	
1	CLKI	IP	PCM: Serial Clock In.
2	BOOTEN1	IP+PD	The combined state of BOOTEN1 and BOOTEN2, upon RESET, determine the Function Image™ load interface.
3	BOOTEN2	IP+PD	The combined state of BOOTEN1 and BOOTEN2, upon RESET, determine the Function Image™ load interface.
4	DVSS	PWR	Negative supply rail (ground) for the digital on-chip circuits.
5	DVDD3V3	PWR	3.3V positive supply rail for the digital on-chip circuits. This pin should be decoupled to DVSS by capacitors mounted close to the supply pins.
6	GPIOA	BI	General Purpose I/O.
7	RESETN	IP	Logic input used to reset the device (active low).
8	GPIOB	BI	General Purpose I/O.
9	GPIOC	BI	General Purpose I/O.
10	DVSS	PWR	Negative supply rail (ground) for the digital on-chip circuits.
11	SPKR2	OP	Single ended output for speaker.
12	AVDD	PWR	Positive 3.3V supply rail for the analogue on-chip circuit. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to AVSS by capacitors mounted close to the device pins.
13	SPKR1VSS	PWR	Negative supply rail (ground) for the on-chip speaker driver circuit.
14	SKPR1P	OP	Low impedance differential driver to the external speaker; ‘P’ is positive, ‘N’ is negative. Together these are referred to as the SPKR1 output.
15	SPKR1N	OP	
16	SPKR1VDD	PWR	Positive supply rail for the on-chip speaker driver circuit. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to SPKR1VSS by capacitors mounted close to the device pin.
17	ANAOUTP	OP	Differential outputs for main audio; ‘P’ is positive, ‘N’ is negative. Together these are referred to as ANAOUT.
18	ANAOUTN	OP	
19	MONOUTP	OP	Differential outputs for monitor audio; ‘P’ is positive, ‘N’ is negative. Together these are referred to as MONOUT.
20	MONOUTN	OP	
21	AVSS	PWR	Negative supply rail (ground) for the analogue on-chip circuits
22	DACREF		DAC reference voltage, connect to AVSS.
23	ANAIN2P	IP	Input (IP) and feedback (FB) connections to single ended audio input 2. Gain and filtering circuitry can be constructed around these pins. Together these are referred to as ANAIN2.

64-pin Q1/L9	Pin		Signal Description
Pin No.	Name	Type	
24	ANAIN2FB	OP	
25	NC	NC	
26	NC	NC	
27	VBIAS	OP	Internally generated bias voltage of approximately AVDD/2. If VBIAS is power saved this pin will present a high impedance to AVDD. This pin must be decoupled to AVSS by a capacitor mounted close to the device pins; no other connections should be made.
28	ANAINP	IP	Differential inputs for main audio; 'P' is positive, 'N' is negative. Together these are referred to as the ANAIN.
29	ANAINN	IP	
30	ADCREF		ADC reference voltage; connect to AVSS.
31	NC	NC	Do not connect.
32	NC	NC	Do not connect.
33	NC	NC	Do not connect.
34	NC	NC	Do not connect.
35	NC	NC	Do not connect.
36	NC	NC	Do not connect.
37	AVDD	PWR	Positive 3.3V supply rail for the analogue on-chip circuit. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to AVSS by capacitors mounted close to the device pins.
38	AVSS	PWR	Negative supply rail (ground) for the analogue on-chip circuits.
39	NC	NC	Do not connect.
40	NC	NC	Do not connect.
41	NC	NC	Do not connect.
42	NC	NC	Do not connect.
43	DVSS	PWR	Negative supply rail (ground) for the digital on-chip circuits.
44	DVCORE1	PWR	Digital core supply, nominally 1.8V. By default this will be supplied by an on-chip regulator, although an option is available to use an external regulator. This pin should be decoupled to DVSS by capacitors mounted close to the device pins and connected with a power supply track to DVCORE2. For details see programming register P1.19 in section 11.1.2 Program Block 1 – Clock Control
45	DVDD3V3	PWR	3.3V positive supply rail for the digital on-chip circuits. This pin should be decoupled to DVSS by capacitors mounted close to the supply pins.
46	NC	NC	Do not connect.
47	DVSS	PWR	Negative supply rail (ground) for the digital on-chip circuits.

64-pin Q1/L9	Pin		Signal Description
Pin No.	Name	Type	
48	DVSS	PWR	Negative supply rail (ground) for the digital on-chip circuits.
49	XTALN	OP	Output of the on-chip xtal oscillator inverter.
50	XTAL/CLOCK	IP	Input to the oscillator inverter from the xtal circuit or external clock source.
51	NC	NC	Do not connect.
52	NC	NC	Do not connect.
53	SCLK	IP	C-BUS serial clock input from the µC.
54	RDATA	TS OP	3-state C-BUS serial data output to the µC. This output is high impedance when not sending data to the µC.
55	CDATA	IP	C-BUS serial data input from the µC.
56	CSN	IP	C-BUS chip select input from the µC.
57	IRQN	OP	'wire-Orable' output for connection to the Interrupt Request input of the µC. This output is pulled down to DVSS when active and is high impedance when inactive. An external pull-up resistor is required.
58	DVCORE2	PWR	Digital core supply, nominally 1.8V. Normally this will be supplied by the on-chip regulator, although an option is available to use an external regulator. This pin should be decoupled to DVSS by capacitors mounted close to the device pins and connected with a power supply track to DVCORE1. For details see programming register P1.19 in section 11.1.2 Program Block 1 – Clock Control.
59	SDO	OP	*While booting FI:* SPI: Master Out Slave In (MOSI). *While running FI:* PCM: Serial Data Out.
60	FSO	OP	PCM: Frame Sync Out.
61	SDI	IP	*While booting FI:* SPI: Master In Slave Out (MISO). *While running FI:* PCM: Serial Data In.
62	SSOUT0	OP	SPI: Slave Select Out 0.
63	CLKO	OP	*While booting FI:* SPI: Serial Clock (SCLK). *While running FI:* PCM: Serial Clock Out.
64	FSI	BI	PCM: Frame Sync In.
EXPOSED METAL PAD	SUBSTRATE	~	On this device, the central metal pad (which is exposed on the Q1 package only) may be electrically unconnected or, alternatively, may be connected to Analogue ground (AV_{SS}). **No other electrical connection is permitted.**

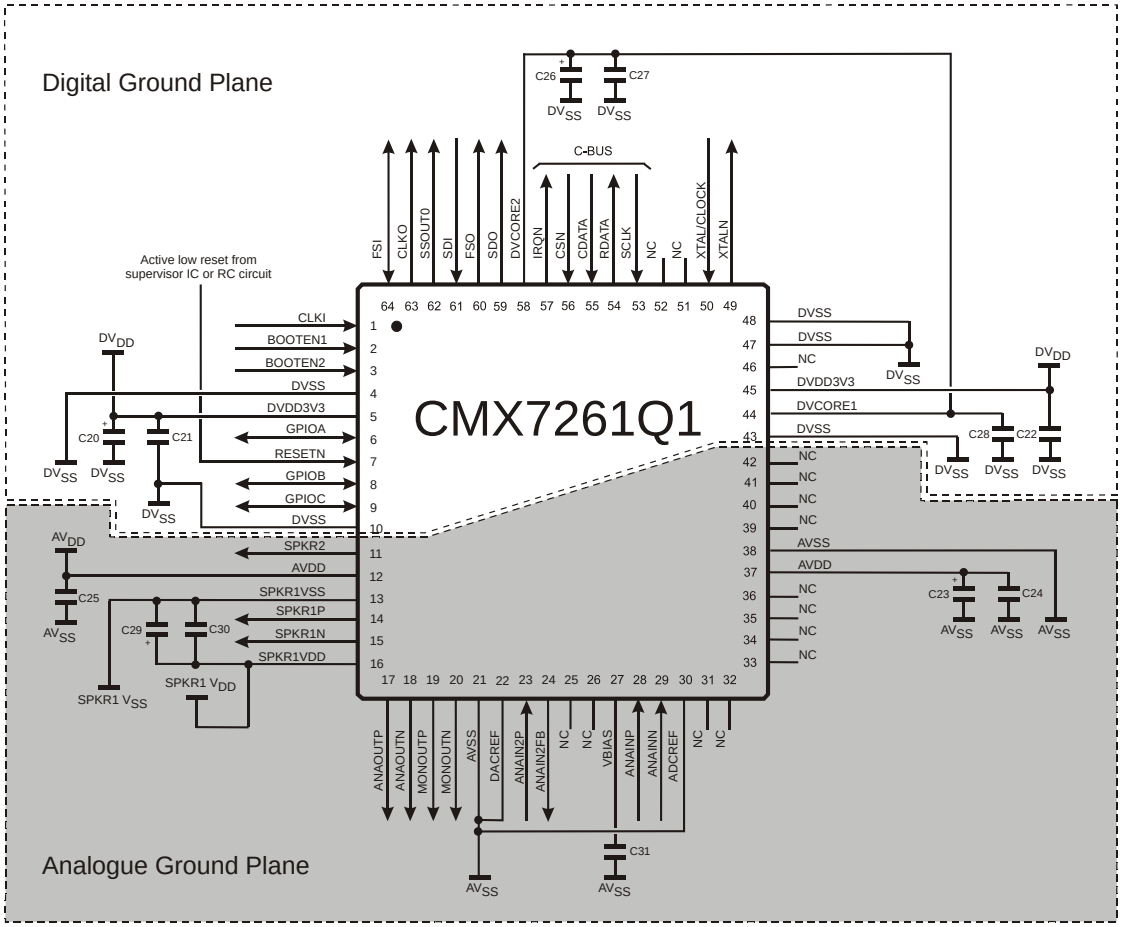
Notes:
IP = Input (+ PU/PD = internal pull-up / pull-down resistor)
OP = Output
BI = Bidirectional
TS OP = 3-state Output
PWR = Power Connection
NC = No Connection - should NOT be connected to any signal

4.1 Signal Definitions

Table 2 Definition of Power Supply and Reference Voltages

Signal Name	Pins	Usage
AV_{DD}	AVDD	Power supply for analogue circuits
DV_{SS}	DVSS	Ground for all digital circuits
V_{BIAS}	VBIAS	Internal analogue reference level, derived from AV_{DD}
DV_{DD3v3}	DVDD3V3	3.3V positive supply rail for the digital on-chip circuits
DV_{CORE}	DVCORE1, DVCORE2	Power for digital core voltage of approximately 1.8V
AV_{SS}	AVSS	Ground for all analogue circuits

5 PCB Layout Guidelines and Power Supply Decoupling



C20	10µF	C26	22µF
C21	10nF	C27	10nF
C22	10nF	C28	10nF
C23	10µF	C29	10µF
C24	10nF	C30	10nF
C25	10nF	C31	100nF

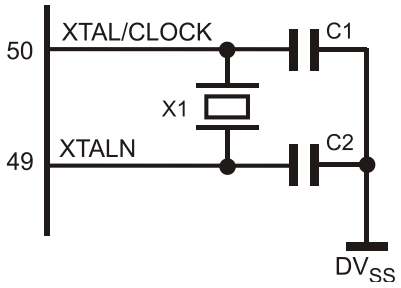
Figure 3 CMX7261 Power Supply and De-coupling

Notes:

To achieve good noise performance, VDD and VBIAS decoupling and protection of the receive path from extraneous in-band signals are very important. It is recommended that the printed circuit board is laid out with a ground plane in the CMX7261 area to provide a low impedance connection between the VSS pins and the VDD and VBIAS decoupling capacitors.

6 External Components

6.1 Xtal Interface



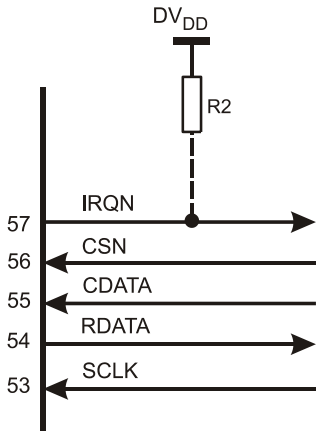
X1 For frequency range see section 9.1.2 Operating Limits
C1 22pF Typical
C2 22pF Typical

Figure 4 Recommended External Components – Xtal Interface

Notes:

- The clock circuit can operate with either a xtal or external clock generator. If using an external clock generator it should be connected to the XTAL/CLOCK pin and the xtal and other components are not required. For external clock generator frequency range see section 9.1.2 Operating Limits. When using an external clock generator the XTAL oscillator circuit may be disabled to save power, see 11.1.2 Program Block 1 – Clock Control for details.
- The tracks between the xtal and the device pins should be as short as possible to achieve maximum stability and best start up performance. It is also important to achieve a low impedance connection between the xtal capacitors and the ground plane.
- The DVSS to the xtal oscillator capacitors C1 and C2 should be of low impedance and preferably be part of the DVSS ground plane to ensure reliable start up. For correct values of capacitors, C1 and C2 refer to the documentation of the xtal used.

6.2 C-BUS Interface



R2 10k - 100kΩ

Figure 5 Recommended External Components – C-BUS Interface

Note: If the IRQN line is connected to other compatible pull-down devices only one pull-up resistor is required on the IRQN node.

6.3 PCM and Serial Port Interface

The CMX7261 can be connected to an external codec using its PCM port. The CMX7261 can also load its FI from an external serial memory. Pins 59, 61 and 63 act as serial port pins whilst booting the FI and as PCM pins whilst the FI is in operation. For more information refer to section 4 Pin and Signal List.

Booting from an external serial memory or connecting with an external codec are both optional.

The schematic in Figure 6 shows the connections required when using an external codec with the CMX7261 as a slave device. The schematic also shows the connections required for interfacing to an external serial memory for FI booting.

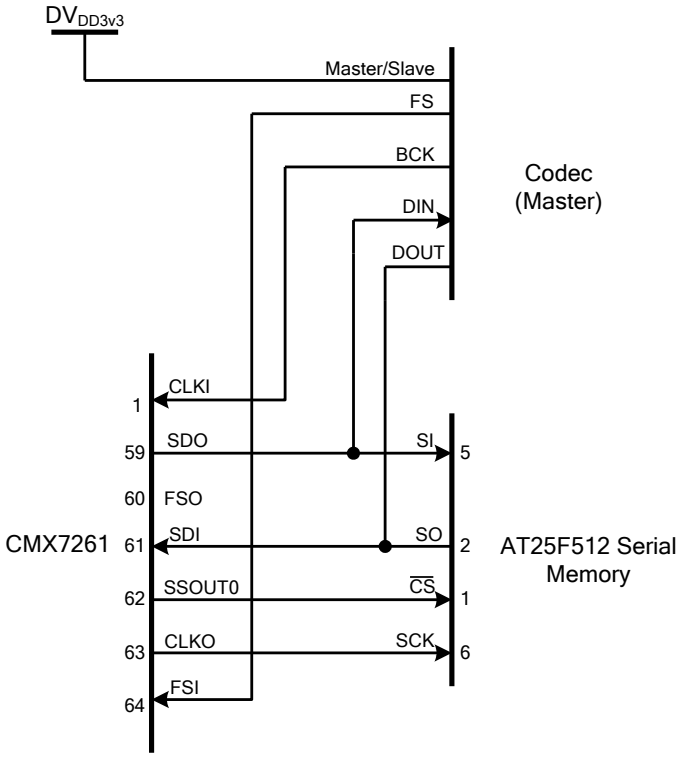


Figure 6 Interfacing the CMX7261 to an External Codec (master) and Serial Memory

The schematic in Figure 7 shows the connections required when using an external codec as a slave device to the CMX7261. The schematic also shows the connections required for interfacing to an external serial memory for FI booting.

Hardware design must ensure that, when booting from external serial memory, no device other than the external serial memory drives the serial port interface pins.

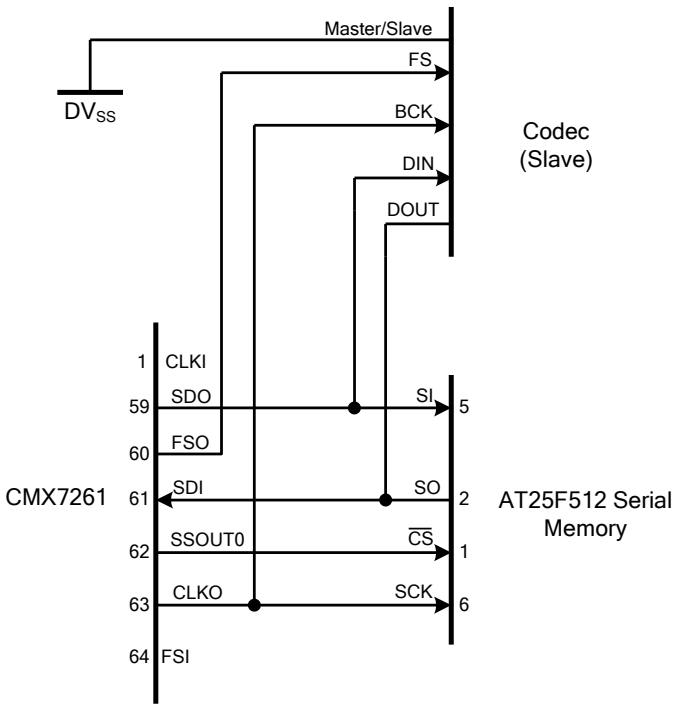


Figure 7 Interfacing the CMX7261 to an External Codec (slave) and Serial Memory

6.4 Audio Output

6.4.1 Audio Output Routing

The CMX7261 has four possible analogue outputs: two differential outputs – ANAOUT and MONOUT, a low impedance differential output speaker driver – SPKR1 and a single ended output – SPKR2, that can drive a headset/earpiece.

The CMX7261's two DACs (Analogue Out DAC and Monitor Out DAC) can output analogue waveforms on any or all of the four outputs (ANAOUT, MONOUT, SPKR1 and SPKR2). Figure 8 Analogue Audio Output Routing, shows the analogue output signal routing and control.

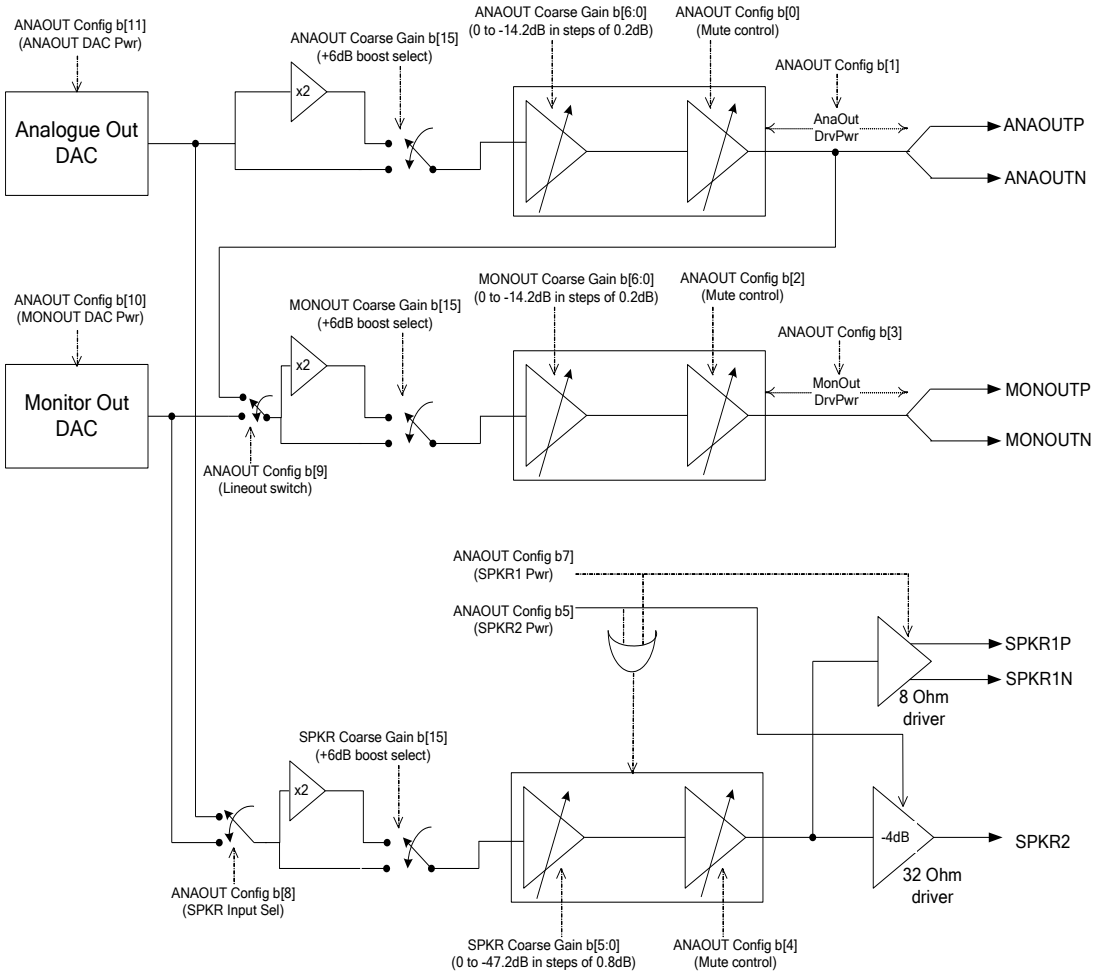


Figure 8 Analogue Audio Output Routing

The registers that control the analogue audio output routing are:

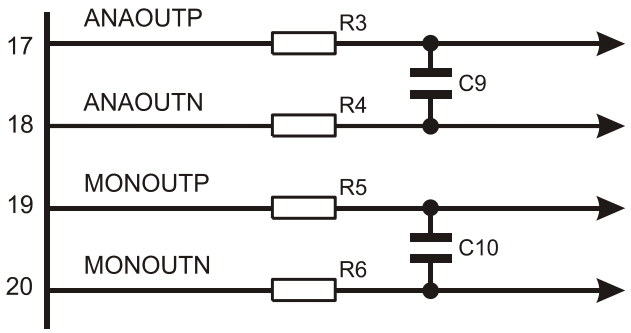
- 10.1.27 ANAOUT Config - $B3 write
- 10.1.28 ANAOUT Coarse Gain - $B4 write
- 10.1.29 MONOUT Coarse Gain - $B5 write
- 10.1.30 SPKR Coarse Gain - $B6 write

NOTE: If lower operating current is desired, it is recommended that unused outputs be powered down using the ANAOUT Config - $B3 write register.

6.4.2 Audio Output Reconstruction Filter

The CMX7261 ANAOUT and MONOUT outputs provide internal reconstruction filtering.
To complete the reconstruction filter, the external RC network shown in
Figure 9 should be used for each of the differential outputs.

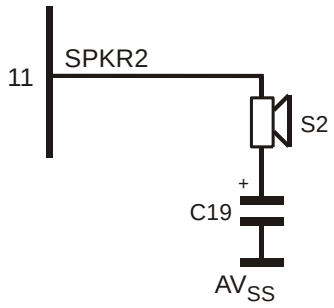
The SPKR1 and SPKR2 outputs do not need any external reconstruction filter.



Bandwidth (kHz)	R3-R6 (kOhms)	C9-C10 (pF)
12.5	22	270

Figure 9 Recommended External Components – ANAOUT/MONOUT Reconstruction Filter

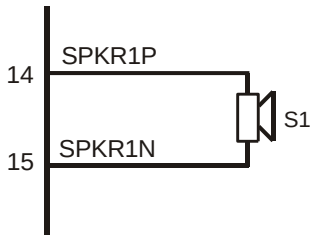
The CMX7261 SPKR2 output provides a single ended audio output that can be used to drive an earpiece or headphone, as shown in Figure 10.



S2 32Ω nominal
C19 100µF

Figure 10 Recommended External Components – Speaker2 Output

The CMX7261 SPKR1 output can be used to drive a speaker as shown in Figure 11.



S1 8Ω nominal

Figure 11 Recommended External Components – Speaker1 Output

Care should be taken to avoid shorting any of the speaker outputs to one another or to VSS or VDD. An external RC filter may be added across SPKR1P and SPKR1N pins if clock noise needs further reduction.

6.5 Audio Input

6.5.1 Audio Input Routing

The CMX7261 has two possible analogue inputs: a differential input – ANAIN and a single ended input – ANAIN2.

The CMX7261's ADC can sample any one of the two analogue inputs. Figure 12 shows the analogue input signal routing and control.

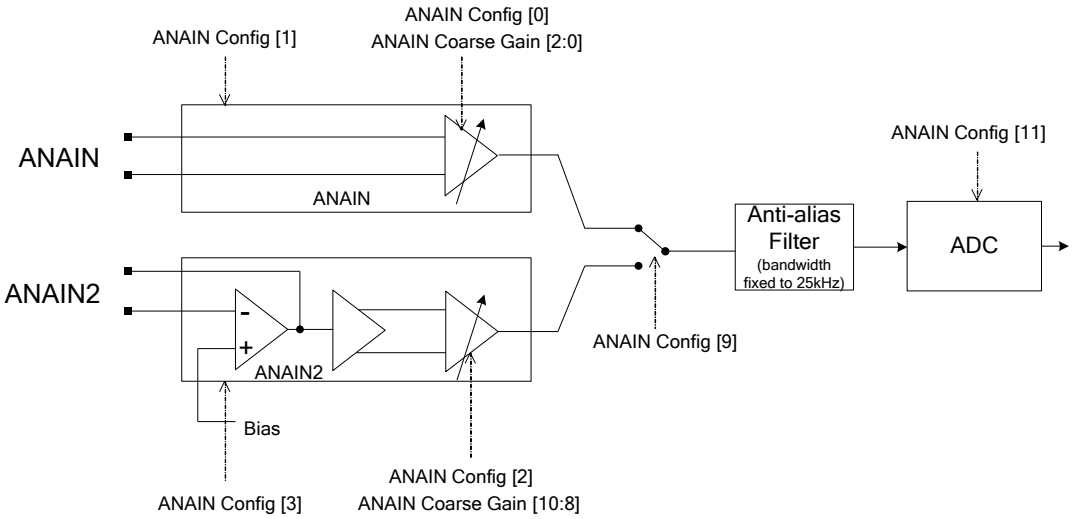


Figure 12 Analogue Audio Input Routing

The registers that control the analogue audio input routing are:

- 10.1.25 ANAIN Config - $B0 write
- 10.1.26 ANAIN Coarse Gain - $B1 write

NOTE: If lower operating current is desired, it is recommended that unused inputs be powered down using the ANAIN Config - $B0 write register.

6.5.2 Differential Audio Input

The device has a 25kHz anti-alias low-pass filter in the analogue audio input path which should be sufficient for most applications; however, if additional filtering is required it can be done at the input to the device. The frequency response (including the anti-alias filter) is shown in Figure 13.

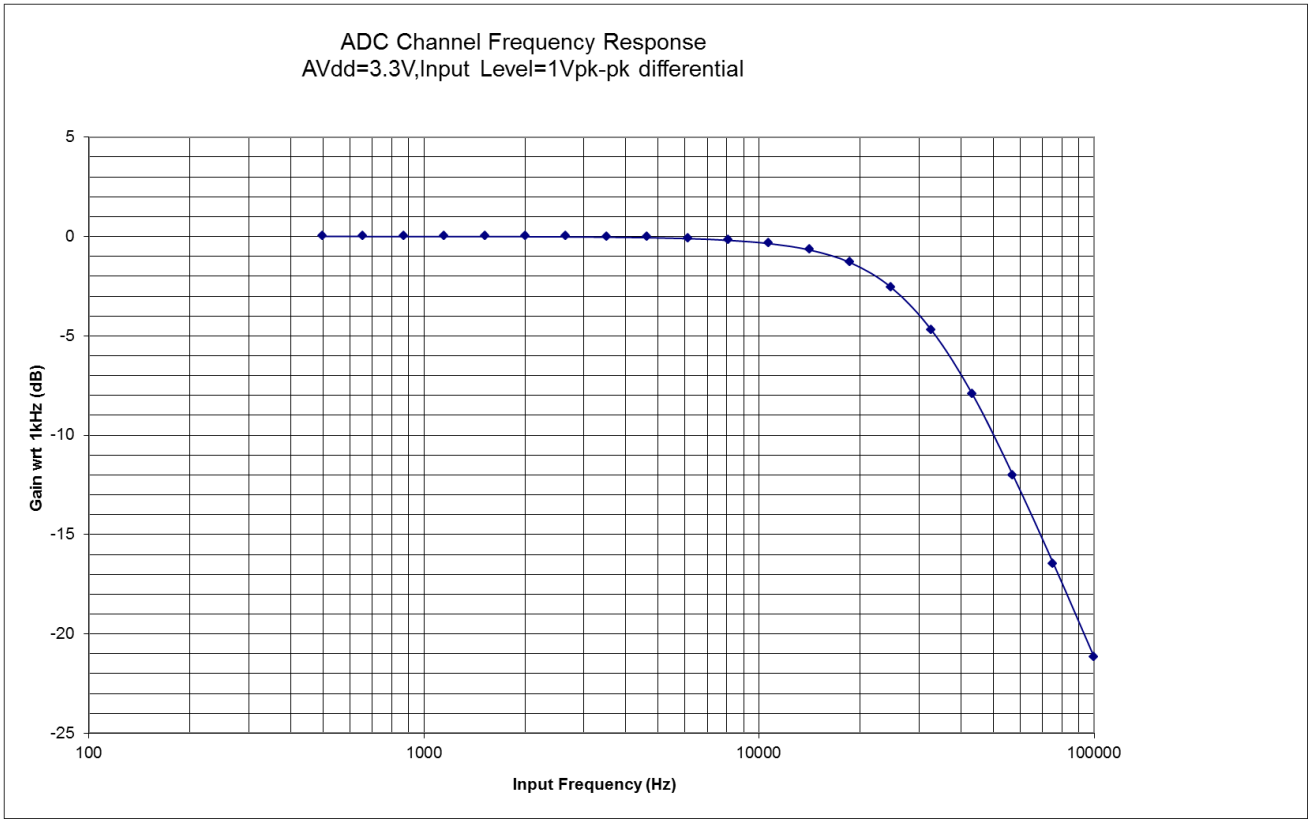
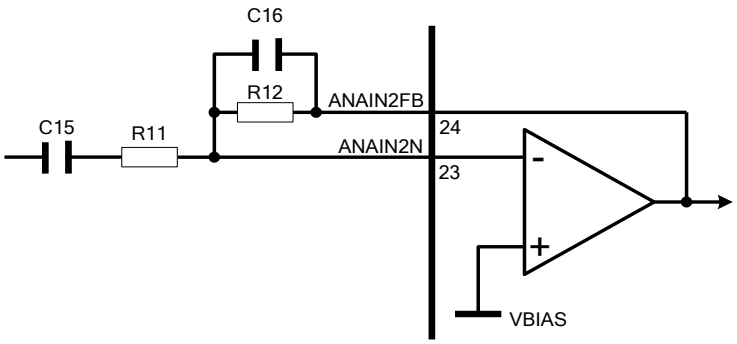


Figure 13 ADC Channel Frequency Response

The input impedance of the ANAIN pins varies with the input gain setting, see section 9.1.3 Operating Characteristics.

6.5.3 Single-Ended Audio Input Interface

A single ended input can be connected to the CMX7261 using the ANAIN2 pins. Gain and filtering circuitry can be constructed around these pins, as shown in Figure 14.



C15	See below
C16	100pF
R11	See below
R12	100kΩ

Figure 14 Recommended External Components – Single-Ended Audio Input Interface

R11 should be selected to provide the required DC gain (assuming C15 is not present) as follows:

$$\left|GAIN_{ANAIN\,2}\right| \quad = \quad 100k\Omega / R11$$

The gain should be such that the resultant output at the pins is within the input signal range.

C15 should be selected to maintain the lower frequency roll-off of the ANAIN2 input as follows:

$$C15 \quad \geq \quad 0.1\mu F \quad \text{x} \quad \left|GAIN_{ANAIN\,2}\right|$$

The high frequency cut off $= \left(\frac{1}{2\pi.R12.C16}\right)$

The low frequency cut off $= \left(\frac{1}{2\pi.R11.C15}\right)$

6.6 GPIO Pins

All GPIO pins are configured as inputs with an internal bus-hold circuit, after the Function Image™ has been loaded. This avoids the need for users to add external termination (pullup/pulldown) resistors onto these inputs. The bus-hold is equivalent to a 75kΩ resistor either pulling up to logic 1 or pulling down to logic 0. As the input is pulled to the opposite logic state by the user, the bus-hold resistor will change, so that it also pulls to the new logic state. The internal bus-hold can be disabled or re-enabled using programming register P1.20 in Program Block 1 – Clock Control.

7 General Description

7.1 CMX7261 Features

The CMX7261 is a multi-transcoder chip that performs encoding and decoding of various vocoder standard formats. When loaded with FI-2 the CMX7261 will encode and decode linear PCM, G.711 (A-law and μ-law) and G.723.1, as well as transcoding between these standards. The CMX7261 can be operated either as a half duplex or as a full duplex transcoder. Full duplex operation means that a type of transcoding may be specified on one channel and the opposite transcoding will then be implemented on a second audio stream.

A flexible power control facility allows the device to be placed in its optimum powersave mode when not actively processing signals.

The device includes a crystal clock generator, with phase locked loop to enable operation from a range of reference xtal frequencies.

Block diagrams of the device are shown in Figure 1.

Encoder Functions:

- Analogue voice to PCM encoding (μ-law or A-law according to G.711 standard).
- Analogue voice to G.723.1 encoding.

Decoder Functions:

- PCM decoding to analogue voice.
- G.723.1 decoding to analogue voice.

Transcoder Functions (Half-Duplex):

- PCM μ / A / linear to G.723.1 transcoding.
- PCM μ / A / linear to PCM μ / A / linear transcoding.

Transcoder Functions (Full-Duplex):

- Two separate audio streams (channel-1, channel-2) are processed simultaneously.
- Channel-1 may process audio using a Decoder, Encoder or Transcoder function.
- Channel-2 will process audio in the reverse manner to channel-1. For example, if channel-1 is configured to transcode from linear PCM to G.723.1, channel-2 will transcode from G.723.1 to linear PCM.

Interface:

- Optimised C-BUS (4-wire, high speed synchronous serial command/data bus) interface to host for control and data transfer, including streaming C-BUS for efficient data transfer.
- Input data can come through the analogue audio input or, C-BUS or from an external PCM device connected to CMX7261's PCM port.
- Output data can be sent to the analogue audio output or, C-BUS or, to an external PCM device connected to CMX7261's PCM port.
- Open drain IRQ to host.
- Three GPIO pins.
- Serial memory or C-BUS (host) boot mode.

7.2 Signal Interfaces

In half duplex mode the transcoder output can be sent to one, any two, or all of the three possible output ports – C-BUS (for transfer to host controller), PCM (for transfer to external DAC) or analogue audio output. In full duplex mode a single output must be selected. The input to the transcoder must come from one of the three input ports – C-BUS (input data from the host controller), PCM (from the external ADC) or analogue audio input.

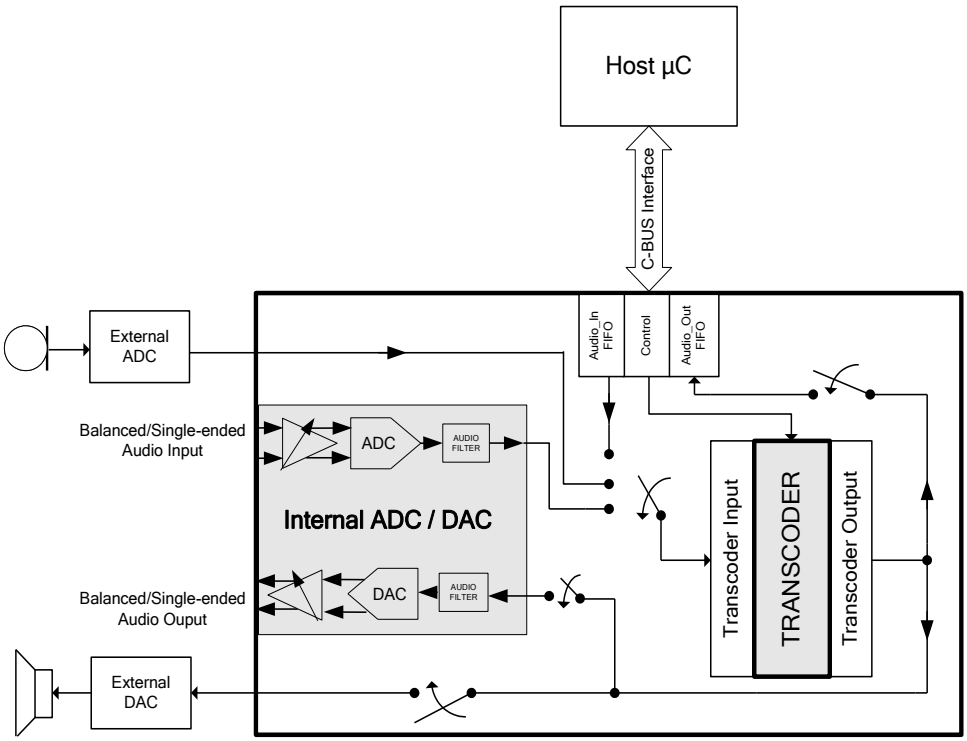


Figure 15 CMX7261 Inputs and Outputs

8 Detailed Descriptions

8.1 Xtal Frequency

The CMX7261 is designed to work with a xtal or an external frequency oscillator within the ranges specified in section 9.1.3. Programming registers P1.0-P1.6 in Program Block 1 – Clock Control (see User Manual) must be loaded with the correct values to ensure that the device will work to specification with the user selected clock frequency. A table of configuration values can be found in Table 8 for a range of Xtal or external oscillator frequencies.

8.2 Host Interface

A serial data interface (C-BUS) is used for command, status and data transfers between the CMX7261 and the host µC; this interface is compatible with Microwire™, SPI™ and other similar interfaces. Interrupt signals notify the host µC when a change in status has occurred; the µC should read the Status register across the C-BUS and respond accordingly. Interrupts only occur if the appropriate mask bit has been set, see Interrupt Operation.

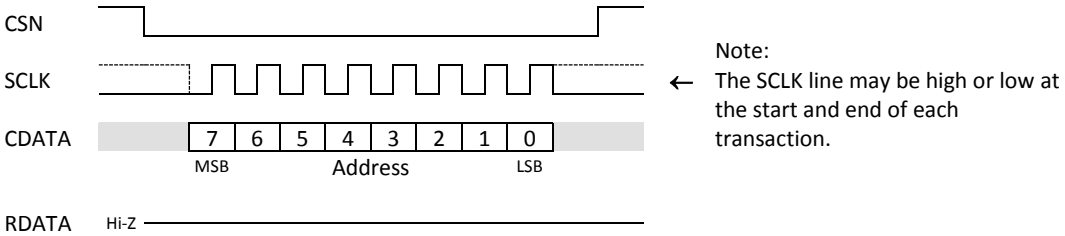
8.2.1 C-BUS Operation

This block provides for the transfer of data and control or status information between the CMX7261 internal registers and the host µC over the C-BUS serial bus. Single register transactions consist of a single Register Address byte sent from the µC, which may be followed by a data word sent from the µC to be written into one of the CMX7261's Write Only Registers, or a data word read out from one of the CMX7261's Read Only Registers. Streaming C-BUS transactions consist of a single Register Address byte followed by many data bytes being written to or read from the CMX7261. All C-BUS data words are a multiple of 8 bits wide, the width depending on the source or destination register. Note that certain C-BUS transactions require only an address byte to be sent from the µC, no data transfer being required. The operation of the C-BUS is illustrated in Figure 16.

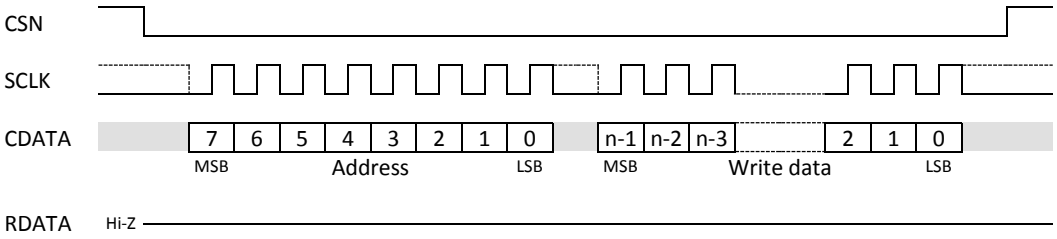
Data sent from the µC on the CDATA (command data) line is clocked into the CMX7261 on the rising edge of the SCLK input. Data sent from the CMX7261 to the µC on the RDATA (reply data) line is valid when SCLK is high. The CSN line must be held low during a data transfer and kept high between transfers. The C-BUS interface is compatible with most common µC serial interfaces and may also be easily implemented with general purpose µC I/O pins controlled by a simple software routine. Section 9.1.5 (C-BUS Timing) gives detailed C-BUS timing requirements.

Note that, due to internal timing constraints, there may be a delay of up to 60µs between the end of a C-BUS write operation and the device reading the data from its internal register.

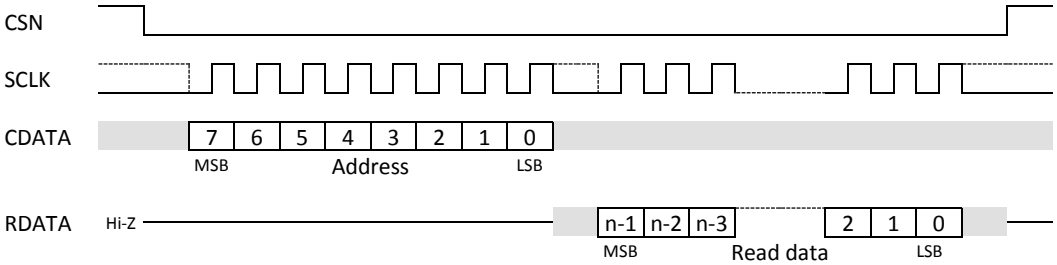
C-BUS single byte command (no data)



C-BUS n-bit register write



C-BUS n-bit register read



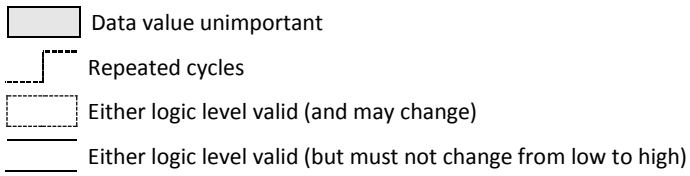
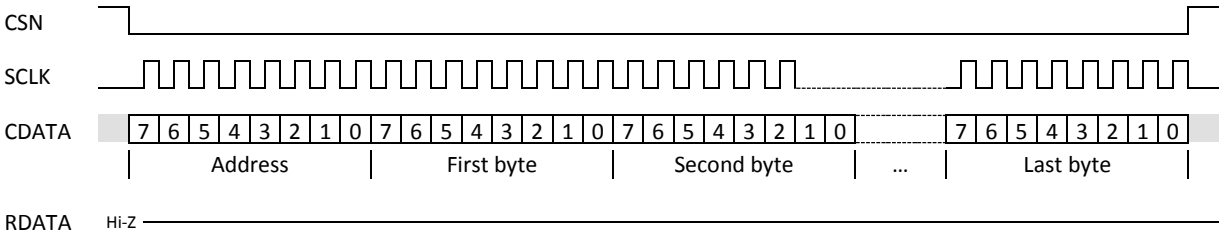


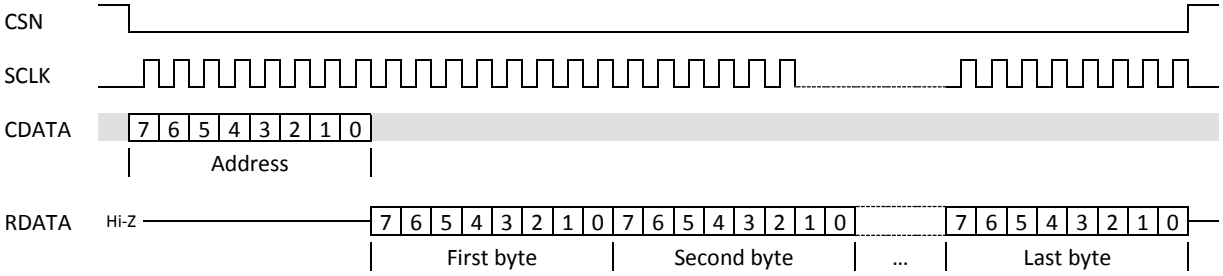
Figure 16 Basic C-BUS Transactions

To increase the data bandwidth between the µC and CMX7261, certain of the C-BUS read and write registers are capable of data-streaming operation. This allows a single address byte to be followed by the transfer of multiple read or write data words, all within the same C-BUS transaction. This can significantly increase the transfer rate of large data blocks, as shown in Figure 17.

Example of C-BUS data-streaming (8-bit write register)



Example of C-BUS data-streaming (8-bit read register)



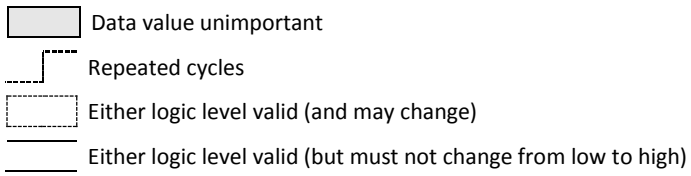


Figure 17 C-BUS Data-Streaming Operation

Notes:

1. For Command byte transfers only the first 8 bits are transferred ($01 = Reset)
2. For single byte data transfers only the first 8 bits of the data are transferred
3. The CDATA and RDATA lines are never active at the same time. The Address byte determines the data direction for each C-BUS transfer.
4. The SCLK can be high or low at the start and end of each C-BUS transaction
5. The gaps shown between each byte on the CDATA and RDATA lines in the above diagram are optional; the host may insert gaps or concatenate the data as required.

8.3 Function Image™ Loading

The Function Image™ (FI), which defines the operational capabilities of the device, may be obtained from the CML Technical Portal, following registration. This is in the form of a 'C' header file, which can be included into the host controller software or programmed into an external serial memory. The Function ImageTM size can never exceed 128kbytes, although a typical FI will be considerably less than this. Note that the BOOTEN1, 2 pins are only read at power-on, when the RESETN pin goes high, or following a C-BUS General Reset, and must remain stable throughout the FI loading process. Once the FI load has completed, the BOOTEN1, 2 pins are ignored by the CMX7261 until the next power-up or Reset.

The BOOTEN 1, 2 pins are both fitted with internal low current pull-up devices.
For serial memory load operation, BOOTEN2 should be pulled low by connecting it to DVss either directly or via a 47k resistor (seeTable 3).
Whilst booting, the boot loader will return the checksum of each block loaded in the C-BUS Audio Out FIFO. The checksums can be verified against the published values to ensure that the FI has loaded correctly.
Once the FI has been loaded, the CMX7261 performs these actions:

(1) The product identification code is reported in the C-BUS Audio Out FIFO
(2) The FI version code is reported in C-BUS Audio Out FIFO.

Table 3 BOOTEN Pin States

	BOOTEN2	BOOTEN1
C-BUS host load	1	1
Reserved	1	0
Serial Memory load	0	1
Reserved	0	0

8.3.1 FI Loading from Host Controller

The FI can be included into the host controller software build and downloaded into the CMX7261 at power-up over the C-BUS interface, using the Audio In FIFO. For Function Image™ load, the FIFO accepts raw 16-bit Function Image™ data (using the Audio In FIFO data word - $49 write register), there is no need for distinction between control and data fields. The BOOTEN 1, 2 pins must be set to the C-BUS load configuration, the CMX7261 powered or Reset, and then data can then be sent directly over the C-BUS to the CMX7261.

If the host detects a brownout, the BOOTEN 1, 2 pins should be set to re-load the FI. A General Reset should then be issued or the RESETN pin used to reset the CMX7261 and the appropriate FI load procedure followed.

Streaming C-BUS may be used to load the Audio In FIFO Data8 - $48 write register with the Function Image™, and the Audio In FIFO Level - $4B read register used to ensure that the FIFO is not allowed to overflow during the load process.

The download time is limited by the clock frequency of the C-BUS; with a 5MHz SCLK it should take less than 250ms to complete even when loading the largest possible Function Image™.

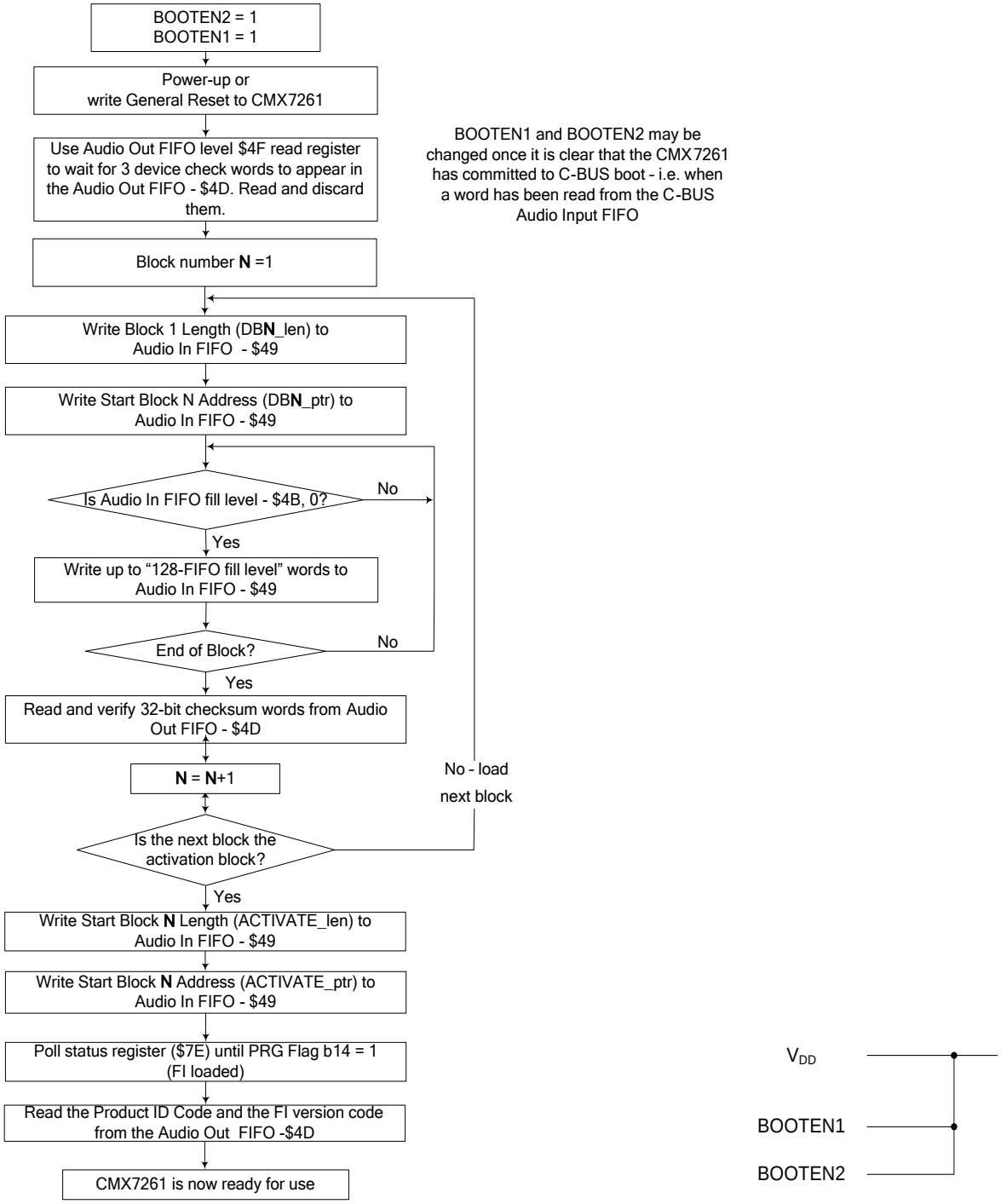


Figure 18 FI Loading from Host

8.3.2 FI Loading from Serial Memory

The FI must be converted into a format for the serial memory programmer (normally Intel Hex) and loaded into the serial memory by either the host or an external programmer. The serial memory should contain the same data stream as written to the Audio In FIFO shown in Figure 18. The most significant byte of each 16-bit word should be stored first in serial memory.

The serial memory should be interfaced to the CMX7261 using SSOUT0 as the chip select and PCM port pins, which act as an SPI port whilst booting (refer section 4 Pin and Signal List). Section 6.3 PCM and Serial Port Interface, shows the connections required for interfacing the AT25F512 Serial Flash memory with CMX7261.

The CMX7261 needs to have the BOOTEN pins set to serial memory load, and then on power-on, following the RESETN pin becoming high, or following a C-BUS General Reset, the CMX7261 will automatically load the data from the serial memory without intervention from the host controller.

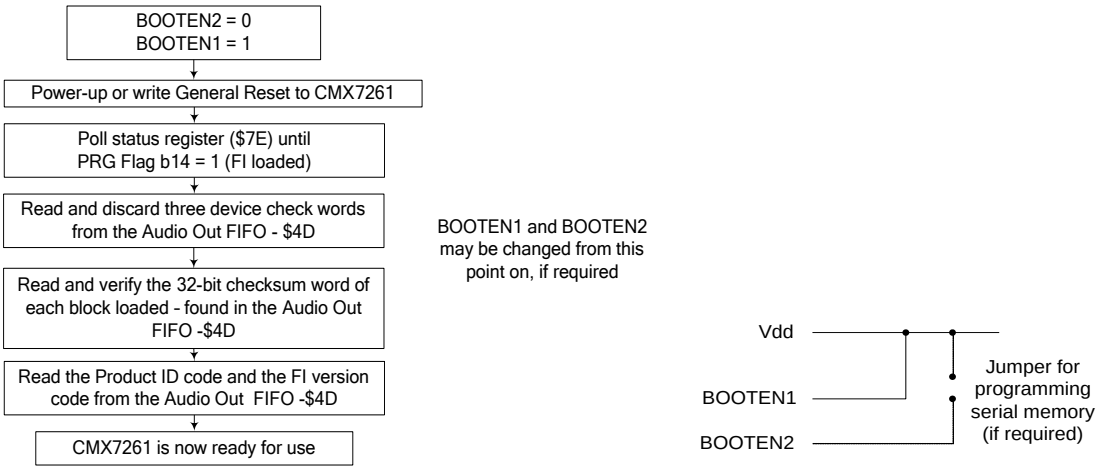


Figure 19 FI Loading from Serial Memory

The CMX7261 has been designed to function with the AT25F512 Serial Flash memory, however other manufacturers' parts may also be suitable. The time taken to load the FI should be less than 500ms even when loading the largest possible Function Image™.

8.4 Coding Formats

This section provides a brief description about the various coding standards handled by the CMX7261 when loaded with FI-2.x. The motivation behind all the voice coding standards described here is to compress analogue voice in order to reduce the bandwidth required to transmit it.

8.4.1 G.711

The G.711 standard is an ITU recommendation for audio companding. The standard specifies coding of linear PCM speech at 8 ksamples/s into logarithmic PCM speech at 8 ksamples/s – a coded data rate of 64 kbits/second.

The general principle behind companding is that for large sample values the exact value of the sample is not that important, so the signal can be quantised without loss of quality. However, when the sample value is small excessive quantisation would lead to poor quality speech. The result is that as the sample amplitude increases less resolution is required and, compared to linear PCM, compression is possible.

There are two variants: µ-law and A-law.

- µ-law is used primarily in North America – codes 14-bit linear PCM to 8-bit logarithmic PCM
- A-law is used in the rest of the world – codes 13-bit linear PCM to 8-bit logarithmic PCM

A single input sample maps onto a single companded sample, with no memory or algorithmic delay. The algorithm is lossy – if linear PCM speech is A-law or µ-law encoded and then decoded back into linear PCM the resulting audio will not be identical sample by sample but should sound similar.

In addition to companding, the G.711 standard specifies that A-law encoded samples should have even bits inverted. This is to provide many 0/1 transitions to assist signal reception when the data is transmitted using a modem. Inverting the even bits is equivalent to XORing the data with 0x55.

The G.711 standard specifies that µ-law encoded samples should be inverted, equivalent to XORing with 0xFF.

8.4.2 G.723.1[1]

G.723.1 is an ITU recommendation for coding speech samples at 8 ksamples/s with a 30ms frame size. This translates to 240 PCM samples per G.723.1 frame.

The vocoder produces a compressed bit stream at either 5.3 kbits/s or 6.3 kbits/s depending on the selected mode of operation.In addition, G.723.1 Annex A defines a discontinuous transmission (DTX) capability.

With the DTX enabled a Voice Activity Detection (VAD) decision will detect the end of speech and will instead start encoding the background noise with a greatly reduced bandwidth requirement. Instead of a full size voice frame a much shorter Silence Insertion Descriptor (SID) frame is transmitted and then no further frames are transmitted until a change in the input signal triggers a new SID frame or until voice is detected again.
At the decoder a received SID frame will result in generation of comfort noise to fill the period of non-transmitted frames.

[1] CML acknowledges that the device contains an implementation of the G.723.1 standard, rights to which are held by third parties who may claim and/or be entitled to compensation in connection with their implementation. It is the users' responsibility to obtain any licence that may be required directly from holders of such rights if using G.723.1 functionality. Licence details are available from Sipro Lab Telecom (www.sipro.com). User hereby waives any right to seek damages or other compensation by way of suit or other action against CML Microsystems Plc in connection with any such standards.

8.5 Transcoding Description

Internally the CMX7261 decodes the input audio data to linear PCM before encoding into a desired output format. Once the transcoder is configured, the following steps happen inside the CMX7261:

1. A frame of input audio is first passed through the 'Decoder' block (refer Figure 1 Block Diagram) where it is decoded from the input format configured in the Input Type - $54 write register, to linear PCM.
2. The output of the 'Decoder' is held internally in linear PCM format and this is then passed through the 'Encoder' block (refer Figure 1 Block Diagram) where it is encoded to the output format configured in the Output Type - $56 write register. In the case of G.723.1 encoding mode the currently configured rate and VAD option is read from the G.723.1 Vocoder Options - $5E write register.
3. Optionally the linear PCM output from the Decoder can be monitored using the MONOUT pins. This facility is provided for debug purposes and can be switched off, to conserve power.

The steps above describe transcoding of a single audio channel. Full duplex mode provides two such audio channels with the limitation that one channel provides the reverse transcoding of the other.

8.5.1 Input and Output Frame Sizes

The input and output frame sizes differ between various transcoding formats, as explained in this section.

G.723.1

G.723.1 operates with various sizes of encoded frames, depending on configuration and VAD operation.

A transmitted 30ms G.723.1 frame can correspond to either

24 bytes = 6.3 kbits/s rate, voice)
20 bytes = 5.3 kbits/s rate, voice)
4 bytes = Annex A: Silence Insertion Descriptor (SID) or
0 bytes = Annex A: Silence (no transmission)

These can occur in any order, although silence frames are typically preceeded by a SID frame. Voice frames may change rate at any time and so it is important that the correct length is given for each frame.

At the decoder the length of the frame being passed is signalled using the Audio In FIFO Format - $4A – write register, which must be written prior to writing the frame data into the FIFO. This is set in the Type field, according to the values listed in Table 4.

If a frame error was detected in the underlying transport this should be signalled to the decoder by also setting the CRC flag in the format byte. This will indicate to the decoder that it should attempt Lost Packet Recovery (LPR) for this frame. Once a following frame is received error free this bit must be cleared to zero before it is transferred.

The data for the frame is then written to the Audio In FIFO Data8 - $48 write (Supports streaming C-BUS) register. This may be performed as a streaming CBUS write if required. Care should be taken not to overflow the FIFO so the available space may be checked prior to writing the data.

When DTX (Annex A) is enabled at the remote end there will be periods where no frames are received. During these periods a no-transmission (silence) frame must still be inserted by writing a single 1-byte frame to the Audio In FIFO Data8 - $48 write (Supports streaming C-BUS) register, in order to indicate the position relative to other frames. The value written is important. Because silence frames often occur in a block this may be performed as follows.

1. Write type ($03) to the Audio In FIFO Format - $4A – write register on the first silence frame in a block.

2. Write one byte of data ($03) to Audio In FIFO Data8 - $48 write (Supports streaming C-BUS)register. This must be written for the first silence frame and each one thereafter.

In all cases the length of data written to the FIFO must match the type field which was set in the format byte.

7	6	5	4	3	2	1	0
0	0	0	CRC	0	0	Type	

Type[1:0]	Packet Type	Tx / Rx Length	FIFO Length
00_b	6.3 kbits/s Voice	24 bytes	24 bytes
01_b	5.3 kbits/s Voice	20 bytes	20 bytes
10_b	SID	4 bytes	4 bytes
11_b	Silence (no packet)	0 bytes	1 byte

CRC	(decoder only)
0	Frame was received correctly
1	Frame had CRC errors

Table 4 Encoding of FIFO Format Registers ($4A, $4E) for G.723.1 Operation

For encoder operation the output FIFO operates as the reverse of the decoder. Upon detection of a new packet being produced the host must read the Audio Out FIFO Format - $4E read register to determine the type, and therefore the length, of the next frame in the buffer. This is encoded using the same format as Table 4. The host must then read the correct number of bytes from the Audio Out FIFO Data8 - $4C read (Supports streaming C-BUS) register before transmitting the frame. In the case of a single byte of type $03 (silence) the FIFO must be read once but no data should be transmitted. The CRC flag is not used in encoder mode.

Typical processing delays are shown in Table 5:

Table 5 G723.1 Typical Process Times

Encoder:				
	ADC FIFO	5ms		
	Buffer Input Samples	30ms		
	Algorithm Look-ahead	7.5ms		
	Encode Processing	24.5ms		
		Total:	**67ms**	
Decoder:				
	Decode Processing	4.5ms		
	DAC FIFO	5ms		
		Total:	**9.5ms**	
Encode/Decode Total:				**76.5ms**

G.711

- When decoding G.711 μ/A-law coded audio – each 8-bit input byte will be decoded into a linear PCM sample representing 0.125ms of audio (at 8kHz sampling rate).
- When encoding into G.711 μ/A-law coded audio – each input (at 8kHz sampling rate) will be encoded into an 8-bit sample.

8.5.2 Data Transfer Using C-BUS Interface

Audio data can be transferred to and from the host via C-BUS Audio In and Audio Out FIFOs, each of which provide efficient streaming C-BUS access. The FIFO fill level can be determined by reading the Audio In and Audio Out FIFO levels and controlled using the FIFO Control - $50 write register. Interrupts may be provided on FIFO fill thresholds being reached, or on every 'N' new samples being read from or written to the respective FIFOs.

Each FIFO word is 16-bits long and can be accessed as one 16-bit word or as two bytes – LSByte and MSByte. Word wide FIFO writes involve writing 16-bit words to the Audio In FIFO data word register using either a single write or a streaming C-BUS. The word written is transferred to the Audio In FIFO and its fill level is updated.

Byte wide FIFO writes involve writing to the Audio In FIFO data byte register using either a single write or a streaming C-BUS. The contents of the Audio In FIFO data byte register are transferred to the Audio In FIFO (with undefined data in the MSByte) and its fill level is updated.

Likewise a word read from the Audio Out FIFO data word read register will return the oldest Audio Out FIFO data word and Audio Out FIFO fill level is updated. Reading the Audio Output data byte register will read the oldest Audio Out FIFO data word, discard the MSByte and return the LSByte. Audio Out FIFO fill level is also updated. In summary:

Operation	Effect
Audio In FIFO Data word Wr	Data word is added to Audio In FIFO. Audio In FIFO fill level is updated.
Audio In FIFO Data byte Wr	Audio In FIFO Data byte written is added to Audio In FIFO and its fill level is updated. The MSByte is a "don't care" byte.
Audio Out FIFO Data word Rd	Oldest Audio Out FIFO data word is removed from FIFO and returned; Audio Out FIFO fill level is updated.
Audio Out FIFO Data byte Rd	Oldest Audio Out FIFO data word is removed from FIFO, its MSByte is discarded and its LSByte is returned. Audio Out FIFO fill level is updated.

Figure 20 shows the C-BUS interface to the Audio In and Audio Out FIFOs.

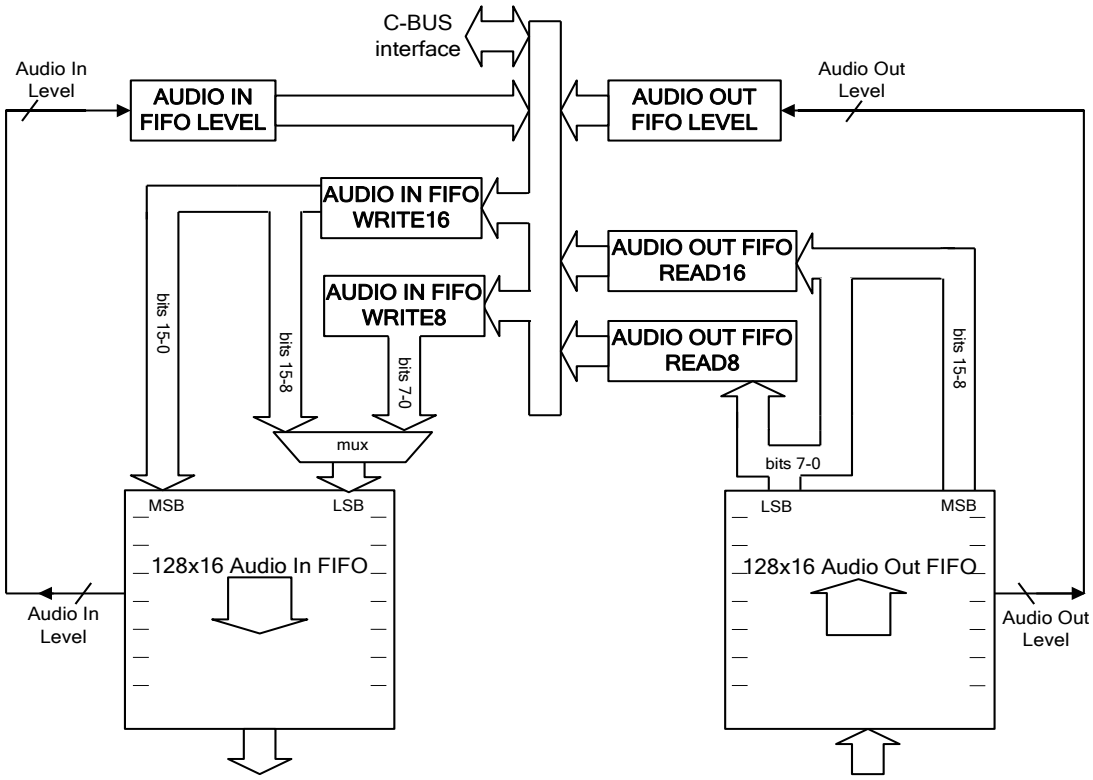


Figure 20 Audio Input and Audio Output FIFOs

The type of input data selected using the Input Type - $54 write register will determine whether the Audio In FIFO write 16 or 8 bit registers should be used for C-BUS audio input. The type of output data selected using the Output Type - $56 write register will determine whether the Audio Out FIFO read 16 or 8 bit registers should be used for C-BUS audio output.

The registers that affect FIFO operation are:

- Audio In FIFO Data8 - $48 write
- Audio In FIFO Data16 word - $49 write (Supports streaming C-BUS)
- Audio Out FIFO Data8 - $4C read
- Audio Out FIFO Data16 - $4D read (Supports streaming C-BUS)Audio In FIFO Level - $4B read
- Audio Out FIFO Level - $4F read
- Audio In FIFO Format - $4A – write
- Audio Out FIFO Format - $4E read
- FIFO Control - $50 write.
- G.723.1 Vocoder Options - $5E write

The remainder of this section explains data transfer to and from the host using the C-BUS interface.

When the input data source is C-BUS:

1. The host must ensure that the Audio In FIFO does not contain audio from previous encoding/decoding operations (see FIFO Control - $50 write register).
2. The Audio Source field in the Mode - $6B write register must be set to indicate that audio input is through the C-BUS interface.
3. The host writes at least a frame of data to the Audio In FIFO (see Audio In FIFO Data8 - $48 write registers). The frame size varies between different vocoders. The following table gives the frame size for various vocoders that exist in the CMX7261.
4. If the FIFO Control - $50 write register is configured correctly, the host will be interrupted when the Audio In FIFO empties to the level specified by the host. Alternatively, if the host has configured the FIFO Count Interrupt - $51 write register, the host will be interrupted when the CMX7261 has read

the specified number of samples from the Audio In FIFO. More data may be loaded into the Audio In FIFO at this stage before data buffered in the CMX7261 runs out, otherwise an under-run will occur.

Input type	*Frame size*
Linear PCM	1 linear PCM sample
G.711 µ/A-law	1 G.711 µ/A-law 8 bit sample
G.723.1	240 words (G.723.1 operates on 240 sample frames). In G.723.1 format, the input varies from 1 to 24 bytes, depending on configuration and input signal classification at the source encoder. Before writing the data the Audio In FIFO Format - $4A – write register must be set to the correct value. For a full description refer to 8.5.1 Input and Output Frame Sizes

In typical operation, input data may be written to the Audio In FIFO prior to starting transcoding, enabling the host to create a buffer of data and therefore avoiding risk of the data running out during transcoding.

When the input data source is PCM or the analogue audio input:
In the case where Audio Source is set to external PCM or analogue audio input, the input data from an external PCM codec or the analogue audio input will be loaded into the Input Buffer, without the host having to intervene in the data transfer process.

If the audio source is external PCM/analogue audio input, and the audio destination is C-BUS – the host must read the output data from the C-BUS quickly enough to maintain real-time constraints. Once started the analogue audio input/external PCM will operate at the selected sample rate regardless of the host C-BUS access rate. If the C-BUS Audio Out FIFO is not read quickly enough by the host a data overflow will occur, which the CMX7261 will indicate to the host.

When the output data destination is C-BUS:

1. The host must ensure that the Audio Out FIFO does not contain audio from previous encoding/decoding operations (see FIFO Control - $50 write register).
2. If the host has configured the FIFO Count Interrupt - $51 write register, it waits for the Count_Out interrupt, at which point the host can read a frame of data from the Audio Out FIFO.
3. Alternatively the FIFO Control - $50 write register may be configured to interrupt when the Audio Out FIFO fills to a specified level, and the host may read the Audio Out FIFO when this interrupt occurs.

When the output data destination is PCM or the Analogue audio output:
When the Audio Destination is set to external PCM or analogue audio output, the data in the Output buffer will sent to the external PCM codec or analogue audio output, without the host having to intervene in the data transfer process.

If the audio destination is external PCM/analogue audio output, and the audio source is C-BUS – the host must provide input data to the C-BUS quickly enough to maintain real-time constraints. Once started, the analogue audio output/external PCM will operate at the selected sample rate regardless of the host C-BUS access rate. If the C-BUS Audio In FIFO is not written quickly enough by the host a data underflow will occur, which the CMX7261 will indicate to the host.

In general, Figure 21 describes operation when data is transferred into the CMX7261 using the Audio In FIFO (see Audio In FIFO Data8 - $48 write registers). Figure 22 describes operation when data is transferred out of the CMX7261 using the Audio Out FIFO (see Audio Out FIFO Data8 - $4C read registers).

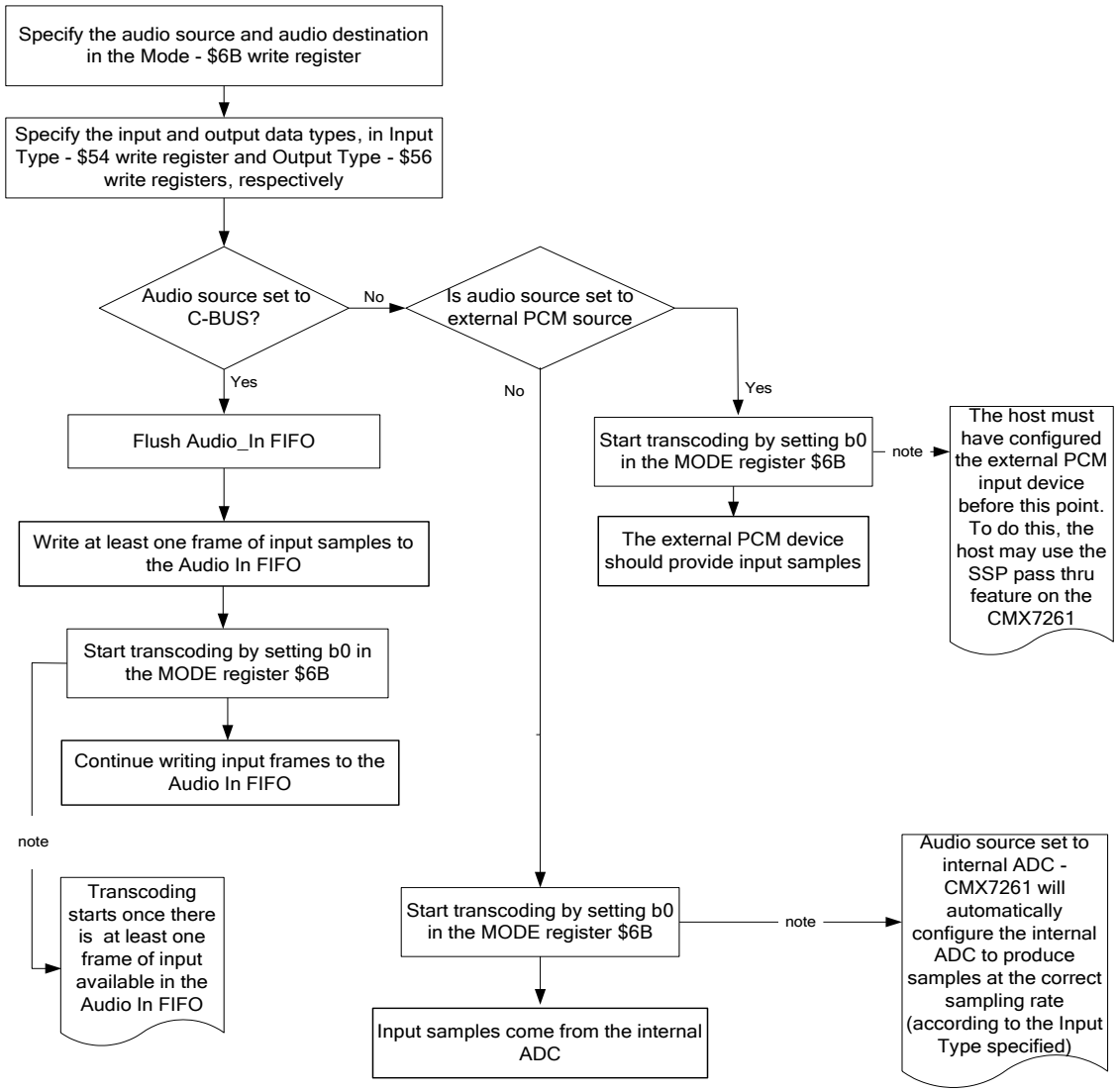


Figure 21 Input Data Transfer into the CMX7261

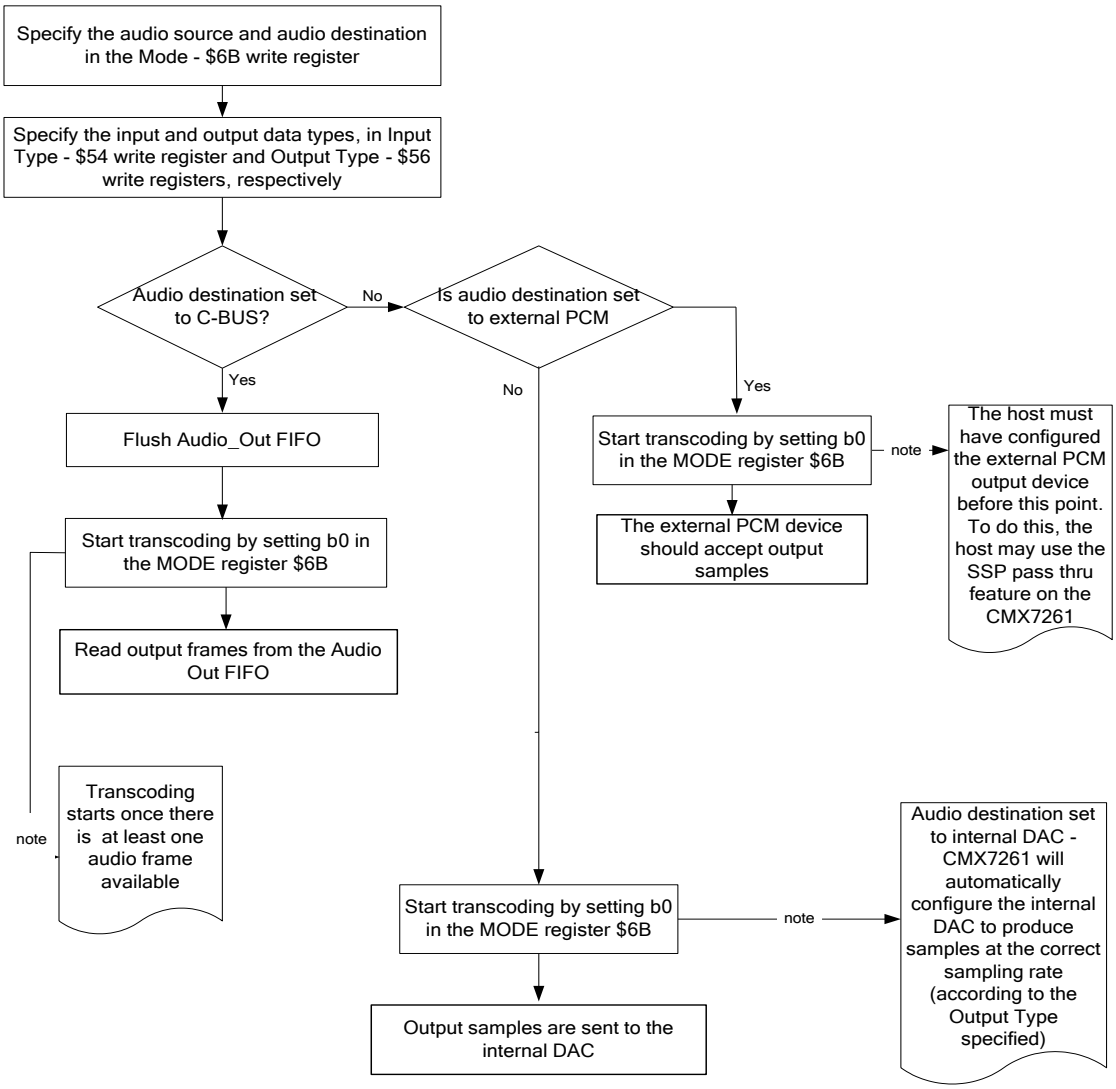


Figure 22 Output Data Transfer from the CMX7261

8.5.3 Data Formats – Packed and Unpacked

For some modes the CMX7261 can accept packed or unpacked data as an input and provide either as an output.

This section describes the bit packing standards to be used with CMX7261. The CMX7261 is capable of accepting packed data as an input and can output packed data. Though the packed data format is intended for use with C-BUS inputs and outputs, it applies equally well for external PCM inputs and outputs if the external PCM device has some digital logic to pack and unpack data according to the format mentioned in this section.

G.723.1 – Data

G.723.1 does not allow further packing. All data should be transferred using the 8 bit FIFO registers, 1 byte at a time. Streaming C-BUS may be employed to reduce the time taken to transfer the vocoder frame data.

G.711 – Packed Data

G.711 standard μ/A-law audio coding produces an 8-bit output per input sample. A packed data mode results in two bytes being packed into a 16-bit input word. The MSByte of the word will contain the first G.711 coded byte and the LSByte will contain the last/most recent G.711 coded byte, as shown below:

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
First/oldest G.711 byte								Last/most recent G.711 byte							

In order to transfer packed G.711 bytes as an input, the host must write the packed data words to the Audio In FIFO data word register (Audio In FIFO Data16 word - $49 write (Supports streaming C-BUS).

The G.711 standard describes two processing stages – convert linear PCM to a μ/A-law sample (compression) and then XOR the resulting sample with a mask to ensure that many bit transitions happen within the data (to aid data transmission and reception via a modem). Both packed and unpacked G.711 data may be optionally XORed with a mask as specified by the G.711 standard.

G.711 – Unpacked Data

Single G.711 coded bytes may be written to the Audio In FIFO data byte register (Audio In FIFO Data8 - $48 write).

B7	B6	B5	B4	B3	B2	B1	B0
G.711 coded byte							

The G.711 standard describes two processing stages – convert linear PCM to a μ/A-law sample (compression) and then XOR the resulting sample with a mask to ensure that many bit transitions happen within the data (to aid data transmission and reception via a modem). Both packed and unpacked G.711 data may be optionally XORed with a mask as specified by the G.711 standard.

Linear PCM Samples

Linear PCM samples are always transferred using one 16-bit word per sample. Input is through the Audio In FIFO data word register (Audio In FIFO Data16 word - $49 write (Supports streaming C-BUS) or the PCM input and output through the Audio Out FIFO data word register (Audio Out FIFO Data16 - $4D read (Supports streaming C-BUS), or PCM output. Various input sample formats are possible – the sample resolution may be 13 or 14 bits for example, or the sample may be signed or unsigned. The CMX7261 is capable of processing each of these types of data – specified using the Input Type - $54 write and Output Type - $56 write registers.

8.6 Device Control

Once the Function Image™ is loaded, the CMX7261 can be set into one of two main modes using the Mode - $6B write register:

- Idle mode – for configuration or low power operation
- Transcode mode – for encoding or decoding or transcoding a single audio channel between analogue/PCM/G.723.1 or G.711 format audio.
- Enc-Dec mode – a test mode which encodes LPCM to a selected compressed audio format and then decodes it again – providing the ability to evaluate audio quality
- Full duplex mode – for encoding, decoding or transcoding one audio channel between analogue/PCM/G.723.1 or G.711 format audio, whilst performing the reverse encoding, decoding or transcoding on a second channel.

These modes are described in the following sections. All control is carried out over the C-BUS interface: either directly to operational registers or, for parameters that are not likely to change during operation, using the Programming Register - $6A write in idle mode.

To conserve power when the device is not actively processing a signal, place the device into idle mode. Additional power saving can be achieved by disabling unused hardware blocks, however, most of the hardware power saving is automatic. Note that the BIAS block must be enabled to allow any of the Analogue Input or Output blocks to function. It is only possible to write to the Programming register whilst in Idle mode. See:

- Programming Register - $6A write
- Mode - $6B write
- Programming Register Operation
- Bias Control - $B7 write.

8.6.1 Normal Operation Overview

In normal operation (after the CMX7261 is configured), the required mode must be selected and correctly formatted data input and read out. This process is carried out by selecting the transcoding type and specifying the input audio source and output audio destination. Such options are required to be configured correctly before transcoding/encoding/decoding can begin.

For continuous transcoding operation, data must be transferred into and out of the CMX7261. Audio transfer into the CMX7261 can be through the analogue audio input, from an external PCM device, or the host can feed in the data using C-BUS interface. Similarly, the transcoded output can be transferred out of the CMX7261 using the analogue audio ouput, or using the PCM interface to an external PCM device or to the host using the C-BUS interface. C-BUS transfers use the Audio In FIFO to transfer data into the CMX7261, and the Audio Out FIFO to transfer data out of the CMX7261. The Status register is used to indicate that the data has been dealt with. The CMX7261 can be configured to interrupt the host on FIFO fill level or when it has read/written a specified number of samples from the Audio In/Out FIFOs.

In the process of transcoding the most significant registers are:

- Mode - $6B write
- IRQ Status - $7E read
- IRQ Enable - $6C write
- Audio In FIFO Data8 - $48 write
- Audio In FIFO Data16 word - $49 write (Supports streaming C-BUS)
- Audio Out FIFO Data8 - $4C read
- Audio Out FIFO Data16 - $4D read (Supports streaming C-BUS)
- Audio In FIFO Format - $4A – write
- Audio Out FIFO Format - $4E read
- Audio In FIFO Level - $4B read

- Audio Out FIFO Level - $4F read
- G.723.1 Vocoder Options - $5E write

8.6.2 Transcoder Operation

The many CMX7261 features provide significant flexibility however, basic encoding, decoding or transcoding can be carried out easily by just understanding the operation of just a few registers.

Half-duplex transcoder operation is illustrated by Figure 23 and the following detailed example.

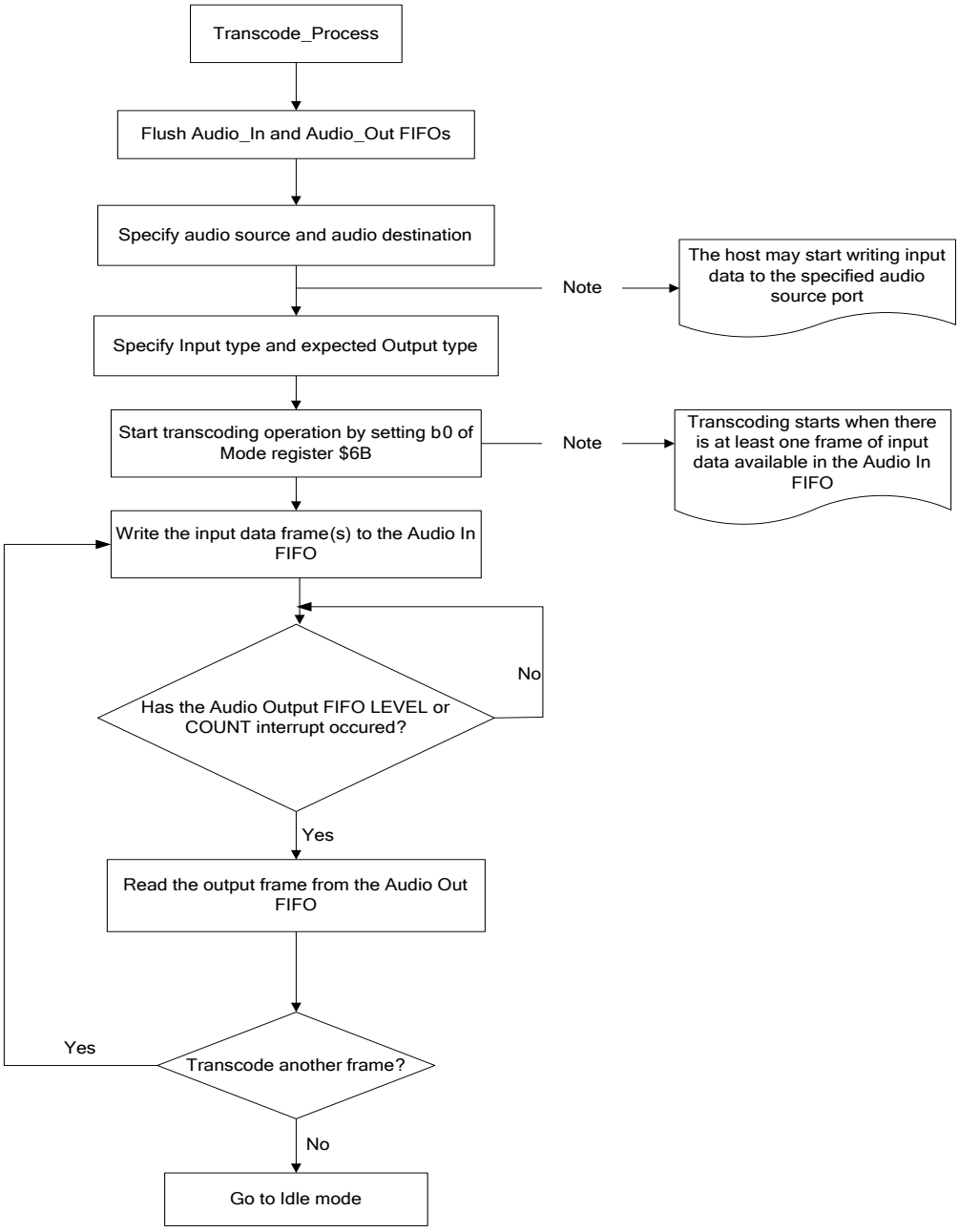


Figure 23 Transcoder Operation Flowchart

8.6.2.1 Basic Operation (Half-duplex)

Example: The following table explains the process involved in transcoding from G.711 A-law packed input to G.723.1 output when the input comes from Audio In FIFO and the output is sent to the Audio Out FIFO:

Step No.	C-BUS Operation	Action	Description
1	Write $8080 to FIFO Control - $50 write	Flush the audio in and audio out FIFO	To ensure that no data is remaining from any previous transcoding operation
2	Write $0011 to the Input Type - $54 write register	Specify the input data type	Specifies the format of the input data that the CMX7261 expects. In this case, the input data type is specified as G.711 A-law packed data.
3	Write $0005 to the Output Type - $56 write register	Specify the Output data type	Specifies the format of the output data expected from CMX7261. In this case, the expected output data type is specified as G.723.1 data.
4	Write $0110 to the Mode - $6B write register	Specify Audio Source and Audio Destination	Specifies the input and output ports' audio. In this case both are set to C-BUS.
5	Write 240 data bytes (120 writes for packed data) to the Audio In FIFO – see Audio In FIFO Data8 - $48 write registers	Prime the Input buffer with a frame of data	This provides a buffer of 240 samples (G.723.1 operates on 240 sample frames) for the CMX7261 to start the transcoding operation on request. This can be written as a series of smaller blocks without requiring 240 samples to be collected first. Encoding will not proceed until 240 samples have been received.
6	Write $2801 to the FIFO Count Interrupt - $51 write register	Specify when the host should be interrupted	This tells the CMX7261 to interrupt the host when it has written a new frame to the Audio Out FIFO, or read $28 words from the Audio In FIFO In, G.723.1 output mode the format byte must first be checked to determine the number of output bytes to be read out. For a full description of this process refer to 8.5.1 Input and Output Frame Sizes
7	Write $0111 to the Mode - $6B write register	Start transcoding	Commands the CMX7261 to start the transcoding operation. If there is not enough data in the Input buffer for the specified transcoding mode, the CMX7261 will wait until it has enough data to start transcoding.
8	Check the IRQ Status - $7E read register for bits 2 or 3 – Count_Out or Count_In interrupts	Count_Out: Indicates an output frame is available	The input data has been transcoded into the desired format, and the host can now read a frame of data from the Audio Out FIFO
		Count_In: Indicates that a frame of input data has been read	There is now space for more input G.711 samples to be written to the Audio In FIFO. This should be done promptly to ensure uninterrupted transcoding.
9	Continue Transcoding		Repeat steps 8 as required

The procedure described above can be adapted, to achieve different transcoding modes, with different input and output ports. Transcoding from the G.711 A-law packed data to G.723.1 formatted data will continue as long as there is enough input data and the mode bits (b1-0) of Mode - $6B write register has not changed. The registers used for basic operation are:

- Mode - $6B write
- Input Type - $54 write
- Output Type - $56 write
- IRQ Status - $7E read
- Audio In FIFO Data8 - $48 write
- Audio In FIFO Data16 word - $49 write (Supports streaming C-BUS)

- Audio Out FIFO Data8 - $4C read
- Audio Out FIFO Data16 - $4D read (Supports streaming C-BUS)
- Audio In FIFO Format - $4A – write
- Audio Out FIFO Format - $4E read
- FIFO Count Interrupt - $51 write
- FIFO Control - $50 write
- G.723.1 Vocoder Options - $5E write

8.6.2.2 Full-duplex operation

Example: The following flowchart and table explains the process involved in transcoding from G.711 A-law packed input to Analogue Audio, for channel-1. In addition, simultaneously transcoding from Analogue Audio to G.711 A-law packed output, for channel-2.

The channel-1 input comes from Audio In FIFO and the output is sent to Analogue Out.

Channel-2 is automatically set to transcode from Analogue Audio to G.711A packed data. Channel-2 input and output ports are automatically set to:
Channel-2 input port = Analogue In
Channel-2 output port = Audio Out FIFO.

NOTE: In full-duplex operation, multiple output ports cannot be enabled for either channel. Each channel will have only one output port.

Full-duplex transcoder operation is illustrated by Figure 24 and the following detailed example.

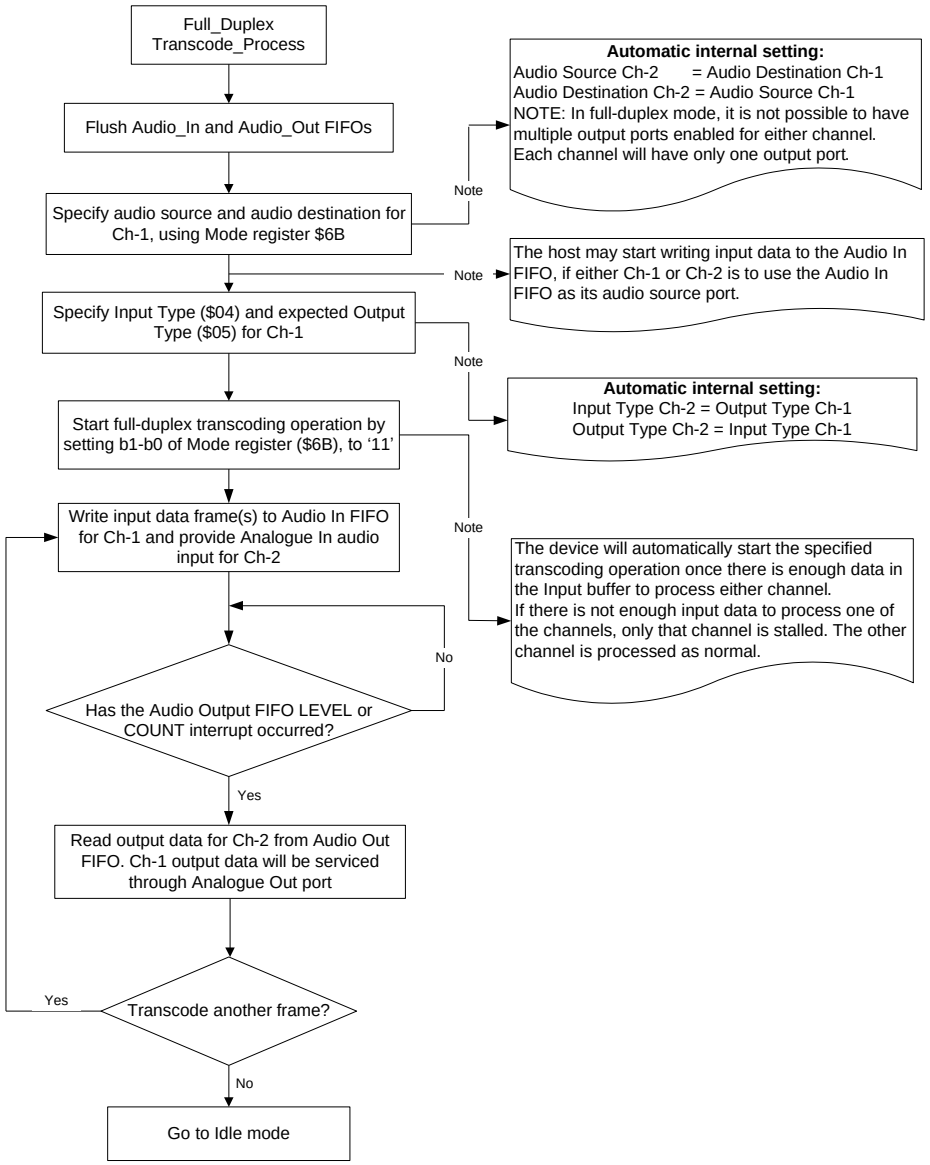


Figure 24 Full duplex Transcoder Operation Flowchart

Step No.	C-BUS Operation	Action	Description
1	Write $8080 to FIFO Control - $50 write	Flush the audio in and audio out FIFO	To ensure that no data is remaining from any previous transcoding operation
2	Write $0011 to the Input Type - $54 write register	Specify the input data type for Ch-1	Specifies the format of the input data that the CMX7261 expects for Ch-1. In this case, the input data type for Ch-1 is specified as G.711 A-law packed data. This action automatically sets the output data type for Ch-2 as G.711 A-law packed data.
3	Write $0004 to the Output Type - $56 write register	Specify the Output data type for Ch-1	Specifies the format of the output data expected from CMX7261 for Ch-1. In this case, the expected output data type is specified as 16-bit linear PCM samples at 8KHz. This action automatically sets the input data type for Ch-2 as 16-bit linear PCM samples at 8KHz.

4	Write $0120 to the Mode - $6B write register	Specify Audio Source and Audio Destination for Ch-1	Specifies the input and output ports for Ch-1. Here input port for Ch-1 is set to Audio In FIFO and output port for Ch-1 is set to Analogue Out. This action automatically sets the input port for Ch-2 to Analogue In and output port for Ch-2 to Audio Out FIFO.
5	Write G.711A packed data words to the Audio In FIFO for Ch-1. Simultaneously, provide Analogue In audio input for Ch-2	Prime the Input buffer with a frame of data, for both Ch-1 and Ch-2	This provides a buffer samples for the CMX7261 to start full-duplex transcoding operation on request.
6	Write $0505 to the FIFO Count Interrupt - $51 write register	Specify when the host should be interrupted	This tells the CMX7261 to interrupt the host when it has written 5 new data words to the Audio Out FIFO, or read 5 words from the Audio In FIFO.
7	Write $0123 to the Mode - $6B write register	Start full-duplex transcoding	Commands the CMX7261 to start full-duplex transcoding operation. If there is not enough data in the Input buffer for either channel, only that channel's processing is stalled. The other channel is processed as normal. The stalled channel's processing resumes when there is enough input data is present for that channel.
8	Check the IRQ Status - $7E read register for bits 2 or 3 – Count_Out or Count_In interrupts	Count_Out:Indicates an output frame is available	The input data has been transcoded into the desired format, and the host can now read a frame of data from the Audio Out FIFO.
		Count_In: Indicates that a frame of input data has been read	There is now space for a further 5 words, of G.711 A-law packed words to be written to the Audio In FIFO. This should be done promptly to ensure uninterrupted transcoding.
9	Continue Transcoding		Repeat steps 8 as required

The procedure described above can be adapted, to achieve different transcoding modes, with different input and output ports. Full-duplex Transcoding from G.711 A-law packed data to analogue audio and vice-versa will continue as long as there is enough input data and the mode bits (b1-0) of the Mode - $6B write register have changed. The registers used for basic operation are:

- Mode - $6B write
- Input Type - $54 write
- Output Type - $56 write
- IRQ Status - $7E read
- Audio In FIFO Data8 - $48 write
- Audio In FIFO Data16 word - $49 write (Supports streaming C-BUS)
- Audio Out FIFO Data8 - $4C read
- Audio Out FIFO Data16 - $4D read (Supports streaming C-BUS)
- Audio In FIFO Format - $4A – write
- Audio Out FIFO Format - $4E readFIFO Count Interrupt - $51 write
- FIFO Control - $50 write
- G.723.1 Vocoder Options - $5E write

Using a fixed size for the FIFO Count interrupt is not recommended for use with G.723.1 due to the variable length frames which can be produced. It may be preferable to use a value of 1 to report that a write has occurred, and use this to trigger a check of the Audio Out FIFO Format - $4E read register.

8.6.3 Device Configuration (Using the Programming Register)

While in idle mode the Programming register becomes active providing access to the Program Blocks. Program Blocks allow configuration of the CMX7261. Features that can be configured include:

- Configuration of PCM Port rate and word format
- Configuration of the CMX7261 to operate with a non-default XTAL input frequency

Full details of how to configure these aspects of device operation are given in section 11 in the User Manual.

8.6.4 Device Configuration (Using dedicated registers)

Some device features may be configured using dedicated registers. This allows for configuration outside of idle mode. Configuration of the following features is possible:

- Gain, power saving and muting of the analogue audio output
- Gain, power saving and muting of the analogue audio input
- Gain and muting of any linear PCM output signal
- Gain and muting of any linear PCM input signal.

The registers that allow configuration of these features are:

- ANAIN Coarse Gain - $B1 write
- ANAOUT Coarse Gain - $B4 write
- ANAOUT Config - $B3 write
- ANAIN Config - $B0 write.

8.6.5 Interrupt Operation

The CMX7261 can produce an interrupt output when various events occur. Examples of such events include FIFO fill levels being reached or an output overflow when processing audio data.

Each event has an associated Status register bit and an Interrupt Mask register bit. The interrupt mask register is used to select which status events will trigger an interrupt on the IRQN line. Events can be masked using the IRQ mask bit (bit 15) or individually masked using the Interrupt Mask register. Enabling an interrupt by setting a mask bit (0→1) after the corresponding Status register bit has already been set to 1 will also cause an interrupt on the IRQN line. The IRQ bit (bit 15) of the Status register reflects the IRQN line state.

All interrupt flag bits in the Status register are cleared and the interrupt request is cleared following the command/address phase of a C-BUS read of the Status register. See:

- IRQ Status - $7E read
- IRQ Enable - $6C write.

8.6.6 PCM Port

The CMX7261 features a PCM port, which can be used to communicate with an external PCM codec. This can be used as an alternative to the internal ADC and DAC converters. The PCM port can be used for input, output or both, and can be configured for wide range of modes, sample rates and word formats via the programming register. Once configured and enabled, via the mode register, the PCM port operates automatically, transferring data between the CMX7261 and the external PCM codec.

In addition, there is the facility to send configuration or other data words to the external PCM device. There is no facility to read back responses to these configuration words. See:

- 11.1.3 Program Block 2 – PCM Port Config
- 10.1.19 PCM Talkthrough Data - $63 write

8.7 Signal Level Optimisation

The internal signal processing of the CMX7261 will operate with wide dynamic range and low distortion only if the signal level at all stages in the signal processing chain is kept within the recommended limits. For a device working from a 3.3V supply, the signal range which can be accommodated without distortion is specified in 9.1.3 Operating Characteristics. Signal gain and dc offset can be manipulated as follows:

8.7.1 Audio Output Path Levels

The signals output from ANAOUT and MONOUT have independent gain controls. The Fine Output adjustment has a maximum attenuation of 6dB and no gain, whereas the Coarse Output adjustment has a variable attenuation of up to 14.2dB and 6dB gain.

The ANAOUT and MONOUT signals may be independently inverted. Inversion is achieved by selecting a negative value for the (linear) Fine Output adjustment. See:

- 10.1.28 ANAOUT Coarse Gain - $B4 write.
- 10.1.27 ANAOUT Config - $B3 write.

8.7.2 Audio Input Path Levels

The Coarse Input has a variable gain of up to +22.4dB and no attenuation. With the lowest gain setting (0dB), the maximum allowable input signal level at the ANAIN pins is specified in section 9.1.3 Operating Characteristics.

A Fine Input level adjustment is provided, although the CMX7261 should operate correctly with the default level selected. Inversion is achieved by selecting a negative value for the (linear) Fine Input gain adjustment.
It should be noted that if the maximum allowable signal input level is exceeded, signal distortion will occur regardless of the internal attenuation. See:

- 10.1.16 Fine Gain Channel-1 - $5B write.
- 10.1.17 Fine Gain Channel-2 - $5C write.
- 10.1.25 ANAIN Config - $B0 write.
- 10.1.26 ANAIN Coarse Gain - $B1 write.

8.8 C-BUS Register Summary

ADDR. (hex)	Read/ Write	REGISTER	Word Size (bits)
$01	W	C-BUS RESET	0
$48	W	Audio In FIFO Data Byte	8
$49	W	Audio In FIFO Data Word	16
$4A	W	Audio In FIFO Format	8
$4B	R	Audio In FIFO Level	8
$4C	R	Audio Out FIFO Data Byte	8
$4D	R	Audio Out FIFO Data Word	16
$4E	R	Audio Out FIFO Format	8
$4F	R	Audio Out FIFO Level	8
$50	W	FIFO Control	16
$51	W	FIFO Count Interrupt	16
$54	W	Input Type	16
$56	W	Output Type	16
$58	W	Signal Control	16
$5B	W	Fine Gain Channel-1	16
$5C	W	Fine Gain Channel-2	16
$5E	W	G.723.1 Vocoder Options	16
$63	W	PCM Talkthrough Data	16
$64	W	GPIO Control	16
$79	R	GPIO Input	16
$69	W	Reg Done Select	16
$6A	W	Programming Register	16
$6B	W	Mode	16
$6C	W	IRQ Enable	16
$7E	R	IRQ Status	16
$7F	R	Mode Register Readback	16
$B0	W	ANAIN Config	16
$B1	W	ANAIN Coarse Gain	16
$B3	W	ANAOUT Config	16
$B4	W	ANAOUT Coarse Gain	16
$B5	W	MONOUT Coarse Gain	16
$B6	W	SPKR Coarse Gain	16
$B7	W	Bias Control	16

Table 6 C-BUS Registers

All other C-BUS addresses are reserved and must not be accessed.

9 Performance Specification

9.1 Electrical Performance

9.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

ESD Warning: This high performance RF integrated circuit is an ESD sensitive device which has unprotected inputs and outputs. Handling and assembly of this device should only be carried out at an ESD protected workstation.

	Min.	Max.	Units
Power Supplies			
DV_{DD} - DV_{SS}	-0.3	4.0	V
DV_{CORE} - DV_{SS}	-0.3	2.16	V
AV_{DD} - AV_{SS}	-0.3	4.0	V
SPKR1 V_{DD} – SPKR1 V_{SS}	-0.3	4.0	V
Voltage on any pin to V_{SS}	-0.3	IOV_{DD} + 0.3	V
Voltage differential between power supplies			
DV_{DD} and AV_{DD}	0	0.3	V
DV_{SS} and AV_{SS}	0	50	mV
Current into or out of any pin, except power supply pins, SPKR1P and SPKR1N	-20	20	mA
Current into or out of power supply pins, SPKR1P and SPKR1N	-120	120	mA

Q1 Package (64-pin VQFN)	**Min.**	**Max.**	**Units**
Total Allowable Power Dissipation at Tamb = 25°C		3500	mW
... Derating		35.0	mW/˚C
Storage Temperature	-55	+125	˚C
Operating Temperature	-40	+85	˚C

L9 Package (64-pin LQFP)	**Min.**	**Max.**	**Units**
Total Allowable Power Dissipation at Tamb = 25°C		1690	mW
... Derating		16.9	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

9.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Min	Typ	Max.	Units
DV_{DD} - DV_{SS}	3.0	3.3	3.6	V
DV_{CORE} - DV_{SS}	1.7	1.8	1.9	V
AV_{DD} - AV_{SS}	3.0	3.3	3.6	V
SPKR1 V_{DD} – SPKR1 V_{SS}	3.0	3.3	3.6	V
Voltage differential between power supplies				
DV_{DD} and AV_{DD}	0	–	0.3	V
DV_{SS} and AV_{SS}	0	–	50	mV
Operating Temperature	-40	–	+85	°C
Xtal Frequency	4.0	–	12.288	MHz
External Clock Frequency	9.6	–	24.576	MHz

Notes:

DV_{DD} = AV_{DD} = SPKR1 V_{DD} = "IOV_{DD}"
DV_{SS} = AV_{SS} = SPKR1 V_{SS} = "V_{SS}"

9.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

External components as recommended in Section 6, External Components.
Maximum load on digital outputs = 30pF.
Xtal Frequency = 9.6MHz±0.01% (100ppm); Tamb = −40°C to +85°C.
AV_{DD} = DV_{DD} = 3.0V to 3.6V.
Reference Signal Level = 308mV rms at 1kHz with AV_{DD} = 3.3V.
Signal levels track with supply voltage, so scale accordingly.
Signal to Noise Ratio (SNR) in bit rate bandwidth.
Input stage gain = 0dB. Output stage attenuation = 0dB.

Current consumption figures quoted in this section apply to the device only when loaded with CMX7261 FI-2.0.0.0. Current consumption may vary with Function Image™.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
XTAL/CLK	20				
Input Logic '1'		70%	–	–	DV_{DD}
Input Logic '0'		–	–	30%	DV_{DD}
Input Current (Vin = DV_{DD})		–	–	40	µA
Input Current (Vin = DV_{SS})		-40	–	–	µA
C-BUS Interface and Logic Inputs					
Input Logic '1'		70%	–	–	DV_{DD}
Input Logic '0'		–	–	30%	DV_{DD}
Input Leakage Current (Logic '1' or '0')	22	-1.0	–	1.0	µA
Input Capacitance		–	–	7.5	pF
C-BUS Interface and Logic Outputs					
Output Logic '1' (I_{OH} = 2mA)		90%	–	–	DV_{DD}
Output Logic '0' (I_{OL} = -5mA)		–	–	10%	DV_{DD}
"Off" State Leakage Current	22	-1.0	–	1.0	µA
V_{BIAS}	21				
Output Voltage Offset wrt AV_{DD}/2 (I_{OL} < 1µA)		–	±2%	–	AV_{DD}
Output Impedance		–	50	–	kΩ

Notes:

20 Characteristics when driving the XTAL/CLK pin with an external clock source.

21 Applies when utilising V_{BIAS} to provide a reference voltage to other parts of the system. When using V_{BIAS} as a reference, V_{BIAS} must be buffered. V_{BIAS} must always be decoupled with a capacitor as shown in Section 6 External Components.

22 Tamb = 25°C, not including any current drawn from the device pins by external circuitry.

AC Parameters			Notes	Min.	Typ.	Max.	Unit
XTAL/CLK Input							
'High' Pulse Width			30	15	–	–	ns
'Low' Pulse Width			30	15	–	–	ns
Input Impedance (at 9.6MHz)							
	Powered-up	Resistance		–	150	–	kΩ
		Capacitance		–	20	–	pF
	Powered-down	Resistance		–	300	–	kΩ
		Capacitance		–	20	–	pF
Xtal Start-up Time (from powersave)				–	20	–	ms
V_{BIAS}							
Start-up Time (from powersave)				–	30	–	ms
Single-Ended ANAIN2 Input							
Input Impedance			31	–	> 10	–	MΩ
Input voltage range			34	–	–	20 to 80	%AV_{DD}
Load resistance (on pin 24)				47	–	–	kΩ
Amplifier open loop voltage gain							
(I/P = 1mV rms at 100Hz)				–	80	–	dB
Unity gain bandwidth				–	1.0	–	MHz
SNR			36	–	79	–	dB
Differential ANAIN Input							
Input Impedance, enabled			31	10	–	140	kΩ
Input Impedance, muted or powersaved				–	200	–	kΩ
Input Voltage Range			32	–	–	20 to 80	%AV_{DD}
SNR			36	–	79	–	dB
Programmable Input Gain Stages			35				
Gain (at 0dB)			33	-0.5	0	+0.5	dB
Cumulative Gain Error							
(wrt attenuation at 0dB)			33	-1.0	0	+1.0	dB
Gain range				–	0 to +22.4	–	dB
Gain step				–	3.2	–	dB

Notes:

30 Timing for an external input to the XTAL/CLOCK pin.

31 With no external components connected.

32 Centered about $AV_{DD}/2$; after multiplying by the gain of input circuit (with external components connected).

33 Design Value. Overall attenuation input to output has a tolerance of 0dB ±1.0dB.

34 Voltage range at the feedback pin to ensure input buffer does not limit.

35 Applies to ANAIN2 and ANAIN

36 1kHz, 1 Vp-p input

AC Parameters (continued)	Notes	Min.	Typ.	Max.	Unit
ANAOUT Output – Differential **MONOUT Output - Differential**					
Power-up to Output Stable	40	–	50	100	µs
Output Coarse Gain Attenuator					
Attenuation (at 0dB)		-0.2	0	+0.2	dB
Cumulative Attenuation Error					
(wrt attenuation at 0dB)		-0.6	0	+0.6	dB
Attenuation Step		–	0.2	–	dB
Attenuation Range		–	0 to -14.2	–	dB
Output Boost		–	+6	–	dB
Output Impedance	41	–	600	–	Ω
Output Voltage Range	43	0.3	–	AV_{DD}-0.3	V
Load Resistance		20	–	–	kΩ
SNR		–	70	–	dB
SPKR1 Speaker Output, **SPKR2 Earpiece Output**					
Power-up to Output Stable	40	–	50	100	µs
Output Coarse Gain Attenuator					
Attenuation (at 0dB)		-0.5	0	0.5	dB
Cumulative Attenuation Error					
(wrt attenuation at 0dB)		-1.0	0	1.0	dB
Attenuation Step		–	0.8	–	dB
Attenuation Range		–	0 to -47.2	–	dB
Output Boost		–	+6	–	dB
Output Power (SPKR1 Outputs)	44	–	–	140	mW
Output Voltage Range (SPKR1 Outputs)	45, 46	0.75	–	AV_{DD} – 0.75	V
Output Voltage Range (SPKR2 Outputs)	47	0.5	–	AV_{DD} – 0.5	V
SNR		–	70	–	dB
Resistance					
SPKR1 Speaker Output	41	8	–	–	Ω
SPKR2 Earpiece Output	41	32	–	–	Ω

Notes:

40 Power-up refers to issuing a C-BUS command to turn on an output. These limits apply only if V_{BIAS} is on and stable. At power supply switch-on, the default state is for all blocks, except the XTAL and C-BUS interface, to be in placed in powersave mode.

41 Small signal impedance, at AV_{DD} = 3.3V and Tamb = 25°C.

43 Centered about $AV_{DD}/2$; with respect to the output driving a 20kΩ load to $AV_{DD}/2$.

44 Differential power output into a 8Ω load at AV_{DD} = 3.0V.

45 For each output pin.

46 With respect to the outputs driving a differential load of 8Ω.

47 With respect to the output driving a 32Ω load to $AV_{DD}/2$.

AC Parameters (continued)	Notes	Min.	Typ.	Max.	Unit
Audio Input Filter (all inputs)					
Bandwidth at 8 ksps (+1, -3dB wrt 1kHz)		300	–	3500	Hz
Bandwidth at 16 ksps (+1, -3dB wrt 1kHz)		300	–	7000	Hz
Audio Output Filter (all outputs) **Frequency Response**					
1kHz (reference)		–	0	–	dB
3.7kHz		–	-3	–	dB
4.5kHz		–	-15	–	dB
5kHz		–	-50	–	dB

AC Parameters (continued)	Notes	Min.	Typ.	Max.	Unit
Processing Delays					
Loop-Back test	48				
G.723.1 6.3 kbits/sec ($54=$0005)		–	76.5	–	ms
G.723.1 5.3 kbits/sec ($54=$0005)		–	76.5	–	ms
G711 uLaw ($54=$0002)		–	15	–	ms
G711 A-Law ($54=$0001)		–	15	–	ms
PCM ($54=$0004)		–	15	–	ms

Notes:

48 ANAIN to SPKR2 out

9.1.4 CMX7261: 7261 FI-2.x Parametric Performance

For the following conditions unless otherwise specified:

External components as recommended in section 6.
Maximum load on digital outputs = 30pF.
Clock source = 19.2MHz ±0.01% (100ppm) external clock input; Tamb = –40°C to +85°C.
AV_{DD} = DV_{DD} = 3.0V to 3.6V.
Reference signal level = 308mV rms at 1kHz with AV_{DD} = 3.3V
Signal levels track with supply voltage, so scale accordingly.
Signal to Noise Ratio (SNR) in bit rate bandwidth.
Input stage gain = 0dB, Output stage attenuation = 0dB.

All figures quoted in this section apply to the device only when loaded with 7261FI-2.0.0.0. The use of other Function Images™ can modify the parametric performance of the device. Current consumption may vary with Function Image™.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Supply Current	50				
Idle mode					
DI_{DD}	51	–	670	–	µA
AI_{DD}	52	–	17	–	µA
Transcoding mode – DI_{DD}					
G.723.1 Decoder 6.3 kbits/sec	53, 55	–	10	–	mA
G.723.1 Decoder 5.3 kbits/sec	53, 55	–	10	–	mA
G.723.1 Encoder 6.3 kbits/sec	54, 55	–	24	–	mA
G.723.1 Encoder 5.3 kbits/sec	54, 55	–	22	–	mA
G.711 A-law Encoder (Register $56 = $11)	53, 55	–	1.7	–	mA
G.711 A-law Decoder (Register $54 = $11)	53, 55	–	1.7	–	mA
Transcoding mode					
Additional current for activating Analogue In port					
DI_{DD}		–	4.4	–	mA
AI_{DD}		–	3.3	–	mA
Additional current for activating Analogue Out port					
DI_{DD}		–	0.3	–	mA
AI_{DD}		–	7.8	–	mA

Notes:

50 Tamb = 25°C, not including any current drawn from the device pins by external circuitry.

51 Using external clock input, XTAL oscillator circuit powered down, and all GPIOs set to output and low using the GPIO Control - $64 write register.

52 All analogue sections are powered down by setting both ANAIN Config - $B0 write and ANAOUT Config - $B3 write registers to 0.

53 Audio source is set to Audio In FIFO, Audio destination is set to Audio Out FIFO.
Input rate and output rates are set to 8kHz.
G.723.1 VAD (Annex A) is not in use. Decoder Post Filter (PF) is enabled.

54 Audio source is set to Audio In FIFO, Audio destination is set to Audio Out FIFO.
Input and output rate is set to 8kHz.
G.723.1 VAD (Annex A) is not in use. Encoder HPF is enabled.

55 Provisional figure

9.1.5 C-BUS Timing

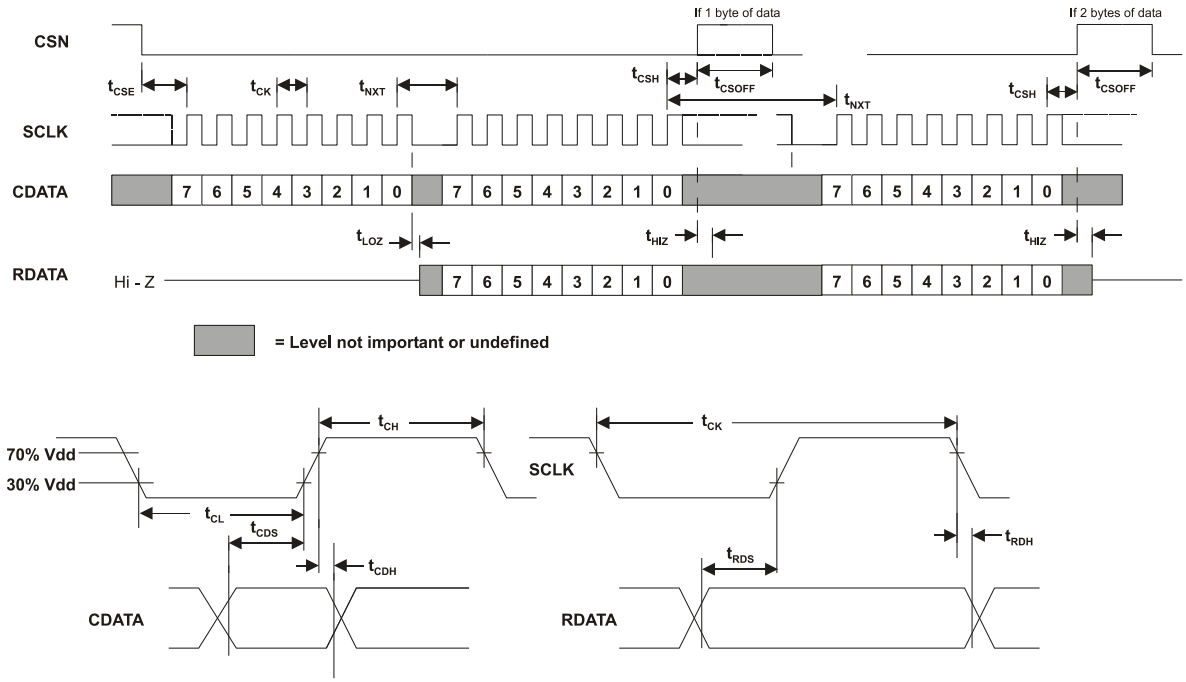


Figure 25 C-BUS Timing

C-BUS Timing		Notes	Min.	Typ.	Max.	Unit
t_{CSE}	CSN Enable to SCLK high time		100	–	–	ns
t_{CSH}	Last SCLK high to CSN high time		100	–	–	ns
t_{LOZ}	SCLK low to RDATA output enable Time		0.0	–	–	ns
t_{HIZ}	CSN high to RDATA high impedance		–	–	1.0	µs
t_{CSOFF}	CSN high time between transactions		1.0	–	–	µs
t_{NXT}	Inter-byte time		100	–	–	ns
t_{CK}	SCLK cycle time		100	–	–	ns
t_{CH}	SCLK high time		50	–	–	ns
t_{CL}	SCLK low time		50	–	–	ns
t_{CDS}	CDATA set-up time		75	–	–	ns
t_{CDH}	CDATA hold time		25	–	–	ns
t_{RDS}	RDATA set-up time		50	–	–	ns
t_{RDH}	RDATA hold time		0	–	–	ns

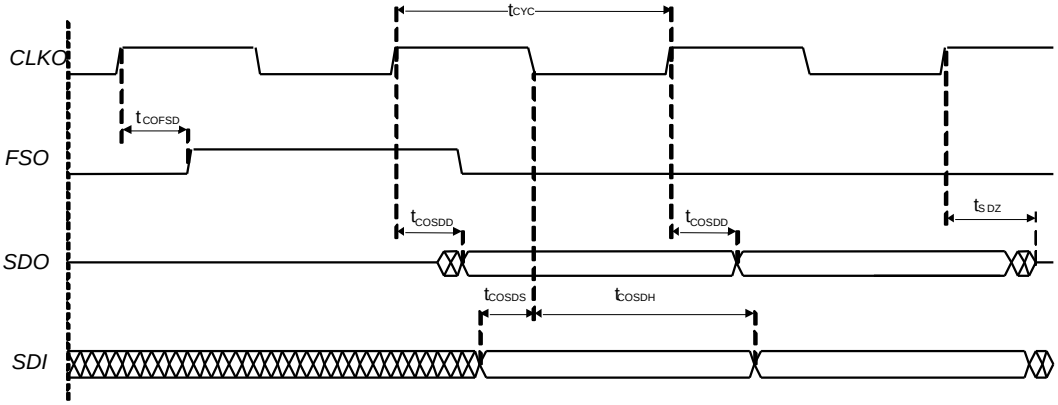
Notes:
1. Depending on the command, 1 or 2 bytes of CDATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. RDATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
2. Data is clocked into the peripheral on the rising SCLK edge.
3. Commands are acted upon at the end of each command (rising edge of CSN).
4. To allow for differing µC serial interface formats C-BUS compatible ICs are able to work with SCLK pulses starting and ending at either polarity.
5. Maximum 30pF load on IRQN pin and each C-BUS interface line.

These timings are for the latest version of C-BUS and allow faster transfers than the original C-BUS timing specification. The CMX7261 can be used in conjunction with devices that comply with the slower timings, subject to system throughput constraints.

9.2 PCM Port Timing

9.2.1 PCM Internal Clock

PCM Master; Internal Clock Generator



PCM Slave; Internal Clock Generator

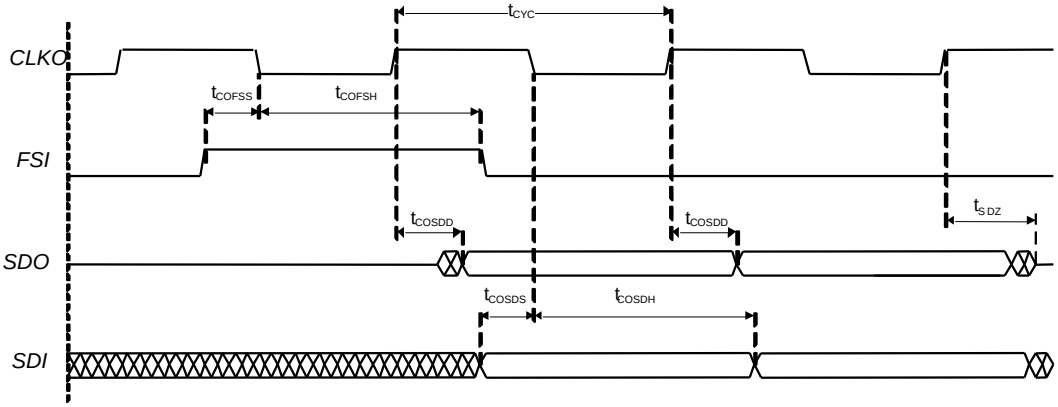
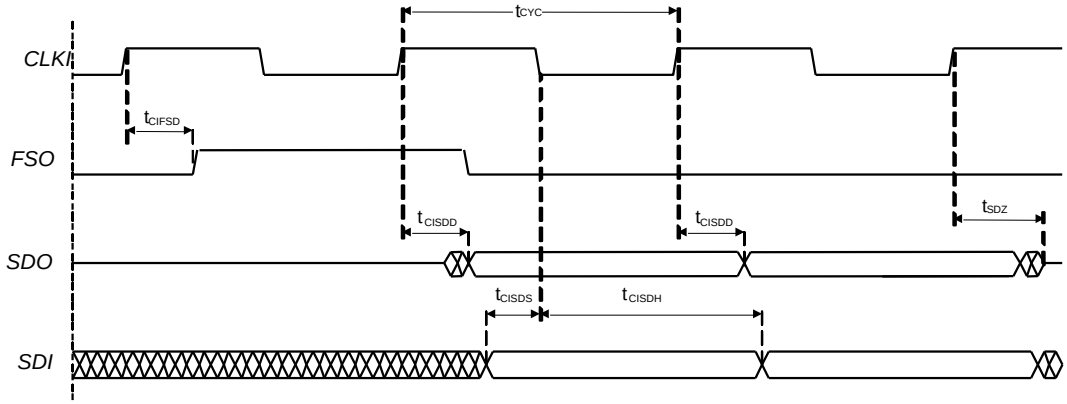


Figure 26 PCM Internal Clock Timings

PCM Internal Clock Timings		Notes	Min.	Typ.	Max.	Units
t_{CYC}	CLKO or CLKI cycle time	2	150	–	–	ns
t_{COFSD}	CLKO to FSO delay		-15	0	+15	ns
t_{COSDD}	CLKO to SDO delay		-15	0	+15	ns
t_{COSDS}	CLKO to FSO delay		8	–	–	ns
t_{COSDH}	CLKO to FSO delay		7	–	–	ns
t_{SDZ}	CLKO or CLKI to SDO tristate	1	-14	10	37	ns

9.2.2 PCM External Clock

PCM Master; External Clock Generator



PCM Slave; External Clock Generator

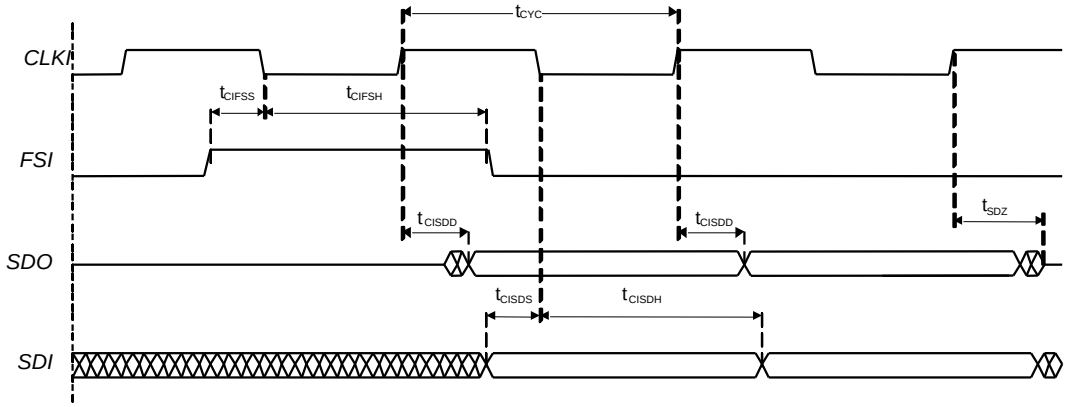
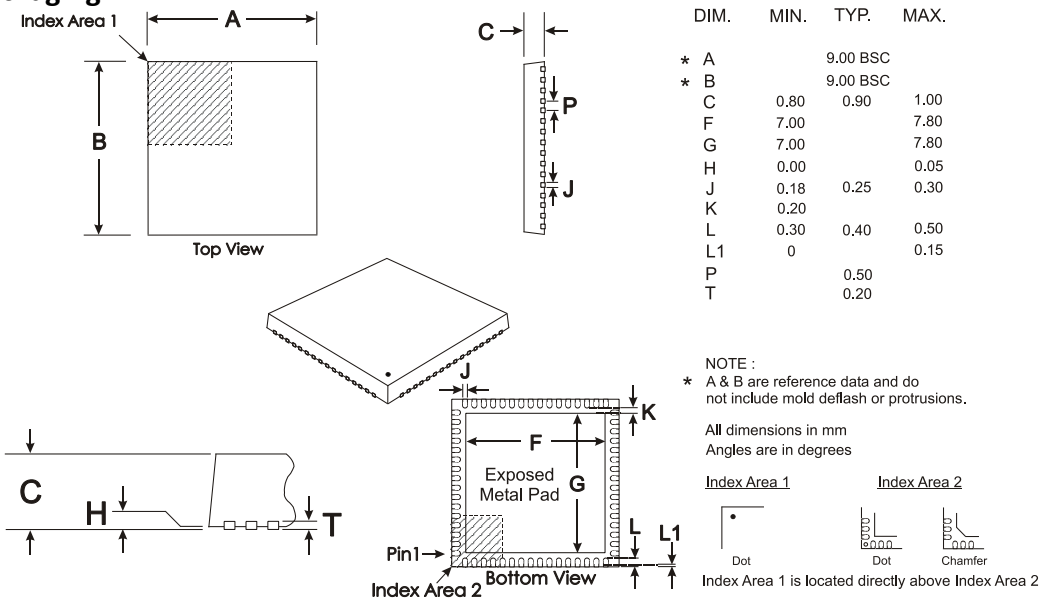


Figure 27 PCM External Clock Timings

PCM External Clock Timings		Notes	Min.	Typ.	Max.	Units
t_{CYC}	CLKO or CLKI cycle time	2	150	–	–	ns
t_{CIFSD}	CLKI to FSO delay		2	0	42	ns
t_{CISDD}	CLKI to SDO delay		2	0	42	ns
t_{CISDS}	CLKI to FSO delay		8	–	–	ns
t_{CISDH}	CLKI to FSO delay		7	–	–	ns
t_{SDZ}	CLKI or CLKO to SDO tristate	1	-14	10	37	ns

9.3 Packaging



DIM.	MIN.	TYP.	MAX.
* A		9.00 BSC	
* B		9.00 BSC	
C	0.80	0.90	1.00
F	7.00		7.80
G	7.00		7.80
H	0.00		0.05
J	0.18	0.25	0.30
K	0.20		
L	0.30	0.40	0.50
L1	0		0.15
P		0.50	
T		0.20	

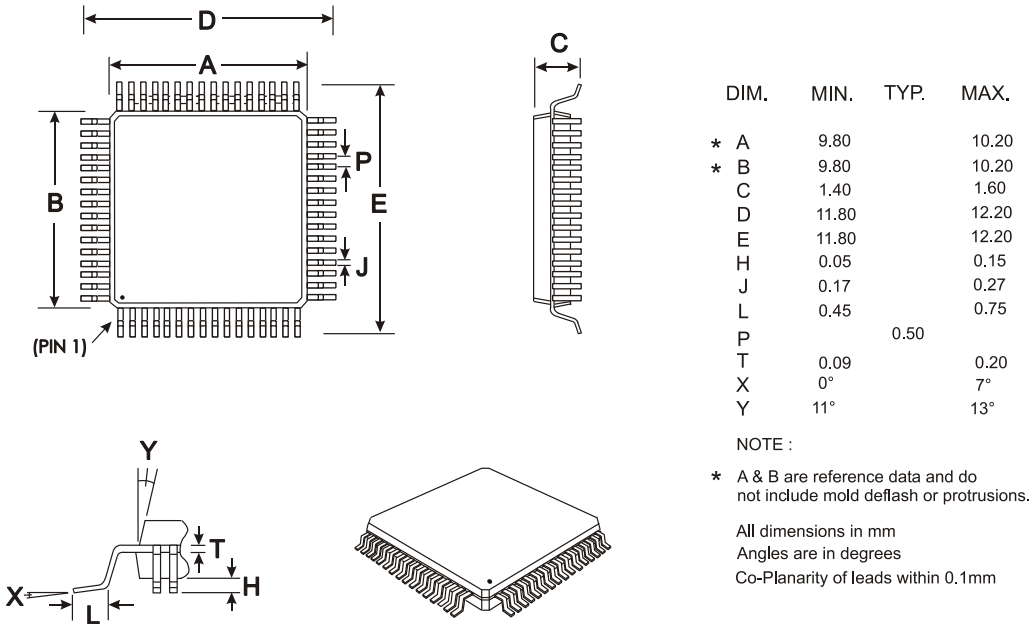
NOTE :
* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 28 Mechanical Outline of 64-pin VQFN (Q1)

Order as part no. CMX7261Q1



DIM.	MIN.	TYP.	MAX.
* A	9.80		10.20
* B	9.80		10.20
C	1.40		1.60
D	11.80		12.20
E	11.80		12.20
H	0.05		0.15
J	0.17		0.27
L	0.45		0.75
P		0.50	
T	0.09		0.20
X	0°		7°
Y	11°		13°

NOTE :
* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees
Co-Planarity of leads within 0.1mm

Figure 29 Mechanical Outline of 64-pin LQFP (L9)

Order as part no. CMX7261L9

As package dimensions may change after publication of this datasheet, it is recommended that you check for the latest Packaging Information from the Datasheets page of the CML website: [www.cmlmicro.com].

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