CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CMX7861 *FirmCODEC®*

D/7861_FI-1.x/2 June 2012

DATASHEET

Advance Information

7861FI-1.x Programmable Baseband Interface

Features

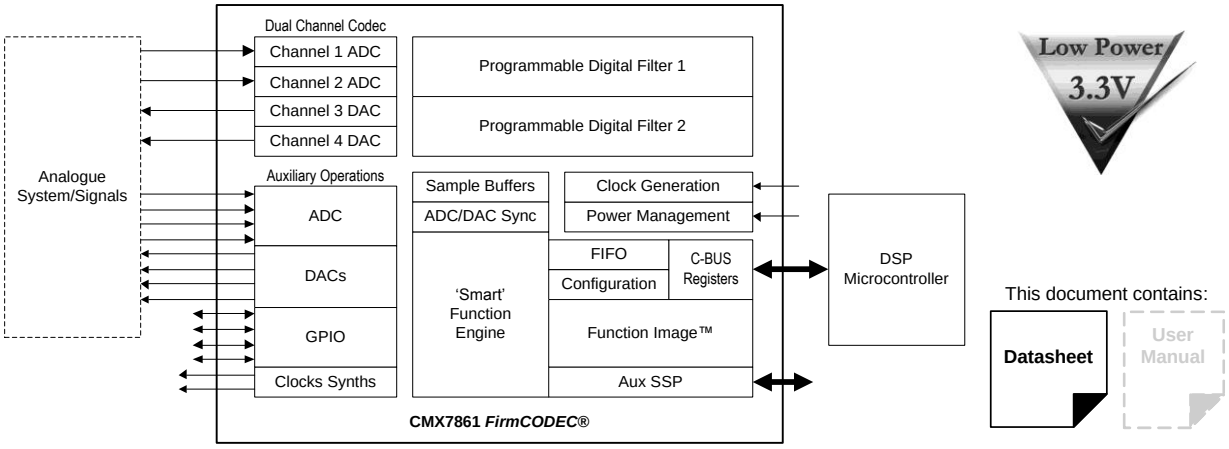
- Dual Channel Codecs
  - Can operate in modem or codec mode
  - Two ADCs 16 bit
  - Two DACs 14 bit
  - Programmable input and output gain
  - Differential/single ended inputs/outputs
- Digital Channel Filters
  - Two fully-programmable digital filters
  - Filter design and configuration support
- Auxiliary ADCs
  - Four 10-bit DACs
  - Autonomous RAMDAC sequencer
- Auxiliary ADC
  - One 10-bit ADC with four-input MUX
  - ADC averaging, trip on high/low 'watch' modes
- Auxiliary GPIO
  - Four programmable input/outputs
- Auxiliary Synthesised Clock Generators
  - Two programmable clock outputs
- C-BUS Host Serial Interface
  - SPI-like with register addressing
  - Read/write 128-byte FIFOs and data buffers
  - Streamline transfers, low host service latency
- Master SSP Interface
  - External slave device control
  - Serial Flash connection
  - Pass-through (Thru-port) mode expands host C-BUS/SPI capacity

Features Cont.

- Low-power 3.0V to 3.6V operation
- Multiple power-saving options
- Small 64-pin VQFN Package
- Evaluation support
  - PE0601-7861 Evaluation kit
  - PE0002 Interface card

Applications

- General-purpose DSP analogue/digital interface
  - Sensors
  - Control systems
  - Telemetry/SCADA/data modems
- High Performance Narrowband Data Radio
  - DMR
  - APCO P25
  - Software Defined Radio (SDR)
  - 6.25kHz to 25kHz RF channel spacings
  - worldwide compatibility e.g. ETSI, FCC, ARIB, FCC Part 90 per spectral efficiency requirements
- High Performance I/Q Radio Interface
  - Tx and Rx: 'direct connect' to zero IF transceiver
  - Simple external RC filters
  - Digital filter configurable for multiple RF channel spacings (Rx), Default is for DMR
  - I/Q trims



1 Brief Description

1.1 General

The CMX7861 FirmCODEC® is a general-purpose, dual-channel baseband interface device for use in DSP-based systems. The device is a combination of codec, embedded signal processing and auxiliary system support functions that, together, allow simple interfacing to analogue and digital systems.

Single-ended and differential interface options are provided and I/Q-based operation is supported. The device can also be used in radio systems operating with channel bandwidths up to 50kHz, interfacing RF devices to baseband DSP/microcontroller, performing the main data conversion and auxiliary operations for monitoring and control.

Fully-programmable on-chip digital channel filters can be utilised for signal conditioning purposes. Intelligent auxiliary ADC, DAC and GPIO sub-systems perform valuable functions and minimise host interaction and host I/O resources. Two synthesised system clock generators develop clock signals for off-chip use. The C-BUS/SPI master interface expands host C-BUS/SPI ports to control external devices.

The CMX7861 utilises CML's proprietary *FirmASIC*® component technology that enables on-chip sub-systems to be configured by a Function Image™ data file, which is uploaded during device initialisation and defines the device's function and feature set. The Function Image™ can be loaded automatically from a host µC over the C-BUS serial interface or from an external memory device. The device's functions and features can be enhanced by subsequent Function Image™ releases, facilitating in-the-field upgrades.

The CMX7861 operates from a 3.3V supply and includes selectable power saving modes. It is available in a 64-VQFN package.

1.2 Codec and Modem Modes

Two general modes of operation are supported: codec mode and modem mode.

Codec mode is intended for applications where a general purpose codec is required. When in codec mode the CMX7861 will provide digital-to-analogue and analogue-to-digital conversion, producing a flat pass band over the sampled bandwidth. Simple programmable transmit and receive filter options are provided but there are no signal interpolation facilities available, and the maximum sample rate is limited.

Modem mode is suited to applications where the CMX7861 is used to transmit modulated data and receive that data. Modem mode provides a transmit signal interpolator which will aid in the modulation process by converting mapped symbols to a filtered, modulated output. Receive channel filters are also provided, however filter design is more complex than codec mode as ADC and DAC roll off need to be considered when designing filters. Modem mode is, in general, more efficient than codec mode and is capable of providing a higher sample rate.

This datasheet is the first part of a two-part document.

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Information in this datasheet should not be relied upon for final product design. It is always recommended that you check for the latest product datasheet version from the CML website: [www.cmlmicro.com].

1.3 History

Version	Changes	Date
2	Note 32 expanded and Note 48 added in section 8.1.3, to cover dc operation	May 2012
1	First issue	Dec 2011

2 Block Diagrams

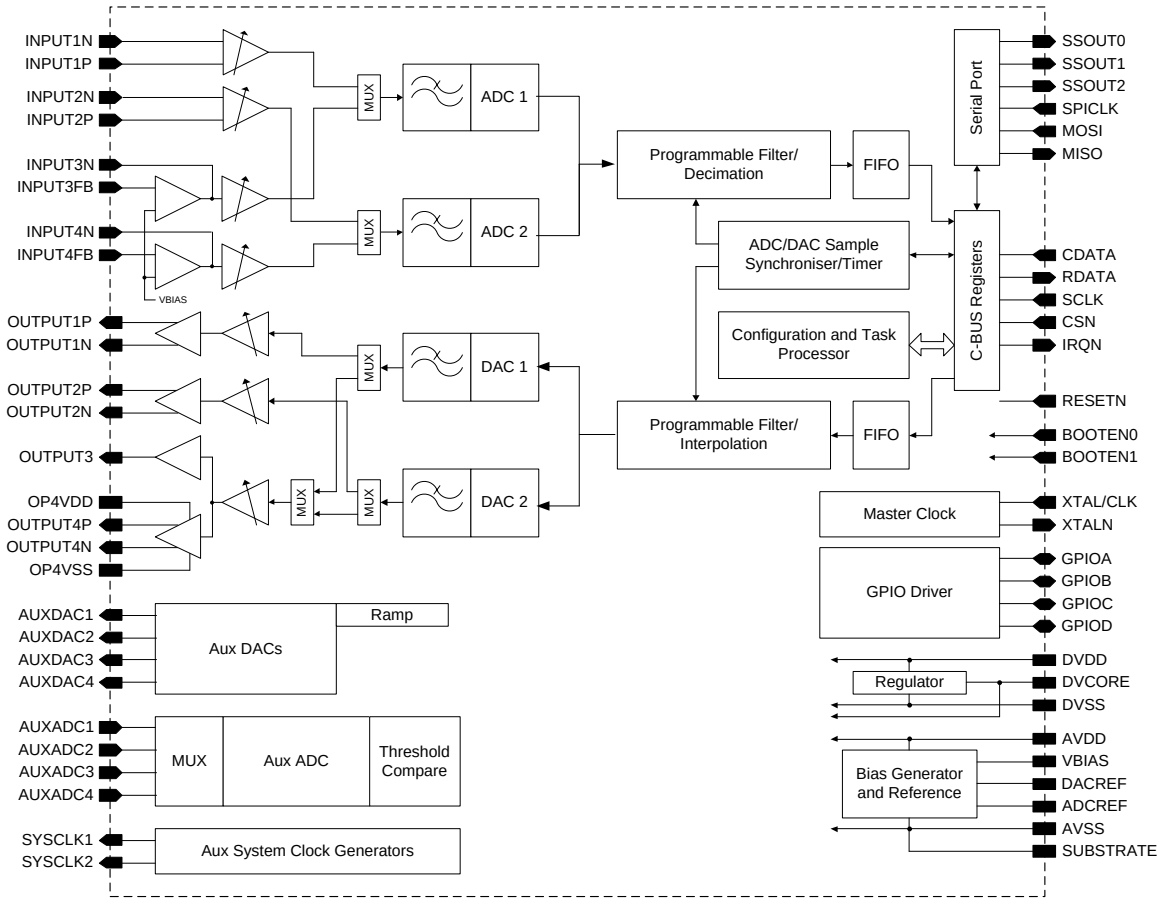


Figure 1 Overall Block Diagram

Figure 1 Illustrates the overall functionality of the CMX7861 and the auxiliary functions.

3 Signal/Pin List

Table 1 Signal/Pin List

Pin	Pin Name	Type	Description
1	GPIOB	BI	General Purpose I/O.
2	BOOTEN1	IP+PU	The combined state of BOOTEN1 and BOOTEN2, upon RESET, determine the Function Image™ load interface.
3	BOOTEN2	IP+PU	
4	DVSS1	PWR	Negative supply rail (ground) for the digital on-chip circuits.
5	DVDD1	PWR	3.3V positive supply rail for the digital on-chip circuits. This pin should be decoupled to DVSS by capacitors mounted close to the device pin.
6	SSOUT2	OP	SPI: Slave Select Out 2
7	RESETN	IP	Logic input used to reset the device (active low).
8	GPIOC	BI	General Purpose I/O.
9	GPIOD	BI	General Purpose I/O.
10	DVSS2	PWR	Negative supply rail (ground) for the digital on-chip circuits.
11	OUTPUT3	OP	Single ended analogue signal output.
12	AVDD1	PWR	Positive 3.3V supply rail for the analogue on-chip circuit. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to AV_{SS} by capacitors mounted close to the device pin.
13	OP4VSS	PWR	Negative supply rail (ground) for the on-chip speaker driver circuit.
14	OUTPUT4P	OP	Low impedance differential output speaker driver. Together these are referred to as Output 4.
15	OUTPUT4N	OP	
16	OP4VDD	PWR	Positive supply rail for on-chip speaker driver circuit. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to OP4VSS by capacitors mounted close to the device pin.
17	OUTPUT1P	OP	Differential outputs; ‘P’ is positive, ‘N’ is negative. Together these are referred to as Output 1. Can also be used as the ‘I’ output in an I/Q based system.
18	OUTPUT1N	OP	
19	OUTPUT2P	OP	Differential outputs; ‘P’ is positive, ‘N’ is negative. Together these are referred to as Output 2. Can also be used as the ‘Q’ output in an I/Q based system.
20	OUTPUT2N	OP	
21	AVSS2	PWR	Negative supply rail (ground) for the analogue on-chip circuits
22	DACREF	PWR	DAC reference voltage, connect to AVss.
23	INPUT3N	IP	Negative input ‘N’ and feedback ‘FB’ connections to a single ended amplifier. Together these are referred to as Input 3. Gain and filtering circuitry can be constructed around these pins.
24	INPUT3FB	OP	

Pin	Pin Name	Type	Description
25	INPUT4N	IP	Negative input 'N' and feedback 'FB' connections to a single ended amplifier. Together these are referred to as Input 4. Gain and filtering circuitry can be constructed around these pins.
26	INPUT4FB	OP	
27	VBIAS	OP	Internally generated bias voltage of approximately $AV_{DD}/2$. If V_{BIAS} is powersaved this pin will be connected via a high impedance to AV_{DD}. This pin must be decoupled to AV_{SS} by a capacitor mounted close to the device pin.
28	INPUT1P	IP	Differential inputs; 'P' is positive, 'N' is negative. Together these are referred to as Input 1. Can also be used as the 'I' Input in an I/Q based system.
29	INPUT1N	IP	
30	ADCREF	PWR	ADC reference voltage, connect to $AV_{SS.}$
31	INPUT2P	IP	Differential inputs; 'P' is positive, 'N' is negative. Together these are referred to as Input 2. Can also be used as the 'Q' Input in an I/Q based system.
32	INPUT2N	IP	
33	AUXADC1	IP	Auxiliary ADC inputs multiplexed to a single ADC with Threshold and Compare operations.
34	AUXADC2	IP	
35	AUXADC3	IP	
36	AUXADC4	IP	
37	AVDD3	PWR	Positive 3.3V supply rail for the analogue on-chip circuit. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to AV_{SS} by capacitors mounted close to the device pin.
38	AVSS3	PWR	Negative supply rail (ground) for the analogue on-chip circuits.
39	AUXDAC1	OP	Auxiliary DAC outputs with DAC1 output having an optional ramping RAMDAC operation.
40	AUXDAC2	OP	
41	AUXDAC3	OP	
42	AUXDAC4	OP	
43	DVSS3	PWR	Negative supply rail (ground) for the digital on-chip circuits
44	DVCORE1	PWR	Digital core supply, nominally 1.8V. This pin should be decoupled to DV_{SS} by capacitors mounted close to the device pins and connected with a power supply track to DVCORE2.
45	DVDD2	PWR	3.3V positive supply rail for the digital on-chip circuits. This pin should be decoupled to DV_{SS} by capacitors mounted close to the device pin.
46	NC	NC	Do not connect.
47	DVSS4	PWR	Negative supply rail (ground) for the digital on-chip circuits.
48	DVSS5	PWR	Negative supply rail (ground) for the digital on-chip circuits.
49	XTALN	OP	Output of the on-chip Xtal oscillator inverter.
50	XTAL/CLK	IP	Input to the oscillator inverter from the Xtal circuit or external clock source.
51	SYSCLK1	OP	Synthesised digital clock output 1.

Pin	Pin Name	Type	Description
52	SYSCLK2	OP	Synthesised digital clock output 2.
53	SCLK	IP	C-BUS serial clock input from the µC.
54	RDATA	TS OP	Three-state C-BUS serial data output to the µC. This output is high impedance when not sending data to the µC.
55	CDATA	IP	C-BUS serial data input from the µC.
56	CSN	IP	C-BUS chip select input from the µC.
57	IRQN	OP	'wire-Orable' output for connection to the Interrupt Request input of the µC. This output is pulled down to DV_{SS} when active and is high impedance when inactive. An external pull-up resistor is required.
58	DVCORE2	PWR	Digital core supply, nominally 1.8V. This pin should be decoupled to DV_{SS} by capacitors mounted close to the device pins, and connected, with a power supply track, to DVCORE1.
59	MOSI	OP	SPI: Master Out Slave In.
60	SSOUT1	OP	SPI: Slave Select Out 1.
61	MISO	IP	SPI: Master In Slave Out.
62	SSOUT0	OP	SPI: Slave Select Out 0.
63	SPICLK	OP	SPI: Serial Clock.
64	GPIOA	BI	General Purpose I/O.
EXPOSED METAL PAD	SUBSTRATE	~	On this device, the central metal pad may be electrically unconnected or, alternatively, may be connected to analogue ground (AVss). **No other electrical connection is permitted.**

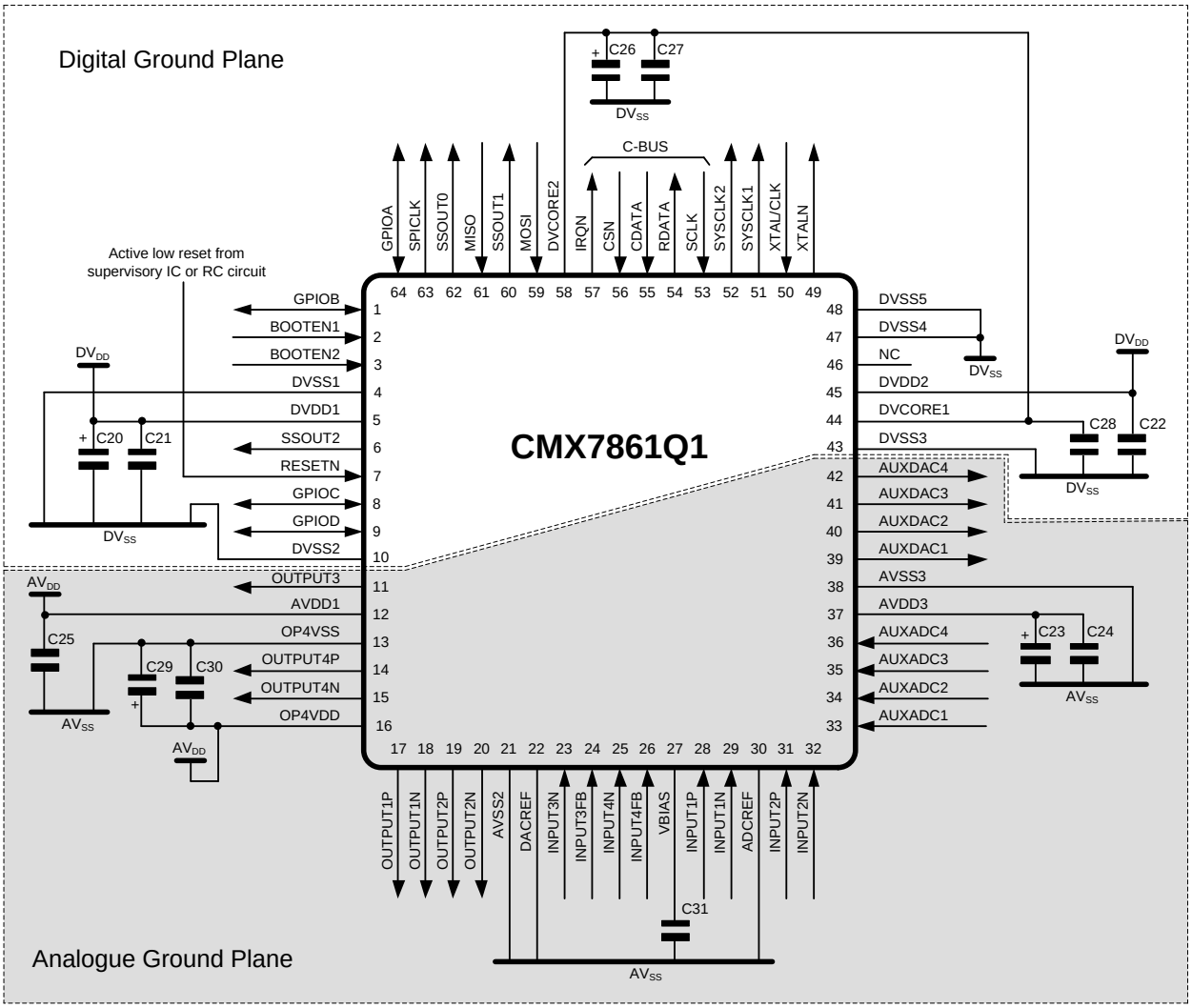
Notes:
IP = Input (+ PU/PD = internal pull-up / pull-down resistor of approximately 75kΩ)
OP = Output
BI = Bidirectional
TS OP = Three-state Output
PWR = Power Connection
NC = No Connection - should NOT be connected to any signal

3.1 Power Supply Signal Definitions

Table 2 Definition of Power Supply and Reference Voltages

Signal Name	Pin name	Usage
AV_{DD}	AVDD1, AVDD2, AVDD3	Power supply for analogue circuits
DV_{DD}	DVDD1, DVDD2	Power supply for digital circuits, nominally 3.3V
DV_{core}	DVCORE1, DVCORE2	Power for digital core voltage of approximately 1.8V
V_{BIAS}	VBIAS	CMX7861 generated bias voltage of approximately $AV_{DD}/2$
DV_{SS}	DVSS1, DVSS2, DVSS3, DVSS4, DVSS5	Ground for digital circuits
AV_{SS}	AVSS1, AVSS2, AVSS3, SUBSTRATE (Optional) DACREF, ADCREF	Ground for analogue circuits

4 PCB Layout Guidelines and Power Supply Decoupling



C20	10µF	C26	22µF
C21	10nF	C27	10nF
C22	10nF	C28	10nF
C23	10µF	C29	10µF
C24	10nF	C30	10nF
C25	10nF	C31	100nF

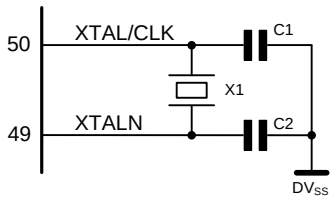
Figure 2 CMX7861 Power Supply and De-coupling

Notes:

To achieve good noise performance, AV_{DD} and V_{BIAS} decoupling and protection of the receive path from extraneous in-band signals is very important. It is recommended that the printed circuit board is laid out with a ground plane in the CMX7861 analogue area to provide a low impedance connection between the AV_{SS} pins and the AV_{DD} and V_{BIAS} decoupling capacitors.

5 External Components

5.1 Xtal Interface



X1 For frequency range see 8.1.2 Operating Limits
C1 22pF typical
C2 22pF typical

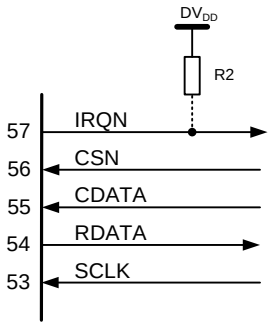
Figure 3 Recommended External Components - Xtal Interface

Notes:
The clock circuit can operate with either a Xtal or external clock generator. If using an external clock generator it should be connected to the XTAL/CLK pin and the Xtal and other components are not required. For external clock generator frequency range see 8.1.2 Operating Limits. When using an external clock generator the Xtal oscillator circuit may be disabled to save power, see 9.2.3 Program Block 1 – Clock Control for details. Also refer to section 7.1 Xtal Frequency.

The tracks between the Xtal and the device pins should be as short as possible to achieve maximum stability and best start up performance. It is also important to achieve a low impedance connection between the Xtal capacitors and the ground plane.

The DV_{SS} to the Xtal oscillator capacitors C1 and C2 should be of low impedance and preferably be part of the DV_{SS} ground plane to ensure reliable start up. For correct values of capacitors C1 and C2 refer to the documentation of the Xtal used.

5.2 C-BUS Interface



R2 10kΩ - 100kΩ

Figure 4 Recommended External Components - C-BUS Interface

Note:
If the IRQN line is connected to other compatible pull-down devices only one pull-up resistor is required on the IRQN node.

5.3 Signal Output

5.3.1 Output Signal Routing

The CMX7861 has four possible analogue outputs:

- Differential output 1 - OUTPUT1P and OUTPUT1N (or I output for an I/Q-based system)
- Differential output 2 - OUTPUT2P and OUTPUT2N (or Q output for an I/Q-based system)
- Single-ended output 3 – OUTPUT3 that can drive headset/earpieces
- Differential output 4 – OUTPUT4P and OUTPUT4N – a low-impedance speaker driver

The CMX7861's two DACs (DAC 1 and DAC 2) can output analogue waveforms on any or all of these four outputs. CMX7861 allows us to connect the two DACs to any of the four analogue outputs.

Due to the highly-flexible nature of the CMX7861 and the multitude of input and output configurations, it is important to clearly understand the differences between Pin/Signal names, and the internal signal streams controlled by most of the registers. To help clarify this situation, the following convention has been used throughout the text and on diagrams within this document:

- Outputs from the device to external systems will be referred to as OUTPUT1, 2, 3, or 4. Where appropriate, OUTPUT 1 and 2 may also be referred to as I and Q outputs respectively (if the description is specifically for an I/Q-based system).
- Internal signal streams routed to the four outputs and processed by the two DACs will be referred to as DAC1 and/or DAC2 samples.

Figure 5 Analogue Output Routing, shows the analogue output signal routing and control.

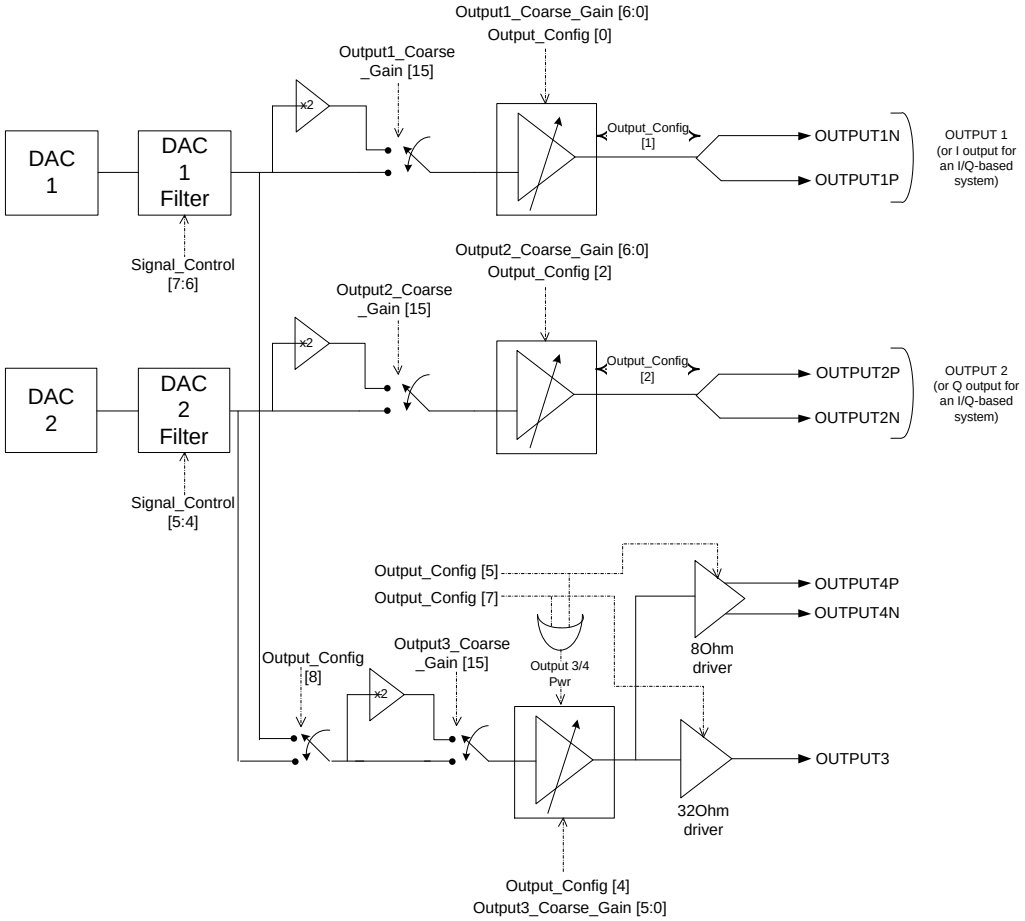


Figure 5 Analogue Output Routing

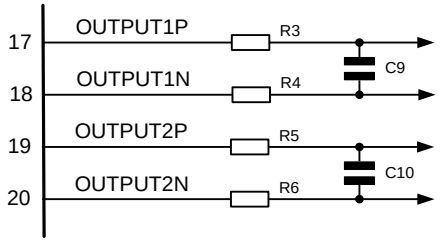
The registers that control analogue output signal routing are described in the following sections:

- 9.1.10 Signal Control - $61 write
- 9.1.21 Output 1 - 4 Configuration - $B3 write
- 9.1.22 Output 1 and 2 Coarse Gain - $B4, $B5 write
- Include Output3 coarse gain register here when it is defined

5.3.2 Output Reconstruction Filter – (I/Q mode)

When output 1 (or I) and output 2 (or Q) are used as I/Q outputs, internal reconstruction filtering is provided with four selectable bandwidths (-3dB point shown in section 9.1.21). The bandwidth of the internal reconstruction filter may be selected using the Output 1 - 4 Configuration - $B3 write or Signal Control - $61 write registers.

To complete the output reconstruction filter one of the following external RC networks should be used for each of the differential outputs. The external RC network should have a bandwidth that matches the bandwidth of the selected internal reconstruction filter.



Bandwidth (kHz)	R3-R6 (kOhms)	C9-C10 (pF)
100	22	33
50	20	75
25	22	150
12.5	22	270

Figure 6 Recommended External Components – I/Q Output Reconstruction Filter

When transmitting an I/Q signal, each I/Q output will produce a signal with bandwidth half the channel bandwidth. A reconstruction filter with a –3dB point close to half the channel bandwidth will therefore have significant roll off within the channel bandwidth – which is undesirable. An appropriate choice for channels occupying up to a 12.5kHz bandwidth (channel bandwidth/2 = 6.25kHz) would be a reconstruction filter of 12.5kHz bandwidth.

5.3.3 Output Reconstruction Filter – Single-ended Outputs

To complete the output reconstruction filter one of the following external RC networks should be used for each of the single-ended outputs. The external RC network should have a bandwidth that matches the bandwidth of the selected internal reconstruction.

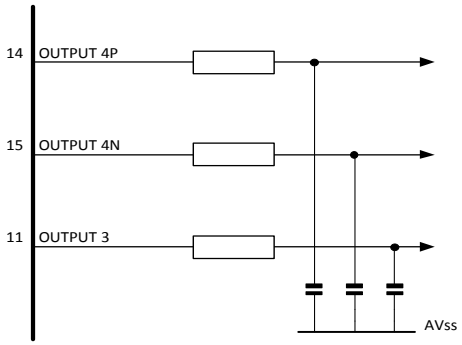


Figure 7 Recommended External Components - Single-ended Outputs Reconstruction Filter

5.4 Signal Input

5.4.1 Input Signal Routing

The CMX7861 has four possible analogue input paths:

- Differential input 1 - INPUT1P and INPUT1N (or I input for an I/Q-based system)
- Differential input 2 – INPUT2P and INPUT2N (or Q input for an I/Q-based system)
- Single-ended input 3 – INPUT3N and INPUT3FB
- Single-ended input 4 – INPUT4N and INPUT4FB

The CMX7861's two ADCs (ADC1 and ADC2) can sample up to two of these inputs. The CMX7861 allows us to connect these four inputs to the two ADCs.

Due to the highly-flexible nature of the CMX7861 and the multitude of input and output configurations, it is important to clearly understand the differences between Pin/Signal names, and the internal signal streams controlled by most of the registers. To help clarify this situation, the following convention has been used throughout the text and on diagrams within this document:

- Inputs to the device from external systems will be referred to as INPUT1, 2, 3, or 4. Where appropriate, INPUT 1 and 2 may also be referred to as I and Q inputs respectively (if the description is specifically for an I/Q-based system).

- Internal signal streams routed from the four inputs and processed by the two ADCs will be referred to as ADC1 and/or ADC2 samples.

Figure 8 Analogue Input Routing, shows the analogue input signal routing and control.

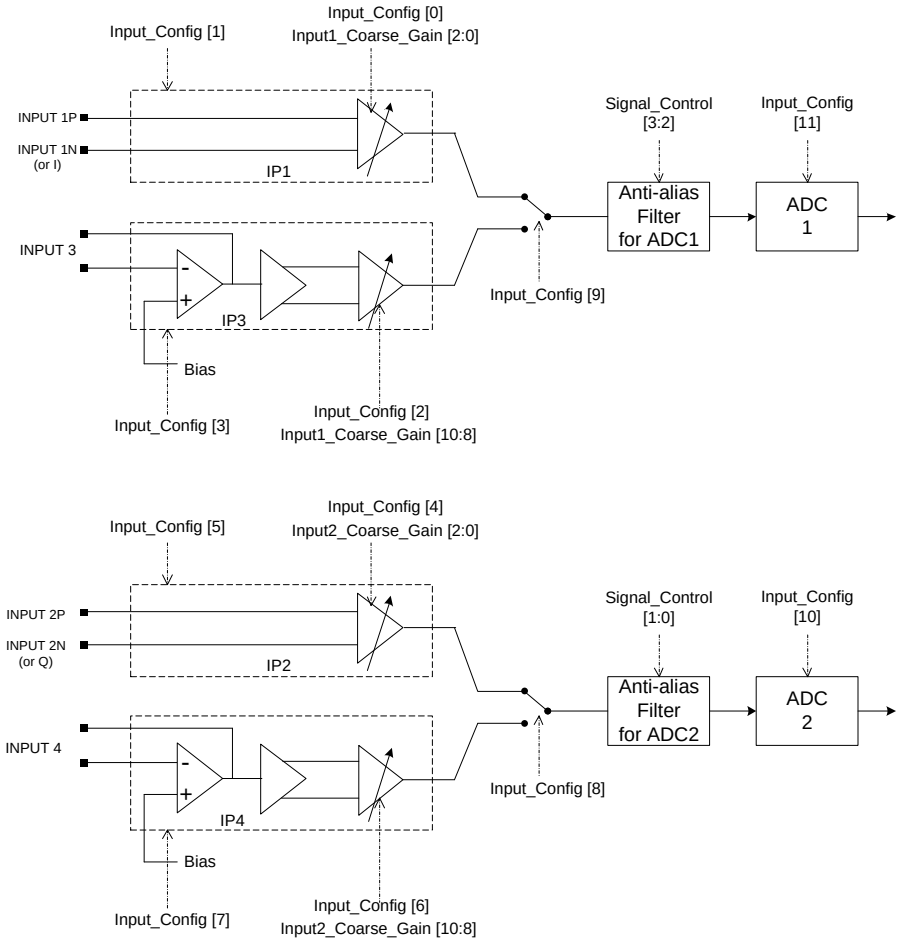


Figure 8 Analogue Input Routing

The registers that control analogue input signal routing are described in the following sections:

- 9.1.10 Signal Control - $61 write
- 9.1.19 Input 1 - 4 Configuration - $B0 write
- 9.1.20 Input 1-4 Coarse Gain - $B1, $B2 write

5.4.2 Input Anti-alias Filter (I/Q mode)

When Input 1 (I) and Input 2 (Q) are used as the inputs to ADCs 1 and 2, the device has a programmable anti-alias filter in the input path, which is controlled using the Input 1 - 4 Configuration - $B0 write or Signal Control - $61 write registers. This should be sufficient for most applications, however if additional filtering is required it can be done at the input to the device.

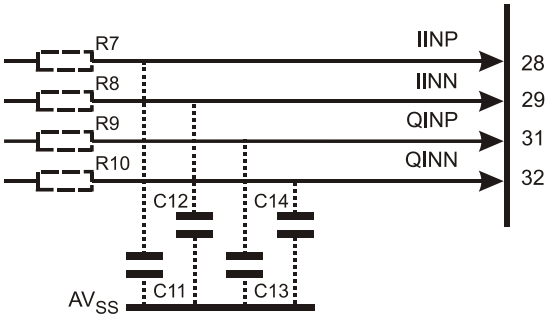
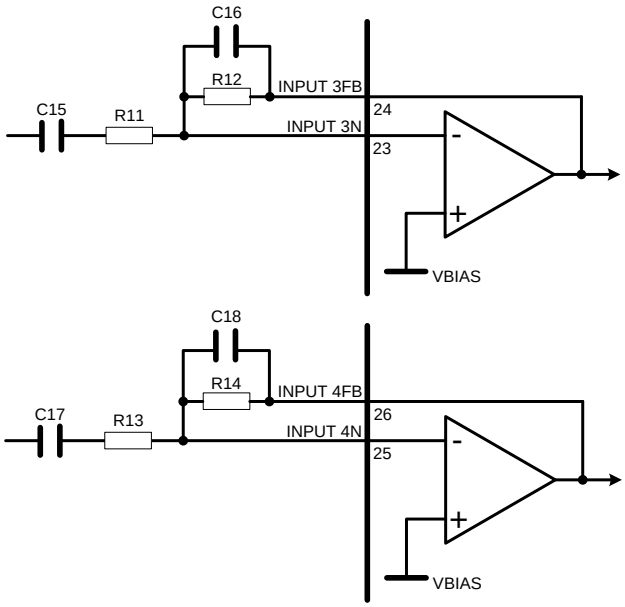


Figure 9 Input Anti-alias FIlter: Inputs 1 and 2

The input impedance of pins 28 to 32 varies with the input gain setting, approx 14kOhm at +22.4dB rising to 100kOhm at 0dB. The output impedance of the circuit driving the inputs shown above should be no more than approximately 1kOhm, for the above RC network R7-10 <= approx. 1kOhm. Recommended values for R7-10 and C11-14 will depend on the filtering required.

5.4.3 Input Anti-alias Filter (Inputs 3 and 4)



C15	See note	C17	See note
C16	100pF	C18	100pF
R11	See note	R13	See note
R12	100kΩ	R14	100kΩ

Figure 10 Input Anti-alias FIlter: Inputs 3 and 4

Notes:

Assuming R12 and R14 at 100kOhm, R11 and R13 should be selected to provide the required dc gain (assuming C15 and C17 are not present) as follows:

$$|GAIN_{AUDIO1}| = 100k\Omega / R11$$

$$|GAIN_{AUDIO2}| = 100k\Omega / R13$$

The gain should be such that the resultant output at the pins is within the input signal range.

C15 and C17 should be selected to maintain the lower frequency roll-off of the AUDIO inputs as follows:

$$C15 \geq 0.1\mu F \times |GAIN_{AUDIO1}|$$

$$C17 \geq 0.1\mu F \times |GAIN_{AUDIO2}|$$

The High Frequency cut off = ~ 16KHz $\left(\frac{1}{2\pi . R_{14} C_{18}} \right)$

The Low Frequency cut off = ~ 16 Hz $\left(\frac{1}{2\pi . R_{13} C_{17}} \right)$

6 General Description

6.1 CMX7861 Features

The CMX7861 *FirmCODEC*® is a general-purpose, dual-channel baseband interface device for use in DSP-based systems and supports duplex operation of two ADC and two DAC channels. Flexibility is the key to the device with target applications being sensors, control and monitoring systems and providing an interface to RF systems.

The device is highly configurable with selectable single-ended and differential inputs and outputs plus the ability to operate in I/Q mode.

A flexible power control facility allows the device to be placed in its optimum powersave mode when not actively processing signals.

On-chip auxiliary functions include: an Xtal clock generator with phase locked loop and buffered output to provide a system clock output (if required) for other devices, a multiplexed input ADC, DAC outputs and GPIO.

Fully-programmable on-chip digital channel filters can be used for signal conditioning purposes prior to passing data to the host DSP. The C-BUS/SPI master interface expands host C-BUS/SPI ports to control external devices.

Block diagrams of the device are shown in section 2.

Note: In the list below, the greyed-out text indicates future planned updates

Tx Functions:

- Single-ended and differential analogue outputs
- Interpolation stage with filtering – providing pulse shape filtering for mapped symbols
- RAMDAC capability for PA ramping control
- Tx trigger feature allowing precise control of burst start time
- Tx burst sequence for automatic RAMDAC ramp and Tx hardware switching

Rx Functions:

- Single-ended and differential analogue inputs
- Rx channel filtering
- Received signal strength indication (RSSI)
- I/Q and Phase/Magnitude output formats for FM systems
- AGC using SPI Thru-Port

Auxiliary Functions:

- Two programmable system clock outputs
- Auxiliary ADC with four selectable input paths
- SPI Thru-Port for interfacing to synthesisers, a Cartesian loop IC (CMX998) and/or other serially-controllable devices
- Four auxiliary DACs, one with built-in programmable RAMDAC

Interface:

- Optimised C-BUS (4-wire, high-speed synchronous serial command/data bus) interface to host for control and data transfer, including streaming C-BUS for efficient data transfer
- Open drain IRQ to host
- Four GPIO pins
- Tx trigger input (provided by GPIOA)
- Serial memory or C-BUS (host) boot mode

6.2 Signal Interfaces

The CMX7861 *FirmCODEC* IC can be used to provide any interface the user requires depending on the data supplied to the device. Typical interfaces are baseband, I/Q and phase/magnitude.

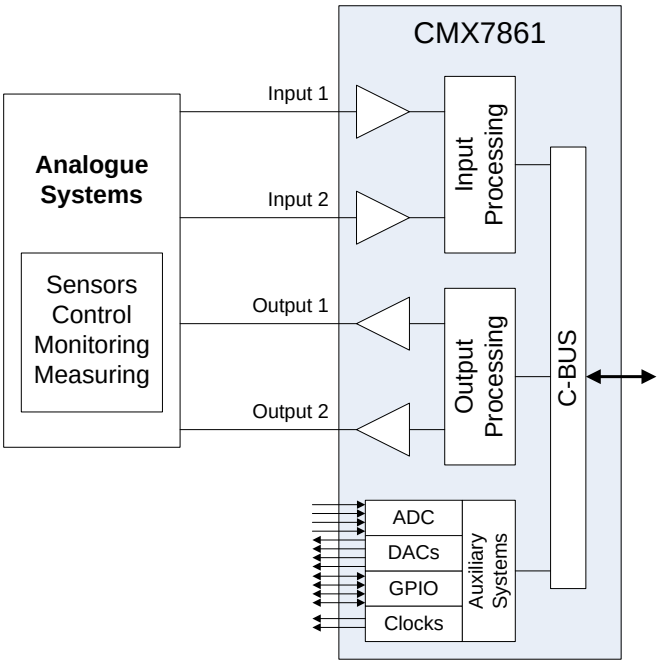


Figure 11 CMX7861 Interface to Analogue Systems

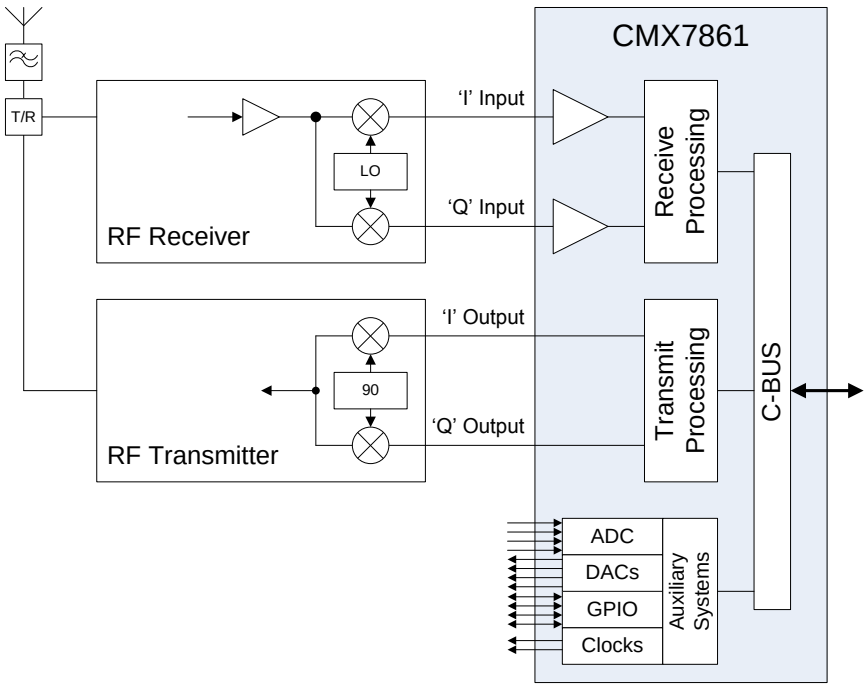


Figure 12 CMX7861 I/Q Tx, I/Q Rx

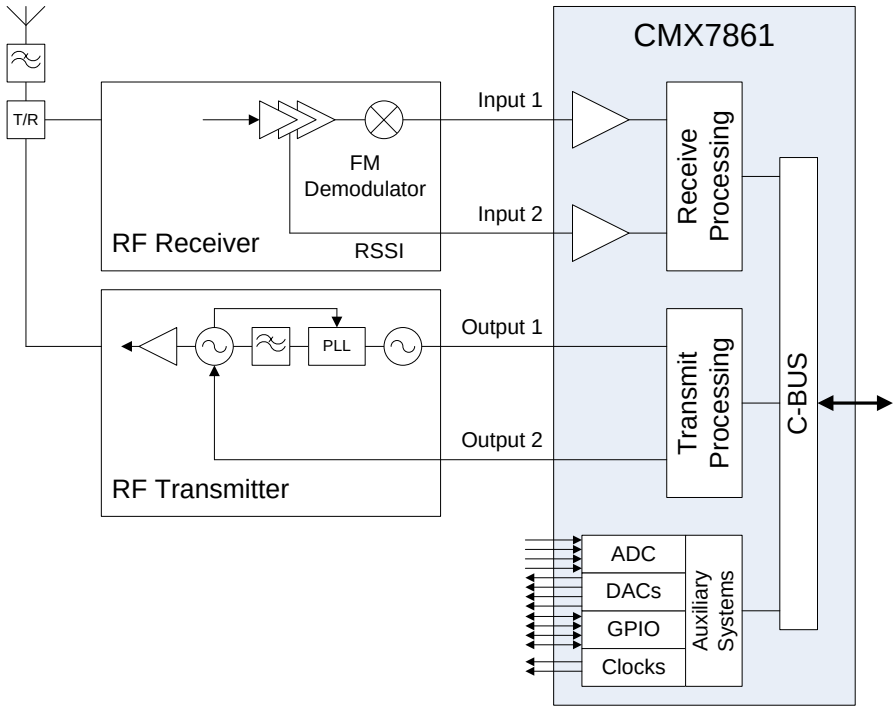


Figure 13 CMX7861 Two-point Tx, Classic FM Limiter-Discriminator Rx

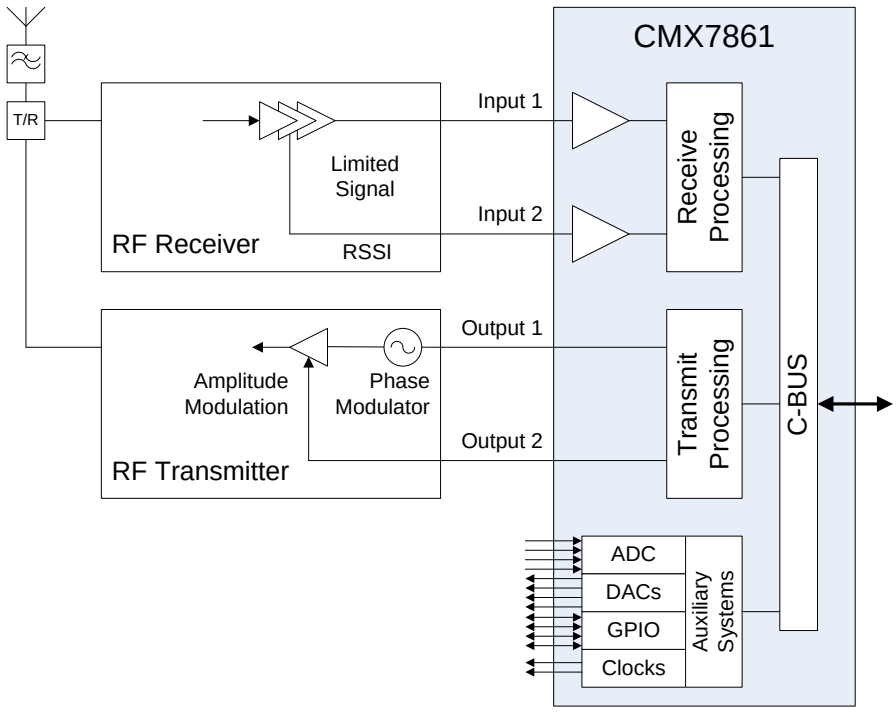


Figure 14 CMX7861 Polar Tx, Amplitude and Phase Rx

7 Detailed Descriptions

7.1 Xtal Frequency

The CMX7861 is designed to work with a Xtal, or an external frequency oscillator within the ranges specified in section 8.1.3 Operating Characteristics. Program Block 1 (see User Manual) must be loaded with the correct values to ensure that the device will work to specification with the user-selected clock frequency. A table of configuration values can be found in Table 17 Xtal/Clock Frequency Settings for Program Block 1, supporting sample rates up to 144k samples per second when the Xtal frequency is 9.6MHz or the external oscillator frequency is 9.6 or 19.2 MHz. Rates other than those tabulated (within this range) are possible, see section 9.2.3 Program Block 1 – Clock Control. Further information can be provided on request. The accuracy of the sample rates provided is affected by the accuracy of the Xtal or oscillator used.

7.2 Host Interface

A serial data interface (C-BUS) is used for command, status and data transfers between the CMX7861 and the host µC; this interface is compatible with Microwire™, SPI™ and other similar interfaces. Interrupt signals notify the host µC when a change in status has occurred; the µC should read the IRQ Status register across the C-BUS and respond accordingly. Interrupts only occur if the appropriate mask bit has been set, see 7.4.5 Interrupt Operation.

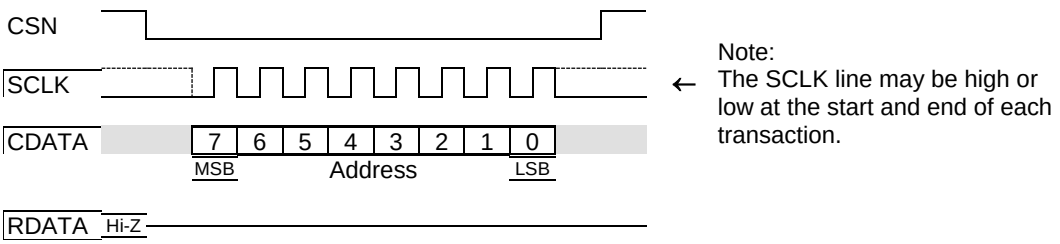
7.2.1 C-BUS Operation

This block provides for the transfer of data and control or status information between the CMX7861 internal registers and the host µC over the C-BUS serial bus. Single register transactions consist of a single register address byte sent from the µC, which may be followed by a data word sent from the µC to be written into one of the CMX7861's write-only registers, or a data word read out from one of the CMX7861's read-only registers. Streaming C-BUS transactions consist of a single register address byte followed by many data bytes being written to or read from the CMX7861. All C-BUS data words are a multiple of 8 bits wide, the width depending on the source or destination register. Note that certain C-BUS transactions require only an address byte to be sent from the µC, no data transfer being required. The operation of the C-BUS is illustrated in Figure 15.

Data sent from the µC on the CDATA (command data) line is clocked into the CMX7861 on the rising edge of the SCLK input. Data sent from the CMX7861 to the µC on the RDATA (reply data) line is valid when SCLK is high. The CSN line must be held low during a data transfer and kept high between transfers. The C-BUS interface is compatible with most common µC serial interfaces and may also be easily implemented with general purpose µC I/O pins controlled by a simple software routine. Section 8.2 C-BUS Timing gives detailed C-BUS timing requirements.

Note that, due to internal timing constraints, there may be a delay of up to 60µs between the end of a C-BUS write operation and the device reading the data from its internal register.

C-BUS single byte command (no data)



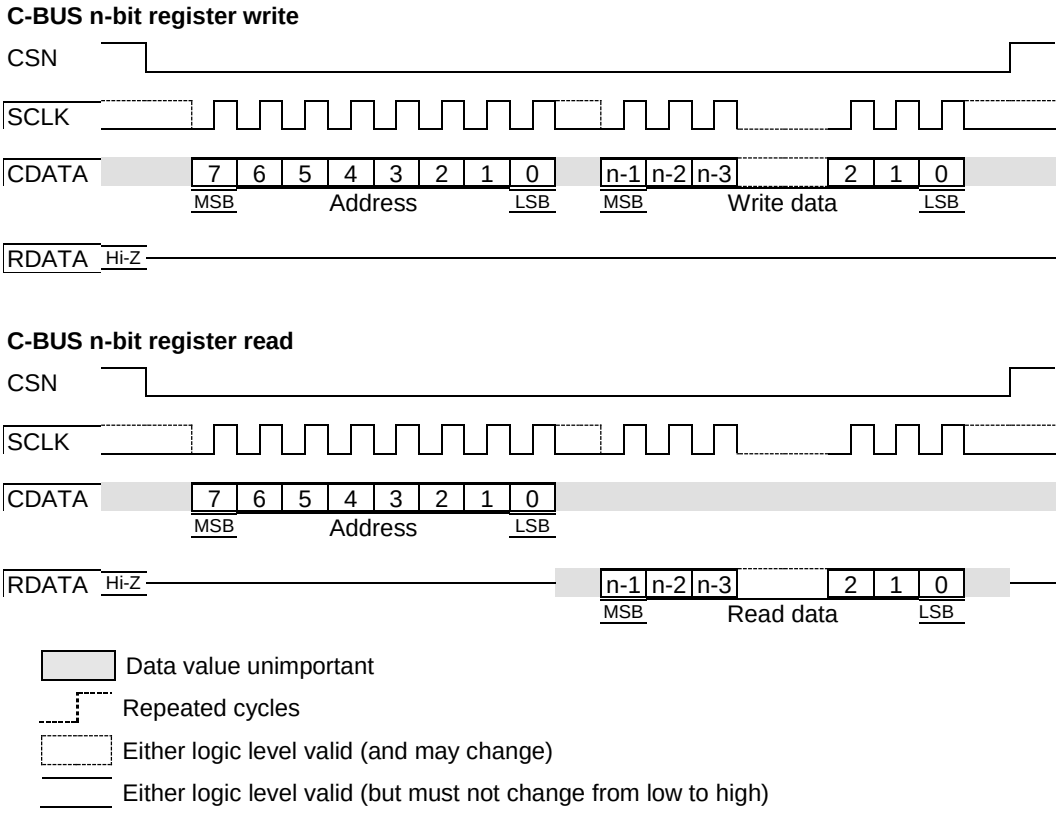
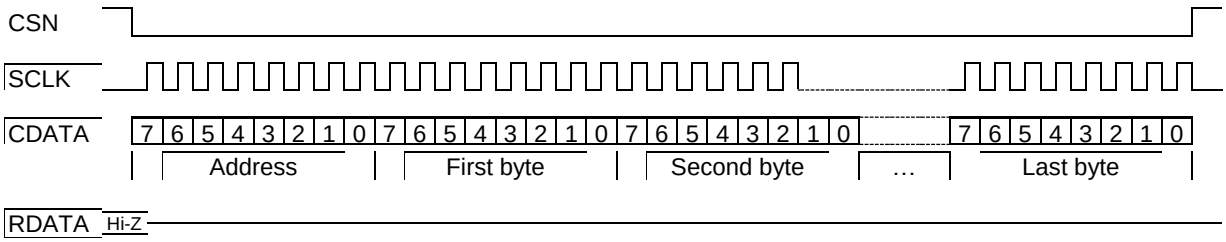


Figure 15 Basic C-BUS Transactions

To increase the data bandwidth between the µC and the CMX7861, certain of the C-BUS read and write registers are capable of data-streaming operation. This allows a single address byte to be followed by the transfer of multiple read or write data words, all within the same C-BUS transaction. This can significantly increase the transfer rate of large data blocks, as shown in Figure 16.

Example of C-BUS data-streaming (8-bit write register)



Example of C-BUS data-streaming (8-bit read register)

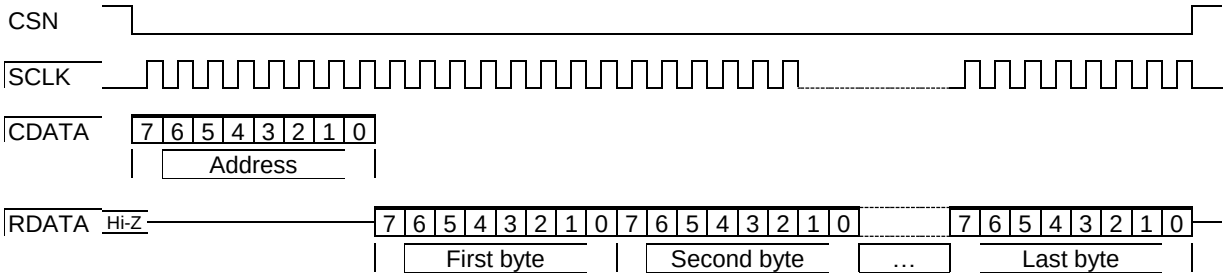


Figure 16 C-BUS Data Streaming Operation

Notes:

1. For Command byte transfers only the first 8 bits are transferred ($01 = Reset)
2. For single byte data transfers only the first 8 bits of the data are transferred
3. The CDATA and RDATA lines are never active at the same time. The address byte determines the data direction for each C-BUS transfer.
4. The SCLK can be high or low at the start and end of each C-BUS transaction
5. The gaps shown between each byte on the CDATA and RDATA lines in the above diagram are optional, the host may insert gaps or concatenate the data as required.

7.3 Function Image™ Loading

The Function Image™ (FI), which defines the operational capabilities of the device, may be obtained from the CML Technical Portal, following registration and authorisation. This is in the form of a 'C' header file which can be included into the host controller software or programmed into an external serial memory. The Function Image™ size will not exceed 128kbytes, although a typical FI will be considerably less than this. Note that the BOOTEN1/2 pins are only read at power-on, when the RESETN pin goes high, or following a C-BUS General Reset, and must remain stable throughout the FI loading process. Once the FI load has completed, the BOOTEN1/2 pins are ignored by the CMX7861 until the next power-up or Reset.

The BOOTEN1 and BOOTEN2 pins are both fitted with internal low-current pull-up devices.

For serial memory load operation, BOOTEN2 should be pulled low by connecting it to DV_{SS} either directly or via a 47k resistor (see Table 3).

Whilst booting, the boot loader will return the checksum of each block loaded in the C-BUS Rx Data FIFO. The checksums can be verified against the values provided with the FI to ensure that the FI has loaded correctly.

Once the FI has been loaded, the CMX7861 performs these actions:

(1) The product identification code ($7861) is reported in the C-BUS Rx Data FIFO
(2) The FI version code is reported in the C-BUS Rx Data FIFO.

Table 3 BOOTEN Pin States

	BOOTEN2	BOOTEN1
C-BUS host load	1	1
reserved	1	0
Serial memory load	0	1
reserved	0	0

7.3.1 FI Loading from Host Controller

The FI can be included into the host controller software build and downloaded into the CMX7861 at power-up over the C-BUS interface, using the Tx FIFO. For Function Image™ load, the FIFO accepts raw 16-bit Function Image™ data (using the Tx FIFO Word) - $49 write register, there is no need for distinction between control and data fields. The BOOTEN1/2 pins must be set to the C-BUS load configuration, the CMX7861 powered or reset, and then data can then be sent directly over the C-BUS to the CMX7861.

If the host detects a brownout, the BOOTEN1 and BOOTEN2 pins should be set to re-load the FI. A General Reset should then be issued or the RESETN pin used to reset the CMX7861 and the appropriate FI load procedure followed.

Streaming C-BUS may be used to load the Tx FIFO Word - $49 write register with the Function Image™, and the Tx FIFO Level - $4B read register used to ensure that the FIFO is not allowed to overflow during the load process.

The download time is limited by the clock frequency of the C-BUS; with a 5MHz SCLK it should take less than 250ms to complete even when loading the largest possible Function Image™.

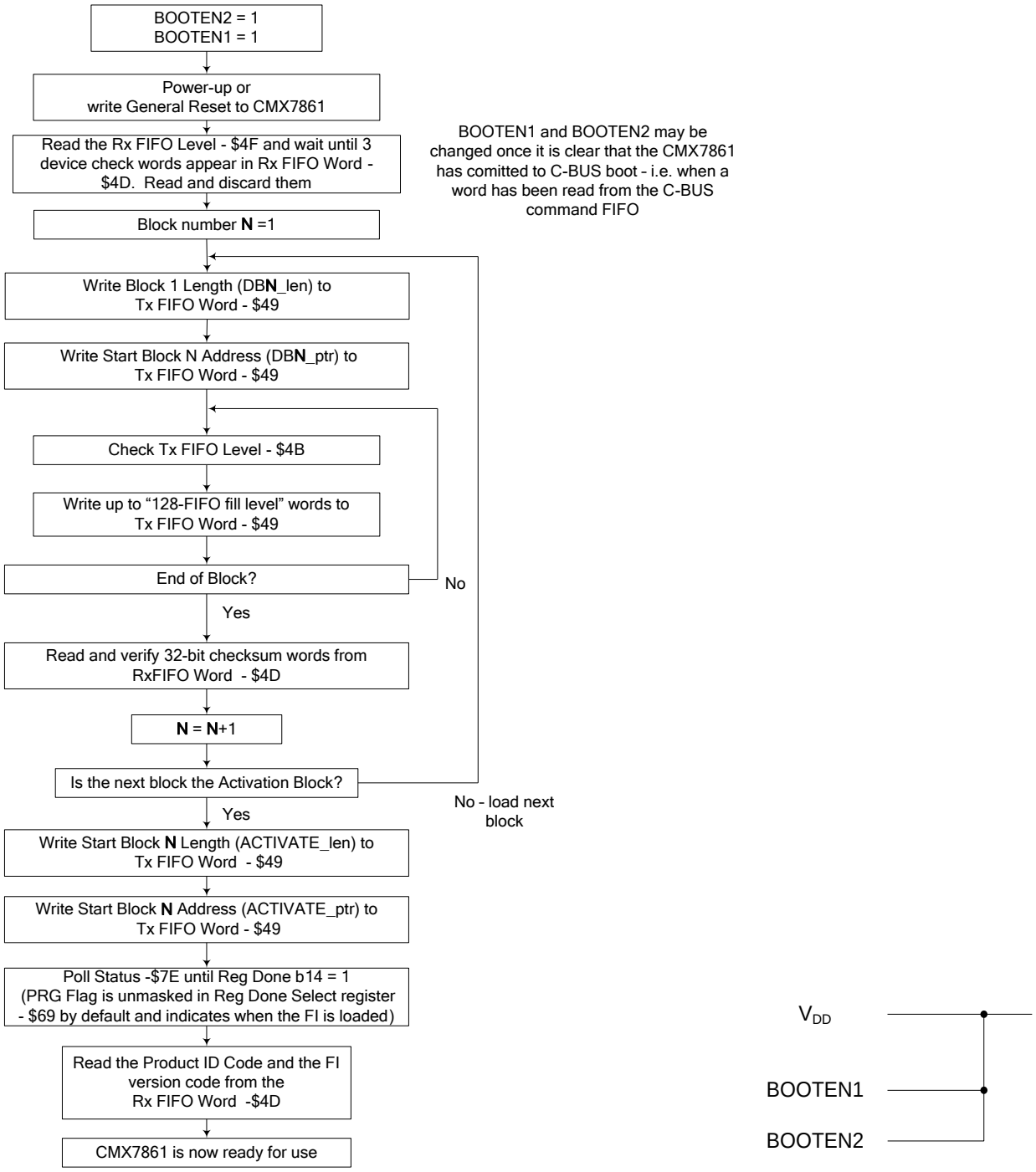


Figure 17 FI Loading from Host

7.3.2 FI Loading from Serial Memory

The FI must be converted into a format for the serial memory programmer (normally Intel Hex) and loaded into the serial memory either by the host or an external programmer. The serial memory should contain the same data stream as written to the Command FIFO shown in Figure 17. The most significant byte of each 16-bit word should be stored first in serial memory.

The serial memory should be interfaced to the CMX7861 SPI Thru-Port using SSOUT0 as the chip select. The CMX7861 needs to have the BOOTEN pins set to Serial Memory Load, and then on power-on following the RESETN pin becoming high, or following a C-BUS General Reset, the CMX7861 will automatically load the data from the serial memory without intervention from the host controller.

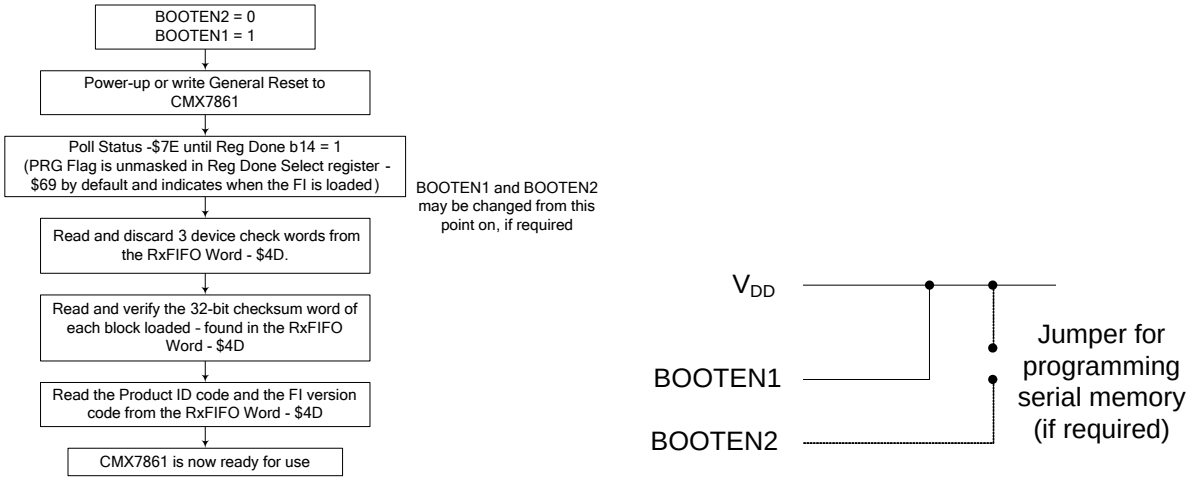


Figure 18 FI Loading from Serial Memory

The CMX7861 has been designed to function with the AT25F512 serial flash device, however other manufacturers' parts may also be suitable. The time taken to load the FI should be less than 500ms even when loading the largest possible Function Image™.

7.4 Device Control

Once the Function Image™ is loaded, the CMX7861 can be set into one of four main modes using the Mode Register- $6B write register:

- Idle mode – for configuration or low power operation
- Transmit mode – DAC operating
- Receive mode – ADC operating
- Duplex mode - DAC and ADC operating.

These four modes are described in the following sections. All control is carried out over the C-BUS interface: either directly to operational registers in transmit, receive and duplex modes or, for parameters that are not likely to change during operation, using the Programming Register - $6A write in Idle mode.

To conserve power when the device is not actively processing a signal, place the device into Idle mode. Additional power-saving can be achieved by disabling unused hardware blocks, however, most of the hardware power-saving is automatic. Note that V_{BIAS} must be enabled to allow any of the Input or Output blocks to function. It is only possible to write to the Programming register whilst in Idle mode. See:

- 9.1.16 Programming Register - $6A write
- 9.1.17 Mode Register- $6B write
- 9.2 Programming Register Operation
- 9.1.24 VBIAS Control - $B7 write.

7.4.1 Normal Operation Overview

In normal operation (after the CMX7861 is configured) the appropriate mode must be selected and samples provided in transmit or retrieved in receive. This process is carried out by selecting the mode (Tx, Rx or Duplex) and selecting which samples are required.

For example, in transmit mode, transmit samples are routed to DAC1 and DAC2 and subsequently to output 1,2,3,or 4.

Output samples should be provided in the Tx FIFO, and samples are received using the Rx FIFO.

The CMX7861 can be configured to interrupt the host on FIFO fill level.

The CMX7861 offers internal buffering of data in addition to the Command and Rx FIFOs in both receive and transmit directions. In the process of burst transmission or reception, the most significant registers are:

- 9.1.17 Mode Register- $6B write
- 9.1.34 IRQ Status - $7E read
- 9.1.18 IRQ Mask - $6C write
- 9.1.3 Tx FIFO Data/Control - $48, $49 and $4A write
- 9.1.26 Receive FIFO Data/Control - $4C, $4D, $4E read
- 9.1.25 Tx FIFO Level - $4B read
- 9.1.27 Receive FIFO Level - $4F read.

7.4.2 Basic Tx and Rx Operation

The CMX7861 has many features that provide a great deal of flexibility, but basic signal transmission and reception can be carried out fairly easily by understanding the operation of just a few registers. There are other ways of controlling signal transmission and reception but basic examples are given below:

Basic Transmit Operation (the DACs are operating)

The following is an example of the transmission of I/Q samples when the device is used in I/Q mode

Note: for this example, a 'DAC1 sample' refers to an I sample, and a 'DAC2' sample refers to a Q sample.

C-BUS Operation	Action	Description
Write $0080 to FIFO Control - $50 write	Flush the Tx FIFO	To ensure that no data is remaining from previous transmissions
Write $8010 to the Tx FIFO Word (see Tx FIFO Data/Control - $48, $49 and $4A write)	Set sample start flag, set DAC1 upper =10	The sample start flag indicates to the CMX7861 that this is the first word of a sample block. The upper byte of the first DAC1 sample =$10.
Write $0020 to the Tx FIFO Word (see Tx FIFO Data/Control - $48, $49 and $4A write)	Clear sample start flag, set DAC1 lower=$20	The high to low transition of the sample start flag indicates to the CMX7861 that this is the second word of a sample block. The lower byte of the first DAC1 sample =$20, so the first DAC1 sample =$1020.
Write 2 DAC2 sample data bytes: $30 and $40 to the TxFIFO Data Byte - see Tx FIFO Data/Control - $48, $49 and $4A write	Complete the sample block	DAC2 upper=$30, DAC2 lower=$40, so the first DAC2 sample=$3040. Streaming C-BUS may be used for faster data loading.
Write 8 groups of 4 data bytes (32 bytes total) to the TxFIFO Data Byte - see Tx FIFO Data/Control - $48, $49 and $4A write	Create a buffer of 8 sample blocks	The sequence DAC1 upper, DAC1 lower, DAC2 upper, DAC2 lower is repeated 8 times, in order to create a buffer, so that the host does not need to write data as promptly for the rest of the transmission. Streaming C-BUS may be used for faster data loading. The sample start flag may be left low.
Write $0043 to Mode Register- $6B write	Start transmission	Initiates a transmission beginning with the first DAC1 and DAC2 sample pair
Poll the Tx FIFO Level - $4B read register, wait until there are less than 32 data bytes in the Tx FIFO	Wait until there is space for new samples to be loaded into the Tx FIFO.	The choice of 32 data bytes as a level is fairly arbitrary – here we want to make sure that there is space for the amount of data that we provide in the next step.
Write 8 groups of 4 data bytes (32 bytes total) to the TxFIFO Data Byte - see Tx FIFO Data/Control - $48, $49 and $4A write	Provide 8 more sample blocks	Provide more samples to continue the transmission. Streaming C-BUS may be used for faster data loading. The sample start flag may be left low. This and the previous step continue for as long as the transmission.
Write $8600 to the Tx FIFO Word (see Tx FIFO Data/Control - $48, $49 and $4A write)	Indicate end of transmission	This indicates to the CMX7861 that DAC1 and DAC2 samples are about to intentionally run out.
Poll the IRQ Status - $7E read register for bit 10 – Tx Done = 1	Wait until the transmission ends	The transmission has completed. It is now possible to transition to other modes, or transmit another burst using the Mode Register- $6B write register.

The procedure described above can be adapted, providing DAC1 or DAC2 samples and servicing the Tx FIFO with different fill levels. The FIFO Control - $50 write, IRQ Status - $7E read and IRQ Mask - $6C write registers can be used to configure the CMX7861 to interrupt the host once the Tx FIFO fill level drops below a specified threshold.

Basic Receive Operation (the ADCs are operating)

The following is an example of receiving I/Q samples when the device is used in I/Q mode

Note: for this example, an 'ADC1 sample' refers to an I sample, and an 'ADC2' sample refers to a Q sample.

C-BUS Operation	Action	Description
Write $8000 to FIFO Control - $50 write	Flush the Rx FIFO	To ensure that no data is remaining from previous sample reception
-	Apply input signal	The input signal should contain a waveform of significant amplitude and within the bandwidth of the CMX7861, given its ADC configuration
Write $0403 to Mode Register- $6B write	Start reception	Initiates reception of ADC1/ADC2 samples. These will propagate through the CMX7861 and become available in the Rx FIFO
Poll the Receive FIFO Level - $4F read register, wait until there are at least 4 data bytes in the Rx FIFO	Wait until there is one sample block in the Rx FIFO	A sample block is available, this will be read in the following steps
Read the Rx FIFO Word – see Receive FIFO Data/Control - $4C, $4D, $4E read	Read start flag, ADC1 upper	Read the Rx FIFO Word register and verify that the most significant bit is set. This indicates the start of a sample block. The lower 8 bits of the value returned are the 8 most significant bits of the ADC1 sample.
Read the Rx FIFO Data Byte register – see Receive FIFO Data/Control - $4C, $4D, $4E read	Read ADC1 lower	Reading the data byte only is more efficient than reading the whole Rx FIFO Word. The value returned is the 8 least significant bits of the ADC1 sample. This step may be combined with the one below using streaming C-BUS to improve efficiency further.
Read the Receive FIFO Data Byte (see Receive FIFO Data/Control - $4C, $4D, $4E read) 2 more times	Retrieve the ADC2 sample: ADC2 upper, ADC2 lower	The ADC2 sample is read from the Receive Data FIFO.
Poll the Receive FIFO Level - $4F read register, wait until there are at least 4 data bytes in the Rx FIFO	Wait until there is a second sample block in the Rx FIFO	A sample block is available, this will be read in the next step
Read the Receive FIFO Data Byte (see Receive FIFO Data/Control - $4C, $4D, $4E read) 4 more times	Retrieve the ADC1 and ADC2 samples: ADC1 upper, ADC1 lower, ADC2 upper, ADC2 lower	Another ADC1/ADC2 sample block is read from the Rx FIFO. Streaming C-BUS may be used to reduce transfer overhead.
-	Repeat as required	The last 2 steps may be repeated as many times as required. It is possible to wait for a higher Rx FIFO fill level, and to stream many sample blocks from the CMX7861 at once.
-	End of reception	Once enough samples have been received a mode change (using the Mode Register- $6B write register) will stop reception.

The procedure described above can be adapted, receiving ADC1 or ADC2 samples and servicing the Rx FIFO with different fill levels. The FIFO Control - $50 write, IRQ Status - $7E read and IRQ Mask - $6C write registers can be used to configure the CMX7861 to interrupt the host once the Rx FIFO fill level rises above a specified threshold.

The registers used for basic transmission and reception are:

- 9.1.17 Mode Register- $6B write
- 9.1.34 IRQ Status - $7E read
- 9.1.3 Tx FIFO Data/Control - $48, $49 and $4A write
- 9.1.26 Receive FIFO Data/Control - $4C, $4D, $4E read
- 9.1.4 FIFO Control - $50 write.

7.4.3 Device Configuration (Using the Programming Register)

While in Idle mode the Programming register becomes active. The Programming register provides access to the Program Blocks. Program Blocks allow configuration of the CMX7861 during major mode change. Features that can be configured include:

- Configuration of RAMDAC profile
- Configuration of System Clock outputs
- Configuration of SPI Thru-Port rate and word format
- Configuration of transmit and receive filters.

Full details of how to configure these aspects of device operation are given in section 9.2, in the User Manual.

7.4.4 Device Configuration (Using dedicated registers)

Some device features may be configured using dedicated registers. This allows for configuration outside of Idle mode. Configuration of the following features is possible:

- Auxiliary ADC detect thresholds
- Auxiliary ADC input selection and averaging mode
- Output gain
- Output dc offsets.

The registers that allow configuration of these features are:

- 9.1.8 DAC1/DAC2 Output Control - $5D, $5E write
- 9.1.9 ADC1/ADC2 Input Control - $5F, $60 write
- 9.1.20 Input 1-4 Coarse Gain - $B1, $B2 write
- 9.1.22 Output 1 and 2 Coarse Gain - $B4, $B5 write
- 9.1.21 Output 1 - 4 Configuration - $B3 write
- 9.1.19 Input 1 - 4 Configuration - $B0 write
- 9.1.5 AuxADC1-4 Control - $51 to $54 write
- 9.1.6 AuxADC1-4 Threshold- $55 to $58 write
- 9.1.10 Signal Control - $61 write.

7.4.5 Interrupt Operation

The CMX7861 can produce an interrupt output when various events occur. Examples of such events include FIFO threshold being reached, an overflow of the internal data buffering in receive, or completion of transmission whilst in transmit.

Each event has an associated IRQ Status register bit and an IRQ Mask register bit. The IRQ Mask register is used to select which status events will trigger an interrupt on the IRQN line. All events can be masked using the IRQ mask bit (bit 15) or individually masked using the IRQ Mask register. Enabling an interrupt by setting a mask bit ($0 \rightarrow 1$) after the corresponding IRQ Status register bit has already been set

to 1 will also cause an interrupt on the IRQN line. The IRQ bit (bit 15) of the IRQ Status register reflects the IRQN line state.

All interrupt flag bits in the IRQ Status register are cleared and the interrupt request is cleared following the command/address phase of a C-BUS read of the IRQ Status register. See:

- 9.1.34 IRQ Status - $7E read
- 9.1.18 IRQ Mask - $6C write.

7.4.6 Signal Control

The CMX7861 offers four signal inputs: Input 1 (or I in an I/Q-based system), Input 2 (or Q in an I/Q-based system), Input 3 and Input 4. It offers four signal outputs: Output 1 (or I in an I/Q-based system), Output 2 (or Q in an I/Q-based system), Output 3 and Output 4.. The analogue gain/attenuation of each input and output can be set individually.

During I/Q transmit, I Output and Q Output will output in-phase and quadrature output signals. They may be independently inverted and their gains changed. During I/Q receive, I Input and Q Input will accept in-phase and quadrature modulated signals. They may be independently inverted and their gains changed.

See:

- 9.1.8 DAC1/DAC2 Output Control - $5D, $5E write
- 9.1.9 ADC1/ADC2 Input Control - $5F, $60 write
- 9.1.20 Input 1-4 Coarse Gain - $B1, $B2 write
- 9.1.22 Output 1 and 2 Coarse Gain - $B4, $B5 write
- 9.1.23 Output 3 and 4 Coarse Gain - $B6 write
- 9.1.21 Output 1 - 4 Configuration - $B3 write
- 9.1.19 Input 1 - 4 Configuration - $B0 write.

7.4.7 Tx Mode Processing

In Tx mode the 7861FI-1.x provides two independent DAC outputs. Often these may be used to generate In-phase and quadrature signal outputs for I/Q baseband modulation but they are general purpose and can re-create two unrelated signals. The signal processing chain is shown below:

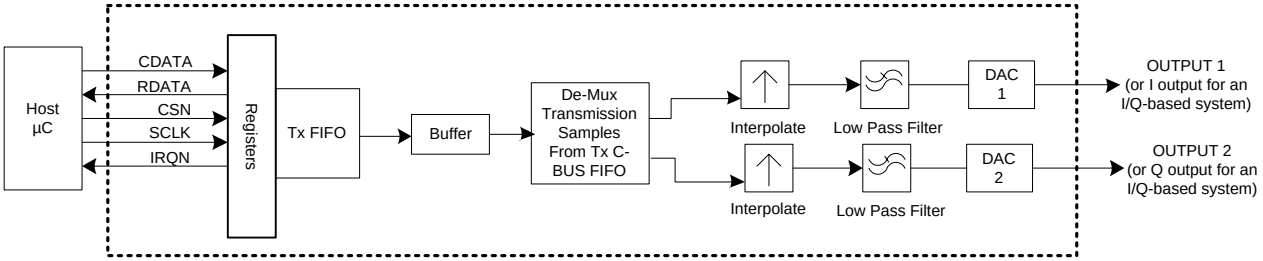


Figure 19 Tx Mode Processing

The Interpolation stage and user-programmable low-pass filter stage shown in Figure 19 Tx Mode Processing are both optional. When deactivated, the host must provide samples at the sample rate which the CMX7861 was configured to run at. This provides the ability to recreate any format of signal (subject to bandwidth constraints), but requires a lot of data to be transferred between host and CMX7861.

When producing frequency modulation and using the CMX7861 to produce 2-point modulation of GFSK or 4FSK signals, it is beneficial to activate the interpolation stage and low pass filter. To do this the filter must be designed correctly, with knowledge of the required number of samples per symbol and the interpolation factor must be configured to match. Typical filter designs would be root raised cosine, raised

cosine or Gaussian. The result is that the host may then feed mapped symbols (typically with 2, 4 or 8 levels) with the I symbol equal to the Q symbol into the CMX7861 which will interpolate and apply the pulse shaping filtering. The result is two signals on the I and Q outputs, which are not a quadrature signal but instead are suitable for providing two-point modulation to an FM modulator.

When producing phase or phase and amplitude modulations and using the CMX7861 to produce the I,Q baseband signal, it is beneficial to activate the interpolation stage and low pass filter. Typical applications are producing QPSK, QAM or π/4DQPSK modulation. To do this the filter must be designed correctly, with knowledge of the required number of samples per symbol, the interpolation factor must be configured to match. Typical filter designs would be root raised cosine or raised cosine. The result is that the host may then feed mapped symbols representing the mapped I/Q constellation points into the CMX7861 which will interpolate and apply the pulse shaping filtering. The result is a filtered baseband quadrature signal on the I and Q outputs which are suitable for converting to RF.

In either the FM modulation or phase/amplitude modulation examples above the CMX7861 provides additional processing- removing the requirement for filtering from the host, and reducing the data transfer rate required from the chosen sample rate down to the symbol rate.

7.4.8 Rx Mode Processing

In Rx mode the 7861FI-1.x provides two independent ADC inputs. Often these may be used to sample in-phase and quadrature signals for I/Q baseband demodulation by the host, but they are general purpose and can sample two unrelated signals. The signal processing chain is shown below:

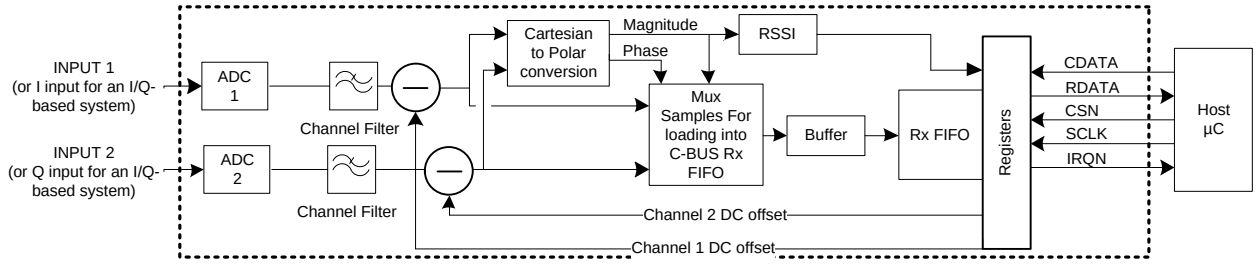


Figure 20 Rx Mode Processing

The CMX7861 receive processing provides user programmable channel filtering in order to reduce host processing load. In the general case, the filtered I/Q samples may simply be retrieved by the host from the Rx FIFO. This is the expected configuration for sampling two arbitrary signals, or using the CMX7861 in a QPSK or QAM receiver. In the case of a QPSK or QAM receiver the channel filters often provide a root raised cosine response matched to the transmit filtering. Built-in filters are provided which fulfil this purpose.

When receiving FM signals using an I/Q input the CMX7861 provides part of the FM demodulation process. Once filtered, I and Q dc offsets [1]may be removed by the CMX7861 but must be computed by the host. This allows a cartesian to polar conversion to take place and to correctly compute the instantaneous phase of the received I,Q vector. The phase samples, along with I and Q samples, are provided in the Rx FIFO for the host to use in the FM demodulation process.

When receiving FM signals using a limiter discriminator receiver the CMX7861 may be configured to provide filtering matched to the transmitter modulating signal. This may be interfaced to either the I or Q input (we are not sampling a quadrature signal in this case), with a typical RSSI signal from the receiver

fed into the other ADC. The CMX7861 can be configured to average the RSSI samples and to provide them to the host, alongside the filtered Limiter discriminator output.

7.4.9 Duplex Mode

The duplex mode combines transmit and receive modes. Both transmit and receive operate simultaneously with the same signal processing involved as described in sections 7.4.7 Tx Mode Processing and 7.4.8 Rx Mode Processing.

[1]I/Q dc offsets are often introduced by radio receiver hardware. It is essential to calculate and remove them prior to demodulation. In the case of FM demodulation, they must be removed prior to calculation of signal phase, so this correction is required within the CMX7861.

7.4.10 Other Modes

The CMX7861 provides a pass-through diagnostic mode. This results in the I/Q inputs being channel filtered, any dc offsets subtracted and the resulting signal being passed out of the I and Q outputs.

When receiving QAM or QPSK signals the pass-through mode may be used to observe the matched filtered I/Q constellation diagram. Note however that if a significant frequency error exists between transmitter and receiver the constellation diagram will appear to rotate rapidly and be difficult to interpret.

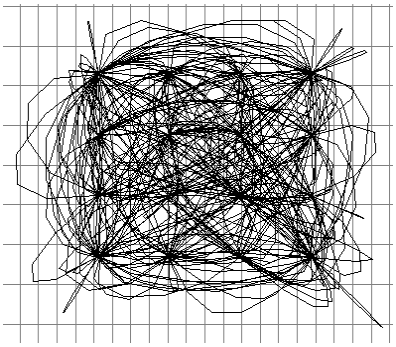


Figure 21 Constellation Diagram – no frequency or phase error

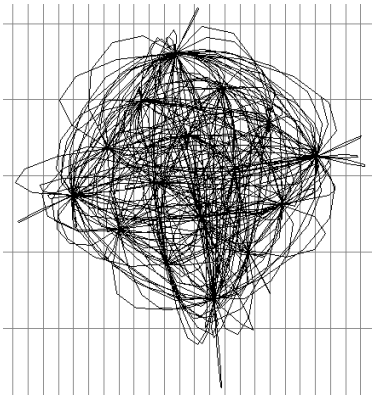


Figure 22 Constellation Diagram – phase error

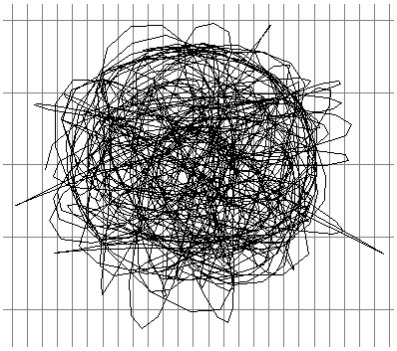


Figure 23 Constellation Diagram – frequency error

When receiving FM modulated signals through a limiter discriminator receiver the pass-through mode may be used to observe the matched filtered data (modulating signal) in an eye diagram. One of the CMX7861 GPIO pins may be used as a trigger locked to the sample rate, in order to display an eye diagram on an oscilloscope. Note that best results are often obtained with an analogue oscilloscope.

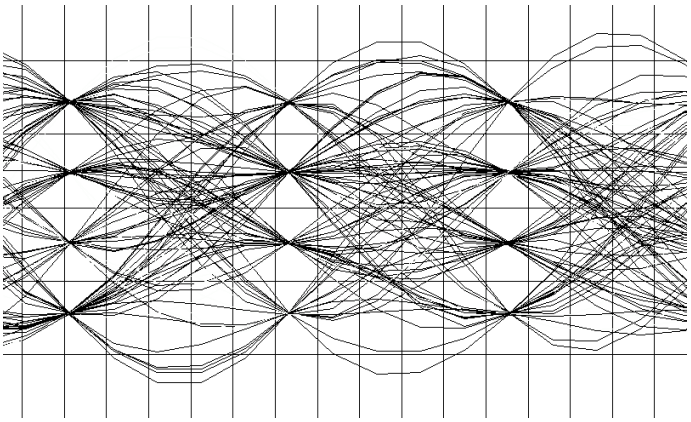


Figure 24 Received Eye Diagram

When enabled as an output, any of the GPIO signals can be configured to produce a pulse train locked to the sample rate of the receiving CMX7861 to aid triggering whilst viewing the constellation or eye diagram (I Output or Q Output alone vs time) or other diagnostic modes in receive. In some cases it is advisable to obtain a trigger pulse that is synchronised to the transmitting modem symbol rate, for example if the transmitted signal comes from a signal generator.

See:

- 9.1.17 Mode Register- $6B write
- 9.1.10 Signal Control - $61 write
- 9.1.13 GPIO Control - $64 write
- 9.2.3 Program Block 1 – Clock Control

7.4.11 Data Transfer

The payload data is transferred to and from the host via the C-BUS Tx and Rx Data FIFOs, each of which provide efficient streaming C-BUS access. FIFO fill level can be determined by reading the Receive FIFO Level and Tx FIFO Level registers and controlled using FIFO Control - $50 write register. Interrupts may be provided on FIFO fill thresholds being reached.

Each FIFO word is 16 bits, with the least significant byte (LSByte) containing data, and the most significant (MSByte) containing control information. The control and data bytes may be written or read together using the Receive FIFO Word and Tx FIFO Word registers, or individually using their byte-wide registers.

Word wide FIFO writes involve writing 16-bit words to the Tx FIFO Word register using either a single write or streaming C-BUS. The whole word written is put into the Tx FIFO, with the upper byte interpreted as control and the lower byte as data. This causes the control byte to be held in the Tx FIFO Control Byte register.

Byte wide FIFO writes involve writing to the Tx FIFO Data Byte register using either single access or streaming C-BUS. This causes the Tx FIFO Control Byte (MSByte) and data written to the Tx FIFO Data Byte (LSByte) registers to be put into the Tx FIFO as one word. The control byte can be written separately as a single byte (this does not result in anything being added to the FIFO) or is preserved from a previous 16-bit Tx FIFO Data Byte write.

Likewise a word read from the Rx Data FIFO will return the Receive FIFO Control Byte in the MSByte and the Receive FIFO Data Byte at the top of the FIFO in the LSByte. Both registers will be updated so that

when read next time they will provide details of the next item in the FIFO. Reading the Receive FIFO Control Byte only will not change the FIFO content. Reading the Receive FIFO Data Byte only will provide the data and remove the item from the FIFO – updating both control and data registers (see also Table 4).

Table 4 FIFO Transfer Summary

Operation	Effect
write Tx FIFO Control Byte register	Tx FIFO control word updated, nothing added to Tx FIFO
write Tx FIFO Data Byte register	Tx FIFO control word + data byte written are added to Tx FIFO
write Tx FIFO Word register	data word (control and data bytes) is added to Tx FIFO. Tx FIFO control word updated for future writes.
read Receive FIFO Control Byte register	Rx FIFO control word is returned, no effect on Rx FIFO contents
read Receive FIFO Data Byte register	Oldest Rx FIFO data byte is removed from FIFO and returned, Rx FIFO Word updated
read Receive FIFO Data Word register	Oldest Rx FIFO data word (control and data bytes) is removed from FIFO and returned, Rx FIFO control word updated

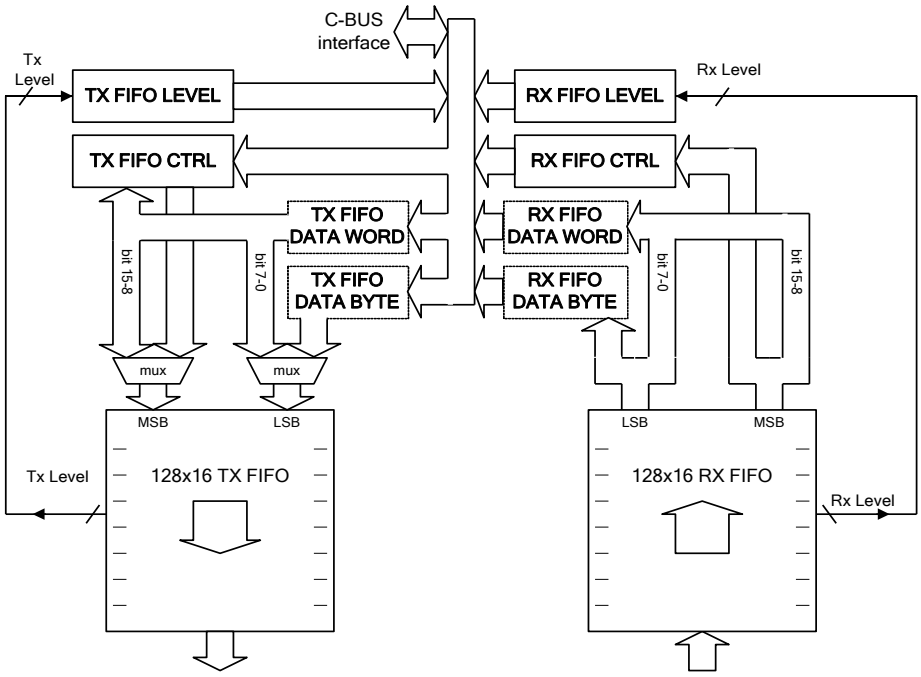


Figure 25 Tx and Rx Data FIFOs

Single channel (DAC1 or DAC2) or dual channel (DAC1 and DAC2) samples may be transmitted using the CMX7861, selected using the Mode Register- $6B write register. Likewise single or dual channels may be received. Duplex operation provides simultaneous output and input. Relevant registers are:

- 9.1.17 Mode Register- $6B write
- 9.1.3 Tx FIFO Data/Control - $48, $49 and $4A write
- 9.1.26 Receive FIFO Data/Control - $4C, $4D, $4E read
- 9.1.25 Tx FIFO Level - $4B read
- 9.1.27 Receive FIFO Level - $4F read
- 9.1.4 FIFO Control - $50 write.

7.4.12 Sample Format

The CMX7861 uses the Tx FIFOs to transmit several types of sample:

Single channel samples for DAC1 or DAC2, for example, an I or Q output
Dual channel DAC1/DAC2 sample pairs, for example an I/Q pair of samples

In receive there are more sample formats available, which include:

Single channel samples for ADC1 or ADC2, for example, an I or Q input
Dual channel ADC1/ADC2 sample pairs, for example, an I/Q pair of samples
Phase, magnitude samples computed by the CMX7861 from sampled I/Q data.

In order to package the variety of sample formats and to provide timing and synchronisation information the CMX7861 uses sample blocks. A sample block consists of control/synchronisation information and sample data. It is packaged so that the control information can be optionally read when it is required – so that data throughput is maximised.

In receive the sample block control information can be read from the Rx FIFO control byte, the sample data can be read from the data byte, or both together from the Rx FIFO Word register.

When read from the Rx FIFO Word register a sample pair will provide the information as shown in Table 5.

Table 5 Rx ADC1/ADC2 sample blocks

	ADC1/ADC2 sample block															
	Rx FIFO control byte								Rx FIFO data byte							
Bit No	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word1	1					0	0	0	Most significant byte of ADC1 sample (upper)							
Word2	0	Rx sample number							Least significant byte of ADC1 sample (lower)							
Word3	0								Most significant byte of ADC2 sample (upper)							
Word4	0								Least significant byte of ADC2 sample (lower)							

ADC1 sample block																
	Rx FIFO control byte								Rx FIFO data byte							
Bit No	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word1	1					0	0	1	Most significant byte of ADC1 sample (upper)							
Word2	0	Rx sample number							Least significant byte of ADC1 sample (lower)							

ADC2 sample block																
	Rx FIFO control byte								Rx FIFO data byte							
Bit No	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word1	1					0	1	0	Most significant byte of ADC2 sample (upper)							
Word2	0	Rx sample number							Least significant byte of ADC2 sample (lower)							

Bit 15 is a synchronisation bit. It will always be set in the first word of a sample block, and cleared in the others. Its purpose is to provide an indication of the start of a sample, so if FIFOs or buffers have been allowed to overflow and samples lost it becomes possible to establish (for example) which is an I and

which is a Q sample. When synchronisation has been established, or if no overflow ever happened it is possible to read only the Rx FIFO data byte and retrieve the raw sample data.

The sample number field is used to establish time of arrival of received sampled data. It provides a time stamp for each received sample and allows the host driver to calculate a Tx sample number field to pass to the CMX7861 to specify time of transmission.

The sample type is indicated using bits 10, 9, 8 of Word 1. This feature allows the host to ask the CMX7861 to continually sample signals whilst dynamically changing the format of sample requested. For example: initially request I/Q, phase, amplitude samples to establish the I/Q dc offset corrections required. Then to provide more efficient operation by only requesting phase samples. The sample type field within the sample block allows the host to establish which samples are from before the dynamic switch and which are from after – ie to confirm the sample type.

A similar format applies to other sampled data types, as shown in Table 6.

Table 6 Rx ADC1/ADC2, Phase/Magnitude sample blocks

	Phase, Magnitude sample block															
	Rx FIFO control byte								Rx FIFO data byte							
Bit No	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word1	1					1	0	0	Most significant byte of Phase sample (Pupper)							
Word2	0	Rx sample number							Least significant byte of Phase sample (Plower)							
Word3	0								Most significant byte of Magnitude sample (Mupper)							
Word4	0								Least significant byte of Magnitude sample (Mlower)							

Phase sample block																
	Rx FIFO control byte								Rx FIFO data byte							
Bit No	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word1	1					1	0	1	Most significant byte of Phase sample (Pupper)							
Word2	0	Rx sample number							Least significant byte of Phase sample (Plower)							

Magnitude sample block																
	Rx FIFO control byte								Rx FIFO data byte							
Bit No	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word1	1					1	1	0	Most significant byte of Magnitude sample (Mupper)							
Word2	0	Rx sample number							Least significant byte of Magnitude sample (Mlower)							

		ADC1/ADC2, Phase, Magnitude sample block															
		Rx FIFO control byte								Rx FIFO data byte							
Bit No	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word1	1					1	1	1	Most significant byte of ADC1 sample (upper)							
Word2	0	Rx sample number							Least significant byte of ADC1 sample (lower)							
Word3	0								Most significant byte of ADC2 sample (upper)							
Word4	0								Least significant byte of ADC2 sample (lower)							
Word5	0								Most significant byte of Phase sample (Pupper)							
Word6	0								Least significant byte of Phase sample (Plower)							
Word7	0								Most significant byte of Magnitude sample (Mupper)							
Word8	0								Least significant byte of Magnitude sample (Mlower)							

Similarly to the sample block format provided by the CMX7861, samples for transmission contain sampled data and optional control information. See Table 7 for details.

Bit 15 is a synchronisation bit, which the CMX7861 will always process. When the CMX7861 detects a 1 to 0 transition in the synchronisation bit it will treat that as the start of a sample block. When no 1 to 0 transition is detected it will continue to count Tx FIFO entries and assume that each frame is complete. This mechanism allows the host to optionally provide control information when required and to maximise C-BUS throughput by just writing the Tx data byte at other times.

Tx Time Block: This block instructs the CMX7861 to wait until a specified time before allowing further samples to be output. 'Time' is specified as the sample number at which to begin transmitting. This allows synchronisation of the transmitted signal with received signals. For example, having detected a framesync when processing sample N the host can specify that a transmission should occur at sample number N+k to ensure transmit – receive synchronisation. This is of particular use in time division multiple access (TDMA) slotted systems. The host can read the current time as seen by CMX7861 using the Sample Time - $7D read register.

Tx End Block: This block allows that host to optionally specify the end of transmission. In situations where the host needs to know the precise moment when the transmission ends, such as bursty transmissions, the host may write a Tx End Block as the last data word in the Tx FIFO Data/Control - $48, $49 and $4A write register.

When Tx End Block is written by the host, the CMX7861 signals a Tx Done status bit in the IRQ Status - $7E read register after outputting the last Tx sample. This feature can be used by the host to ramp down the power amplifier at the end of a transmission.

Table 7 Tx DAC1/DAC2 sample blocks

	DAC1/DAC2 Sample Pair															
	Tx FIFO control byte								Tx FIFO data byte							
Bit No	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word1	1					0	0	0	Most significant byte of DAC1 sample (upper)							
Word2	0								Least significant byte of DAC1 sample (lower)							
Word3	0								Most significant byte of DAC2 sample (upper)							
Word4	0								Least significant byte of DAC2 sample (lower)							

	DAC1 Sample Only															
	Tx FIFO control byte								Tx FIFO data byte							
Bit No	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word1	1					0	0	1	Most significant byte of DAC1 sample (upper)							
Word2	0								Least significant byte of DAC1 sample (lower)							

	DAC2 Sample Only															
	Tx FIFO control byte								Tx FIFO data byte							
Bit No	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word1	1					0	1	0	Most significant byte of DAC2 sample (upper)							
Word2	0								Least significant byte of DAC2 sample (lower)							

	Tx Time Block															
	Tx FIFO control byte								Tx FIFO data byte							
Bit No	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word1	1					1	1	1	Most significant byte of Time							
Word2	0								Least significant byte of Time							

	Tx End Block															
	Tx FIFO control byte								Tx FIFO data byte							
Bit No	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word1	1					1	1	0	Don't Care							

7.4.13 Data Buffering

To expand the buffering capabilities of the CMX7861 two internal buffers are provided:

A Tx buffer which buffers transmit data from the Tx FIFO.
An Rx buffer which buffers received data yet to be loaded into the Rx data FIFO.

Transfer between the FIFOs and their respective buffers will occur regardless of mode. Such transfer is not instantaneous so the FIFO fill levels should be used to indicate how much data the host may read or write at any time.

The Internal Buffer Fill Level - $70 read register allows the buffer fill levels to be read; their contents will be flushed when the respective FIFO is flushed.

See:
- 9.1.4 FIFO Control - $50 write
- 9.1.28 Internal Buffer Fill Level - $70 read.

7.4.14 Managing Data Transfer

In transmit it is important to avoid an underflow – if an output sample is required and one is not available, transmission will not be continuous. This is indicated by the Tx Empty flag in the IRQ Status - $7E read becoming set. It is advisable to pre-load data into the Tx FIFO before transmission begins.

In receive it is important to avoid an overflow – if a sample is received and space to store it is not available in the CMX7861, reception will not be continuous. This is indicated by the Rx OV flag in the IRQ Status - $7E read becoming set.

FIFO levels or FIFO level IRQs may be used to manage the data flow. For both transmit and receive operation.

7.4.15 GPIO Pin Operation

The CMX7861 provides four GPIO pins, each pin can be configured independently as an input or an output.

See:
- 9.1.13 GPIO Control - $64 write
- 9.1.32 GPIO Input - $79 read.

7.4.16 Auxiliary ADC Operation

The inputs to the four Auxiliary ADCs can be independently routed from any of four dedicated AUXADC input pins or the two main inputs. Auxiliary ADCs can be disabled to save power. BIAS in the VBIAS Control - $B7 write register must be enabled for Auxiliary ADC operation.

Averaging can be applied to the ADC readings by selecting the relevant bits in the AuxADC1-4 Control - $51 to $54 write registers. This is a rolling average system such that a proportion of the current data will be added to the last value. The proportion is determined by the value of the average counter in the AuxADC1-4 Control - $51 to $54 write registers. Setting the average counter to zero will disable the averager, for an average value of 1; 50% of the current value will be applied, for a value of 2 = 25%, 3 = 12.5%, continuing up to the maximum useful value of 11 = 0.0488%.
High and low thresholds may be independently applied to both ADC channels (the comparison is applied after averaging, if this is enabled) and an IRQ generated when an input exceeds the high or low threshold, or on every sample as required. The thresholds are programmed via the AuxADC1-4 Threshold- $55 to $58 write register.

Auxiliary ADC data is read back in the AuxADC1-4 Read - $71 to $74 read registers and includes the threshold status as well as the actual conversion data (subject to averaging, if enabled).

The AuxADC sample rate is selected using Program Block 1 – Clock Control.

See:
- 9.1.5 AuxADC1-4 Control - $51 to $54 write
- 9.1.6 AuxADC1-4 Threshold- $55 to $58 write
- 9.1.29 AuxADC1-4 Read - $71 to $74 read
- 9.2.3 Program Block 1 – Clock Control
- 9.1.24 VBIAS Control - $B7 write.

7.4.17 Auxiliary DAC/RAMDAC Operation

The four Auxiliary DACs are programmed via the AuxDAC1-4 Control - $59 to $5C write registers. AuxDAC1 may also be programmed to operate as a RAMDAC which will autonomously output a pre-programmed profile at a programmed rate. The AuxDAC1-4 Control - $59 to $5C write register, with b12 set, controls the RAMDAC mode of operation. The RAMDAC ramp rate is controlled by the Internal system clock rate, which changes between active CS/Tx/Rx modes and Idle mode. Therefore it is inadvisable to return to Idle mode prior to RAMDAC ramp completion.

The default profile is a Raised Cosine (see Table 16 in the user manual), but this may be over-written with a user-defined profile by writing to Program Block 0. The AuxDAC outputs hold the user-programmed level during a powersave operation if left enabled, otherwise they will return to zero.

See:

- 9.1.7 AuxDAC1-4 Control - $59 to $5C write
- 9.2.2 Program Block 0 – RAMDAC
- 9.2.3 Program Block 1 – Clock Control

7.4.18 SPI Thru-Port

The CMX7861 offers an SPI Thru-Port which allows the host, using the main C-BUS interface, to command the CMX7861 to read or write up to three external SPI/C-BUS devices attached to the CMX7861. The CMX7861 acts as a SPI/C-BUS master in this mode, controlling three chip selects, clock and data out (MOSI), and receiving data in (MISO).

Each individual SPI/C-BUS device can be independently configured using Program Block 6 – SPI Thru-Port Configuration to have clock speed, inter-frame guard period and clock phase/polarity to match the specification of the slave SPI/C-BUS device attached. In order to offer a simpler, more convenient interface, a device can be designated C-BUS, rather than SPI. This means that data read/written is assumed to be in the format:

Address byte, data byte1 (optional), data byte 2 (optional).

In each case the CMX7861, as the master, drives the address and data for a write operation, or drives the address and receives the data for a read operation. Commands can be called 0, 1 or 2 byte reads or writes – with a 0 byte write typically being a reset command. As the word format is known, then for convenience only the desired read data is returned to the host.

SPI mode is a little more flexible. No assumption is made about the SPI word format, nor any assumption that the length is a whole number of bytes.

See:

- 9.1.11 SPI Thru-Port Control - $62 write
- 9.1.12 SPI Thru-Port Write - $63 write
- 9.1.31 SPI Thru-Port Read - $78 read
- 9.2.8 Program Block 6 – SPI Thru-Port Configuration

7.5 Digital System Clock Generators

The CMX7861 includes a two-pin Xtal oscillator circuit. This can either be configured as an oscillator, as shown in section 5.1, or the XTAL/CLK input can be driven by an externally-generated clock. The crystal (Xtal) source frequency is typically 9.6MHz and if an external oscillator is used, the input frequency is typically 9.6 or 19.2 MHz. For both cases reference frequencies in the range specified in 8.1.2 Operating Limits may be used.

7.5.1 Main Clock Operation

A digital PLL is used to create the main clock for the internal sections of the CMX7861. The configuration of the main clock and the internal clocks derived from it are controlled using Program Block 1 – Clock Control.

The CMX7861 defaults to settings appropriate for a 19.2MHz externally-generated clock with a sample rate of 48000 samples/s, however if a different reference frequency is to be used, or a different sample rate required, then Program Block entries P1.1 to P1.6 will need to be programmed appropriately at power-on. A table of preferred values is provided in Table 17 and Table 18 in the User Manual along with details of how to calculate settings for other sample rates and crystal frequencies.

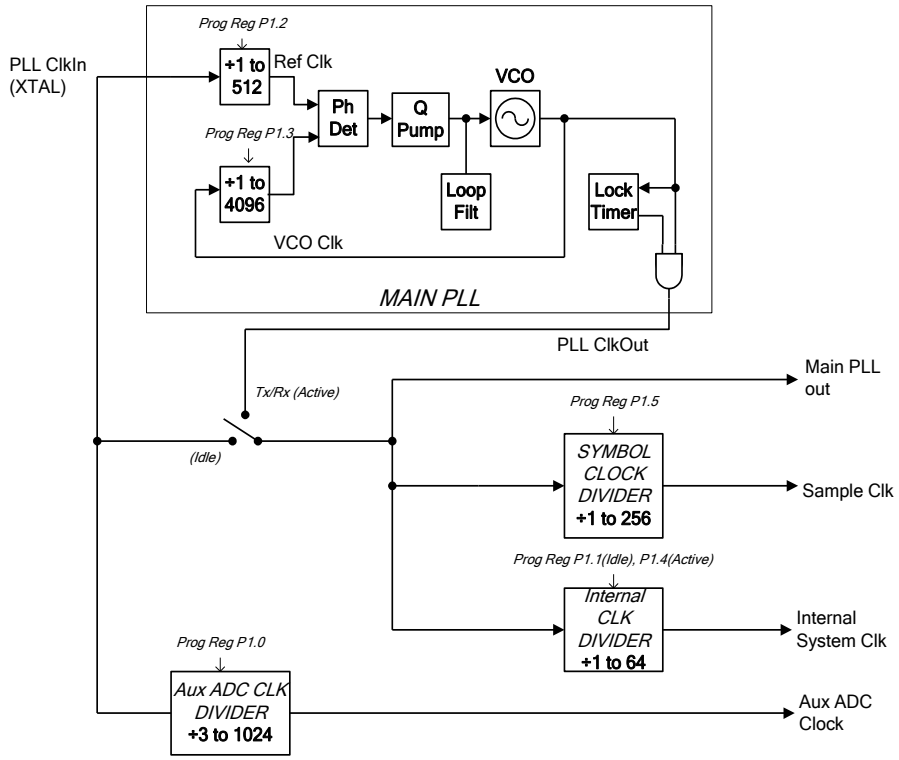


Figure 26 Main Clock Generation

See:

- 9.2.3 Program Block 1 – Clock Control.

7.5.2 System Clock Operation

Two System Clock outputs, SYSCLK1 and SYSCLK2, are available to drive additional circuits, as required. The System Clock circuitry is shown in Figure 27 Digital System Clock Generation Schemes.

Having chosen the input frequency source, system clock generation may be by simply dividing the input frequency source, or via its own phase locked loop. The system clock PLL does not affect any other

internal operation of the CMX7861 – so if a frequency that is not a simple fraction of the Xtal is required, it can be used with no side effects. There is one phase locked loop, with independent output dividers to provide phase locked output signals.

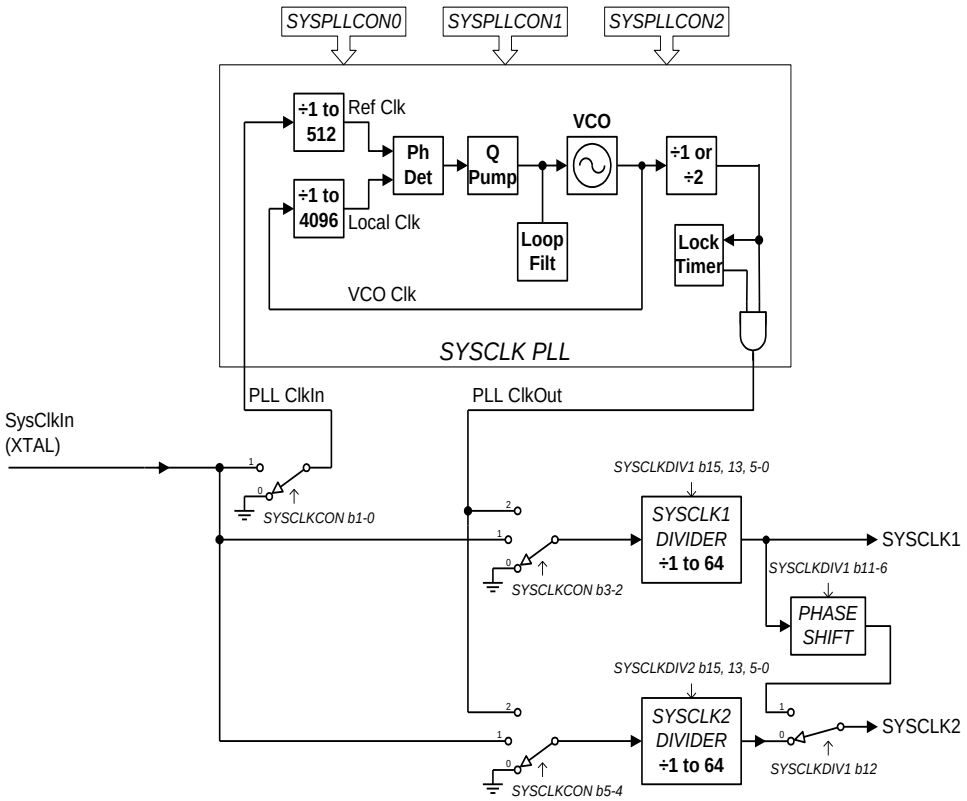


Figure 27 Digital System Clock Generation Schemes

See:

- 9.2.3 Program Block 1 – Clock Control.

7.6 Signal Level Optimisation

The internal signal processing of the CMX7861 will operate with wide dynamic range and low distortion only if the signal level at all stages in the signal processing chain is kept within the recommended limits. For a device working from a 3.3V supply, the signal range which can be accommodated without distortion is specified in 8.1.3 Operating Characteristics. Signal gain and dc offset can be manipulated as follows:

7.6.1 Transmit Path Levels

For the maximum signal out of Outputs1-4, the signal level at the output of the CMX7861 is set to be 0dB, the Fine Output adjustment has a maximum attenuation of 6dB and no gain, whereas the Coarse Output adjustment has a variable attenuation of up to 14.2dB and 6dB gain.

The signals output from DAC1 and DAC2 may be independently inverted. Inversion is achieved by selecting a negative value for the (linear) Fine Output adjustment. When transmitting I/Q format signals inverting one of the I/Q pair has a similar effect to swapping I with Q.

DC offsets may be added to the signal. However, care must be taken that the combination of gain and dc offset does not cause the signal to clip at any point in the signal processing chain, which is: fine gain

followed by dc offset addition, followed by coarse gain. Fine gain and dc offset addition are implemented prior to digital to analogue conversion, coarse gain is applied after digital to analogue conversion.

See:

- 9.1.8 DAC1/DAC2 Output Control - $5D, $5E write
- 9.1.22 Output 1 and 2 Coarse Gain - $B4, $B5 write.

7.6.2 Receive Path Levels

Inputs 1 to 4 each have a variable gain of up to +22.4dB and no attenuation. With the lowest gain setting (0dB), the maximum allowable input signal level at the Input pins is specified in section 8.1.3 Operating Characteristics.

A fine input level adjustment is provided, although the CMX7861 should operate correctly with the default level selected. The primary purpose of the Fine Input level adjustment is to allow independent inversion of the sampled signals in ADC1 and 2. Inversion is achieved by selecting a negative value for the (linear) Fine Input gain adjustment. When receiving I/Q format signals, inverting one of the I/Q pair has a similar effect to swapping I with Q.

DC offsets can be removed by the CMX7861, the offset to remove is selected by the host. Fine gain and dc offset addition are implemented after analogue to digital conversion, coarse gain is applied before analogue to digital conversion.

It should be noted that if the maximum allowable signal input level is exceeded, signal distortion will occur regardless of the internal dc offset removal or attenuation.

See:

- 9.1.9 ADC1/ADC2 Input Control - $5F, $60 write
- 9.1.19 Input 1 - 4 Configuration - $B0 write.

7.7 Application Information

7.7.1 ADC and DAC Filters

Information on how to design user-configurable filters for the CMX7861 will be the subject of a separate application note. Contact CML Technical Support for further information.

ADC Filters

The ADC filter coefficients may be programmed using the Programming Registers (Program Block 8), see:

- 9.2.10 Program Block 8 – Custom Rx Channel Filter

DAC Filters

The DAC filter coefficients may be programmed using the Programming Registers (Program Block 9), see:

- 9.2.11 Program Block 9 – Custom Tx Filter

7.7.2 ADC and DAC Sample Timing Synchronisation

In applications where the timing of DAC samples has to be synchronised to signals processed on the ADC (e.g. in a TDMA systems) it is essential to be able to measure the time of arrival of ADC samples, and to synchronise samples output through the DAC to them. In order to achieve this the CMX7861 provides sample synchronisation as shown in Figure 28 ADC/DAC Sample Timing Synchronisation.

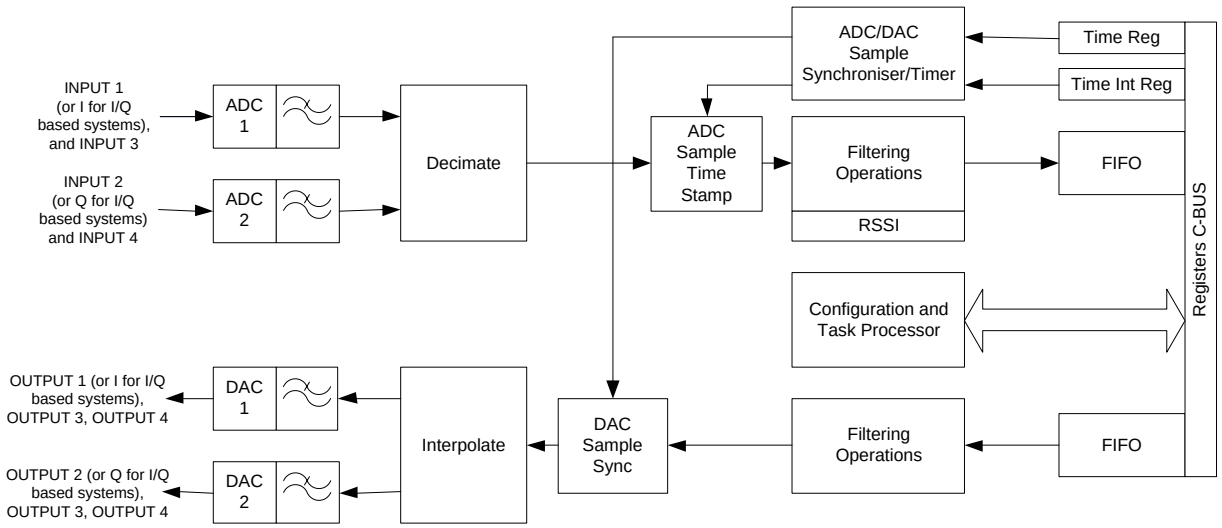


Figure 28 ADC/DAC Sample Timing Synchronisation

The CMX7861 will count at the selected sample rate and output the counter value in the Sample Time - $7D read. When in receive each input sample will be time stamped with the sample time, the time stamp can be optionally read using the Receive FIFO. Using this mechanism the time of arrival of a received framesync can be determined.

Using the 'Tx Time Block', which is described in section 7.4.12, a transmission can be scheduled to appear at a specified sample time. As the CMX7861 contains a single counter for input and output samples the result is a transmission at a precise time delay from the received framesync.

The sample counter will run even when the ADCs or DACs are inactive, allowing low-power operation without losing time synchronisation. To further save overall system power the counter can be compared to the Sample Timer Interrupt - $65 write register by the CMX7861 and when the two are equal the CMX7861 will interrupt the host microcontroller.

7.8 Codec And Modem Mode Descriptions

7.8.1 Codec Mode

Codec mode provides the ability to sample at rates up to 72kHz and provides a signal bandwidth of 30.96kHz with that sample rate. With this bandwidth constraint, the *FirmCODEC* provides ADCs and DACs to sample or reproduce any arbitrary waveform, for example, left/right stereo or control signals.

Whilst in Codec mode the CMX7861 provides optional user-programmable filtering on the input signal, and on the output signal. Filter design is straightforward, requiring an understanding of normal filter design and interpolation by 2. ADC and DAC roll off can be ignored because compensation is automatic.

Limited filter choices are possible when in codec mode. When in transmit either the codec mode filter or a user-programmable filter must be selected using Program Register P4.1. When in receive the ADC Compensation filter must be selected using Program Register P4.1. These constraints limit the value of Program Register P4.1 to $0102 or $0802. The receive user filter in codec mode is configured using Program Block 10 – Custom Rx Codec Mode Filter. This filter becomes active by selecting codec mode, and inactive when selecting modem mode.

7.8.2 Modem Mode

Modem mode is intended to be used in a radio modem application where the DACs are used to produce modulation and the ADCs to sample the received signal for reception. In both cases the number of samples per modem symbol is often an important factor when deciding on a sample rate, rather than simply the signal bandwidth. This often results in relatively narrow band signal when compared to the sample rate, which can be up to 144kHz.

During transmit, filters are provided which allow production of any size QAM (4,16, 32 etc.) or PSK (QPSK, pi/4DQPSK, pi/8D8PSK etc.). To do this the user provides mapped symbols in the form of I/Q samples at their modem symbol rate. The *FirmCODEC* applies pulse shaping filters and produces the transmit I/Q signal for up-conversion by radio hardware. In doing this it typically interpolates the signal by a factor of 4 to 10. Various pulse-shaping filters are provided, with user-programmable filters and interpolation rates. The same architecture provides pulse-shaping filtering for GFSK/4FSK type modulations, where the resulting signal drives a 2-point modulation transmitter. Again the user provides the sample at the symbol timing instant and the *FirmCODEC* provides pulse shaping filtering.

During receive, the *FirmCODEC* provides sampling and channel filtering (for an I/Q receiver) with a sample rate of up to 144kHz. This is useful for both QAM/QPSK style modulations and FSK/GFSK type signals. Samples and/or the phase and amplitude of received samples can be provided. Phase and amplitude information is useful for FM demodulation which is completed by the controlling processor. In some configurations the ADCs will provide matched filters for the modem receiver. In addition, short bursty transmissions may be synchronised to received samples, providing TDMA support.

The use of user-programmable filters (in transmit) means that consideration needs to be given to DAC roll off and compensation. This means that an output signal needs to have bandwidth considerably less than 0.5xFs. This is not uncommon in modem designs. In receive, consideration needs to be given to ADC roll off and this must be compensated for over the bandwidth of the wanted input signal. For further information, please contact CML Technical Support.

7.9 C-BUS Register Summary

Table 8 C-BUS Registers

ADDR. (hex)	Read/ Write	REGISTER	Word Size (bits)	User Manual Page	Section
$01	W	C-BUS General Reset	0	64	9.1.2
$48	W	Transmit FIFO Data Byte	8	65	9.1.3
$49	W	Transmit FIFO Word	16	65	9.1.3
$4A	W	Transmit FIFO Control Byte	8	65	9.1.3
$4B	R	Transmit FIFO Level	8	77	9.1.25
$4C	R	Receive FIFO Data Byte	8	77	9.1.26
$4D	R	Receive FIFO Word	16	77	9.1.26
$4E	R	Receive FIFO Control Byte	8	77	9.1.26
$4F	R	Receive FIFO Level	8	78	9.1.27
$50	W	FIFO Control	16	65	9.1.4
$51 to $54	W	AuxADC1-4 Control	16	66	9.1.5
$55 to $58	W	AuxADC1-4 Threshold	16	66	9.1.6
$59 to $5C	W	AuxDAC1-4 Control	16	67	9.1.7
$71 to $74	R	AuxADC1-4 Read	16	78	9.1.29
$5D	W	DAC1 Output Control	16	67	9.1.8
$5E	W	DAC2 Output Control	16	67	9.1.8
$5F	W	ADC1 Input Control	16	68	9.1.9
$60	W	ADC2 Input Control	16	68	9.1.9
$61	W	Signal Control	16	69	9.1.10
$65	W	Sample Timer Interrupt	16	71	9.1.14
$69	W	Reg Done Select	16	72	9.1.15
$70	R	Internal Buffer Fill Level	16	78	9.1.28
$77	R	RSSI	16	78	9.1.30
$62	W	SPI Thru-Port Control	16	70	9.1.11
$63	W	SPI Thru-Port Write	16	71	9.1.12
$64	W	GPIO Control	16	71	9.1.13
$78	R	SPI Thru-Port Read	16	79	9.1.31
$79	R	GPIO Input	16	79	9.1.32
$7D	R	Sample Time	16	79	9.1.33
$6A	W	Programming	16	72	9.1.16
$6B	W	Mode	16	72	9.1.17
$6C	W	IRQ Mask	16	74	9.1.18
$7E	R	IRQ Status	16	80	9.1.34
$7F	R	Mode Readback	16	80	9.1.35
$B0	W	Input 1 to 4 Configuration	16	74	9.1.19
$B1	W	Input 1 to 4 Coarse Gain	16	75	9.1.20
$B2	W	Input 1 to 4 Coarse Gain	16	75	9.1.20
$B3	W	Output 1 to 4 Configuration	16	76	9.1.21
$B4	W	Output 1 and 2 Coarse Gain	16	76	9.1.22
$B5	W	Output 1 and 2 Coarse Gain	16	76	9.1.22
$B7	W	V_{BIAS} Control	16	77	9.1.24

All other C-BUS addresses are reserved and must not be accessed.

8 Performance Specification

8.1 Electrical Performance

8.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Power Supplies			
DV_{DD} - DV_{SS}	-0.3	4.0	V
DV_{CORE} - DV_{SS}	-0.3	2.16	V
AV_{DD} - AV_{SS}	-0.3	4.0	V
Voltage on any digital pin to DV_{SS}	-0.3	DV_{DD} + 0.3	V
Voltage on any analogue pin to AV_{SS}	-0.3	AV_{DD} + 0.3	V
Current into or out of any pin except power supply pins: OP4VDD and OP4VSS	-20	+20	mA
Current in to or out of power supply pins: OP4VDD and OP4VSS	-120	+120	mA

Q1 Package (64-pin VQFN)	**Min.**	**Max.**	**Units**
Total Allowable Power Dissipation at Tamb = 25ºC		3500	mW
... Derating		35.0	mW/ºC
Storage Temperature	-55	+125	ºC
Operating Temperature	-40	+85	ºC

8.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Min	Typ	Max.	Units
DV_{DD} - DV_{SS}	3.0	3.3	3.6	V
DV_{CORE} - DV_{SS}	1.7	1.8	1.9	V
AV_{DD} - AV_{SS}	3.0	3.3	3.6	V
$OP4V_{DD}$ – OP4Vss	3.0	3.3	3.6	V
Operating Temperature	-40	–	+85	°C
Xtal Frequency	3.0	–	12.288	MHz
External Clock Frequency	3.0	–	24.576	MHz

8.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

External components as recommended in Section 5, External Components.
Maximum load on digital outputs = 30pF.
Xtal Frequency = 9.6MHz±0.002% (20ppm); Tamb = –40°C to +85°C.
AV_{DD} = DV_{DD} = 3.0V to 3.6V.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Supply Current	2				
All Powersaved					
AI_{DD} + DI_{DD}	1	–	1.0	–	µA
Idle Mode	3				
DI_{DD}	4	–	550	–	µA
AI_{DD}		–	17	–	µA
Additional Current for One Auxiliary System Clock (output running at 5MHz – SysCLKPLL active)					
DI_{DD} (DV_{DD} = 3.3V, DV_{CORE} = 1.8V)		–	900	–	µA
Additional Current for one Auxiliary System Clock (output running at 4.8MHz – SysCLKPLL not required)					
DI_{DD} (DV_{DD} = 3.3V, DV_{CORE} = 1.8V)		–	675	–	µA
Additional Current for Each Auxiliary ADC					
DI_{DD} (DV_{DD} = 3.3V, DV_{CORE} = 1.8V)		–	190	–	µA
Additional Current for Each Auxiliary DAC	5				
AI_{DD} (AV_{DD} = 3.3V)		–	210 to 370	–	µA

Notes:
1. Idle mode with V_{BIAS} disabled.
2. Tamb = 25°C, not including any current drawn from the device pins by external circuitry.
3. System Clocks, Auxiliary circuits disabled, but all other digital circuits (including the Main Clock PLL) enabled and V_{BIAS} enabled.
4. Using external clock input, Xtal oscillator circuit powered down.
5. A lower current is measured when outputting the smallest possible dc level from an Auxiliary DAC, a higher current is measured when outputting the largest possible dc value.

DC Parameters (continued)	Notes	Min.	Typ.	Max.	Unit
XTAL/CLK	20				
Input Logic '1'		70%	–	–	DV_{DD}
Input Logic '0'		–	–	30%	DV_{DD}
Input Current (Vin = DV_{DD})		–	–	40	µA
Input Current (Vin = DV_{SS})		–40	–	–	µA
C-BUS Interface and Logic Inputs					
Input Logic '1'		70%	–	–	DV_{DD}
Input Logic '0'		–	–	30%	DV_{DD}
Input Leakage Current (Logic '1' or '0')	2	–1.0	–	1.0	µA
Input Capacitance		–	–	7.5	pF
C-BUS Interface and Logic Outputs					
Output Logic '1' (I_{OH} = 2mA)		90%	–	–	DV_{DD}
Output Logic '0' (I_{OL} = -5mA)		–	–	10%	DV_{DD}
"Off" State Leakage Current	2	–1.0	–	1.0	µA
V_{BIAS}	21				
Output Voltage Offset wrt $AV_{DD}/2$ (I_{OL} < 1µA)		–	±2%	–	AV_{DD}
Output Impedance		–	50	–	kΩ

Notes:
20 Characteristics when driving the XTAL/CLK pin with an external clock source.
21 Applies when utilising V_{BIAS} to provide a reference voltage to other parts of the system. When using V_{BIAS} as a reference, V_{BIAS} must be buffered. V_{BIAS} must always be decoupled with a capacitor, as shown in section 4.

AC Parameters		Notes	Min.	Typ.	Max.	Unit
XTAL/CLK Input						
'High' Pulse Width		30	15	–	–	ns
'Low' Pulse Width		30	15	–	–	ns
Input Impedance (at 9.6MHz)						
Powered-up	Resistance		–	150	–	kΩ
	Capacitance		–	20	–	pF
Powered-down	Resistance		–	300	–	kΩ
	Capacitance		–	20	–	pF
Xtal Start-up Time (from powersave)			–	20	–	ms
SYSCLK1/2 Outputs						
SysPLL Operating Frequency			38	–	250	MHz
SysCLK1/2 Output Frequency			–	–	20	MHz
Rise Time			–	–	13.5	ns
Fall Time			–	–	6	ns
V_{BIAS}						
Start-up Time (from powersave)			–	30	–	ms
Differential Inputs 1 and 2 (I/Q Inputs)						
Resolution			–	16	–	bits
Sample Rate			–	–	144	ksps
SNR			–	–	144	ksps
4 kHz bandwidth			–	86	–	dB
8 kHz bandwidth			–	83	–	dB
Input Impedance, Enabled		31	10	–	140	kΩ
Input Impedance, Muted or Powersaved				200		kΩ
Maximum Input Voltage Excursion		32	–	–	20 to 80	%AV_{DD}
Single Ended Inputs 3 and 4						
Input Impedance		31	–	>10	–	MΩ
Input Voltage Range		32	–	–	10 to 90	%AV_{DD}
Amplifier Open Loop Voltage Gain (I/P = 1mV rms at 100Hz)			–	80	–	dB
Unity Gain Bandwidth			–	1.0	–	MΩ
Programmable Input Gain Stage						
Gain (at 0dB)		33	−0.5	0	+0.5	dB
Cumulative Gain Error (w.r.t. attenuation at 0dB)		33	−1.0	0	+1.0	dB

Notes:

30 Timing for an external input to the XTAL/CLK pin.

31 With no external components connected.

32 For each input pin and for AV_{DD} = 3.3V, the maximum allowed signal swing is: (3.3 x 0.8) - (3.3 x 0.2) = 2.0V. If used for dc voltages, it is recommended that the maximum allowed signal swing (with the Input Gain at 0dB) be reduced to (3.3 x 0.75) - (3.3 x 0.25) = 1.65V, to avoid “idle tone” production.

33 Design Value. Overall attenuation input to output has a design tolerance of 0dB ±1.0dB.

AC Parameters	Notes	Min.	Typ.	Max.	Unit
Differential Outputs 1 and 2 (I/Q Outputs), Outputs 3 and 4					
Power-up to Output Stable	40	–	50	100	µs
SINAD (3.4 kHz bandwidth)	48	–	78	–	dB
Output Voltage Range: Outputs 1 and 2	41, 44	0.3	–	AV_{DD} - 0.3	V
Output voltage Range: Output 3	45	0.5	–	AV_{DD} - 0.5	V
Output Voltage Range: Output 4	44, 46	0.75	–	AV_{DD} - 0.75	V
Output Power: Output 3	47	–	–	140	mW
Load Resistance:					
Outputs 1 and 2	42	20	–	–	kΩ
Output 3	42	32	–	–	Ω
Output 4	42	8	–	–	Ω
Output Impedance: Output 1 and 2	42	–	600	–	Ω
Output 1 and 2, Course Gain Attenuators	43				
Attenuation (at 0dB)		−0.2	0	+0.2	dB
Cumulative Attenuation Error (w.r.t. attenuation at 0dB)		−0.6	0	+0.6	dB
Output 3 and 4, Course Gain Attenuators	43				
Attenuation (at 0dB)		−0.5	0	+0.5	dB
Cumulative Attenuation Error (w.r.t. attenuation at 0dB)		−1.0	0	1.0	dB

Notes:

40 Power-up refers to issuing a C-BUS command to turn on an output. These limits apply only if V_{BIAS} is on and stable. At power supply switch-on, the default state is for all blocks, except the XTAL and C-BUS interface, to be in placed in powersave mode.

41 For each output pin. With respect to the output driving a 20kΩ load to $AV_{DD}/2$.

42 Small signal impedance, at AV_{DD} = 3.3V and Tamb = 25°C.

43 Figures relate to attenuator block only. Design Value. Overall attenuation input to output has a design tolerance of 0dB ±1.0dB.

44 The levels of I/Q Output Fine Gain and Offset (registers $5D and $5E) should be adjusted so that the output voltage remains between 20% and 80% of AV_{DD} on each output pin (when 0dB of coarse output gain is used). This will produce the best performance when the device operates with AV_{DD} = 3.3V.

45 With respect to the output driving a 32Ω load to $AV_{DD}/2$.

46 With respect to the outputs driving a differential load of 8Ω.

47 Differential power output into an 8Ω load at AV_{DD} =3.0V.

48 If intended to be used to produce stable dc voltages, it is recommended that external filtering be used to reduce the amplitude of any “idle tones” that may be produced.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Auxiliary Signal Inputs (AuxADC1-4)					
Source Output Impedance	50	–	–	24	kΩ
Auxiliary 10-Bit ADC					
Resolution		–	10	–	Bits
Conversion Time	51	–	225	–	µs
Sample Rate		1	–	512	Hz
Input Impedance					
Resistance		–	TBD	–	MΩ
Capacitance		–	5	–	pF
Offset Error	53, 54	–	–	±18	mV
Integral Non-linearity	53, 54	–	–	±2	LSBs
Differential Non-linearity	52, 53	–	–	±1	LSBs
Auxiliary 10-Bit DACs					
Resolution		–	10	–	Bits
Conversion Time	51	–	60	–	µs
Settling Time to 0.5 LSB		–	10	–	µs
Offset Error	53, 54	–	–	±20	mV
Resistive Load		5	–	–	kΩ
Integral Non-linearity	53, 54	–	–	±4	LSBs
Differential Non-linearity	52, 53	–	–	±1	LSBs

Notes:
50 Denotes output impedance of the driver of the auxiliary input signal, to ensure <1 bit additional error under nominal conditions.
51 Typical – based on 9.6MHz Xtal or external oscillator.
52 Guaranteed monotonic with no missing codes.
53 Specified between 2.5% and 97.5% of the full-scale range.
54 Calculated from the line of best fit of all the measured codes.

8.1.4 Performance Characteristics

For the following conditions unless otherwise specified:
External components as recommended in section 5.
Maximum load on digital outputs = 30pF.
Xtal Frequency = 9.6MHz ±0.002% (20ppm); Tamb = –40°C to +85°C.
AV_{DD} = DV_{DD} = 3.0V to 3.6V.
Input stage gain = 0dB, Output stage attenuation = 0dB.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Supply Current					
Rx Mode					
DI_{DD} (96,000samples/s)	60	–	TBD	–	mA
AI_{DD} (AV_{DD} = 3.3V)	60	–	7.7	–	mA
Tx Mode					
DI_{DD} (96,000samples/s)	61	–	TBD	–	mA
AI_{DD} (AV_{DD} = 3.3V)	61	–	8.0	–	mA

Notes:
60 Two signal ADC at specified sample rate, all auxiliary functions powersaved.
61 Two signal DAC at specified sample rate, all auxiliary functions powersaved.

8.2 C-BUS Timing

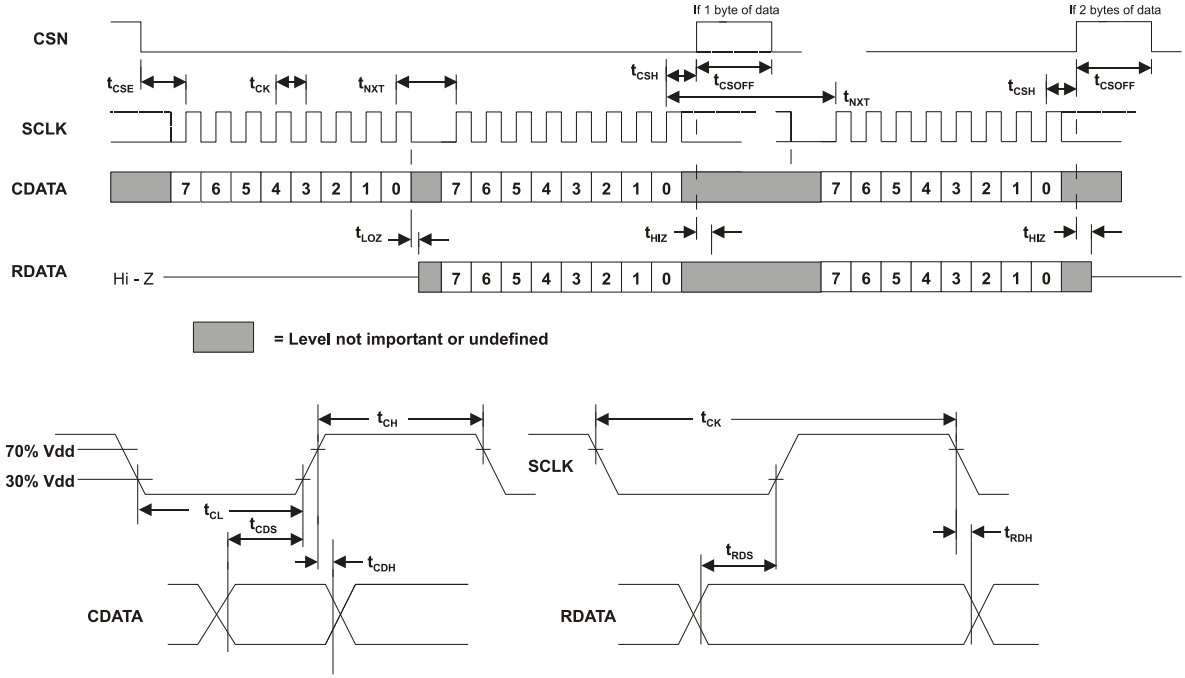


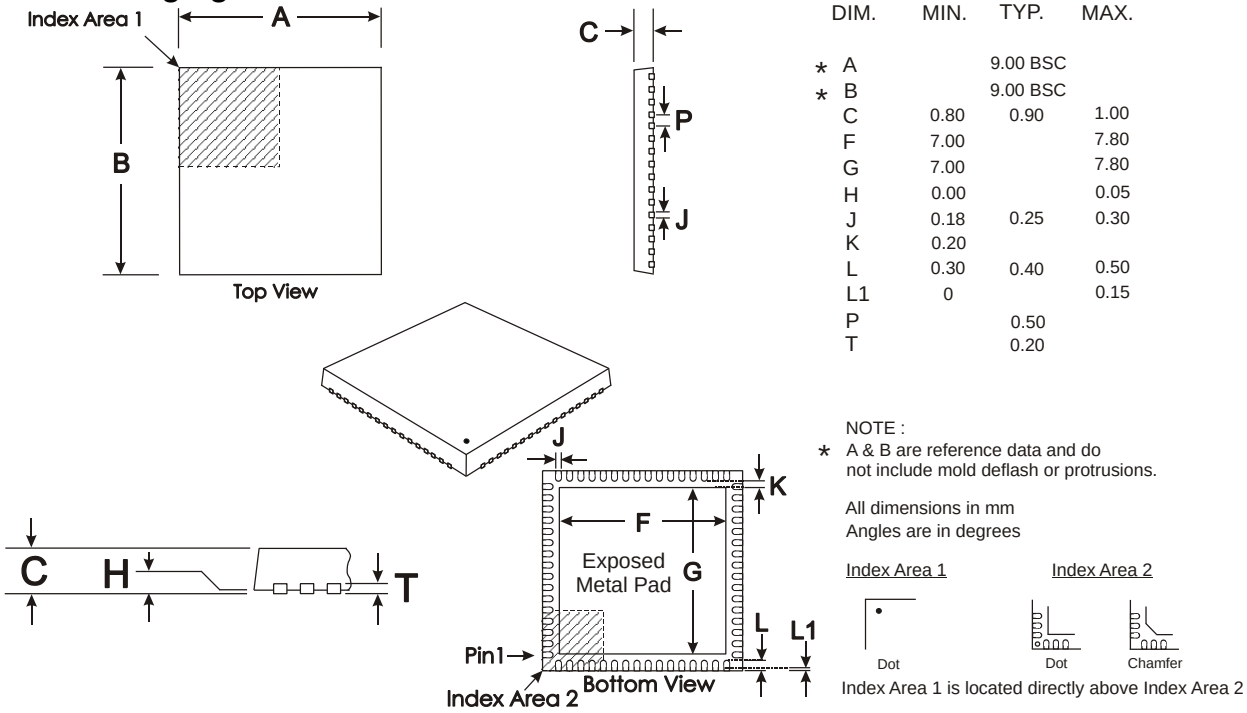
Figure 29 C-BUS Timing

C-BUS Timing		Notes	Min.	Typ.	Max.	Unit
t_{CSE}	CSN Enable to SCLK high time		100	–	–	ns
t_{CSH}	Last SCLK high to CSN high time		100	–	–	ns
t_{LOZ}	SCLK low to RDATA output enable Time		0.0	–	–	ns
t_{HIZ}	CSN high to RDATA high impedance		–	–	1.0	µs
t_{CSOFF}	CSN high time between transactions		1.0	–	–	µs
t_{NXT}	Inter-byte time		100	–	–	ns
t_{CK}	SCLK cycle time		100	–	–	ns
t_{CH}	SCLK high time		50	–	–	ns
t_{CL}	SCLK low time		50	–	–	ns
t_{CDS}	CDATA set-up time		75	–	–	ns
t_{CDH}	CDATA hold time		25	–	–	ns
t_{RDS}	RDATA set-up time		50	–	–	ns
t_{RDH}	RDATA hold time		0	–	–	ns

Notes:
1. Depending on the command, 1 or 2 bytes of CDATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. RDATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
2. Data is clocked into the peripheral on the rising SCLK edge.
3. Commands are acted upon between the last rising edge of SCLK of each command and the rising edge of the CSN signal.
4. To allow for differing µC serial interface formats C-BUS compatible ICs are able to work with SCLK pulses starting and ending at either polarity.
5. Maximum 30pF load on IRQN pin and each C-BUS interface line.

These timings are for the latest version of C-BUS and allow faster transfers than the original C-BUS timing specification. The CMX7861 can be used in conjunction with devices that comply with the slower timings, subject to system throughput constraints.

8.3 Packaging



	DIM.	MIN.	TYP.	MAX.
*	A		9.00 BSC	
*	B		9.00 BSC	
	C	0.80	0.90	1.00
	F	7.00		7.80
	G	7.00		7.80
	H	0.00		0.05
	J	0.18	0.25	0.30
	K	0.20		
	L	0.30	0.40	0.50
	L1	0		0.15
	P		0.50	
	T		0.20	

NOTE :
* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Index Area 1 Index Area 2

Index Area 1 is located directly above Index Area 2

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 30 Mechanical Outline of 64-pin VQFN (Q1)

Order as part no. CMX7861Q1

As package dimensions may change after publication of this datasheet, it is recommended that you check for the latest packaging information from the Design Support/Package Information page of the CML website: [www.cmlmicro.com].

About *FirmASIC*®

CML's proprietary *FirmASIC*® component technology reduces cost, time to market and development risk, with increased flexibility for the designer and end application. *FirmASIC*® combines Analogue, Digital, Firmware and Memory technologies in a single silicon platform that can be focused to deliver the right feature mix, performance and price for a target application family. Specific functions of a *FirmASIC*® device are determined by uploading its Function Image™ during device initialisation. New Function Images™ may be later provided to supplement and enhance device functions, expanding or modifying end-product features without the need for expensive and time-consuming design changes. *FirmASIC*® devices provide significant time to market and commercial benefits over Custom ASIC, Structured ASIC, FPGA and DSP solutions. They may also be exclusively customised where security or intellectual property issues prevent the use of Application Specific Standard Products (ASSP's).

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