CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CMX8341
Digital PMR (dPMR) Baseband Processor

D/8341/7 January 2014

DATASHEET

Advance Information

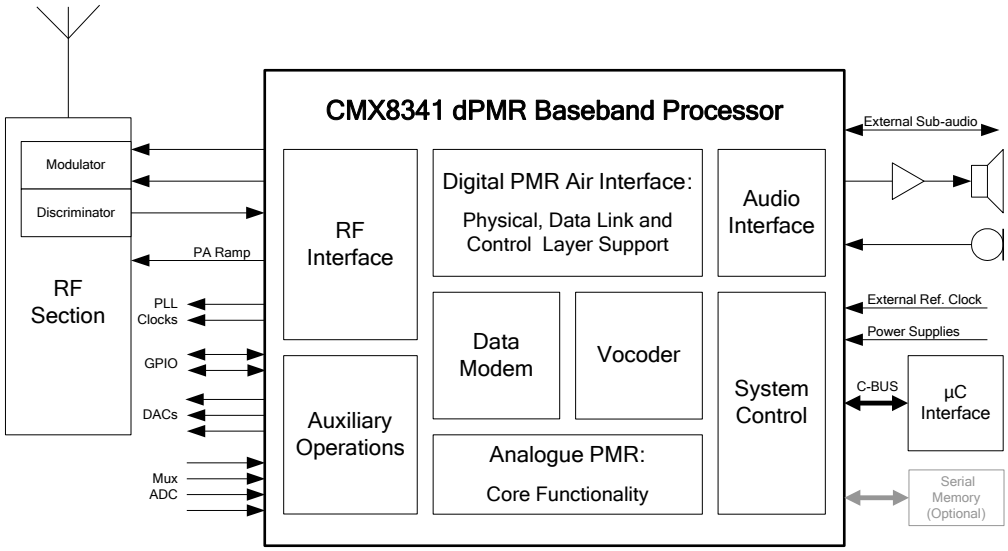
8341 FI-1.x Dual-mode Analogue PMR and Digital PMR (dPMR) Baseband Processing

Features

- Digital PMR (dPMR) Baseband Processor
  - dPMR (ETSI TS 102 490) Compliant
  - Air Interface Physical Layer (Layer 1)
  - Air Interface Data Link layer (Layer 2)
  - 4FSK Modem
    - Soft-decision Decoding
    - AFSD (Automatic Frame Sync Detection)
- RALCWI Vocoder
  - Fully Embedded Implementation
  - No Licensing or Royalty payments
  - 3600bps Over Air Data Rate (2400bps Voice plus 1200bps Robust FEC)
  - 4-bit Viterbi Soft-decision Decoding
- Analogue PMR (Legacy mode)
  - Full Audio Band Processing
  - Sub-audio Filtering
  - CTCSS and DCS
  - 12.5 and 25kHz Channel Filters
- Built on *FirmASIC*™ Technology
  - Function Image™ 8341FI-1.x Required
  - Serial Memory or Host Loading
  - Integration Roadmap
- Auxiliary functions
  - 2 System Clock Outputs
  - Tx PA Ramp DAC
  - 3 DACs, 4 inputs Multiplexed to 2 ADCs
  - GPIO
  - Tx Enable and Rx Enable Outputs
- Half-duplex Operation
- Input from RF Discriminator
- 2-point Modulation Drivers
- Audio Output with Volume Control
- Microphone Input
- Low Power Operation
- LQFP packaging

Applications

- Low Cost Digital PMR Radios
- Low Cost Digital PMR with Legacy Analogue PMR Mode



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1 Brief Description

The 8341FI-1.x Function Image™ (FI) implements a half-duplex digital PMR processor including: 4FSK modem, a large proportion of the dPMR™ Air Interface; Physical, Data Link and Control layers, and an embedded low bit rate RALCWI Vocoder (with no license or royalties required).

In conjunction with a suitable host and a limiter/discriminator based RF transceiver, a compact, low cost, low power digital PMR radio conforming to ETSI's dPMR standard TS 102 490 can be realised. Both ISF and CSF configurations are supported, including built-in support for BCD addressing modes. Dual mode, analogue/digital PMR operation can also be achieved with the CMX8341. The device is also compatible with ETSI's dPMR standard TS 102 658 for Mode 1 operation.

The embedded functionality of the CMX8341, managing voice and data systems autonomously including the Vocoder minimises host microcontroller interactions enabling the lowest operating power and therefore the longest battery life for a dPMR radio.

The CMX8341 utilises CML's proprietary *FirmASIC*® component technology. On-chip sub-systems are configured by a Function Image™: this is a data file that is uploaded during device initialisation and defines the device's function and feature set. The Function Image™ can be loaded automatically from an external serial memory or host µController over the built-in C-BUS serial interface. The device's functions and features may be enhanced by subsequent Function Image™ releases, facilitating in-the-field upgrades. This document refers specifically to the features provided by Function Image™ 8341 FI-1.x.

Other features include two auxiliary ADCs with four selectable inputs and four auxiliary DAC interfaces (with an optional RAMDAC on the first DAC output, to facilitate transmitter power ramping).

The device has flexible powersaving modes and is available in the L8 (LQFP) package.

This Datasheet is the first part of a two-part document comprising Datasheet and User Manual: the User Manual can be obtained by registering your interest in this product with your local CML representative.

Text in grey may be implemented in later versions of the Function Image™ 8341 FI-1.x.

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It is always recommended that you check for the latest product datasheet version from the Datasheets page of the CML website: [www.cmlmicro.com].

1.1 History

Version	Changes	Date
7	Figure 9 Updated to match latest ETSI version 8.4.4 Add text about analogue mode selection 8.5.3 Tx mode test added 8.5.5 Rx mode dPMR added 8.5.6 Rx mode raw added Table 10 Rx mode raw added 10.1.5 RAMDAC and DAC2 tonegen updated to latest descriptions 10.1.10 Add input invert bit $B0:b7 10.1.11 Clarification to setting $B1:b1,0 10.1.20 Rx raw mode added, Tx test mode (repeated word for dPMR Assoc. test modes) added 10.1.22 $C3 register description describes digital functions (as well as analogue), RAMDAC multiplier added 10.1.23 $C5 bit definitions corrected (matches 7131/7141FI-1 and FI-5) 10.1.25 $C7:b7 (enable/disable vocoder control) added 10.1.24 Add note on Prog Flag cleared in Rx and Tx modes 10.1.26 Pass-through description updated 10.1.28 $CA bit definitions corrected (matches FI-1 and FI-5) 10.1.29 $CB bit definitions corrected (matches FI-1 and FI-5) 10.2.3 Rx analogue pass-through added	28/01/14
6	Pin 50 now connects to Pin 49. Figure 2 and pinout table corrected. Correction of bit order in Table 8. Sync Mode and Reset/Abort descriptions added to 8.5. Bit error and value to stop RAMDAC clarified in 10.1.5 Bit settings clarified in 10.1.22 Setting of P1.20 added to 10.2.2 Bit settings clarified in 10.2.3	24/10/12
5	Rx Pass-through mode added – same as RxEye mode, but without the RRC filter Bug in setting SPI Codec SCLK polarity fixed Internal sub-audio now enabled by default, P2.0 default value changed to $E030 Description of reset/abort added to 11.1.20 Minimum Rx Input Level now specified in 9.1.4 dPMR MoU references changed to dPMR Association Corrected Tx PRBS command to $0032 (not $0023) References to ATB010 removed	30/5/12
4	Added CTCSS and DCS internal generation/detection Removed references to raw mode Added reference to TS 102 658 Mode 1 Removed Figure 28 and added FI Updates	15/6/11
3	Standardisation with CMX7141 FI-5.x Datasheet and User Manual EEPROM references changed to serial memory Minor typographical improvements	7/6/11
2	Corrections and additions following further review of Advance document. Addition of analogue PMR functions in FI-1.0.0.1	26/1/11
1	Original document, prepared for initial release	04/11/10

This is Advance Information; changes and additions may be made to this specification. Parameters marked TBD or left blank will be included in later issues. Items that are highlighted or greyed out should be ignored. These will be clarified in later issues of this

document. **Information in this advance document should not be relied upon for final product design.**

2 Block Diagram

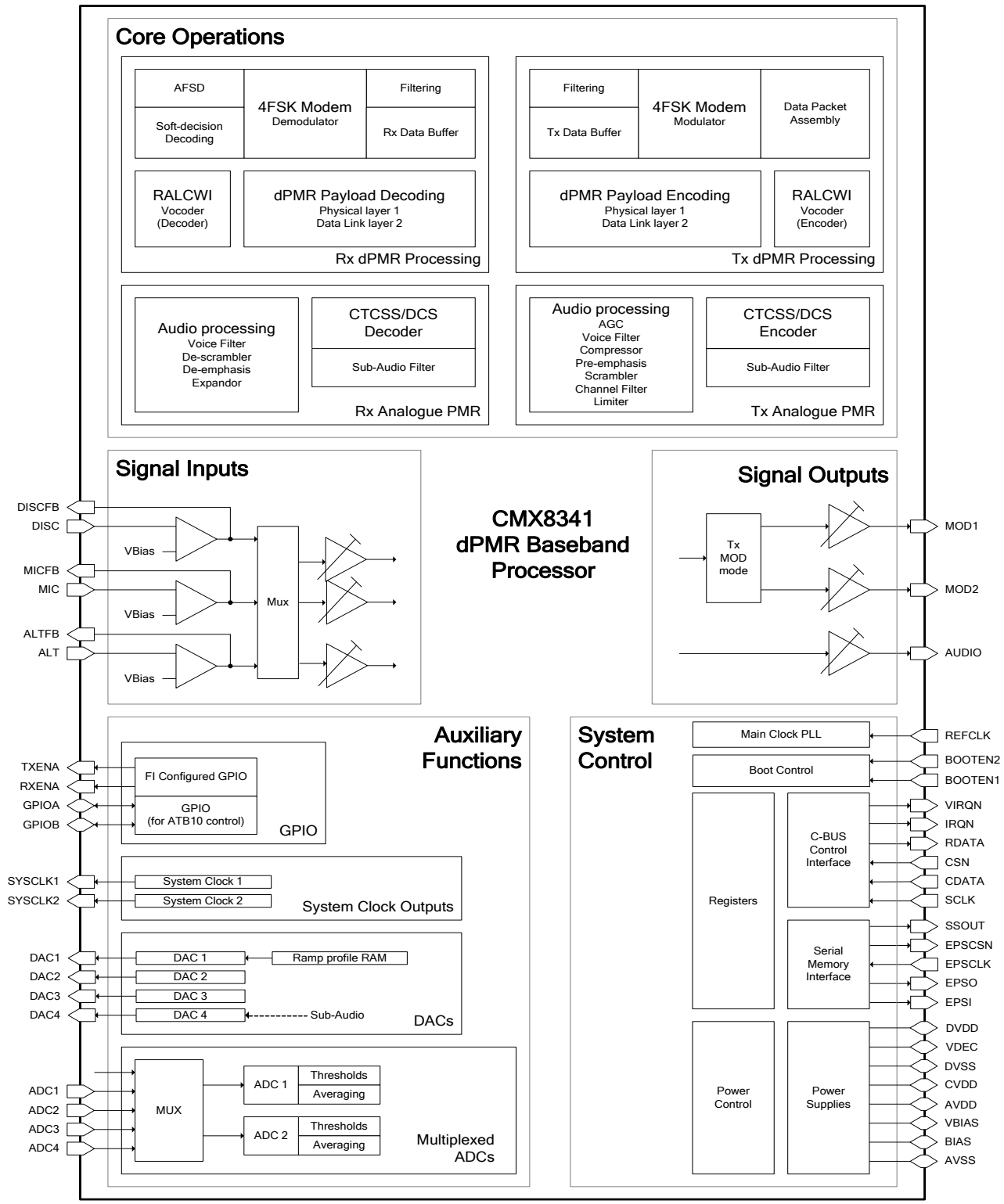


Figure 1 Block Diagram

3 Signal List

CMX8341L8	Pin		Description
Pin No.	Name	Type	
1	GPIOB	IP + PU or OP	General-purpose input/output.
3	SYSCLK1	OP	Synthesised Digital System Clock Output 1
7	TXENA	OP	Tx Enable – active low when in Tx
10	DISC	IP	Channel 1 inverting input
11	-	-	Connect to pin 41
12	DISCFB	OP	Channel 1 input amplifier feedback
13	-	-	Connect to pin 27 (BIAS)
15	ALT	IP	Channel 2 inverting input
16	ALTFB	OP	Channel 2 input amplifier feedback
18	MICFB	OP	Channel 3 input amplifier feedback
20	MIC	IP	Channel 3 inverting input
22	OUTP	OP	Audio Positive Output in digital radio mode
23	MOD1	OP	Modulator 1 output
24	MOD2	OP	Modulator 2 output
25	OUTN	OP	Audio Negative Output in digital radio mode. Leave unconnected if switching between the digital (OUTP) output and the analogue (AUDIO) output. See Figure 4.
28	AUDIO	OP	Audio output in analogue radio mode
29	AUXADC1	IP	Auxiliary ADC input 1
30	AUXADC2	IP	Auxiliary ADC input 2
33	AUXADC3	IP	Auxiliary ADC input 3
34	AUXADC4	IP	Auxiliary ADC input 4
			Each of the two ADC blocks can select its input signal from any one of these input pins, or from the MIC, ALT or DISC input pins. See section 8.9 for details.
36	AUXDAC1	OP	Auxiliary DAC output 1
37	AUXDAC2	OP	Auxiliary DAC output 2
41	-	-	Connect to pin 11
42	AUXDAC3	OP	Auxiliary DAC output 3
48	AUXDAC4	OP	Auxiliary DAC output 4 / Filtered Sub-Audio Output
50	SYNC	BI	SYNC output. Connect to pin 49.
54	-	-	Connect to pin 56
55	REFCLK	IP	Input from the external clock source
56	-	-	Connect to pin 54

CMX8341L8	Pin		Description
Pin No.	Name	Type	
59	CDATA	IP	C-BUS Command Data: Serial data input from the µC.
61	RDATA	T/S	C-BUS Reply Data: A 3-state C-BUS serial data output to the µC. This output is high impedance when not sending data to the µC.
62	SSOUT	OP	Serial Memory Interface – Chip Select. Connect to pin 92
64	RESETN	IP	Vocoder section General Reset (active low, no pullup)
69	SCLK	IP	C-BUS Serial Clock: The C-BUS serial clock input from the µC.
71	SYSCLK2	OP	Synthesised Digital System Clock Output 2
73	CSN	IP	C-BUS Chip Select: The C-BUS chip select input from the µC - there is no internal pullup on this input (active low).
76	EPSI	OP	Serial Memory Interface – Data Output from CMX8341
78	EPSCLK	OP	Serial Memory Interface – Clock
81	EPSO	IP + PD	Serial Memory Interface – Data Input to CMX8341
83	EPSCSN	OP	Serial Memory Interface – Memory Select (active low)
84	BOOTEN1	IP + PD	Used in conjunction with BOOTEN2 to determine the operation of the bootstrap program.
86	-	-	Connect to pin 78 (EPSCLK)
87	BOOTEN2	IP + PD	Used in conjunction with BOOTEN1 to determine the operation of the bootstrap program.
88	-	-	Connect to pin 76 (EPSI)
90	-	-	Connect to pin 81 (EPSO)
91	IRQN	OP	C-BUS Interrupt Request: A 'wire-ORable' output for connection to the Interrupt Request input of the µC. Pulled down to DV_{SS} when active and is high impedance when inactive. An external pull-up resistor (R1) is required.
92	-	-	Connect to pin 62 (SSOUT)
93	VIRQN	OP	Connect an external pull-up resistor (R2) to DVDD
97	RXENA	OP	Rx Enable – active low when in Rx mode.
98	GPIOA	IP + PU or OP	General-purpose input/output.

CMX8341L8 Pin No.	Pin Name	Pin Type	Description
Power Supplies and No Connections			
32, 47, 57, 60, 66, 70, 72, 74, 94	DVDD	PWR	DV_{DD}: Digital +3.3V supply rail. This pin should be decoupled to DV_{SS} by capacitors mounted close to the device pins.
53, 95	VDEC	PWR	V_{DEC}: Internally generated 2.5V supply voltage. Must be decoupled to DV_{SS} by capacitors mounted close to the device pins. No other connections allowed.
31, 96	CVDD	PWR	Digital core +1.8V supply rail. This pin should be decoupled to DV_{SS} by capacitors mounted close to the device pins.
4, 6, 44, 49, 51, 52, 63, 65, 68, 85, 89, 100	DVSS	PWR	DV_{SS}: Negative Digital Supply
5, 9, 17, 19, 21, 40	AVSS	PWR	AV_{SS}: Negative Analogue Supply
2, 14, 26,35	AVDD	PWR	AV_{DD}: Analogue +3.3V supply rail. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to AV_{SS} by capacitors mounted close to the device pins.
8	VBIAS	PWR	Internally generated bias voltage of about $AV_{DD}/2$, except when the device is in 'Powersave' mode when voltage on VBIAS pin will discharge to AV_{SS}. Must be decoupled to AV_{SS} by a capacitor mounted close to the device pins. No other connections allowed. Do not connect to BIAS pin.
27	BIAS	PWR	Internally generated bias voltage of about $AV_{DD}/2$, except when the device is in 'Powersave' mode when voltage on BIAS pin will discharge to AV_{SS}. Must be decoupled to AV_{SS} by a capacitor mounted close to the device pins No other connections allowed. Do not connect to VBIAS pin.
38, 39, 43, 45, 46, 58, 67, 75, 77, 79, 80, 82, 99	n/c	NC	Do not make any connection to this pin

Notes:
IP = Input
IP + PU = Input with internal pullup resistor
IP + PD = Input with internal pulldown resistor
OP = Output
BI = Bidirectional Digital Signal
T/S = 3-state Digital Output
PWR = Power Supply
NC = No Connection

3.1 Signal Definitions

Table 1 Definition of Power Supply and Reference Voltages

Signal Name	Pins	Usage
AV_{DD}	AVDD	3.3V Power supply for analogue circuits
DV_{DD}	DVDD	3.3V Power supply for digital circuits
DV_{CORE}	CVDD	1.8V Power supply for digital circuits
V_{DEC}	VDEC	2.5V Internally-derived power supply for digital circuits
V_{BIAS}	VBIAS, BIAS	1.65V Internally-derived power supply for analogue circuits
AV_{SS}	AVSS	Ground for all analogue circuits
DV_{SS}	DVSS	Ground for all digital circuits

4 External Components

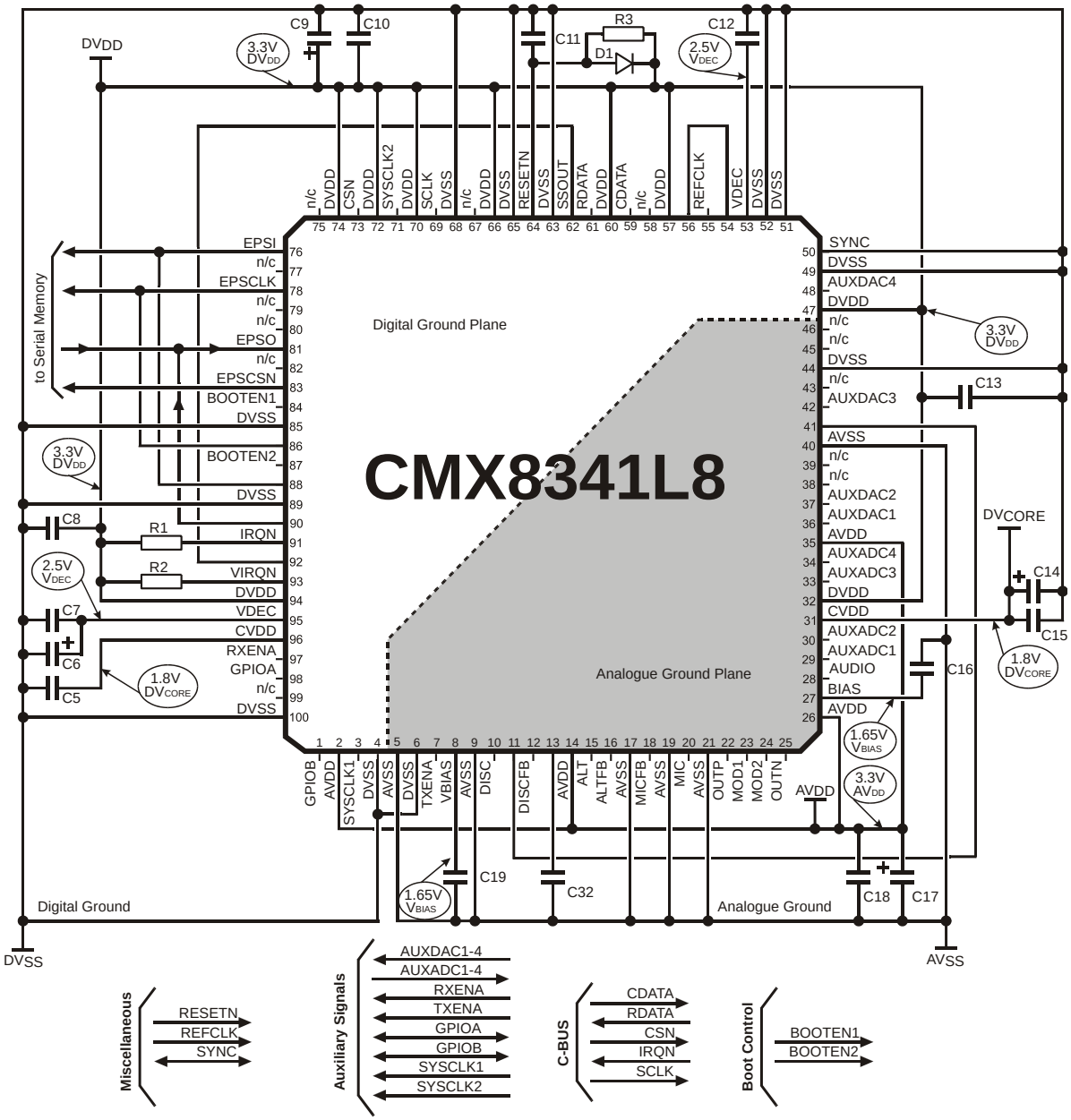


Figure 2 Recommended External Components

To achieve good noise performance, V_{DD} decoupling is very important. It is recommended that the printed circuit board is laid out with analogue and digital ground planes in the CMX8341 area to provide a low impedance connection between the V_{SS} pins and the V_{DD} decoupling capacitors.

Table 2 Recommended Component Values

R1	100kΩ		R9	100kΩ		C1	n/f		C8	10nF		C16	100nF		C24	100pF
R2	100kΩ		R10	100kΩ		C2	n/f		C9	10µF		C17	10µF		C25	100pF
R3	470kΩ		R11	22kΩ		C3	n/f		C10	10nF		C18	10nF		C26	470pF
R4	10kΩ		R12	100kΩ		C4	n/f		C11	1.0µF		C19	100nF		C27	470pF
R5	100kΩ		R13	22kΩ		C5	100nF		C12	10nF		C20	1.0µF		C28	100pF
R6	100kΩ		R14	100kΩ		C6	10µF		C13	10nF		C21	1.0µF		C29	100pF
R7	100kΩ		D1	1N4148		C7	10nF		C14	10µF		C22	n/f		C30	1.0µF
R8	100kΩ		TG1	TS5A459DBVR					C15	100nF		C23	100pF		C31	1.0µF
															C32	100nF

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated. Please also refer to Figure 4.

4.1 Component Value Selection

1. R7 should be selected to provide the desired dc gain of the discriminator input, as follows:
$$|GAIN_{DISC}| = 100k\Omega / R7$$
2. The gain should be such that the resultant output at the DISCFB pin is within the DISC input signal range specified in 8.12.2. For 4FSK modulation, this signal should be dc coupled from the Limiter/ Discriminator output.
3. R6 should be selected to provide the desired dc gain (assuming C21 is not present) of the alternative input as follows:
$$|GAIN_{ALT}| = 100k\Omega / R6$$
4. The gain should be such that the resultant output at the ALTFB pin is within the alternative input signal range specified in 8.12.
5. R5 should be selected to provide the desired dc gain (assuming C20 is not present) of the microphone input as follows:
$$|GAIN_{MIC}| = 100k\Omega / R5$$
6. The gain should be such that the resultant output at the MICFB pin is within the microphone input signal range specified in 8.12.1. For optimum performance with low signal microphones, an additional external gain stage may be required.
7. C21 and C20 should be selected to maintain the lower frequency roll-off of the MIC and ALT inputs as follows:
$$C21 \geq 1.0\mu F \times |GAIN_{ALT}|$$
$$C20 \geq 30nF \times |GAIN_{MIC}|$$
8. ALT and ALTFB connections allow the user to have a second discriminator, microphone input or external sub-audio signalling source. Component connections and values are as for the respective DISC and MIC networks. If this input is not required, the ALT pin should be connected to AV_{SS}.

9. AUDIO output is only used in the Function Image™ 8341FI-1.x when analogue audio functions are selected. The OUTP digital audio output is passed through a transmission gate (TG1), so that it can be turned off when digital mode is not selected.

4.2 Reference Clock Frequency

The Function Image™ 8341 FI-1.x is designed to work with an external reference clock source of 19.2MHz, connected to the REFCLK pin.

4.3 Serial Memory Connections

Connections for a typical 512Kbyte serial memory are shown below:

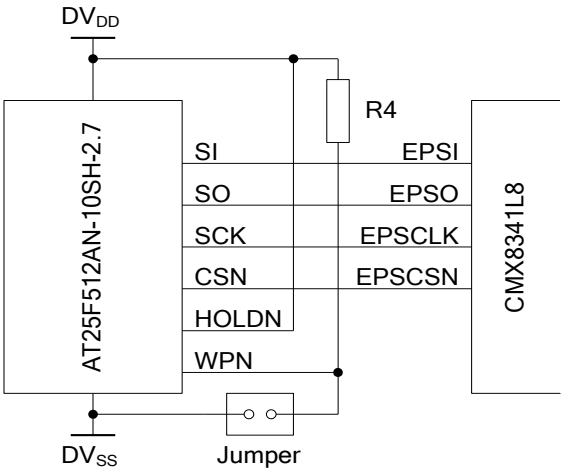


Figure 3 Serial Memory Connections

4.4 Other Connections

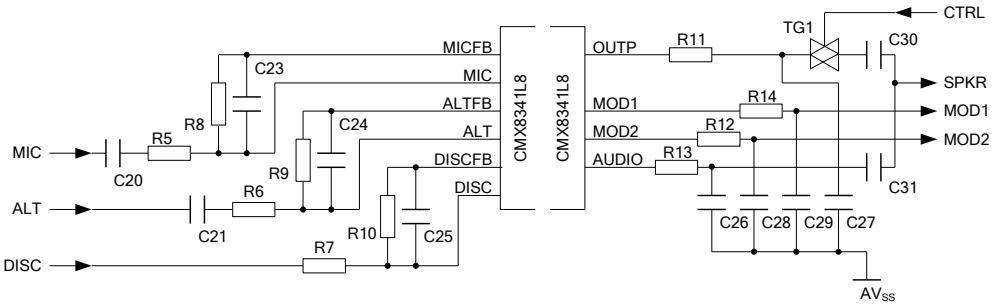


Figure 4 Other Connections

4.5 Autonomous Signal Routing

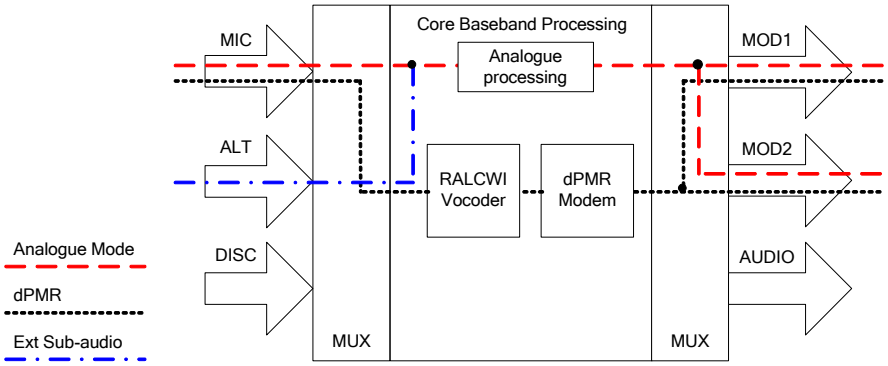


Figure 5 Tx Routing – Autonomous mode

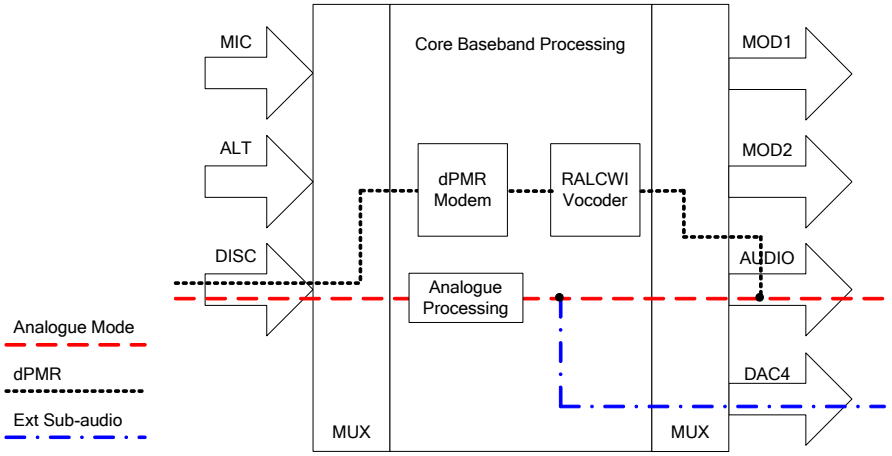


Figure 6 Rx Routing – Autonomous mode

5 General Description

A block diagram of the device is shown in Figure 1. A flexible power control facility allows the device to be placed in its optimum powersave mode when not actively processing signals. The device includes a reference clock input and provides 2 x PLL system clock outputs for general use, if required.

5.1 Product Features

5.1.1 dPMR Features

The 8341FI-1.x Function Image™ is intended for use in half duplex digital PMR equipment using 4FSK modulation at 4800bps suitable for 6.25kHz channel systems.

Complete dPMR baseband processing is provided, including the RALCWI Vocoder function. Much of the dPMR ETSI TS 102 490 standard Air Interface protocol is embedded in the 8341FI-1.x Function Image™ operation namely:

Air Interface Physical Layer 1

- 4FSK modulation and demodulation
- Bit and symbol definition
- Frequency and symbol synchronisation
- Transmission burst building and splitting

Air Interface Data Link Layer 2

- Channel coding (FEC, CRC)
- Interleaving, de-interleaving and bit ordering
- Frame and superframe building and synchronising
- Burst and parameter definition
- Link addressing (source and destination)
- Interfacing of voice applications (voice data) with the Physical Layer
- Data bearer services
- Exchanging signalling and/or user data with the Call Control Layer
- Automatic Own-ID and Group-ID detection

5.1.2 Analogue PMR Features

The device provides legacy analogue PMR operation including:

- Complete voice processing
  - 300Hz HPF
  - 12.5kHz channel filter
  - 25kHz channel filter
  - Hard Limiter with anti-splatter filter
  - Compandor
  - Scrambler
  - Voice AGC
  - Level adjust
- Inband Tone generation
- External Sub-audio filtering
- Internal sub-audio (CTCSS and DCS) generation and detection

The selection of these Analogue processing modes is controlled by the Analogue Mode bits in the Modem Control register, $C1:b15-8.

5.1.3 Universal PMR Functions

These include:

- RAMDAC operation
- TxEnable (TXENA) and Rx Enable (RXENA) hardware signals
- Two-point modulation outputs
- Hard or soft data output options
- Embedded RALCWI Vocoder

5.1.4 Auxiliary Functions

- Two programmable system clock outputs
- Two auxiliary ADCs with four selectable external input paths
- Four auxiliary DACs, one with built-in programmable RAMDAC
- GPIO pins

5.1.5 System Interface

- Optimised C-BUS (4-wire high-speed synchronous serial command/data bus) interface to host for control and data transfer
- Open drain IRQ to host
- Serial memory boot mode
- C-BUS (host) boot mode

5.2 Aspects of System Design

5.2.1 dPMR Data Transfer

When transmitting, an initial block of payload or control channel data will need to be loaded from the host into the C-BUS TxData registers. The CMX8341 can then format and transmit that data while at the same time loading in the following data blocks from the host or the Vocoder section.

When receiving, the host needs to consider that when a signal is received over the air there will be a processing delay while the CMX8341 filters, demodulates and decodes the output data before presenting it to the host or the Vocoder section. For the best performance, voice payload data can be output in soft-decision (4-bit log-likelihood ratio) format, compatible with the Vocoder section, although this mode increases the data transfer rate over C-BUS by a factor of four.

5.2.2 RSSI Measurement

The AuxADC provided by the CMX8341 can be used to detect the Squelch or RSSI signal from the RF front-end while the device is in Rx or Idle mode. This allows a significant degree of powersaving within the CMX8341 and avoids the need to wake the host up unnecessarily. The host programmable AuxADC thresholds allow for user selection of squelch threshold settings.

5.2.3 Serial Memory Connection

A Serial Memory interface with a dedicated chip select pin (EPSCSN) connects the external serial memory, which may be used to hold the contents of the Function Image™, to the CMX8341.

6 dPMR Modem Description

This modem is set to run at 4800bps, occupying a 6.25kHz bandwidth RF channel. It has been designed such that, when combined with suitable RF, host controller and appropriate control software, it meets the requirements of the EN 301 166 standards. See www.etsi.org for details of these standards.

TS 102 490 is available on the ETSI web site (www.etsi.org), which describes a 6.25kHz channel spacing FDMA dPMR system. This standard uses a 4FSK modulation scheme with an over-air bit rate of 4800bps (ie. 2400 symbols per second). With respect to dPMR formatted modes of operation, this document should be read in conjunction with the ETSI standard.

The dPMR standard does not specify a voice coding algorithm: the RALCWI Vocoder in the CMX8341 is suitable for this purpose.

Version 1.5.1 of TS 102 490 section 5.16 introduces two additional vocoder control bits which specify which vocoder is in use for a particular voice call. These additional bits are supported by the 8341FI-1.x Function Image™ and should be set appropriately by the host. These have been further defined by the dPMR Association as:

Version	Vocoder
00	AMBE+2
01	To be selected by Chinese DRA
10	RALCWI
11	Manufacturer defined

6.1 Modulation

The dPMR 4FSK modulation scheme as defined in TS 102 490 section 12 operates in a 6.25kHz channel bandwidth with a deviation index of 0.29 and has an over-air bit rate of 4800bps (2400 symbols per second). RRC filters are implemented in both Tx and Rx with a filter “alpha” of 0.2. The maximum frequency error is +/-625Hz and the CMX8341 can adapt to the maximum time-base clock drift of 2ppm over the duration of a 180-second burst. Figure 9 shows the basic parameters of the 4FSK modulation, symbol mapping and filtering requirements.

Figure 7 and Figure 8 show a transmitted PRBS waveform, as recorded on a spectrum analyser in 36k span and zero-span mode, having been two-point modulated using a suitable RF transmitter.

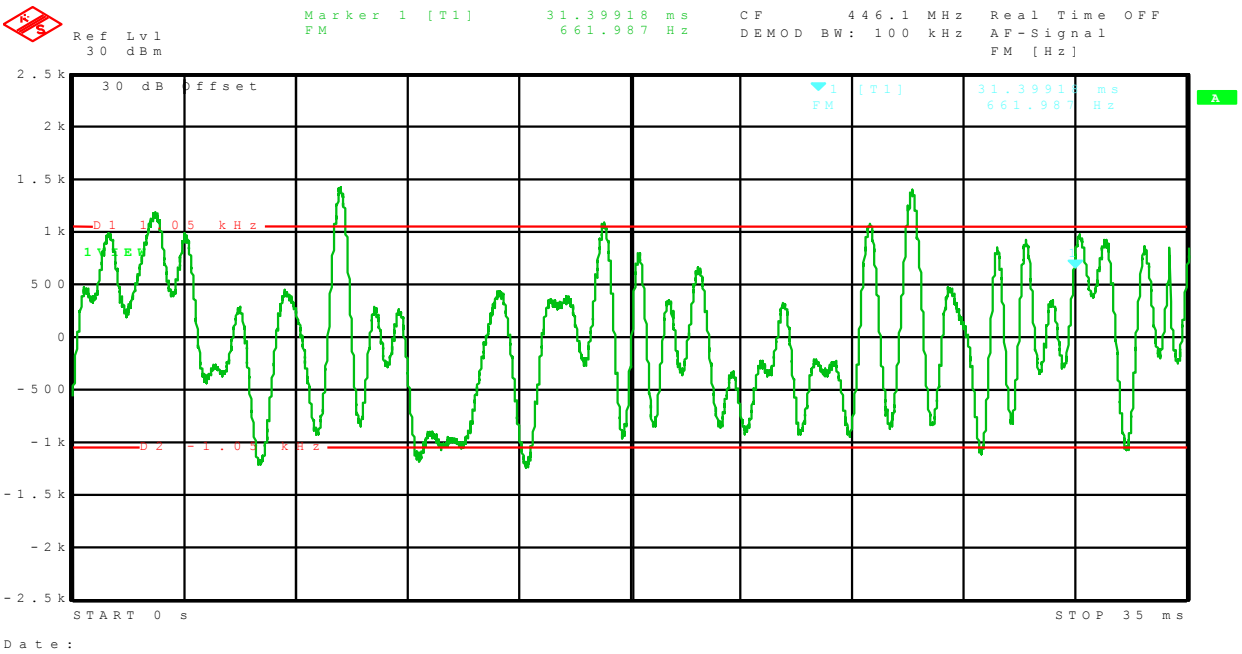


Figure 7 4FSK PRBS Waveform - Modulation

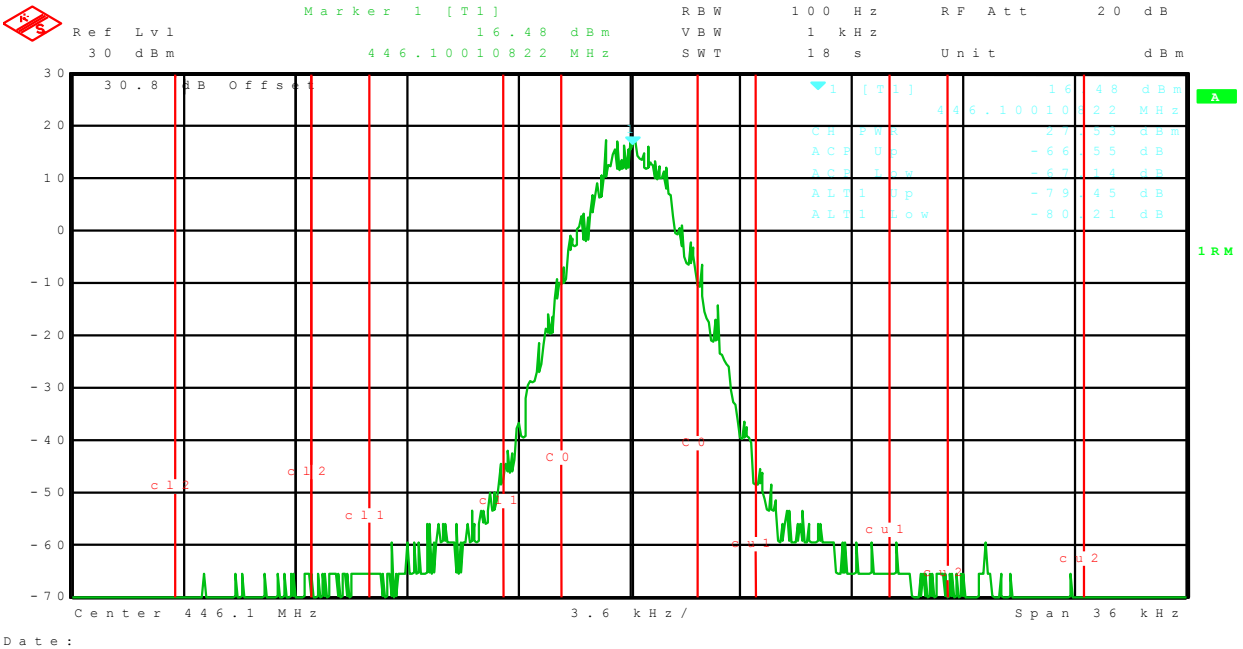
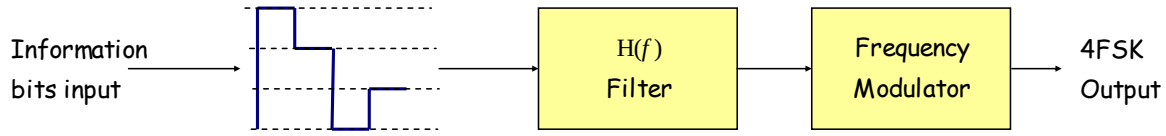


Figure 8 4FSK PRBS Waveform - Spectrum

*Tx Baseband Filter

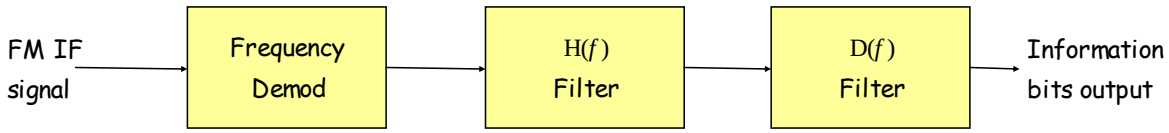


$$|H(f)| = \begin{cases} 1 & , \quad 0 \le |f| < (1-\alpha)/2T \\ \cos[(T/4\alpha)(2\pi|f| - \pi(1-\alpha)/T] & , \quad (1-\alpha)/2T \le |f| < (1+\alpha)/2T \\ 0 & , \quad (1+\alpha)/2T \le |f| \end{cases}$$

$\alpha = 0.2 \quad T = 1/2400$

4 FSK Deviation		
Di-bit	Symbol	Deviation
01_2	+3	+1 050Hz
00_2	+1	+350Hz
10_2	-1	-350Hz
11_2	-3	-1050Hz

*Rx Baseband Filter



$$|H(f)| = \begin{cases} 1 & , \quad 0 \le |f| < (1-\alpha)/2T \\ \cos[(T/4\alpha)(2\pi|f| - \pi(1-\alpha)/T] & , \quad (1-\alpha)/2T \le |f| < (1+\alpha)/2T \\ 0 & , \quad (1+\alpha)/2T \le |f| \end{cases}$$

$$|D(f)| = \frac{\pi f T}{\sin(\pi f T)}$$

$\alpha = 0.2 \quad T = 1/2400$

Figure 9 dPMR Modulation Characteristics

6.2 Internal Data Processing

The CMX8341 operates as a half-duplex device, either receiving signals from the RF circuits in Rx mode, or sourcing signals to the RF circuits in Tx mode. It also has a low power Idle mode to support battery saving protocols. The internal data processing blocks for Tx and Rx modes are illustrated in Figure 10.

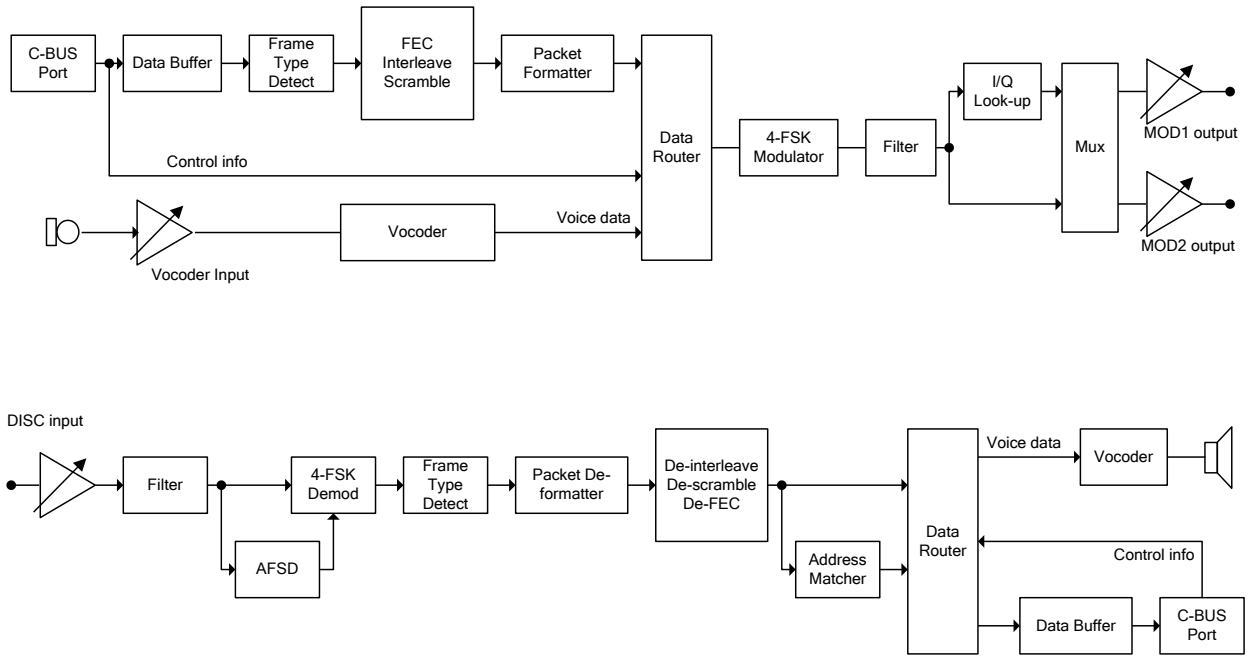


Figure 10 Internal Data Processing Blocks

6.3 Frame Sync Detection and Demodulation

The analogue signal from the limiter/discriminator of the external RF section should be applied to one of the CMX8341 inputs (normally the DISC input) where it can be adjusted to the correct level either by selection of the feedback resistor or using the CMX8341 Input Gain settings. The signal is filtered using a Root-Raised Cosine filter and Inverse Rx Sinc filter matching the filters applied in the transmitter, then passed to the AFSD (Automated Frame Sync Detector) block which extracts symbol and frame synchronisation. During this process the 4FSK demodulator and the following data-processing sections are dormant to minimise power consumption. When frame synchronisation has been achieved the AFSD section is powered down, and timing and symbol-level information is passed to the 4FSK demodulator which starts decoding the subsequent data bits. The CMX8341 can detect the end of a call by scanning the received control channel fields and will automatically disable the demodulator and restart frame sync search when required without host intervention.

A dPMR call begins with a 72-bit (or longer) preamble sequence followed by an 80ms Header Frame, which contains a 48-bit frame sync (FS1 or FS4). Subsequent payload frames contain either a 24-bit frame sync (FS2) or a 24-bit Colour Code. The CMX8341 can scan for all dPMR frame syncs concurrently. It uses FS1 to detect the start of a transmission and this is reported to the host by setting the FS1 Detect bit in the IRQ Status register. It can also optionally use FS2 to perform a “late entry” into an existing call, reported by setting the FS2 Detect bit. The short length of FS2 gives a higher probability of false detections, so by default the CMX8341 will only generate an FS2 Detect if two successive FS2 frame syncs are detected at the correct frame spacing in the received signal.

The frame syncs and Preamble defined in TS 102 490 are always used. When frame synchronisation has been achieved and the 4FSK demodulator is enabled, frame sync detection is switched off and any subsequent frame sync sequences embedded in the received data are not reported to the host.

Table 3 dPMR Frame Format - Call set-up, no ACK

Bit no.		24	48	72	96	120	144	168	192	216	240	264	288	312	336	360	384
		press PTT															
Header	Tx	Preamble			FS1		Header Info 0					CC	Header Info 1				
Frame 1	Tx	FS2	CCH			Payload			Payload			Payload			Payload		
Frame 2	Tx	CC	CCH			Payload			Payload			Payload			Payload		
Frame 3	Tx	FS2	CCH			Payload			Payload			Payload			Payload		
Frame 4	Tx	CC	CCH			Payload			Payload			Payload			Payload		
Frame 1	Tx	FS2	CCH			Payload			Payload			Payload			Payload		
Frame 2	Tx	CC	CCH			Payload			Payload			Payload			Payload		
Frame 3	Tx	FS2	CCH			Payload			Payload			Payload			Payload		
Frame 4	Tx	CC	CCH			Payload			Payload			Payload			Payload		
	Tx	Repeat frames 1 to 4 until PTT released….															
End	Tx	FS3	End Flag														

Table 4 dPMR Frame Format - Call set-up with ACK

Bit no.		24	48	72	96	120	144	168	192	216	240	264	288	312	336	360	384
		press PTT															
Header	Tx	Preamble			FS1		Header Info 0					CC	Header Info 1				
End	Tx	FS3	End Flag														
Ack	Rx	Preamble			FS1		Header Info 0					CC	Header Info 1				
Header	Tx	Preamble			FS1		Header Info 0					CC	Header Info 1				
Frame 1	Tx	FS2	CCH			Payload			Payload			Payload			Payload		
Frame 2	Tx	CC	CCH			Payload			Payload			Payload			Payload		
Frame 3	Tx	FS2	CCH			Payload			Payload			Payload			Payload		
Frame 4	Tx	CC	CCH			Payload			Payload			Payload			Payload		
Frame 1	Tx	FS2	CCH			Payload			Payload			Payload			Payload		
Frame 2	Tx	CC	CCH			Payload			Payload			Payload			Payload		
Frame 3	Tx	FS2	CCH			Payload			Payload			Payload			Payload		
Frame 4	Tx	CC	CCH			Payload			Payload			Payload			Payload		
	Tx	Repeat frames 1 to 4 until PTT released….															
End	Tx	FS3	End Flag														

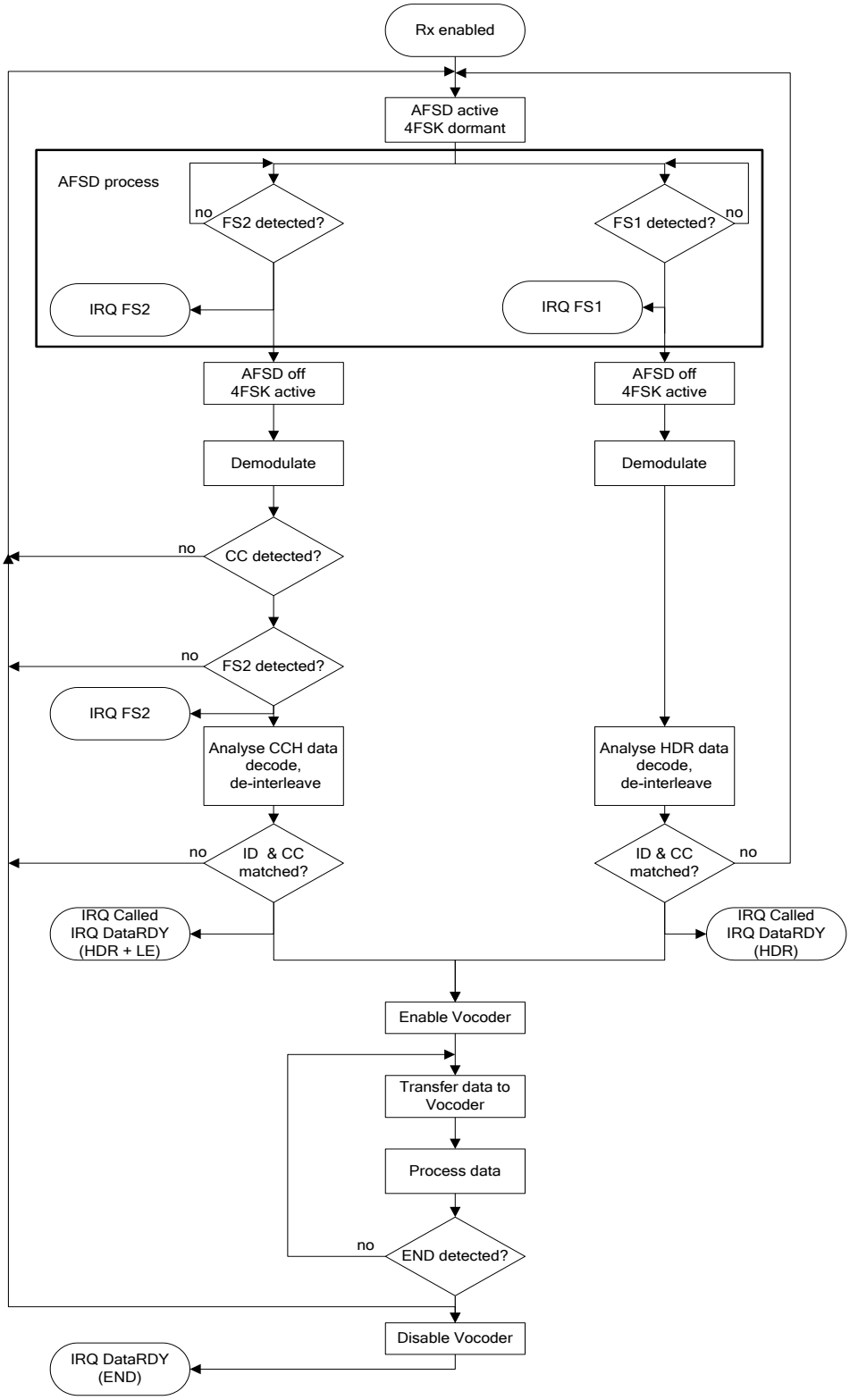


Figure 11 FS Detection

6.4 FEC and Coding

The CMX8341 implements all CRCs, Hamming codes, interleaving and scrambling required by the dPMR standard. CRC failures in control channel fields and coded data blocks are indicated to the host by issuing an “Event” IRQ with a corresponding error code in the Modem Status register, $C9. This relieves the host of a substantial processing load and has the added advantage of reducing the complexity and timing constraints of interfacing between the host and the CMX8341.

The dPMR Header Frame format contains duplicate copies of all control channel fields (in the HI0 and HI1 Header Information blocks) but only one decoded copy of each field will be presented back to the host. On receiving a Header Frame, the CMX8341 decodes both HI blocks, checks CRCs and can accept the call if either block is valid (the other HI block is discarded).

6.5 Voice Coding

The CMX8341 contains a RALCWI vocoder. The CMX8341 uses the Serial Memory Interface port (shared with the boot serial memory) to issue control commands and transfer voice payload data directly to the Vocoder section.

Voice data transferred to the Vocoder section in Rx mode always uses soft decision (4-bit log-likelihood ratio) format. This option is also available for voice payload data routed to the host (Tx mode), although it increases the required data transfer rate over C-BUS by a factor of four.

6.6 Radio Performance Requirements

The CMX8341 demodulator is designed to process a 4FSK signal from a limiter/discriminator source. For optimum performance the signal should not be significantly degraded by filters that are excessively narrow and/or cause significant group delay distortion. Care should be taken in interfacing the device to the radio circuits to maintain the frequency and phase response (both low and high end), in order to achieve optimum performance. Test modes are provided to assist in both the initial design and production set-up procedures.

Further information and application notes can be found at http://www.cmlmicro.com .

6.7 Tone Generator

This allows the user to generate audio tones in the range 300Hz to 3kHz. It will default to 1kHz. A separate level control is provided. C-BUS register $C3 is available for setting the tone frequency (shared with other functions).

7 Analogue PMR Description

7.1 External Sub-Audio Processing

An external Sub-Audio processing path is available for the host to generate or detect sub-audio tones. In Tx, sub-audio tones applied to the ALT input are filtered and then summed with the in-band signal and presented to the MOD1 and MOD2 outputs. In Rx, the sub-audio tones are separated by filters from the received signal applied to the DISC input. The sub-audio signal is then routed to the Auxiliary DAC4 output. The filter used in the path can be set by the Programming register, either a 260Hz Chebyshev suitable for CTCSS or a 150Hz 4-pole Bessel for DCS.

7.2 Internal CTCSS and DCS Generation and Detection

An internal generator/detector is available for the 51 CTCSS tones shown in Table 6 and the 83 DCS codes shown in Table 5. Squelch-tail elimination is provided by inverting the MOD outputs in CTCSS mode or a 134Hz “turn-off tone” in DCS mode. The tone/code to be generated is set by the value in the AuxData/Sub-Audio write register ($C2) in Tx mode and read from the AuxData/Sub-Audio read register ($CC) in Rx mode (see section 10.1.30). The use of the internal generator/detector is determined by Program Block P2.0 b5 and b4 (see section 10.2.3).

7.3 Voice Processing:

A set of Audio Processing blocks are available for use in Analogue mode:

- 300Hz HPF
- 12.5kHz channel filter or 25kHz channel filter
- Hard Limiter with anti-splatter filter
- Compandor
- Scrambler
- Voice AGC
- Level adjust
- In-band audio generator/s in both Rx and Tx paths

The 12.5kHz channel filter will be selected by default, the 25kHz filter can be enabled by setting P2.0:b0.

Note that in analogue mode, the digital mode output of the Vocoder section should be isolated using an external analogue switch (see Figure 4).

300Hz HPF

This is designed to reject signals below 300Hz from the voice path so that sub-audio signalling can be inserted (in Tx) or removed (in Rx) as appropriate. It should be enabled whenever sub-audio signalling is required.

12.5kHz/25kHz Channel Filters

These are designed to meet the requirements of ETSI EN 300 296 for Voice signal processing and feature an upper roll-off at 2.55 and 3.0kHz respectively.

Hard Limiter

This is provided to limit the peak deviation of the radio signal to meet the requirements of ETSI EN 300 296. An anti-splatter filter is included to reduce the effects of any harmonic signals generated in the process. The limiter threshold can be set using P2.3.

Compander

A syllabic compressor/expander is provided, similar to that used in the 7031/7041-FI-1.x to increase the dynamic range of the Voice signal. The unity gain points for Tx and Rx can be set independently using P2.9 and P2.10.

Scrambler

A frequency inversion scrambler is provided to enable a basic level of privacy. The default inversion frequency is 3300Hz, but can be programmed using \$CD:1001_b, however some loss of signal at the band edges may occur due to the channel filter roll-off.

Voice AGC

An automatic gain control system is provided in the voice path, utilising the programmable gain settings of the Input 1 amplifier. When used in conjunction with the hard limiter function, this can compensate for large variations in the MIC input signal without introducing significant distortion. The AGC threshold is programmable using P21. whilst the maximum gain setting and the decay time can be set using P2.2. When this feature is enabled, the host should not attempt to directly control the Input 1 gain setting.

Level Adjust

Independent level adjustments are provided using \$C3 register for the voice, in-band and sub-audio signals, see section 8.12 for further details.

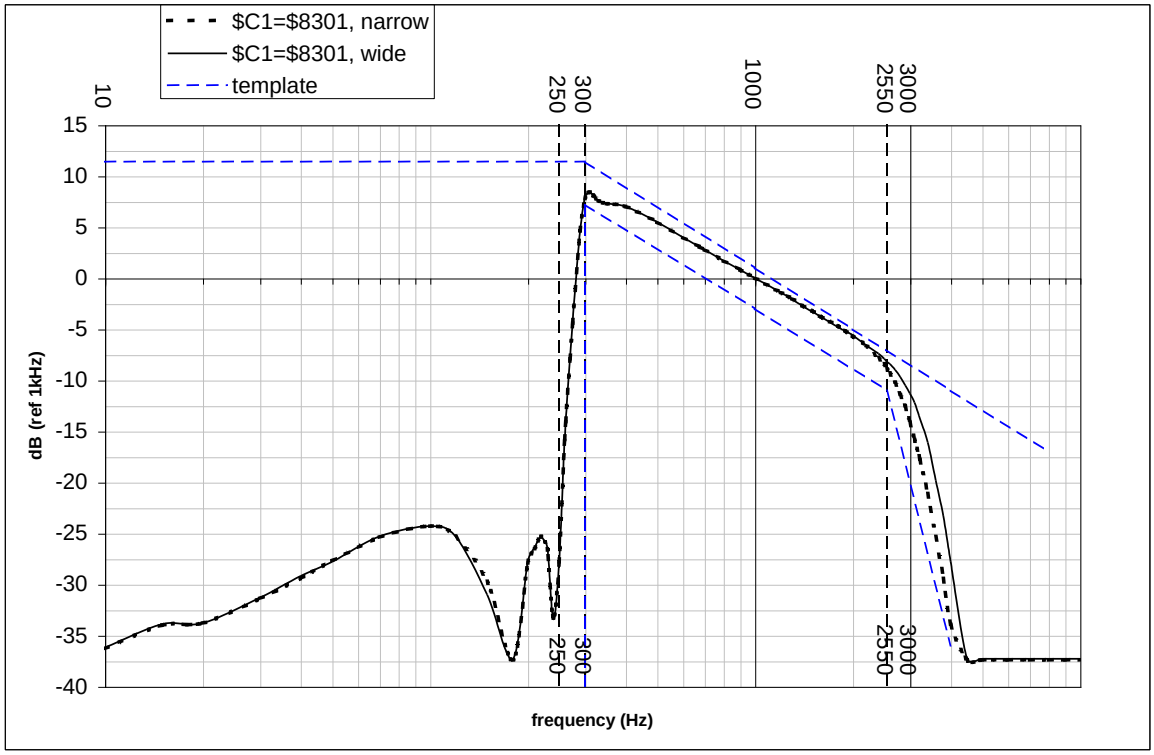


Figure 12 Rx Audio Response

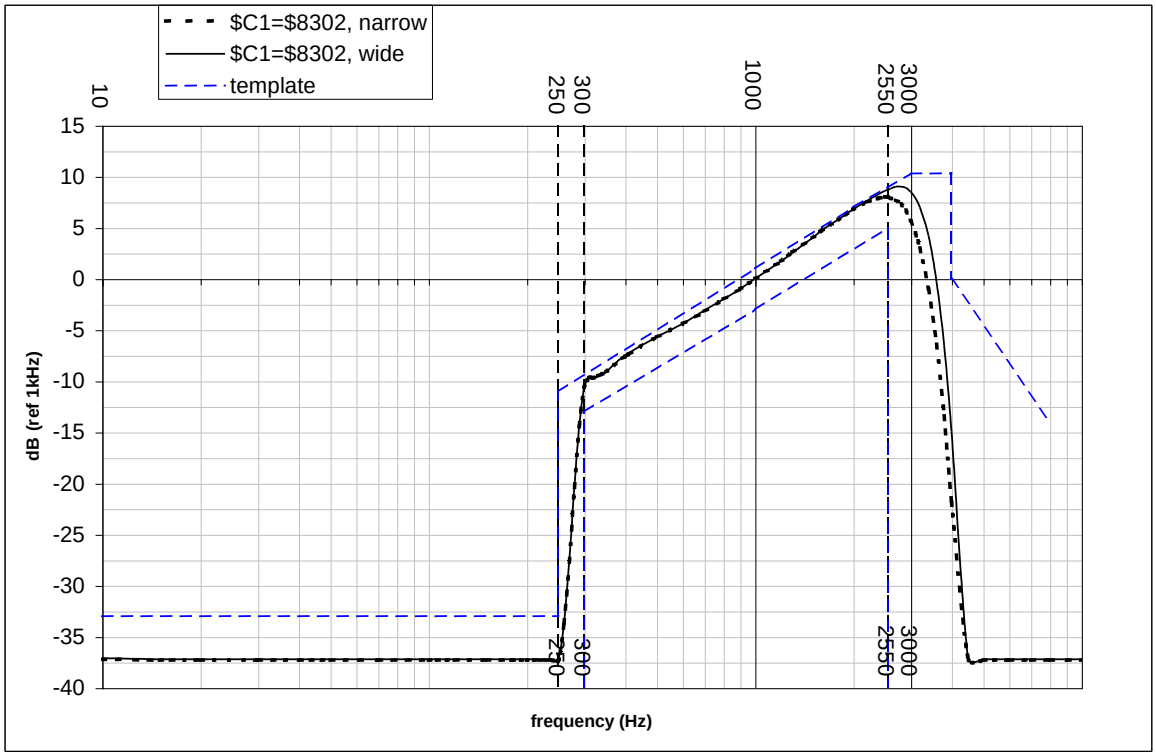


Figure 13 Tx Audio Response

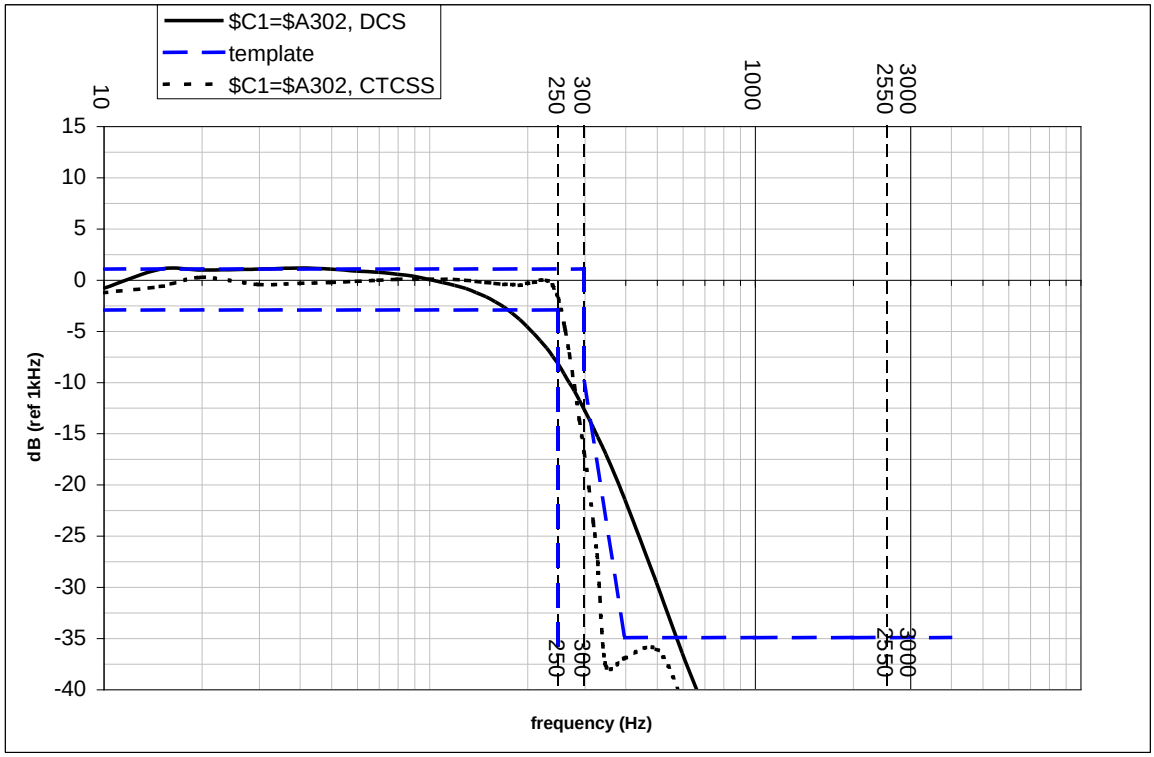


Figure 14 CTCSS and DCS filters

Table 5 DCS codes and values

	Register Value			
DCS Code	**true**		**inverted**	
	Decimal	Hex	Decimal	Hex
no code	0	00	100	64
23	1	01	101	65
25	2	02	102	66
26	3	03	103	67
31	4	04	104	68
32	5	05	105	69
43	6	06	106	6A
47	7	07	107	6B
51	8	08	108	6C
54	9	09	109	6D
65	10	0A	110	6E
71	11	0B	111	6F
72	12	0C	112	70
73	13	0D	113	71
74	14	0E	114	72
114	15	0F	115	73
115	16	10	116	74
116	17	11	117	75
125	18	12	118	76

	Register Value			
DCS Code	**true**		**inverted**	
	Decimal	Hex	Decimal	Hex
311	42	2A	142	8E
315	43	2B	143	8F
331	44	2C	144	90
343	45	2D	145	91
346	46	2E	146	92
351	47	2F	147	93
364	48	30	148	94
365	49	31	149	95
371	50	32	150	96
411	51	33	151	97
412	52	34	152	98
413	53	35	153	99
423	54	36	154	9A
431	55	37	155	9B
432	56	38	156	9C
445	57	39	157	9D
464	58	3A	158	9E
465	59	3B	159	9F
466	60	3C	160	A0

	Register Value			
DCS Code	**true**		**inverted**	
	Decimal	Hex	Decimal	Hex
131	19	13	119	77
132	20	14	120	78
134	21	15	121	79
143	22	16	122	7A
152	23	17	123	7B
155	24	18	124	7C
156	25	19	125	7D
162	26	1A	126	7E
165	27	1B	127	7F
172	28	1C	128	80
174	29	1D	129	81
205	30	1E	130	82
223	31	1F	131	83
226	32	20	132	84
243	33	21	133	85
244	34	22	134	86
245	35	23	135	87
251	36	24	136	88
261	37	25	137	89
263	38	26	138	8A
265	39	27	139	8B
271	40	28	140	8C
306	41	29	141	8D

	Register Value			
DCS Code	**true**		**inverted**	
	Decimal	Hex	Decimal	Hex
503	61	3D	161	A1
506	62	3E	162	A2
516	63	3F	163	A3
532	64	40	164	A4
546	65	41	165	A5
565	66	42	166	A6
606	67	43	167	A7
612	68	44	168	A8
624	69	45	169	A9
627	70	46	170	AA
631	71	47	171	AB
632	72	48	172	AC
654	73	49	173	AD
662	74	4A	174	AE
664	75	4B	175	AF
703	76	4C	176	B0
712	77	4D	177	B1
723	78	4E	178	B2
731	79	4F	179	B3
732	80	50	180	B4
734	81	51	181	B5
743	82	52	182	B6
754	83	53	183	B7
user defined	84	54	184	B8

Table 6 CTCSS codes and values

Register Value		CTCSS tone
Decimal	Hex	Frequency
200	C8	no tone
201	C9	67.0
202	CA	71.9
203	CB	74.4
204	CC	77.0
205	CD	79.7
206	CE	82.5
207	CF	85.4
208	D0	88.5
209	D1	91.5
210	D2	94.8
211	D3	97.4
212	D4	100.0
213	D5	103.5
214	D6	107.2
215	D7	110.9
216	D8	114.8
217	D9	118.8
218	DA	123.0
219	DB	127.3
220	DC	131.8
221	DD	136.5
222	DE	141.3
223	DF	146.2
224	E0	151.4
225	E1	156.7
226	E2	162.2
227	E3	167.9

Register Value		CTCSS tone
Decimal	Hex	Frequency
228	E4	173.8
229	E5	179.9
230	E6	186.2
231	E7	192.8
232	E8	203.5
233	E9	210.7
234	EA	218.1
235	EB	225.7
236	EC	233.6
237	ED	241.8
238	EE	250.3
239	EF	69.3
240	F0	62.5
241	F1	159.8
242	F2	165.5
243	F3	171.3
244	F4	177.3
245	F5	183.5
246	F6	189.9
247	F7	196.6
248	F8	199.5
249	F9	206.5
250	FA	229.1
251	FB	254.1
252	FC	user defined
253	FD	---
254	FE	DCS turn-off
255	FF	invalid tone

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8 Detailed Descriptions

8.1 Reference Frequency

This device is suitable for use with a 19.2MHz external frequency source only.

8.2 Host Interface

A serial data interface (C-BUS) is used for command, status and data transfers between the CMX8341 and the host µC; this interface is compatible with microwire and SPI. Interrupt signals notify the host µC when a change in status has occurred and the µC should read the status register across the C-BUS and respond accordingly. Interrupts only occur if the appropriate mask bit has been set. See section 8.4.2.

The CMX8341 will monitor the state of the C-BUS registers that the host has written-to every 250µs (the C-BUS latency period) hence it is not advisable for the host to make successive writes to the same C-BUS register within this period.

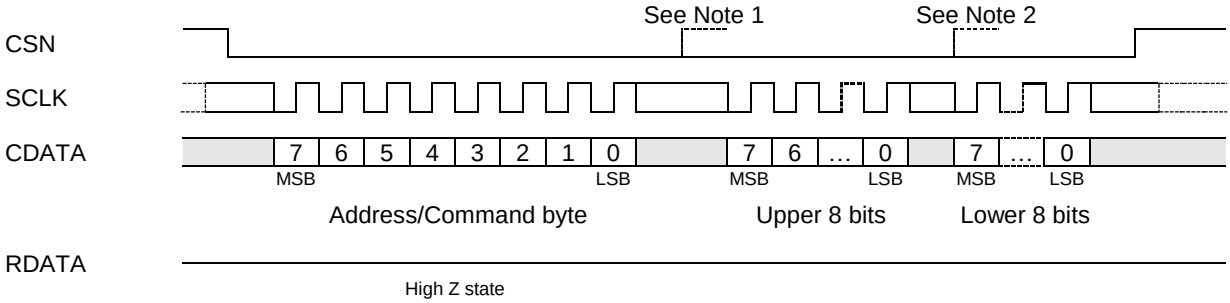
8.2.1 C-BUS Operation

This block provides for the transfer of data and control or status information between the CMX8341's internal registers and the host µC over the C-BUS serial interface. Each transaction consists of a single address byte sent from the µC which may be followed by one or more data byte(s) sent from the µC to be written into one of the CMX8341's write only registers, or one or more data byte(s) read out from one of the CMX8341's read only registers, as shown in Figure 15.

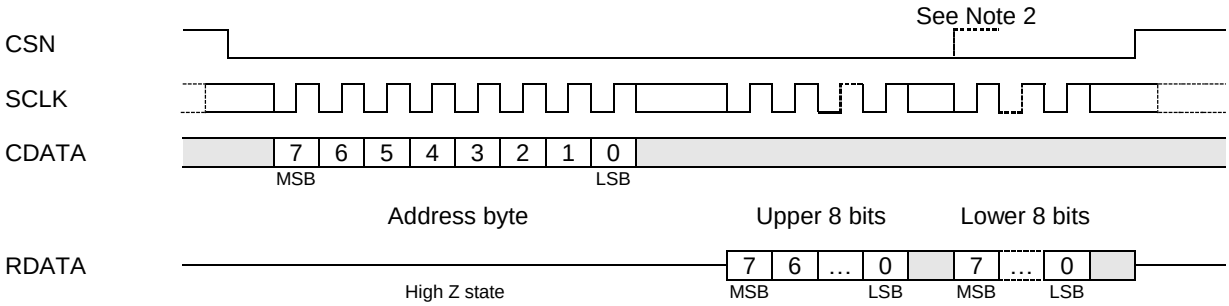
Data sent from the µC on the CDATA (Command Data) line is clocked into the CMX8341 on the rising edge of the SCLK (Serial Clock) input. RDATA (Reply Data) sent from the CMX8341 to the µC is valid when the SCLK is high. The CSN line must be held low during a data transfer and kept high between transfers. The C-BUS interface is compatible with most common µC serial interfaces.

The number of data bytes following an address byte is dependent on the value of the Address byte. The most significant bit of the address or data is sent first. For detailed timings see section 9.2.1. Note that, due to internal timing constraints, there may be a delay of up to 250µs between the end of a C-BUS write operation and the device reading the data from its internal register.

C-BUS Write:



C-BUS Read:



Data value unimportant

Repeated cycles

Either logic level valid (and may change)

Either logic level valid (but must not change from low to high)

Figure 15 C-BUS Transactions

Notes:

1. For Command byte transfers only the first 8 bits are transferred ($01 = Reset).
2. For single byte data transfers only the first 8 bits of the data are transferred.
3. The CDATA and RDATA lines are never active at the same time. The Address byte determines the data direction for each C-BUS transfer.
4. The SCLK input can be high or low at the start and end of each C-BUS transaction.
5. The gaps shown between each byte on the CDATA and RDATA lines in the above diagram are optional, the host may insert gaps or concatenate the data as required.

8.3 Function Image™ Loading

The Function Image™ (FI), which defines the operational capabilities of the device, may be obtained from the CML Technical Portal, following registration. This is in the form of a 'C' header file which can be included into the host controller software or programmed into an external serial memory. The maximum possible size of Function Image™ is 46 kbytes, although a typical FI will be less than this. Note that the BOOTEN pins are only read at power-on or following a C-BUS General Reset and must remain stable throughout the FI loading process. Once the FI load has completed, the BOOTEN pins are ignored by the CMX8341 until the next power-up or C-BUS General Reset.

The BOOTEN pins are both fitted with internal low current pull-down devices.

For C-BUS load operation, both pins should be pulled high by connecting them to DV_{DD} either directly or via a 220kΩ resistor (see Figure 16).

For serial memory load, only BOOTEN1 needs to be pulled high in a similar manner, however, if it is required to program the serial memory in-situ from the host, either a jumper to DV_{DD} or a link to a host I/O pin should be provided to pull BOOTEN2 high when required (see Figure 17). The Serial Memory Interface also controls the Vocoder section using a separate chip select (SSOUT) pin. During boot operations the SSOUT will be disabled. Once the boot operation has completed, the serial memory chip select (EPCSN) will be disabled and the SSOUT will become operational.

Once the FI has been loaded, the CMX8341 performs these actions:

(1) The product identification code ($8341) is reported in C-BUS register $C5

(2) The FI version code is reported in C-BUS register $C9

(3) The two 32-bit FI checksums are reported in C-BUS register pairs $A9, $AA and $B8, $B9

(4) The device waits for the host to load the 32-bit Device Activation Code to C-BUS register $C8

(5) Once activated, the device initialises fully, enters idle mode and becomes ready for use, and the PRG flag (bit 0 of the Status register) will be set.

The checksums should be verified against the published values to ensure that the FI has loaded correctly. Once the FI has been activated, the checksum, product identification and version code registers are cleared and these values are no longer available. If an invalid activation code is loaded, the device will report the value $DEAD in register $A9 and must be power cycled before an attempt is made to re-load the FI and re-activate.

Both the Device Activation Code and the checksum values are available from the CML Technical Portal.

Table 7 BOOTEN Pin States

	BOOTEN2	BOOTEN1
C-BUS Host load	1	1
reserved	1	0
Serial memory load	0	1
No FI load	0	0

Note: In the rare event that a General Reset needs to be issued without the requirement to re-load the FI, the BOOTEN pins must both be cleared to '0' before the command is issued. The Checksum values will be reported and the Device Activation code will need to be sent in a similar manner as that shown in Figure 17. There will not be any FI loading delay. This assumes that a valid FI has been previously loaded and that DV_{DD} has been maintained throughout the reset to preserve the data.

8.3.1 FI Loading from Host Controller

The FI can be included into the host controller software build and downloaded into the CMX8341 at power-up over the C-BUS interface. The BOOTEN pins must be set to the C-BUS load configuration, the CMX8341 powered up and placed into Program Mode, the data can then be sent directly over the C-BUS to the CMX8341.

Each time the Programming register, $C8, is written, it is necessary to wait for the PRG flag (IRQ Status register ($C6) b0) to go high before another write to $C8. The PRG flag going high confirms the write to the Programming register has been accepted. The PRG flag state can be determined by polling the IRQ Status register or by unmasking the interrupt (Interrupt Mask register, $CE, b0).

The download time is limited by the clock frequency of the C-BUS, with a 5MHz SCLK, it should take less than 500ms to complete.

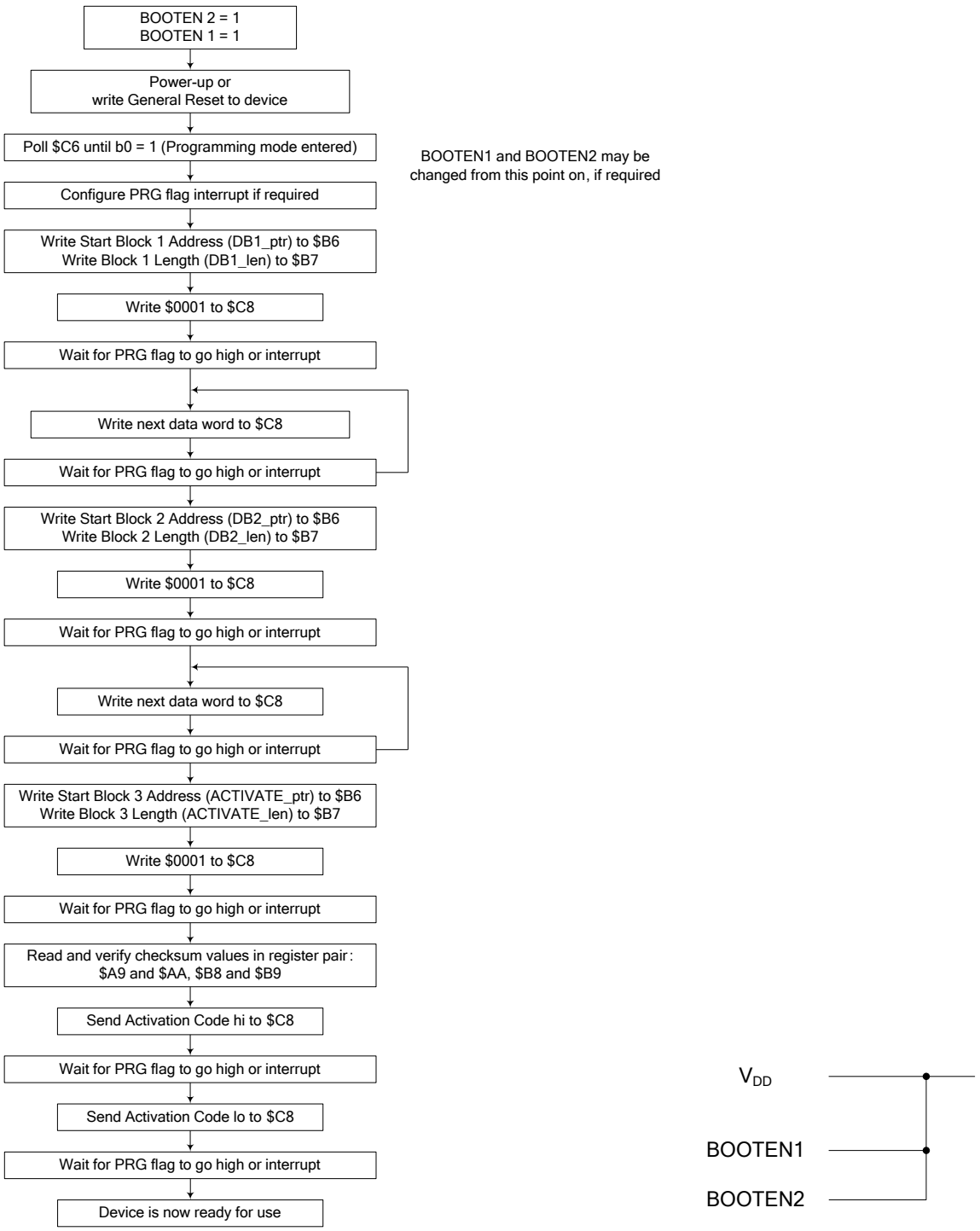


Figure 16 FI Loading from Host

8.3.2 FI Loading from an external Serial Memory

The FI must be converted into a suitable format for a serial memory programmer (normally Intel Hex) and loaded into the external serial memory either by the host or an external programmer. The CMX8341 needs to have the BOOTEN pins set to serial memory load and then on power-on, or following a C-BUS General Reset, the CMX8341 will automatically load the data from the serial memory without intervention from the host controller.

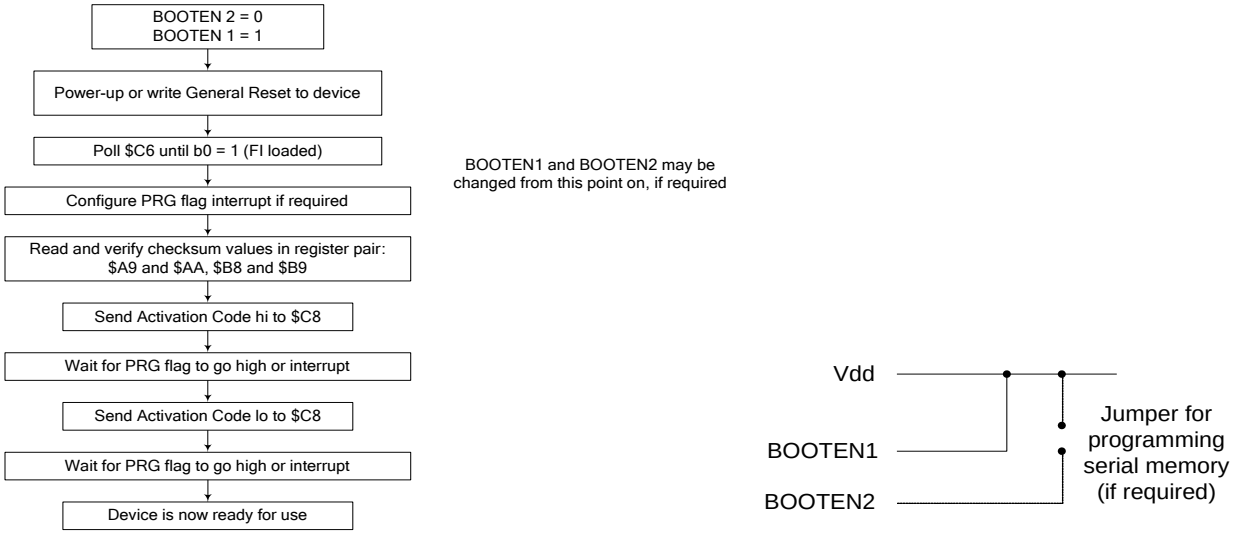


Figure 17 FI Loading from an external Serial Memory

The CMX8341 has been designed to function with either an Atmel AT25HP512 serial EEPROM or the AT25F512 Serial Flash device[1], however other manufacturers' parts may also be suitable. The time taken to load the FI is dependent on the clock frequency: with a 19.2MHz reference clock it should load in less than 1/3rd second.

[1] Note that these two devices have slightly different addressing schemes. The CMX8341 is compatible with both schemes.

8.4 Device Control

The CMX8341 can be set into the relevant mode to suit its environment. These modes are described in the following sections and are programmed over the C-BUS: either directly to operational registers or, for parameters that are not likely to change during operation, via the Programming register ($C8).

For basic operation:

(1) Enable the relevant hardware sections via the Power Down Control register

(2) Set the appropriate mode registers to the desired state

(3) Select the required Signal Routing and Gain

(4) Use the Mode Control register to place the device into Rx or Tx mode.

To conserve power when the device is not actively processing a signal, place the device into Idle mode. This will also command the Vocoder section to enter powersaving mode as well. Additional powersaving can be achieved by disabling any unused hardware blocks, however, care must be taken not to disturb any sections that are automatically controlled. Note that the BIAS block must be enabled to allow any of the Input or output blocks to function.

See:

- Power Down Control - $C0 write
- Modem Control - $C1 write
- Modem Configuration - $C7 write.

8.4.1 General Notes

In normal operation, the most significant registers, in addition to the TxData and RxData blocks, are:

- Modem Control - $C1 write
- IRQ Status - $C6 read
- Analogue Output Gain - $B0 write
- Input Gain and Signal Routing - $B1 write
- AuxData/Sub-audio Write - $C2 write
- Analogue Control - $C3 write

Setting the Mode register to either Rx or Tx will automatically increase the internal clock speed to its operational speed and bring the Vocoder section out of its powersave mode, whilst setting the Mode register to Idle will automatically return the internal clock to a lower (powersaving) speed. To access the Program Blocks (through the Programming register, $C8) the device MUST be in Idle mode.

Under normal circumstances the CMX8341 manages the Main Clock Control automatically, using the default values loaded in Program Block 3.

8.4.2 Interrupt Operation

The CMX8341 will issue an interrupt on the IRQN line when the IRQ bit (bit 15) of the IRQ Status register and the IRQ Mask bit (bit 15) are both set to 1. The IRQ bit is set when the state of the interrupt flag bits in the IRQ Status register change from a 0 to 1 and the corresponding mask bit(s) in the Interrupt Mask register is(are) set. Enabling an interrupt by setting a mask bit ($0 \rightarrow 1$) after the corresponding IRQ Status register bit has already been set to 1 will also cause the IRQ bit to be set.

All interrupt flag bits in the IRQ Status register, except the PRG flag (bit 0), are cleared and the interrupt request is cleared following the command/address phase of a C-BUS read of the IRQ Status register. The PRG flag bit is set to 1 only when it is permissible to write a new word to the Programming register.

See:

- IRQ Status - $C6 read
- Interrupt Mask - $CE write

8.4.3 Signal Routing

The CMX8341 offers a flexible routing architecture, with three signal inputs, a choice of two modulator configurations (to suit 2-point modulation or I/Q schemes) and a single audio output.

See:

- Input Gain and Signal Routing - $B1 write
- Modem Control - $C1 write
- Modem Configuration - $C7 write

The analogue gain/attenuation of each input and output can be set individually. In dPMR mode, the Mic and Speaker gains are set by the Vocoder section, which is controlled through the Analogue Control - $C3 write register. In Analogue mode, the Mic and Speaker gains are set by the Input Gain and Output Gain registers ($B1 and $B0).

See:

- Analogue Output Gain - $B0 write (Tx MOD1 and 2)
- Input Gain and Signal Routing - $B1 write (Rx DISC input, Tx MOD1 and 2)
- Analogue Control - $C3 write (Vocoder section Mic. and Speaker)

Input 1 should be routed to either of the three input sources (ALT, DISC or MIC), which should be connected as shown in Figure 5 and Figure 6. The internal signals Output 1 and Output 2 are used to provide 2-point signals and should be routed to the MOD1 and MOD2 pins, as required.

In dPMR mode the microphone and speaker paths are automatically re-routed to the Vocoder section, when appropriate. This routing is controlled by the data field in the Header Block, which indicates whether the payload is speech data, and the Vocoder section Disable bit in the Modem Control register, $C1.

8.4.4 Modem Control

The CMX8341 operates in one of these operational modes:

- Idle
- Rx
- Tx
- Pass-through, for direct Vocoder access.

At power-on or following a Reset, the device will automatically enter Idle mode, which allows maximum powersaving whilst still retaining the capability of monitoring the AuxADC inputs (if enabled). It is only possible to write to the Programming register whilst in Idle mode. By default, the CMX8341 selects Digital (dPMR Modem) mode, unless any of the Voice, Tone or Sub-Audio bits (b15-13) of the Modem Control register have been set to 1, in which case Analogue mode is selected.

See:

- Modem Control - $C1 write

GPIO1 and GPIO2 pins (allocated to RXENA and TXENA functions by the FI) reflect bits 0 and 1 of the Modem Control register, as shown in Figure 7. These can be used to drive external hardware without the host having to intervene. There are two additional GPIO pins (GPIOA and GPIOB) that are programmable under host control.

Table 8 Modem Mode Selection

Modem Control ($C1) b3-0	Modem Mode	GPIO2 - TXENA	GPIO1 - RXENA
0000	Idle – Low Power Mode	1	1
0001	Rx	1	0
0010	Tx	0	1
0011	*reserved*	x	x
0100	Vocoder section – Pass-through	1	1
0101	*reserved*	x	x
0110	*reserved*	x	x
0111	*reserved*	x	x
1xxx	*reserved*	x	x

The Pass-through mode is used to control and monitor the Vocoder section directly. This cannot be accessed if the CMX8341 is in Rx or Tx modes. This mode will transfer data to/from the TxData0/RxData0 register to the Vocoder section C-BUS register address specified in the Programming register ($C8). See section 8.5.12. The Modem Control bits are ignored in this mode.

Table 9 Modem Control Selection

4FSK Modem Control ($C1) b7-4	Rx	Tx
0000	Rx Idle	Tx Idle
0001	Rx 4FSK Formatted	Tx 4FSK Formatted
0010	Rx 4FSK Raw	*reserved*
0011	Rx 4FSK EYE	Tx 4FSK PRBS
0100	Rx Pass-through	Tx 4FSK Preamble
0101	*reserved*	Tx 4FSK Mod Set-up
0110	Sync	Test
0111	Reset/Abort	Reset/Abort
1xxx	*reserved*	*reserved*

The Modem Mode bits and the Modem Control bits should be set together in the same C-BUS write.

Analogue mode is selected by setting any of bits 15-13. For digital modem operation, b15-13 MUST be cleared to '0'.

In Tx mode, the CMX8341 operates in dPMR Formatted mode. The first block of control channel or payload data should be loaded into the C-BUS TxData registers before executing the mode change. A "DataReady" IRQ will be issued when the registers have been read by the CMX8341 and the host can then supply further blocks of payload data. When all payload data has been transmitted, the CMX8341 will issue a "TxDone" IRQ and the host can then reset the Mode bits to either Rx or Idle as required.

In Rx mode, the received signal should be routed through Input1 (DISC). In dPMR Formatted mode, the CMX8341 will first search for frame synchronisation and, when this has been achieved, the following data is demodulated and supplied to the host through the RxData registers. A "DataReady" IRQ indicates when each new block becomes available. In dPMR Formatted mode, the modem can detect the end of a call and restart frame sync search automatically.

8.5 dPMR Formatted Operation

The CMX8341 performs all frame building/splitting and FEC coding/decoding, which relieves the host controller of a significant processing load. During voice calls the CMX8341 can automatically enable and

control the Vocoder section, and transfer voice payload data from/to it without host intervention. In Rx mode, the CMX8341 monitors address fields in incoming transmissions and only accepts calls if the programmed address requirements are satisfied. This allows the host to remain in a power-down or "sleep" state until it is really necessary to wake up, extending the battery life of the final product design.

8.5.1 Tx Mode

In Tx mode operation ($C1, Modem Control = $0012), the preamble and frame sync are transmitted automatically and data from the TxData Block is then formatted and assembled for transmission, until the mode is changed to Rx, Pass-through or Idle. The first block of data should be loaded into the TxData registers before executing the Modem Mode change to Tx. Data is transmitted msb (most significant bit) first.

The host should write the initial data to the C-BUS TxData registers and then set the Modem Mode to TxFormat and the Mode bits to Tx. As soon as the data block has been read from the C-BUS TxData registers, the DataRDY IRQ will be asserted and the next block of data may be loaded.

The call should be terminated by the host sending an END frame to the device. After the last data bit has left the modulator a "TxDone" IRQ will be issued. At this point it is now safe for the host to change the Modem Control and Modem Mode to Idle ($C1, Modem Control = $0000) and turn the RF transmitter off.

If the Header frame loaded by the host indicates that a voice call is in progress, the device will automatically enable the Vocoder and route encoded Voice packets to the modulator in preference to any data provided by the host over C-BUS. When the host loads the END frame, the device will automatically disable the Vocoder.

8.5.2 Tx Mode (PRBS)

In PRBS mode Tx operation ($C1, Modem Control = $0032), the preamble and frame sync are transmitted automatically, followed by a PRBS pattern conforming to ITU-T O.153 (para 2.1) – giving a 511-bit repeating sequence.

8.5.3 Tx Mode Test

In Test mode ($C1 = $0062), simple test waveforms are generated (defined by the dPMR Association TWG). See section 10.1.20.

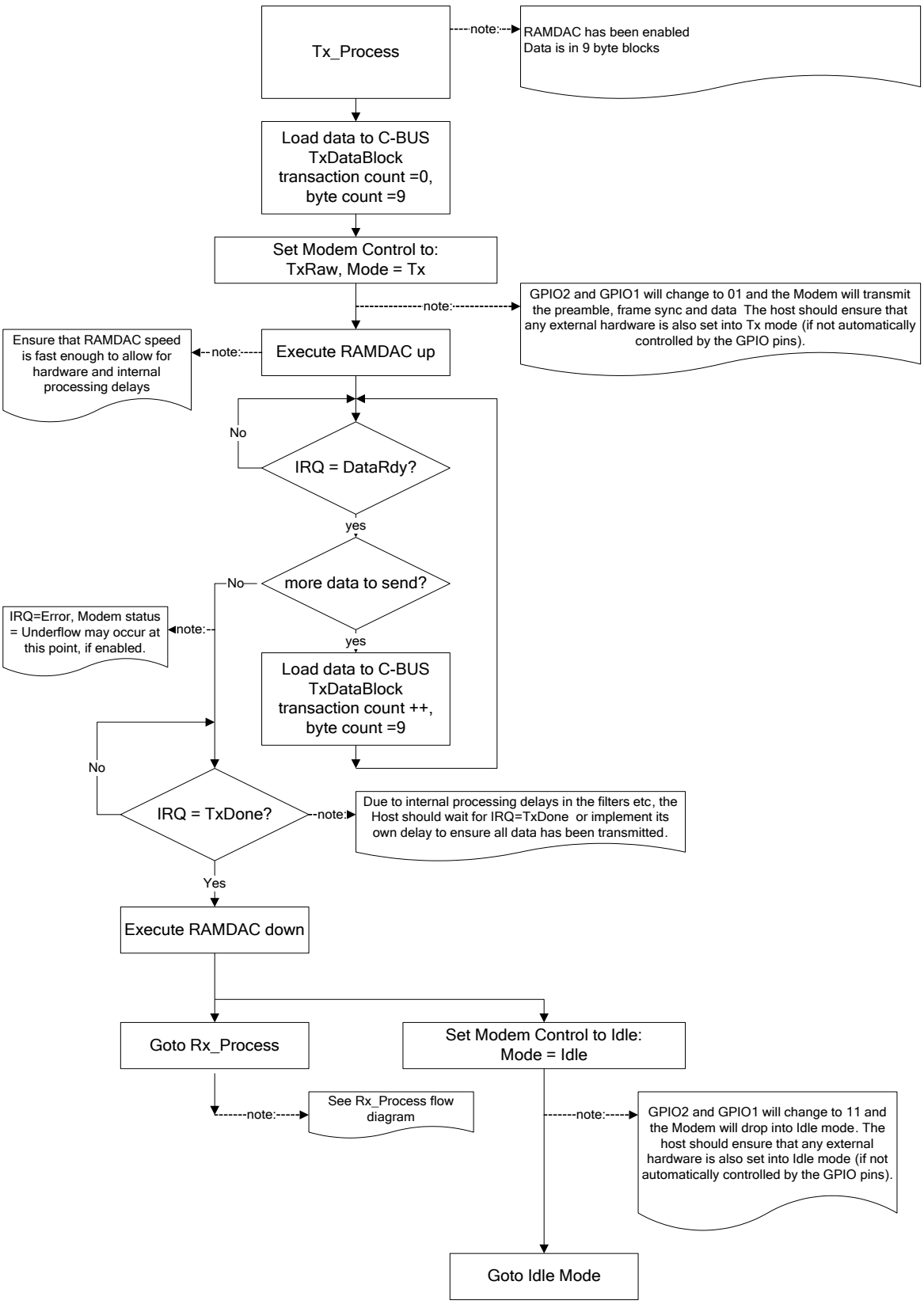


Figure 18 Tx Data Flow

8.5.4 Rx Mode

In Rx mode operation ($C1, Modem Control = $0011), the CMX8341 automatically starts searching for frame synchronisation. When a valid frame sync sequence is detected, an “FS1 Detect” or “FS2 Detect” IRQ is asserted and the data demodulator is enabled. All following payload data is loaded directly into the C-BUS RxData registers with a “DataReady” IRQ to indicate when each new block is available. This continues until the END frame is detected or the Mode is changed to Idle or Tx. The host MUST respond to each “DataReady” IRQ before the RxData registers are overwritten by subsequent payload data blocks.

If “soft” data mode has been selected, the payload data is encoded in 4-bit log-likelihood-ratio format. In this mode the host must be able to service the “DataReady” IRQs and RxData registers at four times the normal rate to avoid overflow.

Alternatively, additional power saving may be achieved by the host monitoring the “Called” IRQ instead, which will only be asserted when the ID match criteria are satisfied. If the recovered Header frame indicates that a Voice call is in progress, the device will automatically route the payload data to the Vocoder in preference to the host C-BUS.

8.5.5 Rx Mode dPMR

In Rx dPMR mode operation ($C1, Modem Control = $0011), the CMX8341 will automatically start searching for frame synchronisation. When a valid frame sync sequence is detected, an ‘FS detect’ IRQ is asserted and the data demodulator is enabled. If the burst is then accepted a ‘Called’ IRQ is asserted and the first Message Info or CCH Info block is loaded into the C-BUS RxData registers with a ‘Data Ready’ IRQ. If the control channel fields indicate that the burst is a voice call, received payload data will be sent to the vocoder for decoding. Otherwise payload data is loaded into the C-BUS RxData registers with a ‘Data Ready’ IRQ to indicate when each new block is available. If ‘soft’ data mode has been selected, the payload data is encoded in 4-bit log-likelihood-ratio format and the host must be able to service the ‘Data Ready’ IRQs and RxData registers at four times the normal rate to avoid overflow.

8.5.6 Rx Mode Raw

Rx Mode Raw is included to facilitate BER measurements. In this mode ($C1, Modem Control = $0021), once a valid frame sync has been detected, all following data received is loaded directly into the C-BUS RxData registers. This continues until the end of the burst (even if there is no valid signal at the input). On exiting Rx Mode Raw, there may be a DataRdy IRQ pending which should be cleared by the host. Note that Rx Mode Raw operation always requires the incoming data to be preceded with a valid Preamble and Frame Sync pattern in order to derive timing information for the demodulator. The device will update the C-BUS RxData registers with Rx payload data as it becomes available. The host MUST respond to the DataRDY IRQ before the RxData registers are over-written by subsequent data from the modem.

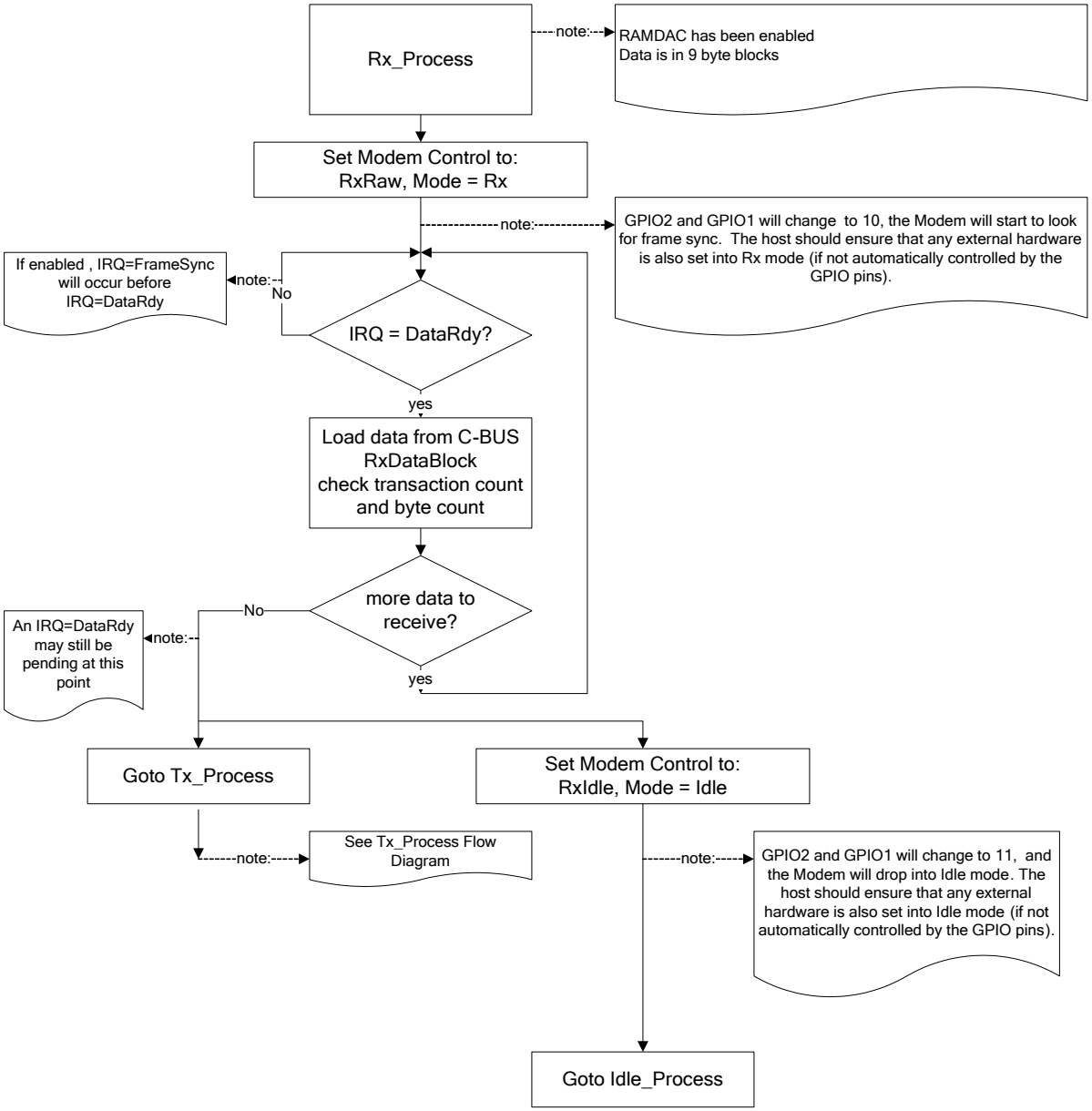


Figure 19 Rx Data Flow

8.5.7 Rx Mode Eye

In Rx 4FSK EYE mode ($C1 = $0031), the filtered received signal is output at the MOD1 pin as an “eye” diagram for test and alignment purposes. A trigger pulse is output at the MOD2 pin to allow viewing on a suitable oscilloscope. The trigger pulse is generated directly from the receiver clock source, not from the input signal.

8.5.8 Rx Mode Pass-through

Rx Pass-through mode ($C1 = $0041), similar to Rx 4FSK Eye mode, but without the RRC filter. The typical response is:

300Hz	-0.6dB
1kHz	0dB (reference)
2kHz	-0.7dB
2.5kHz	-1.4dB
3kHz	-2.4dB
4kHz	-4.9dB
6kHz	-12.2dB

8.5.9 Sync Mode

Sync mode ($C1 = $0061), enters continuous AFSD Synch search mode. Used for test/debug only.

8.5.10 Reset/Abort

From each mode, a Reset/Abort aborts the current state machine and drops into the corresponding (Rx or Tx) Idle mode. The only difference between this and going directly into the corresponding Idle mode is that all of the buffers and filters are flushed out first with Reset/Abort.

In Tx mode a number of test and set-up modes are provided to facilitate test and alignment.

- PRBS (Preamble and Synchronisation Word are automatically transmitted first)
- Continuous preamble: a repeating sequence of [+3 +3 -3 -3] symbols
- Modulation set-up: in two-point mode, a repeating sequence of eight +3 symbols followed by eight -3 symbols, and in I/Q mode a continuous sequence of +3 symbols.

8.5.11 Data Transfer

Payload data is transferred from/to the host using blocks of five Rx and five Tx 16-bit C-BUS registers, allowing up to 72 bits (9 bytes) of data to be transferred in sequence, see Table 10. The lowest 8 bits of the register block are reserved for a Byte Counter, Block ID and a Transaction Counter. The byte count indicates how many bytes in the data block are valid and avoids the need to perform a full five word C-BUS read/write if only a smaller block of data need to be transferred.

Table 10 C-BUS Data Registers

C-BUS Address	Function	C-BUS Address	Function
$B5	Tx data 0-7 and info	$B8	Rx data 0-7 and info
$B6	Tx data 8-23	$B9	Rx data 8-23
$B7	Tx data 24-39	$BA	Rx data 24-39
$CA	Tx data 40-55	$BB	Rx data 40-55
$CB	Tx data 56-71	$C5	Rx data 56-71

Bits 7 and 6 hold the Transaction Counter, which is incremented modulo 4 on every read/write of the Data Block to allow detection of data underflow and overflow conditions. In Tx mode the host must increment the counter on every write to the TxData block and, if the CMX8341 identifies that a block has been written out of sequence, the Event bit (C-BUS register $C6, b14) will be asserted and an IRQ raised, if enabled. The device detects that new data from the host is available by the change in the value of the Transaction Counter, therefore the host should ensure that all the data is available in the TxData block before updating this register (ie, it should be the last register the host writes to in any block transfer). In Rx mode, the CMX8341 will automatically increment the counter every time it writes to the RxData block. If the host

identifies that a block has been written out of sequence, then it is likely that a data overrun condition has occurred and some data has been lost.

8.5.12 Vocoder Section – Pass-through Mode

To allow the host to communicate directly with the Vocoder section for test and configuration purposes, a Pass-through mode is available which allows any Vocoder section C-BUS register to be read or written (as appropriate). This mode uses the Modem Control, TxData0, RxData0, IRQ Status and Program Blocks on the CMX8341.

To write to the Vocoder section:

- Set the CMX8341 to 'Pass-through' mode (Modem Control register, $C1=$0004)
- Wait for the PRG flag to be set ($C6 b0)
- Write the Vocoder section data value to the Txdata0 register ($B5)
- Write the Vocoder section C-BUS address to the Programming register ($C8) with b15=0 and b14=1
- Wait for the PRG flag to be set ($C6 b0).

To read from the Vocoder section:

- Set the CMX8341 to 'Pass-through' mode (Modem Control register, $C1=$0004)
- Wait for the PRG flag to be set ($C6 b0)
- Write the Vocoder section C-BUS address to the Programming register ($C8) with b15=1 and b14=1
- Wait for the PRG flag to be set ($C6 b0)
- Read the Vocoder section data value from the RxData0 register ($B8).

Vocoder section C-BUS addresses are all 8 bits long and should be written to bits 0-7 of the Programming register. Bit 15 is the read/write flag (1 = read, 0 = write) and bit 14 is the register-size flag (0 = 16-bit, 1 = 8-bit). Unused bits should be cleared to zero. When an 8-bit register is read or written, the data occupies the lower 8 bits of the appropriate data register (TxData0 or RxData0).

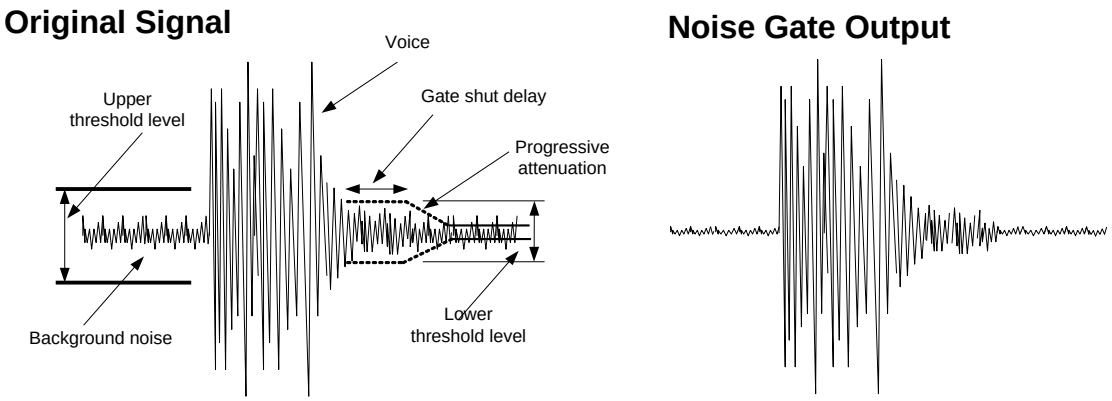
8.5.13 Vocoder Section – Noise Gate

The Vocoder section has an optional, programmable noise gate. This is controlled by the addition of five new 16-bit C-BUS write registers, accessed by Pass-through mode (see section 8.5.12). Once the Function Image™ has been loaded, these new registers will all be set to an initial value of zero. For details of how to configure these registers, see section 10.3.

The purpose of the encoder's noise gate is to remove background noise in between speech pauses. This could be used to remove noise generated in any front-end analogue circuitry, or could be used to help reduce the effects of ambient noise, perhaps with some degree of user control.

Three parameters control this noise gate. An upper threshold level controls the point at which the gate opens and allows audio to pass. A lower threshold level controls the point at which the gate closes, thereby preventing audio from passing. These two parameters together control the hysteresis and prevent 'chattering'. A third parameter controls how many consecutive frames of audio must be below the lower threshold before the gate closes. This 'gate shut delay' prevents the tail end of words (like a trailing 's') from being clipped.

Once the gate shut delay has expired, the gate does not shut abruptly, but closes over a period of 16 frames. Each 20ms frame has progressively more attenuation applied, until the frames are silent. This happens in approximately 6dB steps.



The purpose of the decoder's noise gate is to remove audio artefacts after decoding packets of vocoded silence. The noise gate operation is exactly the same as the encoder's noise gate, however, only the lower threshold level is programmable. The upper threshold level is fixed to be twice the lower threshold level, and the gate shut delay is fixed to be 10 frames, which is 200ms.

8.5.14 dPMR Operating Modes and Addressing

TS 102 490 describes two operating modes for a dPMR radio:

- ISF – Initial Services and Facilities – “out of the box” mode
- CSF – Configured Services and Facilities – “managed” mode.

The CMX8341 can support either of these modes, as selected by b9 of the Modem Configuration register, $C7 (see User Manual section 10.1.25).

The standard also defines two addressing schemes: 24-bit binary or 7-digit BCD (binary-coded-decimal). Radios operating in ISF mode are required to use binary addressing, but in CSF mode either binary or BCD addressing can be used. Both addressing schemes are supported by the CMX8341, selected by b11 in the Modem Configuration register, $C7 (see User Manual section 10.1.25).

The host can load two Own IDs (binary or BCD) into Program Block 1 for use in both Tx and Rx modes. In Tx mode the host can select which of these to send in the “Caller ID” field of the outgoing call. In Rx mode, the CMX8341 compares the “Called ID” field from incoming calls against each of its Own IDs, and will accept the call if a valid ID match is found. Address matching can be disabled using b12 of the Modem Configuration register, $C7, in which case the CMX8341 will accept all incoming calls.

The CMX8341 implements BCD address translation in both Tx and Rx, to relieve the host of the processing required to map BCD digits to over-air binary values. BCD addresses can include wildcard digits in any of the lower four digits, and there are ten BCD “All-Call” addresses with wildcards in all six lower digits. The CMX8341 handles wildcard digits appropriately during address matching in Rx.

Binary addresses do not support group calling with wildcards, but the CMX8341 provides six binary-only Group Call IDs in addition to the two Own IDs. These can be programmed by the host to be used for address matching in Rx only.

TS 102 490 also specifies a system-wide All Call facility using the “Communication Format” field in the Header Frame (TS 102 490 section 5.8). The normal setting for this field is “Peer-to-Peer”, but when set to “Call ALL” the CMX8341 will always accept the call regardless of ISF/CSF mode and all other address settings. The host should take care not to transmit in All Call mode unless actually intended.

8.5.15 ISF Addressing

The services available in ISF mode are described in TS 102 490 section 8.1. Radios using ISF mode provide a style of operation broadly similar to analogue PMR446.

ISF mode requires 24-bit binary addressing to be used, with only the top 8 bits (the Common ID field) in active use for addressing ISF mode devices. The remaining 16 bits must be set to all 1s. This is the default mode of the CMX8341 and the default Common IDs are:

- ID1: $01
- ID2: $02.

The ISF Common All-Call ID is $FF. When in ISF mode the CMX8341 will always accept calls to this address regardless of other address settings.

8.5.16 CSF Addressing

The services available in CSF mode are described in TS 102 490 section 8.2 and Annex A.

CSF mode does not mandate BCD addressing unless the host implements the Standard User Interface, but the advantages of BCD addressing are direct mapping of user keypad entries to destination addresses and the option of wildcard digits to implement group calls. The host can select the addressing mode using b11 of the Modem Configuration register, $C7.

8.5.17 Tx Mode (dPMR formatted)

In Tx dPMR Formatted mode ($C1, Modem Control = $0012), the CMX8341 builds Header, Control Channel and End Information blocks, performs all FEC coding, interleaving and scrambling functions and inserts Frame Sync and Colour Code sequences to generate the required frame formats for transmission. During voice calls the CMX8341 can automatically enable and control the Vocoder section and transfer voice payload data from/to it without host intervention.

The TxData registers are used to transfer Header and End Information fields in addition to payload data. The Block ID field in the TxData0 register informs the CMX8341 how to process each transfer.

b5-4	Block ID
00	HDR - Header Data
01	PLD - Payload Data
10	PLS - Payload Data with Slow Data
11	END - End Data

The host should preload the TxData registers with Header Data before placing the device in Tx dPMR Formatted mode. The CMX8341 reads the “Header Type” field to determine the burst type and then sends the Preamble and Header Frame. If the “Call Information” field indicates that repeated “extended wake-up” Headers are to be sent, the CMX8341 will do so automatically. The Header fields are saved for re-use when building the Control Channel Information blocks in following payload frames: the host does not need to re-load them.

Header Data:

TxData RxData	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	LE	0	Own ID		Header Type				Counter		0	0	1	0	0	1
1	0	0	Call Information											Comms Mode		
2	Version		Format		0	0	0	0	0	0	Colour Code					
3	0	0	0	0	Binary mode: Address – lower 12 bits											
	BCD mode: Address – lower 4 digits K4, K5, K6, K7															
4	0	0	0	0	Binary mode: Address – upper 12 bits											
	0	0	0	0	BCD mode: Address – upper 3 digits K1, K2, K3											

Header Type:	See TS 102 490 section 5.11 (Communication Start, ACK, etc.)
Own ID:	00 = Tx: *reserved* Rx: All call received 01 = Tx: send Own ID 1 (from Program Block 1) Rx: Own ID1 matched 10 = Tx: send Own ID 2 (from Program Block 1) Rx: Own ID2 matched 11 = *reserved*
reserved:	See TS 102 490 section 5.4 (00)
Comms Mode:	See TS 102 490 section 5.7 (sets data type and source, host or vocoder)
LE:	Late-Entry (Rx only) – some data fields may be missing due to Late Entry into the call
Call Information:	See TS 102 490 section 5.10 (includes extended headers, data frame size etc.)
Comms Format:	See TS 102 490 section 5.8 (All-Call or Peer-to-Peer) 00 = Call ALL (Broadcast) 01 = Peer-to-Peer communication 10 = reserved 11 = reserved
Version:	See TS 102 490 section 5.16 (Vocoder Version)

Note: the dPMR Association has agreed standard bit allocations for the voice burst and the host should set this field accordingly.

00 = DVSI AMBE+2
01 = To be selected by Chinese DRA
10 = RALCWI
11 = Manufacturer defined

Colour Code:	6-bit index into the Colour Code table as shown in TS 102 490 section 6.1.5
Address:	Tx: destination (Called) address. Rx: originating (Caller) address.

Payload Data:
See Table 10 and User Manual section 10.1.12

Payload Data with Slow Data:
See Table 10 and User Manual section 10.1.12

End Data:

TxData RxData	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Tx Wait				Ack Req		End Type		Counter		1	1	0	0	1	1
1	0	0	0	0	0	0	*reserved*				0	Status Message				
2	Not used															
3	Not used															
4	Not used															

End Type: See TS 102 490 section 5.12

Ack Request: See TS 102 490 section 5.13

Tx Wait: See TS 102 490 section 5.14

Status Msg: See TS 102 490 section 5.15

reserved: 0000

Depending on the burst type, the CMX8341 will expect the host to load a series of payload data blocks and/or an End Data block (except for ACK bursts which consist of a bare Header Frame). Disconnect bursts contain a repeated Header/End Frame pair but the host should only load single blocks of Header and End Data fields, as the CMX8341 will send the duplicate frames automatically.

If the Vocoder section is enabled and the “Communication Mode” field in the Header Frame indicates a voice call, the CMX8341 will automatically enable the Vocoder section microphone input and route payload data from the Vocoder section for transmission. Note that the Vocoder section takes a finite time to encode the incoming voice data, during which the CMX8341 will automatically insert “silence” data into the payload frames. The host can load an End Frame at any point during the call. To terminate the voice call, the host should place the CMX8341 modem into Tx Idle mode ($C1, Modem Control = $0002). The CMX8341 will disable the Vocoder section and send the End Frame that was loaded previously.

At the end of all dPMR transmissions the CMX8341 will issue a TxDone IRQ when it is safe for the host to place the device back into Idle mode ($C1, Modem Control = $0000).

8.5.18 Rx Mode (dPMR formatted)

In Rx dPMR mode ($C1, Modem Control = $0011), the CMX8341 automatically splits incoming calls to extract Header Information, Control Channel Information and End Information blocks and performs all the necessary de-scrambling, de-interleaving and FEC decoding functions. In speech calls, the CMX8341 can automatically enable the Vocoder section when required and transfer received speech data without host intervention.

The RxData registers are used to transfer Header and End Data fields in addition to payload data. The Block ID field in the RxData0 register informs the host what type of data block each transfer contains. The field layout in the RxData registers for the different transfer types is the same as for Tx dPMR Formatted mode (section 8.5.17).

When placed in Rx dPMR Formatted mode, the CMX8341 automatically starts searching for the dPMR frame sync sequences. In addition to detecting the 48-bit FS1 frame sync at the start of a transmission, the CMX8341 can also perform “late entry” into a call by detecting two successive copies of the 24-bit FS2 sequence at the correct two-frame spacing. When a valid frame sync sequence has been detected, an “FS1 Detect” or “FS2 Detect” IRQ is issued and the data demodulator is enabled.

The CMX8341 then decodes the contents of the Header Frame (after an FS1 detect) or the following four Control Channel Information blocks (after an FS2 detect). The Header Information or Control Channel Information CRCs are checked and processing continues only if a full set of valid fields has been received. Header Frames contain two duplicate Header Information blocks: the CMX8341 checks both block CRCs, uses the first valid block and discards the other.

When repeated “extended wake-up” Header Frames are received (see TS 102 490 section 11.1), the CMX8341 will decode the first valid Header but delay address checking until all following repeat Headers have been received. This maximises the time the host can be kept in powersave.

Address checking now takes place depending on ISF/CSF mode and the addressing mode selected. The “Communications Format” field is checked first: if this is set to “Call ALL” the call is accepted. If not, the “Called station ID” is checked against the device’s Own IDs (programmed by the host into Program Block 1) and if a match is found the call is accepted. In ISF mode, the Common All-Call ID $FF is also always accepted. In any of these cases a “Called” IRQ is issued to the host, otherwise the call is dropped with no further host notification and the CMX8341 returns to frame sync search. Address matching can be disabled by setting b12 of the Modem Configuration register, in which case the CMX8341 will accept all incoming calls.

The Header fields are presented to the host in the RxData block. Late entry is indicated by bit 15 of RxData0: in this case the “Header Type” and “Call Information” fields in the Header Data block returned to the host will not contain valid data, as these fields are only sent in Header Frames and are not re-sent in the Control Channel Information blocks during a call.

Depending on the burst type, the CMX8341 will decode the following payload and/or End Frames and present their contents to the host or vocoder. If the Vocoder section is enabled and the “Communication Mode” field in the Header Frame indicates a voice call, the CMX8341 will automatically enable the Vocoder section speaker output and route payload data to the Vocoder section for decoding. In this mode, the data is transferred in 4-bit Log-Likelihood-Ratio format. Otherwise, payload data is presented to the host in the RxData registers in soft or hard format, as specified. When an End Frame is received, the CMX8341 will report its contents to the host, disable the vocoder (if necessary) and return to frame sync search.

All frame sync sequences, Colour Codes and CRCs contained in payload superframes are checked and an “Event” IRQ is issued when any are received incorrectly. If all the frame sync sequences, Colour Codes and CRCs in a superframe are received incorrectly, the superframe is considered corrupt. The host can set a threshold for consecutive corrupt superframes (in Program Block 0), after which the CMX8341 will issue an “Event” IRQ, drop the call and return to frame sync search.

See:

- RxData 0 - $B8 read
- AuxData/Sub-audio Read - $CC read.

8.5.19 Slow Data

Slow Data may be transferred in voice calls alongside Voice Payload Data, by setting the Block ID to “Payload with Slow Data” and using the AuxData registers. If the Vocoder section is enabled, there will be no voice payload transfers and so dummy payload transfers are used with the Byte Counter field cleared to zero. In Type1 and Type 2 Data calls, the Slow Data field is used to control the data flow over-air and so is generated or decoded by the CMX8341 itself and the only data field that is visible to the host is the “Format” field as defined in TS 102 490 section 5.9.2. which is made available, or supplied by the host, in the lowest 4 bits of the AuxData register.

In Tx mode:

- Load AuxData register with two bytes of Slow Data: AuxData/Sub-audio Write - $C2 write
- Set Communications Mode to “Voice with Slow Data”
- Set BlockID to “Payload with Slow Data”: TxData 0 - $B5 write
- Set Byte Counter field (to zero if Vocoder section is in use): TxData 0 - $B5 write.

The CMX8341 has an internal 64-byte buffer for Slow Data. While the host keeps this internal data buffer “topped-up” the CMX8341 will continue to transmit Slow Data and add the “continuation bits” to the over-air data. Note that only two bytes of Slow Data are sent over-air for every 36 bytes of voice payload, so the buffer may overflow if a large quantity of Slow Data is loaded continuously. The host is expected to track the number of bytes in the buffer.

Bit 10 of the Status register $C6 is set to 1 and an interrupt raised, if unmasked, when there are only two bytes left in the FIFO. When the host allows the internal buffer to empty, the CMX8341 will terminate the

transmission of Slow Data in the current burst. It is not possible to re-start Slow Data transmission within a burst.

In Rx mode:

- BlockID will report “Payload with Slow Data”: RxData 0 - $B8 read
- Communications Mode will report “Voice with Slow Data”
- If payload is being sent to the Vocoder section, then the Byte Counter field will be cleared to zero
- Slow Data is available in the AuxData register: AuxData/Sub-audio Read - $CC read

When the Slow Data transfer has completed, the CMX8341 will stop presenting data to the host.

8.6 Analogue Mode

8.6.1 Tx Mode Analogue

In Analogue PMR mode, the MIC input is processed and summed with either the external sub-audio signal on the ALT input or the internally generated sub-audio signal and then presented at the MOD1 and MOD2 pins. The choice is determined by Program Block P2.0 b5 (see section 10.2.3).

8.6.2 Rx Mode Analogue

In Analogue PMR mode the received signal should be routed through Input1 (DISC). The signal is filtered and processed so that the inband signal is output on the Audio pin and the sub-audio signal is either output on the AuxDAC4 pin or routed to the internal sub-audio detector. The choice is determined by Program Block P2.0 b4 (see section 10.2.3).

8.7 Squelch Operation

Many Limiter/Discriminator chips provide a noise-quieting squelch circuit around an op-amp configured as a filter. This signal is conventionally passed to a comparator to provide a digital squelch signal, which can be routed directly to one of the CMX8341’s GPIO pins or to the host. However with the CMX8341, the comparator and threshold operations can be replaced by one of the AuxADCs with programmable thresholds and hysteresis functions.

See:

- IRQ Status - $C6 read
- Modem Configuration - $C7 write

8.8 GPIO Pin Operation

The CMX8341 provides four GPIO pins. RXENA (GPIO1) and TXENA (GPIO2) are configured to reflect the Tx/Rx state of the Mode register (TXENA and RXENA, active low).

See:

- Modem Configuration - $C7 write.

Note that RXENA and TXENA will not change state until the relevant mode change has been executed by the CMX8341. This is to allow the host sufficient time to load the relevant data buffers and the CMX8341 time to encode the data required prior to its transmission. There is thus a fixed time delay between the GPIO pins changing state and the data signal appearing at the MOD output pins. During the power-on sequence (until the FI has completed its load sequence) these pins have only a weak pull-up applied to them, so care should be taken to ensure that any loading during this period does not adversely affect the operation of the unit.

GPIO A and B are host programmable for input or output using the AuxADC Configuration register, $A7. The default state is input, with a weak pull-up. When set for input, the values can be read back using the Modem Status register, $C9.

8.9 Auxiliary ADC Operation

The inputs to the two auxiliary ADCs can be independently routed from any of the signal input pins under control of the AuxADC Configuration register, $A7. Conversions will be performed as long as a valid input source is selected. To stop the ADCs, the input source should be set to “off”. Register $C0, b6, BIAS, must be enabled for auxiliary ADC operation.

Averaging can be applied to the ADC readings by selecting the relevant bits in the AuxADC Configuration register, $A7. The length of the averaging is determined by the value in P3.0 and P3.1 and defaults to a value of 0. This is a rolling average system such that a proportion of the current data will be added to the last average value. The proportion is determined by the value of the average counter in P3.0 and P3.1.

For an average value of:

0 = 50% of the current value will be added to 50% of the last average value
1 = 25% of the current value will be added to 75% of the last average value
2 = 12.5% etc.

The maximum useful value of this field is 9.
High and Low thresholds may be independently applied to both ADC channels (the comparison is applied after averaging, if this is enabled) and an IRQ generated when a rising edge passes the High threshold or a falling edge passes the Low threshold, see Figure 20. The thresholds are programmed via the AuxADC Threshold register, $CD.

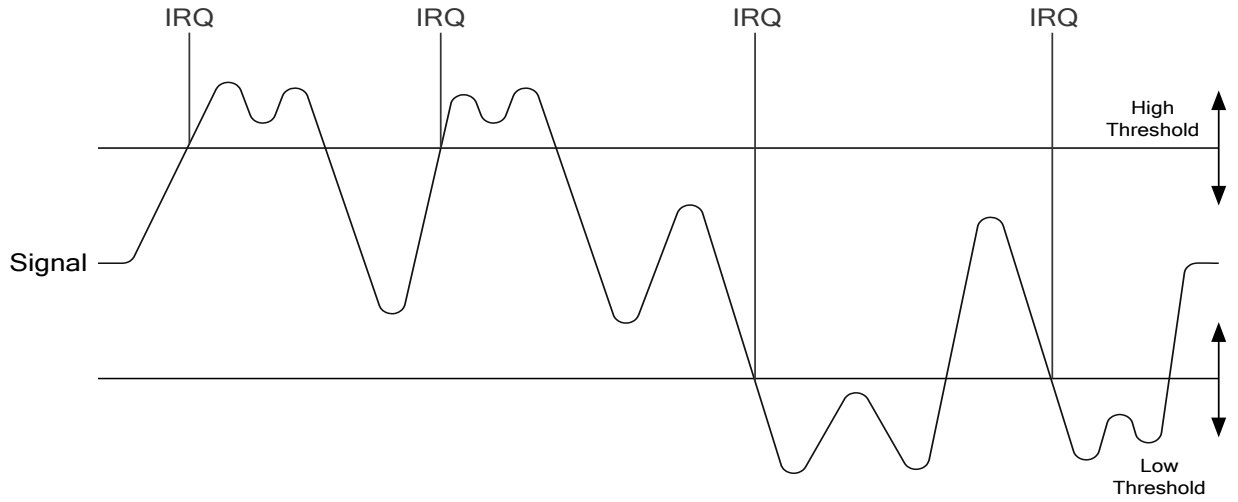


Figure 20 AuxADC IRQ Operation

Auxiliary ADC data is read back in the AuxADC Data registers ($A9 and $AA) and includes the threshold status as well as the actual conversion data (subject to averaging, if enabled).

See:

- AuxADC Configuration - $A7 write
- AuxADC1 Data and Status - $A9 read
- AuxADC2 Data and Status - $AA read
- AuxADC Threshold Data - $CD write.

8.10 Auxiliary DAC/RAMDAC Operation

The four auxiliary DAC channels are programmed via the AuxDAC Data/Control register, $A8. AuxDAC channel 1 may also be programmed to operate as a RAMDAC, which will automatically output a pre-programmed profile at a programmed rate. The AuxDAC Data/Control register, $A8, with b12 set, controls this mode of operation. The default profile is a raised cosine (see Table 15), but this may be over-written

with a user-defined profile by writing to P3.11. The RAMDAC operation is only available in Tx mode and, to avoid glitches in the ramp profile, it is important not to change to Idle or Rx mode whilst the RAMDAC is still ramping. The AuxDAC outputs hold the user-programmed level during a powersave operation if left enabled, otherwise they will return to zero. Note that access to all four AuxDACs is controlled by the AuxDAC Data/Control register, $A8, and therefore to update all AuxDACs requires four writes to this register. It is not possible to simultaneously update all four AuxDACs.

AuxDAC4 is used in Analogue mode to output the filtered Sub-Audio signal.

See:

- AuxDAC Data/Control - $A8 write.

8.11 Digital System Clock Generators

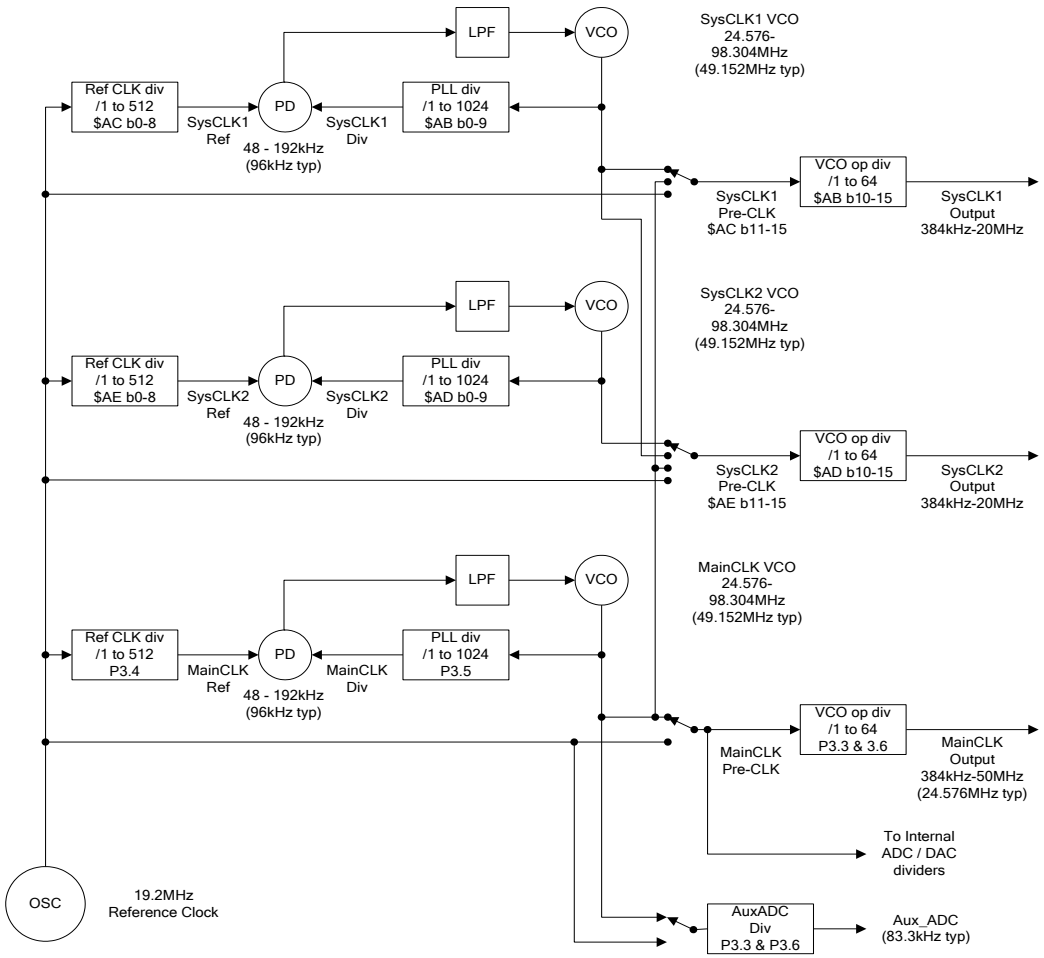


Figure 21 Digital Clock Generation Schemes

The CMX8341 requires a 19.2MHz reference clock source.

8.11.1 Main Clock Operation

A digital PLL is used to create the Main Clock (nominally 24.576MHz) for the internal sections of the CMX8341. At the same time, other internal clocks are generated by division of either the Reference Clock or the Main Clock Pre-Clock. These internal clocks are used for determining the sample rates and conversion times of A-to-D and D-to-A converters, running a General Purpose (GP) Timer and the signal processing block. In particular, it should be noted that in Idle mode the setting of the GP Timer divider directly affects the C-BUS latency (with the default values this is nominally 250µs).

The CMX8341 defaults to the settings appropriate for a 19.2MHz oscillator, as given in P3.2 to P3.7.

See:

- Program Block 3 – AuxDAC, RAMDAC and Clock Control.

8.11.2 System Clock Operation

Two System Clock outputs, SYSCLK1 and SYSCLK2, are available to drive additional circuits, as required. These are digital phase locked loop (PLL) clocks that can be programmed via the System Clock registers with suitable values chosen by the user. The System Clock PLL Configure registers ($AB and $AD) control the values of the VCO Output divider and Main Divide registers, while the System Clock Ref. Configure registers ($AC and $AE) control the values of the Reference Divider and signal routing configurations. The PLLs are designed for a reference frequency of 96kHz. If not required, these clocks can be independently powersaved. The clock generation scheme is shown in the block diagram of Figure 21. Note that at power-on, these pins are disabled.

See:

- SYSCLK 1 and SYSCLK 2 PLL Data - $AB, $AD write
- SYSCLK 1 and SYSCLK 2 REF - $AC and $AE write.

8.12 Signal Level Optimisation

The internal signal processing of the CMX8341 will operate with wide dynamic range and low distortion only if the signal level at all stages in the signal processing chain is kept within the recommended limits. For a device working from a 3.3V ±10% supply, the maximum signal level which can be accommodated without distortion is [(3.3 x 90%) - (2 x 0.3V)] Volts pk-pk = 838mV rms, assuming a sine wave signal. This should not be exceeded at any stage. In Analogue mode, an Input AGC function is provide to optimise the Mic input level across a wide dynamic range. In this mode the effects of Pre-emphasis and De-emphasis as well as overload conditions should be taken into account when determining appropriate input levels.

8.12.1 Transmit Path Levels

For the maximum signal out of the MOD1 and MOD2 attenuators, the signal level at the output of the Modem block is set to be 0dB, The Fine Output adjustment ($C8 P4.2-4.3) has a maximum attenuation of 3.5dB and no gain, whereas the Coarse Output adjustment ($B0: b14-12, b10-8) has a variable attenuation of up to 12dB in 2dB steps and a mute setting (>40dB), and no gain.

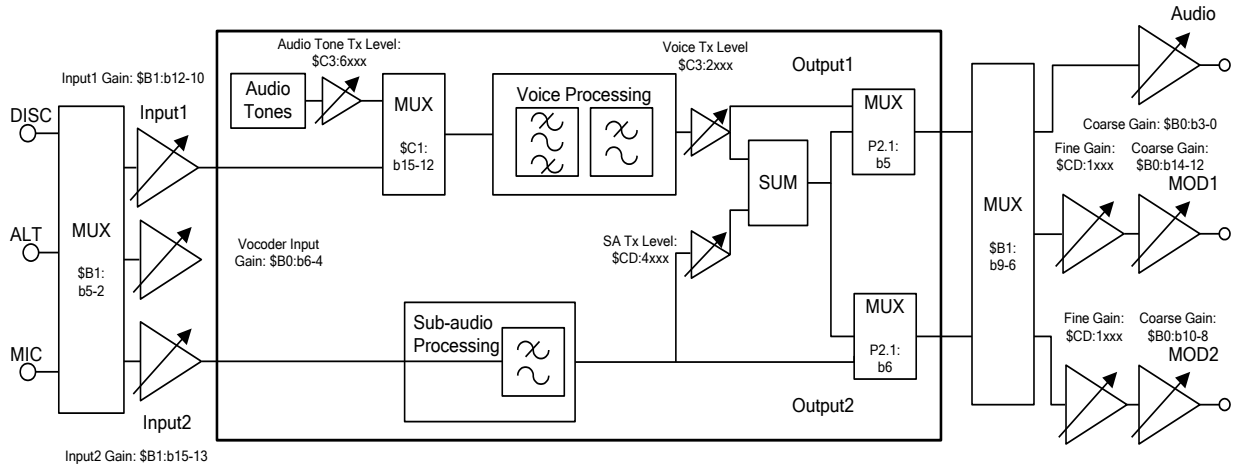


Figure 22 Tx Level Adjustments (Analogue)

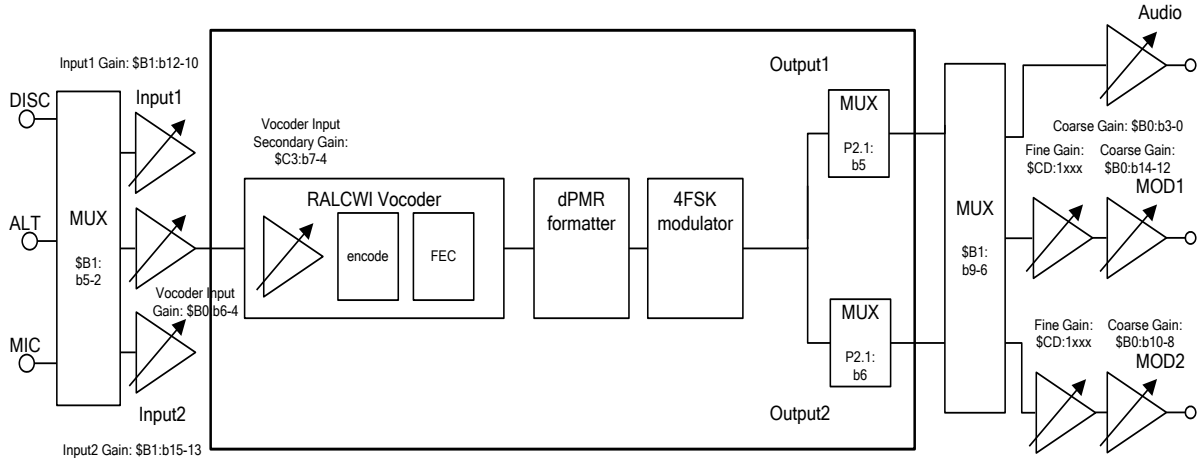


Figure 23 Tx Levels (Digital)

8.12.2 Receive Path Levels

The Coarse Input adjustment ($B1) has a variable gain of up to +22.4dB and no attenuation. With the lowest gain setting (0dB), the maximum allowable input signal level at the DISCFB pin would be 838mV rms. This signal level is an absolute maximum, which should not be exceeded.

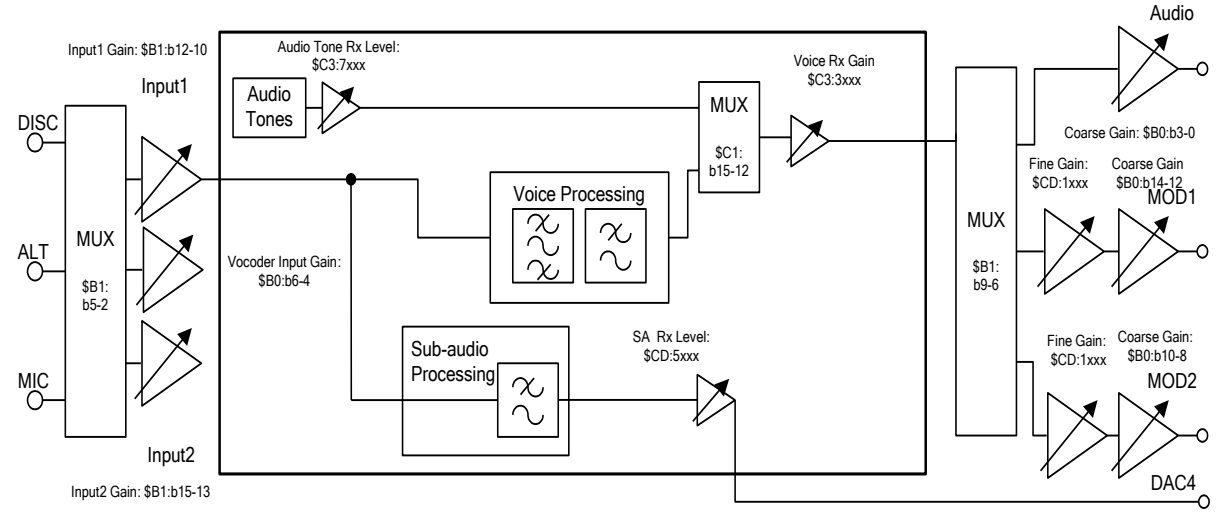


Figure 24 Rx Level Adjustments (Analogue)

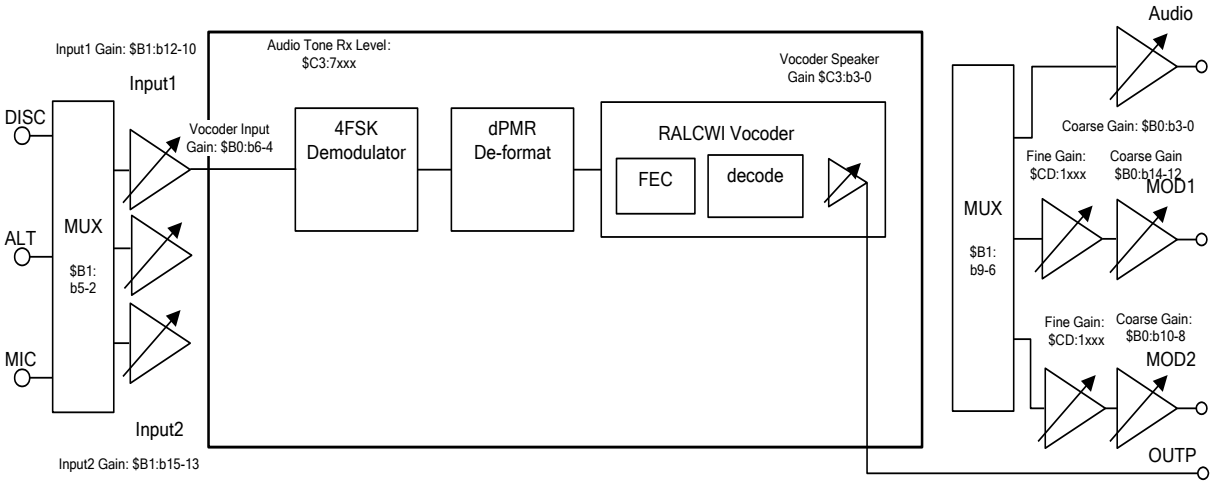


Figure 25 Rx Level Adjustments (Digital)

8.13 Tx Spectrum Plots

The following figure shows the Tx spectrum when using a suitable signal generator as measured on a spectrum analyser using the CMX8341 internal PRBS generator.

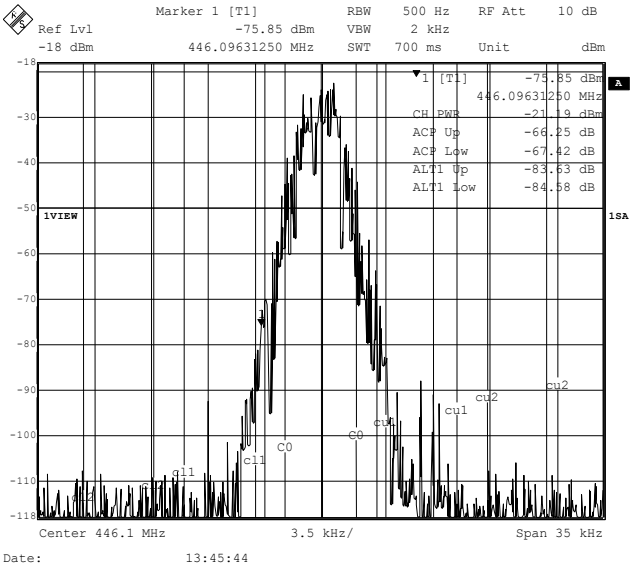


Figure 26 Tx Modulation Spectra - 4800bps

8.14 C-BUS Register Summary

Table 11 C-BUS Registers

ADDR. (hex)		REGISTER	Word Size (bits)
$01	W	C-BUS RESET	0
$A7	W	AuxADC Configuration	16
$A8	W	AuxDAC Data and Control	16
$A9	R	AuxADC1 Data and Status/Checksum 2 hi	16
$AA	R	AuxADC2 Data and Status/Checksum 2 lo	16
$AB	W	SYSCLK 1 PLL Data	16
$AC	W	SYSCLK 1 Ref	16
$AD	W	SYSCLK 2 PLL Data	16
$AE	W	SYSCLK 2 Ref	16
$AF		*reserved*	
$B0	W	Analogue Output Gain	16
$B1	W	Input Gain and Signal Routing	16
$B2		*reserved*	
$B3		*reserved*	
$B4		*reserved*	
$B5	W	TxData 0	16
$B6	W	TxData 1	16
$B7	W	TxData 2	16
$B8	R	RxData 0/Checksum 1 hi	16
$B9	R	RxData 1/Checksum 1 lo	16
$BA	R	RxData 2	16
$BB	R	RxData 3	16
$BC		*reserved*	
$BD		*reserved*	
$BE		*reserved*	
$BF		*reserved*	
$C0	W	Power Down Control	16
$C1	W	Modem Control	16
$C2	W	AuxData/Sub-audio Write	16
$C3	W	Vocoder Section Analogue Gain	16
$C4		*reserved*	
$C5	R	Rx Data 4	16
$C6	R	IRQ Status	16
$C7	W	Modem Configuration	16
$C8	W	Programming Register	16
$C9	R	Modem Status	16
$CA	W	Tx Data 3	16
$CB	W	Tx Data 4	16
$CC	R	AuxData/Sub-audio Read	16
$CD	W	AuxADC Threshold Data	16
$CE	W	Interrupt Mask	16
$CF		*reserved*	

All other C-BUS addresses (including those not listed above) are either reserved for future use or allocated for production testing and must not be accessed in normal operation.

9 Performance Specification

9.1 Electrical Performance

9.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (AV_{DD} - AV_{SS}, DV_{DD} - DV_{SS})	-0.3	4.0	V
Supply (DV_{CORE} - DV_{SS})	-0.3	2.16	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current into or out of any V_{DD} or V_{SS} pins	-120	+120	mA
Current into or out of any other pin	-20	+20	mA

L8 Package	**Min.**	**Max.**	**Units**
Total Allowable Power Dissipation at Tamb = 25ºC		2190	mW
... Derating		21.9	mW/ºC
Storage Temperature	-55	+125	ºC
Operating Temperature	-40	+85	ºC

9.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (AV_{DD} - AV_{SS}, DV_{DD} - DV_{SS})		3.0	3.6	V
Supply (DV_{CORE} - DV_{SS})		1.7	1.9	V
Operating Temperature		-40	+85	ºC
Xtal/External Clock Frequency	1	3.0	24.576	MHz

Note: 1. Correct operation of the device requires the following specific frequencies to be applied:
A reference clock to XTAL/CLK (pin 55) = 19.2MHz ± 100ppm

9.1.3 Operating Characteristics

Details in this section represent design target values and are not currently guaranteed.
For the following conditions unless otherwise specified:

External components as recommended in Figure 2 and Table 2.
Reference clock frequency = 19.2MHz ±0.01% (100ppm); Tamb = –40°C to +85°C.
AV_{DD} = DV_{DD} = 3.0V to 3.6V; DV_{CORE} = 1.7V to 1.9V; V_{DEC} = 2.5V; V_{BIAS} = AV_{DD}/2.
Reference Signal Level = 308mVrms at 1kHz with AV_{DD} = 3.3V.
Signal levels track with supply voltage, so scale accordingly.
Signal to Noise Ratio (SNR) in bit rate bandwidth.
Input stage gain = 0dB. Output stage attenuation = 0dB. Maximum load on digital outputs = 30pF.

Current consumption figures quoted in this section apply to the device when loaded with 8341 FI-1.x only. The use of other Function Images can modify the current consumption of the device.

DC Parameters	Notes	Min.	Typ.	Max.	Units
Supply Current	11				
All Powersaved					
DI_{CORE}		–	50	–	µA
DI_{DD}		–	8	100	µA
AI_{DD}		–	4	20	µA
Idle Mode	12				
DI_{CORE}		–	14.0	–	mA
DI_{DD}		–	1.9	–	mA
AI_{DD}	13	–	1.6	–	mA
Rx Mode (excluding Vocoder Section)	12				
DI_{DD} (4800bps – search for FS)		–	4.7	–	mA
DI_{DD} (9600bps – search for FS)		–	7.5	–	mA
DI_{DD} (4800bps – FS found)		–	2.8	–	mA
DI_{DD} (9600bps – FS found)		–	3.7	–	mA
AI_{DD} (AV_{DD} = 3.3V)		–	1.6	–	mA
Tx Mode (excluding Vocoder Section)	12				
DI_{DD} (4800bps – 2-point)		–	4.3	–	mA
DI_{DD} (9600bps – 2-point)		–	5.2	–	mA
DI_{DD} (4800bps – I/Q)		–	5.4	–	mA
DI_{DD} (9600bps – I/Q)		–	7.3	–	mA
AI_{DD} (AV_{DD} = 3.3V)		–	1.5	–	mA
Vocoder Section					
DI_{CORE}		–	38.0	–	mA
DI_{DD}		–	0.6	–	mA
AI_{DD} (AV_{DD} = 3.3V)	14	–	7.2	–	mA
Additional current for each Auxiliary System Clock (output running at 4MHz)					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	250	–	µA
Additional current for each Auxiliary ADC					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	50	–	µA
Additional current for each Auxiliary DAC					
AI_{DD} (AV_{DD} = 3.3V)		–	200	–	µA

Notes:
11 Tamb=25°C: not including any current drawn from the device pins by external circuitry.
12 System Clocks: auxiliary circuits disabled, but all other digital circuits (including the Main Clock PLL) enabled.
13 May be further reduced by power-saving unused sections.
14 ADC or DAC enabled in Vocoder Section.

DC Parameters (continued)	Notes	Min.	Typ.	Max.	Unit
Reference Clock Input					
Input Logic 1		70%	–	–	DV_{DD}
Input Logic 0		–	–	30%	DV_{DD}
Input Current (Vin = DV_{DD})		–	–	40	µA
Input Current (Vin = DV_{SS})		–40	–	–	µA
C-BUS Interface and Logic Inputs					
Input Logic 1		80%	–	–	DV_{DD}
Input Logic 0		–	–	20%	DV_{DD}
Input Leakage Current (Logic 1 or 0)		–5.0	–	5.0	µA
Input Capacitance		–	–	7.5	pF
C-BUS Interface and Logic Outputs					
Output Logic 1 (I_{OH} = 2mA)		90%	–	–	DV_{DD}
Output Logic 0 (I_{OL} = -5mA)		–	–	10%	DV_{DD}
"Off" State Leakage Current		–	–	10	µA
IRQN (Vout = DV_{DD})		–5.0	–	+5.0	µA
REPLY_DATA (output HiZ)		–5.0	–	+5.0	µA
V_{BIAS}	21				
Output Voltage Offset wrt $AV_{DD}/2$ (I_{OL} < 1µA)		–	±2%	–	AV_{DD}
Output Impedance		–	22	–	kΩ

Notes:

21 Applies when utilising V_{BIAS} to provide a reference voltage to other parts of the system. When using V_{BIAS} as a reference, V_{BIAS} must be buffered. V_{BIAS} must always be decoupled with a capacitor as shown in Figure 2 and Table 2.

AC Parameters		Notes	Min.	Typ.	Max.	Unit
Reference Clock Input						
'High' Pulse Width			15	–	–	ns
'Low' Pulse Width			15	–	–	ns
Input Impedance		31				
Powered-up	Resistance		–	150	–	kΩ
	Capacitance		–	20	–	pF
Powered-down	Resistance		–	300	–	kΩ
	Capacitance		–	20	–	pF
Xtal Start-up Time (from powersave)			–	20	–	ms
System Clk 1/2 Outputs						
Ref. Clock input to CLOCK_OUT timing:						
(in high to out high)		32	–	15	–	ns
(in low to out low)		32	–	15	–	ns
'High' Pulse Width		33	76	81.38	87	ns
'Low' Pulse Width		33	76	81.38	87	ns
V_{BIAS}						
Start-up Time (from powersave)			–	100	–	ms
Microphone, Alternative and Discriminator Inputs (MIC, ALT, DISC)						
Input Impedance		34	–	>10	–	MΩ
Maximum Input Level (pk-pk)		35	–	–	80%	AV_{DD}
Load Resistance (feedback pins)			80	–	–	kΩ
Amplifier Open Loop Voltage Gain (I/P = 1mVrms at 100Hz)			–	80	–	dB
Unity Gain Bandwidth			–	1.0	–	MHz
Programmable Input Gain Stage		36				
Gain (at 0dB)		37	–0.5	0	+0.5	dB
Cumulative Gain Error (wrt attenuation at 0dB)		37	–1.0	0	+1.0	dB

Notes:
31 Characterised and specified at 6.144MHz only.
32 Characteristics when driving the Reference Clock input with an external clock source.
33 6.144MHz Reference Clock selected (scale for 19.2MHz).
34 With no external components connected, measured at DC.
35 Centred about $AV_{DD}/2$; after multiplying by the gain of input circuit (with external components connected).
36 Gain applied to signal at output of buffer amplifier: DISCFB, ALTFB or MICFB
37 Design Value. Overall attenuation input to output has a tolerance of 0dB ±1.0dB

AC Parameters	Notes	Min.	Typ.	Max.	Unit
Modulator Outputs 1/2 and Audio Output (MOD1, MOD2, AUDIO)					
Power-up to Output Stable	41	–	50	100	µs
Modulator Attenuators					
Attenuation (at 0dB)	43	−1.0	0	+1.0	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)		−0.6	0	+0.6	dB
Output Impedance Enabled	42	–	600	–	Ω
Output Impedance Disabled	42	–	500	–	kΩ
Output Current Range (AV_{DD} = 3.3V)		–	–	±125	µA
Output Voltage Range	44	0.5	–	AV_{DD} –0.5	V
Load Resistance		20	–	–	kΩ
Audio Attenuator					
Attenuation (at 0dB)	43	−1.0	0	+1.0	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)		−1.0	0	+1.0	dB
Output Impedance Enabled	42	–	600	–	Ω
Output Impedance Disabled	42	–	500	–	kΩ
Output Current Range (AV_{DD} = 3.3V)		–	–	±125	µA
Output Voltage Range	44	0.5	–	AV_{DD} –0.5	V
Load Resistance		20	–	–	kΩ

Notes:

41 Power-up refers to issuing a C-BUS command to turn on an output. These limits apply only if V_{BIAS} is on and stable. At power supply switch-on, the default state is for all blocks, except the Reference Clock and C-BUS interface, to be in placed in powersave mode.

42 Small signal impedance, at AV_{DD} = 3.3V and Tamb = 25°C.

43 With respect to the signal at the feedback pin of the selected input port.

44 Centred about $AV_{DD}/2$; with respect to the output driving a 20kΩ load to $AV_{DD}/2$.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Auxiliary Signal Inputs (Aux ADC 1 to 4)					
Source Output Impedance	51	–	–	24	kΩ
Auxiliary 10 Bit ADCs					
Resolution		–	10	–	Bits
Maximum Input Level (pk-pk)	54	–	–	80%	AV_{DD}
Conversion Time	52	–	250	–	µs
Input Impedance					
Resistance	57	–	>10	–	MΩ
Capacitance		–	5	–	pF
Offset Error	55, 56	0	–	±10	mV
Integral Non-linearity	55, 56	–	–	±3	LSBs
Differential Non-linearity	53, 55	–	–	±1	LSBs
Auxiliary 10 Bit DACs					
Resolution		–	10	–	Bits
Maximum Output Level (pk-pk), no load	54	80%	–	–	AV_{DD}
Offset Error	55, 56	0	–	±10	mV
Resistive Load		5	–	–	kΩ
Integral Non-linearity	55, 56	–	–	±4	LSBs
Differential Non-linearity	53, 55	–	–	±1	LSBs

Notes:

51 Denotes output impedance of the driver of the auxiliary input signal, to ensure < 1 bit additional error under nominal conditions.
52 With an auxiliary clock frequency of 6.144MHz.
53 Guaranteed monotonic with no missing codes.
54 Centred about $AV_{DD}/2$.
55 Specified between 2.5% and 97.5% of the full-scale range.
56 Calculated from the line of best fit of all the measured codes.
57 Measured at dc.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Vocoder Section Performance					
Sample Rate		–	8	–	ks/s
Data Rate (with FEC)		–	3600	–	bps
Data Rate (without FEC)		–	2400	–	bps
Lower Frequency Limit (internally bandlimited)		60	–	–	Hz
Upper Frequency Limit (internally bandlimited)		–	–	3900	Hz
Encoder Algorithmic Delay	72	–	–	20	ms
Decoder Algorithmic Delay	72	–	–	12	ms
Output Load Impedance (OUTP)		32	–	–	Ω
Output Voltage Range (OUTP)	73	–	–	10 to 90	% AV_{DD}
ADC SINAD	69, 70	–	86	–	dB
DAC SINAD	69, 71	–	80	–	dB

Notes:

69 Internal gain settings are 0dB on input gain for the optimum vocoded level and +6dB on output gain for the optimum vocoded level, subject to further characterisation.

70 The internal ADC is a sigma-delta type which samples at 2.4MHz. It is important that there is no significant energy close to this frequency or at any of its harmonics, thus avoiding the need for an external low-pass anti-alias filter.

71 The internal DAC is a sigma-delta type which samples at 2.4MHz. It will output energy at this frequency and its harmonics. Should this present a problem, it is suggested that some external filtering be used at the audio outputs.

72 Excludes the 20/40/60/80 ms sample collection period.

73 Measured whilst driving a 600Ω resistive load to $AV_{SS.}$

9.1.4 Parametric Performance

Details in this section represent design target values and are not currently guaranteed.

For the following conditions unless otherwise specified:

External components as recommended in Figure 2 and Table 2.
Reference clock frequency = 19.2MHz ±0.01% (100ppm); Tamb = –40°C to +85°C.
AV_{DD} = DV_{DD} = 3.0V to 3.6V; DV_{CORE} = 1.7V to 1.9V; V_{DEC} = 2.5V; V_{BIAS} = AV_{DD}/2.
Reference Signal Level = 308mVrms at 1kHz with AV_{DD} = 3.3V.
Signal levels track with supply voltage, so scale accordingly.
Signal to Noise Ratio (SNR) in bit rate bandwidth.
Input stage gain = 0dB. Output stage attenuation = 0dB. Maximum load on digital outputs = 30pF.

All figures quoted in this section apply to the device when loaded with 8341 FI-1.x only.
The use of other Function Images, can modify the parametric performance of the device.

dPMR Modem	Notes	Min.	Typ.	Max.	Unit
Modem Symbol Rate		2400	–	4800	symbols /sec
Modulation			4FSK		
Filter (RC) Alpha		–	0.2	–	
Tx Output Level (MOD1, MOD2, 2-point)	75	–	2.88	–	Vpk-pk
Tx Output Level (MOD1, MOD2, I/Q)	75	–	2.20	–	Vpk-pk
Tx Adjacent Channel Power (MOD1, MOD2, prbs)	76, 78	-60	–	–	dB
Rx Sensitivity (BER 4800 symbols/sec)	77	–	TBD	–	dBm
Rx Co-channel Rejection	76, 78	15	12	–	dB
Rx Input Level	79	35.4	–	838	mVrms
Rx Input DC Offset		0.5	–	AV_{DD} - 0.5	V

Notes:

75 Transmitting continuous default preamble.
76 See data sheet section 8.13.
77 Measured at baseband – radio design will affect ultimate product performance.
78 For a 6.25kHz/4800bps channel.
79 Measured at DISCFB pin for continuous preamble.

Audio Performance	Notes	Min.	Typ.	Max.	Unit
Audio Compandor					
Attack Time		–	4.0	–	ms
Decay Time		–	13	–	ms
0dB-point	82	–	100	–	mVrms
Compression/Expansion Ratio		–	2:1	–	
Inband Tone Encoder					
Frequency Range		288	–	3000	Hz
Tone Frequency Accuracy		–	–	±0.3	%
Tone Amplitude Tolerance	81	–1.0	0	+1.0	dB
Total Harmonic Distortion	80	–	2.0	4.0	%
Analogue Channel Audio Filtering					
Pass-band (nominal bandwidth):					
12.5kHz Channel	83	300	–	2550	Hz
25kHz Channel	83	300	–	3000	Hz

Audio Performance	Notes	Min.	Typ.	Max.	Unit
Pass-band Gain (at 1.0kHz)		–	0	–	dB
Pass-band Ripple (wrt gain at 1.0kHz)		–2.0	0	+0.5	dB
Stop-band Attenuation		33.0	–	–	dB
Residual Hum and Noise Tx	84	–	–47	–	dBm
Residual Hum and Noise Rx	84	–	–74	–	dBm
Pre-emphasis	83	–	+6	–	dB/oct
De-emphasis	83	–	–6	–	dB/oct
Audio Scrambler					
Inversion Frequency		–	3300	–	Hz
Pass-band		320	–	2900	Hz
Audio Expandor					
Input Signal Range	85	–	–	0.55	Vrms

Notes:

80 Measured at MOD 1 or MOD 2 output.

81 AV_{DD} = 3.3V and Tx Audio Level set to 871mV p-p (308mVrms).

82 AV_{DD} = 3.3V.

83 See Figure 12 and Figure 13

84 Psophometrically weighted. Pre/de-emphasis, Compandor and 25kHz channel filter selected.

85 AV_{DD} = 3.3V.

9.2 Operating Characteristics – Timing Diagrams

9.2.1 C-BUS Timing

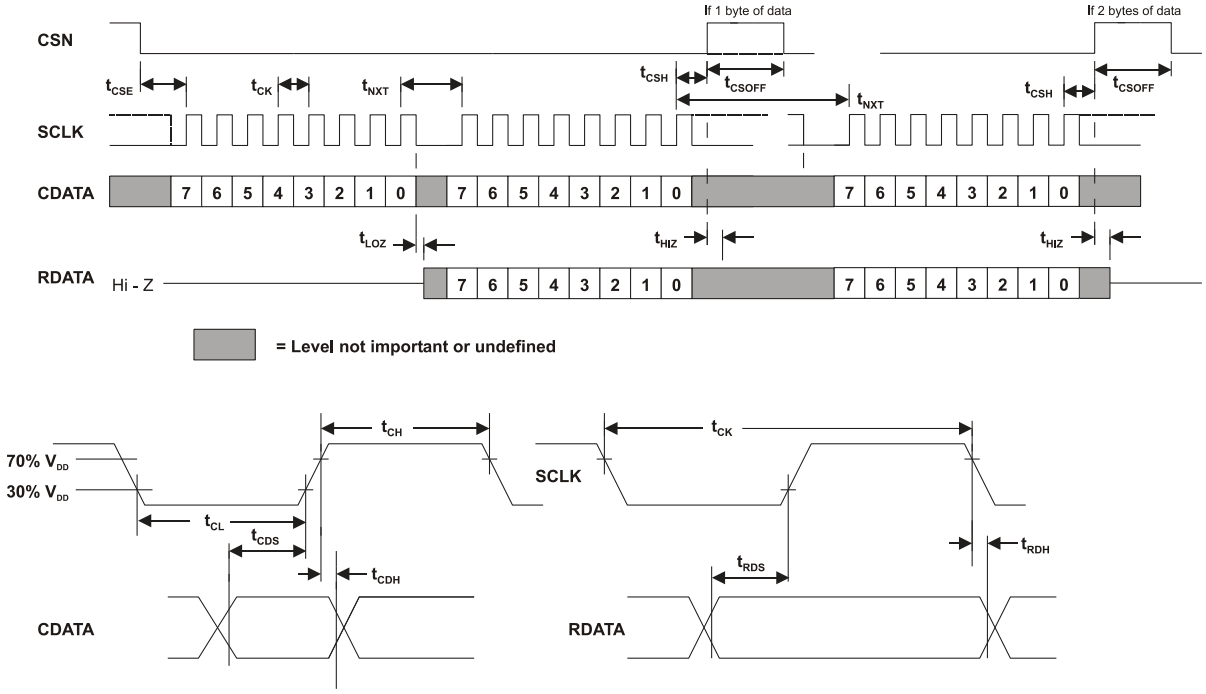


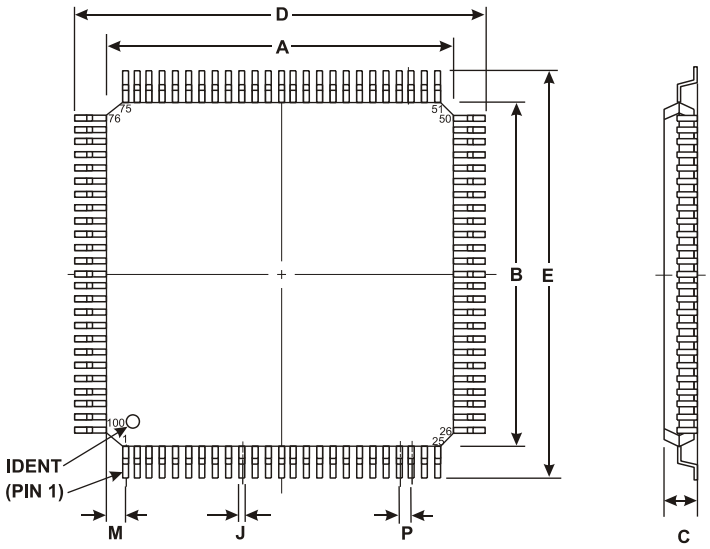
Figure 27 C-BUS Timing

C-BUS Timing		Notes	Min.	Typ.	Max.	Unit
t_{CSE}	CSN Enable to SCLK high time		100	–	–	ns
t_{CSH}	Last SCLK high to CSN high time		100	–	–	ns
t_{LOZ}	SCLK low to RDATA Output Enable Time		0.0	–	–	ns
t_{HIZ}	CSN high to RDATA high impedance		–	–	1.0	µs
t_{CSOFF}	CSN high time between transactions		1.0	–	–	µs
t_{NXT}	Inter-byte time		200	–	–	ns
t_{CK}	SCLK cycle time		200	–	–	ns
t_{CH}	SCLK high time		100	–	–	ns
t_{CL}	SCLK low time		100	–	–	ns
t_{CDS}	CDATA setup time		75	–	–	ns
t_{CDH}	CDATA hold time		25	–	–	ns
t_{RDS}	RDATA setup time		50	–	–	ns
t_{RDH}	RDATA hold time		0	–	–	ns
	C-BUS Latency		–	250	–	µs

Notes: 1. Depending on the command, 1 or 2 bytes of CDATA are transmitted to the peripheral MSB (bit 7) first, LSB (bit 0) last. RDATA is read from the peripheral MSB (bit 7) first, LSB (bit 0) last.
2. Data is clocked into the peripheral on the rising SCLK edge.
3. Commands are acted upon between the last rising edge of SCLK of each command and the rising edge of the CSN signal.
4. To allow for differing µC serial interface formats C-BUS compatible ICs are able to work with SCLK pulses starting and ending at either polarity.
5. Maximum 30pF load on IRQN pin and each C-BUS interface line.

These timings are for the latest version of C-BUS and allow faster transfers than the original C-BUS timing specification. The CMX8341 can be used in conjunction with devices that comply with the slower timings, subject to system throughput constraints.

9.3 Packaging



	DIM.	MIN.	TYP.	MAX.
*	A	13.8		14.2
*	B	13.8		14.2
	C	1.40		1.60
	D	15.8		16.2
	E	15.8		16.2
	H	0.05		0.15
	J	0.17		0.27
	L	0.45		0.75
	M		1.00	
	P		0.50	
	T	0.09		0.20
	X	0°		7°

NOTES : All dimensions in mm

Angles in degrees

* A & B are reference data and do not include mold deflash or protrusions.

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition

Co-Planarity of leads within 0.1mm

Figure 28 L8 Mechanical Outline: *Order as part no. CMX8341L8*

About *FirmASIC*®

CML's proprietary *FirmASIC*® component technology reduces cost, time to market and development risk, with increased flexibility for the designer and end application. *FirmASIC*® combines Analogue, Digital, Firmware and Memory technologies in a single silicon platform that can be focused to deliver the right feature mix, performance and price for a target application family. Specific functions of a *FirmASIC*® device are determined by uploading its Function Image™ during device initialization. New Function Images™ may be later provided to supplement and enhance device functions, expanding or modifying end-product features without the need for expensive and time-consuming design changes. *FirmASIC*® devices provide significant time to market and commercial benefits over Custom ASIC, Structured ASIC, FPGA and DSP solutions. They may also be exclusively customised where security or intellectual property issues prevent the use of Application Specific Standard Products (ASSP's).

Handling precautions: This product includes input protection, however, precautions should be taken to prevent device damage from electro-static discharge. CML does not assume any responsibility for the use of any circuitry described. No IPR or circuit patent licences are implied. CML reserves the right at any time without notice to change the said circuitry and this product specification. CML has a policy of testing every product shipped using calibrated test equipment to ensure compliance with this product specification. Specific testing of all circuit parameters is not necessarily performed.

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