CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CMX885

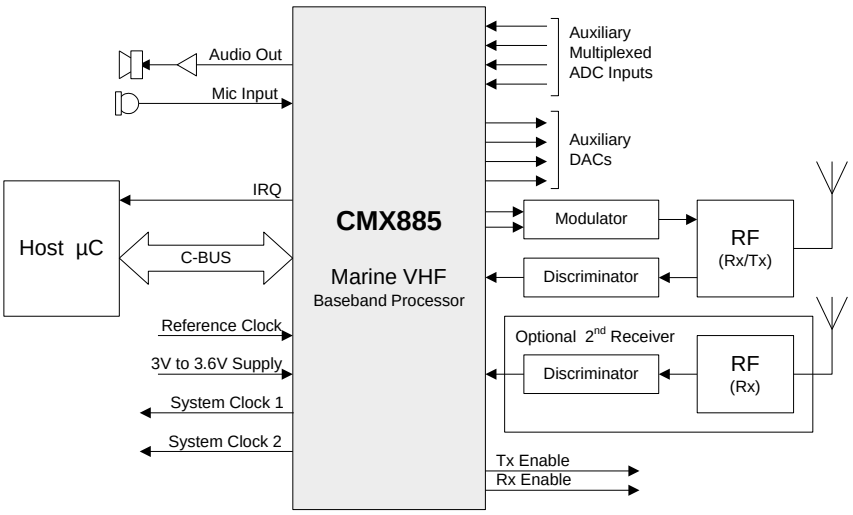
Marine VHF Audio and Signalling Processor

D/885/4 June 2017

Audio and Signalling Processing, DTMF, DSC/ATIS and NOAA with Auxiliary Functions for use in Marine VHF Systems

Features

- **Concurrent Audio/Signalling/Data Operations**
- **Complete Audio-band Processing:**
  - **Selectable Audio Processing Order**
  - **Pre and De-emphasis**
  - **Selectable 2.55/3.0 kHz Filtering**
  - **Limiter**
- **DSC/ATIS Modem for Marine Applications**
- **Programmable Voice Scrambler**
- **Inband Signalling: DTMF, NOAA NWR**
- **C-BUS Serial Interface to Host µController**
- **DTMF and Audio Tone Encoder/Decoder**
- **Small VQFN and LQFP Packages**
- **Dual Auxiliary ADC, 4 Multiplexed Inputs**
- **4 x Auxiliary DACs**
- **Dual Programmable System Clock Outputs**
- **Tx Outputs for Single, Two-Point Modulation**
- **3 x Analogue Inputs (Mic or Discriminator)**
- **Digital Gain Adjustment**
- **Default 3.6864MHz Xtal/Clock**
- **Flexible Powersave Modes**
- **Low-power 3.0V to 3.6V Operation**



1 Brief Description

The CMX885 is a half-duplex, audio, signalling and data processing IC for use in Marine VHF radio systems.

Comprehensive audio processing facilities include complete audio processing, filtering, pre- or de-emphasis and frequency inversion scrambling. Signal routing and filtering is included to assist host µC based signal encoding/decoding applications.

1200bps Digital Selcall (DSC) or Automatic Transmitter Identification System (ATIS) modem with protocol support and NWR decoding are supported.

A DTMF encoder/decoder, a full complement of auxiliary ADCs and DACs and dual synthesised clock outputs are included in this low power PMR processor. The device also has flexible powersaving modes and is available in 48-pin VQFN and LQFP packages.

CONTENTS

Table Page

Figure Page

It is always recommended that you check for the latest product datasheet version from the CML website: [www.cmlmicro.com].

1.1 History

Version	Changes	Date
4	• Figure 1 (Block Diagram): 'Voice Filter' corrected to '300Hz Filter' in Tx audio processing • Section 8.1.18: Removed statement regarding illegal setting of b3 and b2 at the same time • Section 8.2.5: Description for $C8 (P4.9) rewritten and Figure 16-18 updated to improve clarity for default and preferred options for Tx audio filter line-ups • Section 8.2.5: Figure 16 is updated and removed CTCSS input that was previously incorrectly included • Section 7.13.1: Maximum allowable input signal at MICFB pin corrected to 54mV pk-pk (previously stated as 54mV rms) • Section 8.1.27: Table 6 added, providing output 1 and 2 fine gain figures • Section 8.2.5: $C8, P4.2-P4.3: Table added, providing output 1 and 2 fine gain figures • Section 7.6: DCS corrected to DSC • Section 9.1.3: AuxSYSCLK 1 and 2 output timing data added • Section 7.1: Device ident code ($8850) added to description • Section 8.1.27: Description of audio tone level adjustment enhanced by additional text and added examples • Section 8.2.4: Default values of P3.8, P3.9 and P3.10 shown as reserved, do not change • Section 8.1.10: Added recommendation to introduce a period of >700µs between enabling Tx mode and enabling Tx function • Section 8.1.14: Added AuxADC2 reference to b15 description • Section 7.5.1: Footnote added concerning use of an audio scrambler	16/06/17
3	• Clarified operation of Data End bit (b7) for DSC Rx mode in section 8.1.22. • Clarified the need for observing C-BUS latency when writing multiple C-BUS commands in section 7.3. • Minor typographical corrections in table of section 8.1.27, P4.10 and P4.11 values in section 8.2.5.	20/12/2010
2	• Changed "Modem Control" to "Modem Cofiguration" register • Bit references changed to "$C1:b12" style, for consistency • Changed name of $C1:b2 to "Modem Enable" and $C!:b4 to "Modem Source" • Deleted other references to "processing" in the description of $C1 register bits • Deleted the reference to "clearing the En_DSC bit" at the end of section 7.7.1 • Xtal frequency tolerance in section 9.1.4 changed from 100ppm to 30ppm, to meet DSC specifications. • Corrected DAC3 to DAC4 in figure 1. • +1dB and 3dB limits apply to all Rx and Tx responses (figures 6 to 10). Wording changed accordingly in section 7.5. • "write" added to description of Audio Tone register ($CD) in section 7.6. • Reference in $C1 to bits 11-9 should read 11-8 in section 7.6. • Program Block registers P3.2 to P3.6 should read P3.2 - P3.7 in section 7.11.1. • GPIO RXENA and TXENA signals - nomenclature standardised in section 7.12. • Hyperlink added for $C1 in section 8.1. • Correction of $C0 b6 to "BIAS Block Enable" in section 8.1.17. • Merge table rows for $CE b9 in section 8.1.28. • Removed references to MSK: these should be DSC in sections 7.7.1 and 7.7.2. • Clarification of Status register bit 3, Modem Control register bits 3-8 and bit 11, Interrupt Mask register bits 3 and 5. • Footnotes in Parametric Specifications harmonised with table references. • Minor typographical corrections.	8/4/2010
1	• This document created – based on 7041FI-1.x documentation	18/9/2009

2 Block Diagram

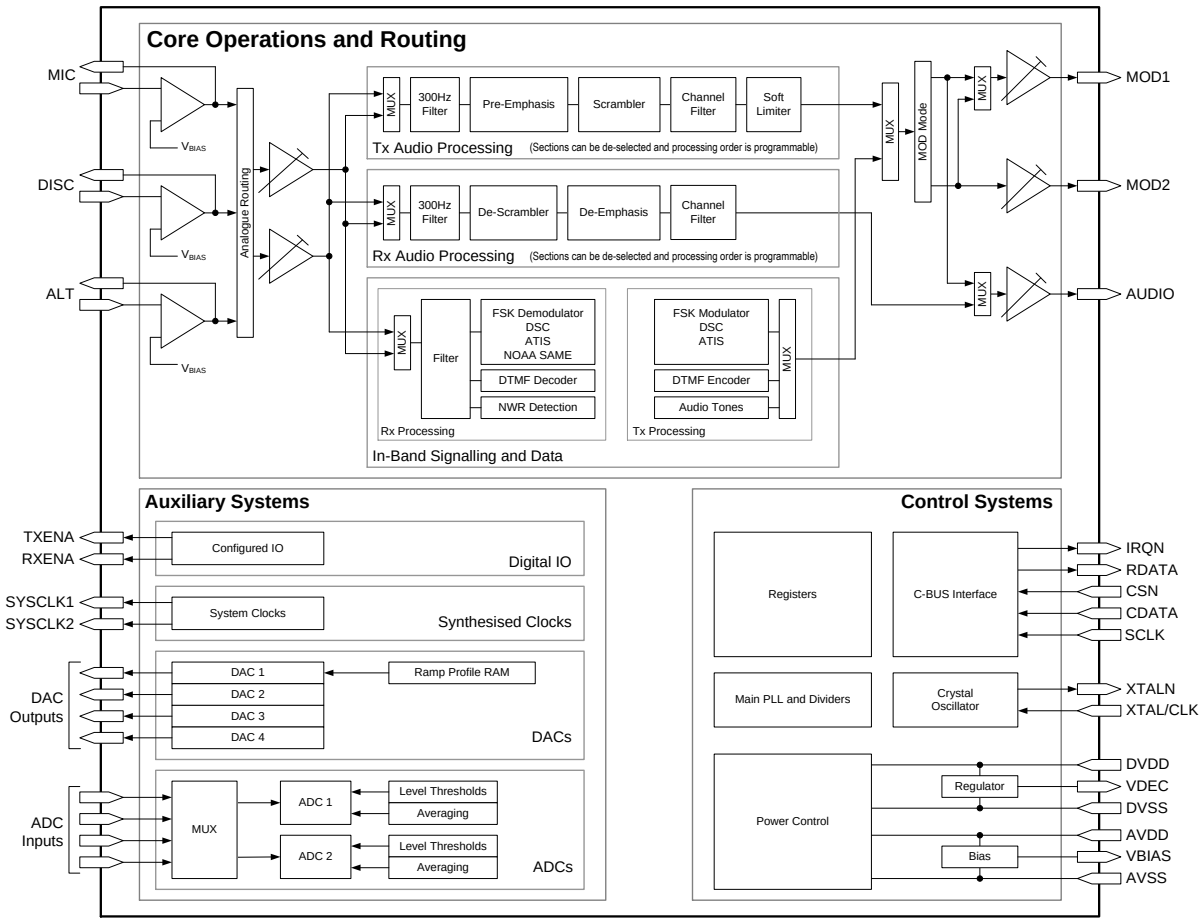


Figure 1 Block Diagram

3 Signal and Pin List

48-pin L4/Q3	Pin Name	Type	Description
1	-	NC	reserved – leave unconnected
2	-	NC	reserved – leave unconnected
3	-	NC	reserved – leave unconnected
4	-	NC	reserved – leave unconnected
5	-	NC	reserved – leave unconnected
6	-	NC	reserved – leave unconnected
7	DVSS	PWR	Digital Ground
8	IRQN	OP	C-BUS: A 'wire-ORable' output for connection to the Interrupt Request input of the host. Pulled down to DV_{SS} when active and is high impedance when inactive. An external pull-up resistor (R1) is required.
9	VDEC	PWR	Internally generated 2.5V digital supply voltage. Must be decoupled to DV_{SS} by capacitors mounted close to the device pins. No other connections allowed.
10	RXENA	OP	Rx Enable – active low when in Rx mode ($C1:b0 = 1)
11	-	NC	reserved – leave unconnected
12	-	NC	reserved – leave unconnected
13	SYSCLK1	OP	Synthesised Digital System Clock Output 1
14	DVSS	PWR	Digital Ground
15	TXENA	OP	Tx Enable – active low when in Tx mode ($C1:b1 = 1)
16	DISCN	IP	Discriminator inverting input
17	DISCFB	OP	Discriminator input amplifier feedback
18	ALTN	IP	ALT inverting input
19	ALTFB	OP	ALT input amplifier feedback
20	MICFB	OP	MIC input amplifier feedback
21	MICN	IP	MIC inverting input
22	AVSS	PWR	Analogue Ground
23	MOD1	OP	Modulator 1 output
24	MOD2	OP	Modulator 2 output
25	VBIAS	OP	Internally generated bias voltage of about $AV_{DD}/2$, except when the device is in 'Powersave' mode when V_{BIAS} will discharge to AV_{SS}. Must be decoupled to AV_{SS} by a capacitor mounted close to the device pins. No other connections allowed.
26	AUDIO	OP	Audio output
27	ADC1	IP	Auxiliary ADC input (1)
28	ADC2	IP	Auxiliary ADC input (2)
29	ADC3	IP	Auxiliary ADC input (3)

48-pin L4/Q3	Pin Name	Type	Description
30	ADC4	IP	Auxiliary ADC input (4)
31	AVDD	PWR	Positive 3.3V supply rail for the analogue on-chip circuits. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to AV_{SS} by capacitors mounted close to the device pins.
32	DAC1	OP	Auxiliary DAC output 1/RAMDAC
33	DAC2	OP	Auxiliary DAC output 2
34	AVSS	PWR	Analogue Ground
35	DAC3	OP	Auxiliary DAC output 3
36	DAC4	OP	Auxiliary DAC output 4
37	DVSS	PWR	Digital Ground
38	VDEC	PWR	Internally generated 2.5V supply voltage. Must be decoupled to DV_{SS} by capacitors mounted close to the device pins. No other connections allowed.
39	XTAL/CLK	IP	Input to the oscillator inverter from the Xtal circuit or external clock source.
40	XTALN	OP	The output of the on-chip Xtal oscillator inverter
41	DVDD	PWR	The 3.3V positive supply rail for the digital on-chip circuits. This pin should be decoupled to DVss by capacitors mounted close to the device pins
42	CDATA	IP	C-BUS: Serial data input from the µC
43	RDATA	TS OP	C-BUS: A 3-state C-BUS serial data output to the µC. This output is high impedance when not sending data to the µC.
44	-	NC	Reserved – do not connect this pin
45	DVSS	PWR	Digital Ground
46	SCLK	IP	C-BUS: The C-BUS serial clock input from the µC
47	SYSCLK2	OP	Synthesised Digital System Clock Output 2
48	CSN	IP	C-BUS: The C-BUS chip select input from the µC - there is no internal pullup on this input
EXPOSED METAL PAD	SUBSTRATE	~	On this device, the central metal pad (which is exposed on Q3 packages only) may be electrically unconnected or, alternatively, may be connected to Analogue Ground (AVss). **No other electrical connections are permitted.**

Notes:
IP = Input (+ PU/PD = internal pullup/pulldown resistor)
OP = Output
BI = Bidirectional
TS OP = 3-state Output
PWR = Power Connection
NC = No Connection - should NOT be connected to any signal

3.1 Signal Definitions

Table 1 Definition of Power Supply and Reference Voltages

Signal Name	Pins	Usage
AV_{DD}	AVDD	Power supply for analogue circuits
DV_{DD}	DVDD	Power supply for digital circuits
V_{DEC}	VDEC	Power supply for core logic, derived from DV_{DD} by on-chip regulator
V_{BIAS}	VBIAS	Internal analogue reference level, derived from AV_{DD}
AV_{SS}	AVSS	Ground for all analogue circuits
DV_{SS}	DVSS	Ground for all digital circuits

4 External Components

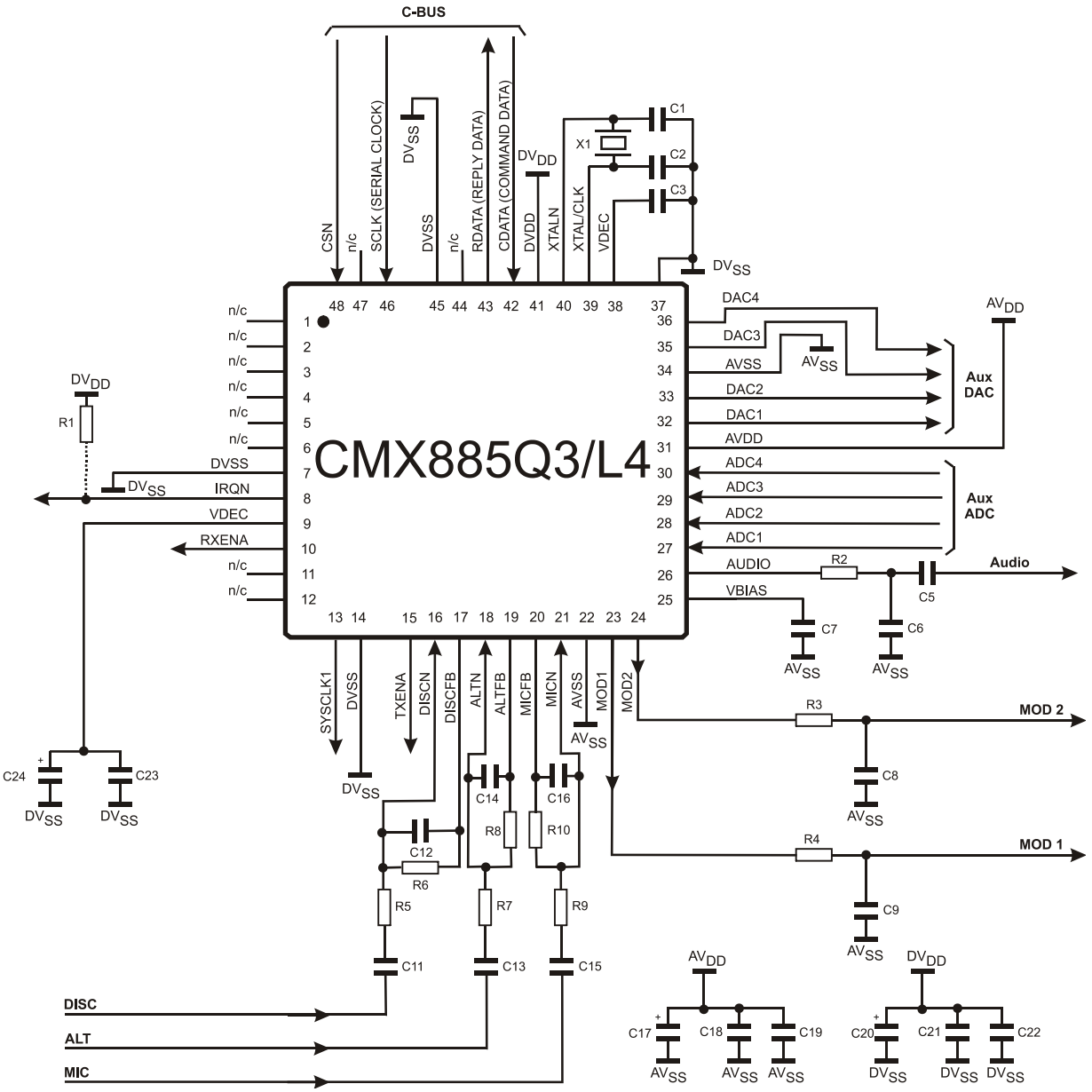


Figure 2 Recommended External Components

R1	100kΩ	C1	18pF	C11	See note 5	C21	10nF
R2	100kΩ	C2	18pF	C12	180pF	C22	10nF
R3	100kΩ	C3	10nF	C13	See note 5	C23	10nF
R4	100kΩ	C4	*not used*	C14	180pF	C24	10µF
R5	See note 2	C5	1nF	C15	See note 5		
R6	100kΩ	C6	100pF	C16	180pF		
R7	See note 3	C7	100nF	C17	10µF		
R8	100kΩ	C8	100pF	C18	10nF	X1	3.6864MHz
R9	See note 4	C9	100pF	C19	10nF		See note 1
R10	100kΩ	C10	*not used*	C20	10µF		

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated.

Notes:

1. X1 can be a crystal or an external clock generator; this will depend on the application. The tracks between the crystal and the device pins should be as short as possible to achieve maximum stability and best start up performance. By default, a 3.6864MHz clock is selected, other values could be used if the various internal clock dividers are set to appropriate values.

2. R5 should be selected to provide the desired dc gain (assuming C11 is not present) of the DISCN input, as follows:

$$|GAIN_{DISCN}| = 100k\Omega / R5$$

   The gain should be such that the resultant output at the DISCFB pin is within the input signal range specified in 7.13.2.

3. R7 should be selected to provide the desired dc gain (assuming C13 is not present) of the ALTN input as follows:

$$|GAIN_{ALTN}| = 100k\Omega / R7$$

   The gain should be such that the resultant output at the ALTFB pin is within the input signal range specified in 7.13.

4. R9 should be selected to provide the desired dc gain (assuming C15 is not present) of the MICN input as follows:

$$|GAIN_{MICN}| = 100k\Omega / R9$$

   The gain should be such that the resultant output at the MICFB pin is within the input signal range specified in 7.13.1. For optimum performance with low signal microphones, an additional external gain stage may be required.

5. C11, C13 and C15 should be selected to maintain the lower frequency roll-off of the MICN, ALTN and DISCN inputs as follows:

$$C11 \geq 100nF \times |GAIN_{DISCN}|$$

$$C13 \geq 100nF \times |GAIN_{ALTN}|$$

$$C15 \geq 30nF \times |GAIN_{MICN}|$$

6. ALTN and ALTFB connections allow the user to have an additional signal input. Component connections and values are as for the respective DISCN and MICN networks. If this input is not required, the ALTN pin should be connected to AVss.

7. C5 (AUDIO output) should be increased to 1.0µF if frequencies below 300Hz need to be used on this pin.

8. A single 10µF electrolytic capacitor (C24, fitted as shown) may be used for smoothing the power supply to both VDEC pins, providing they are connected together on the pcb with an adequate width power supply trace. Alternatively, separate smoothing capacitors should be connected to each VDEC pin. High frequency decoupling capacitors (C3 and C23) must always be fitted as close as possible to both VDEC pins.

5 PCB Layout Guidelines and Power Supply Decoupling

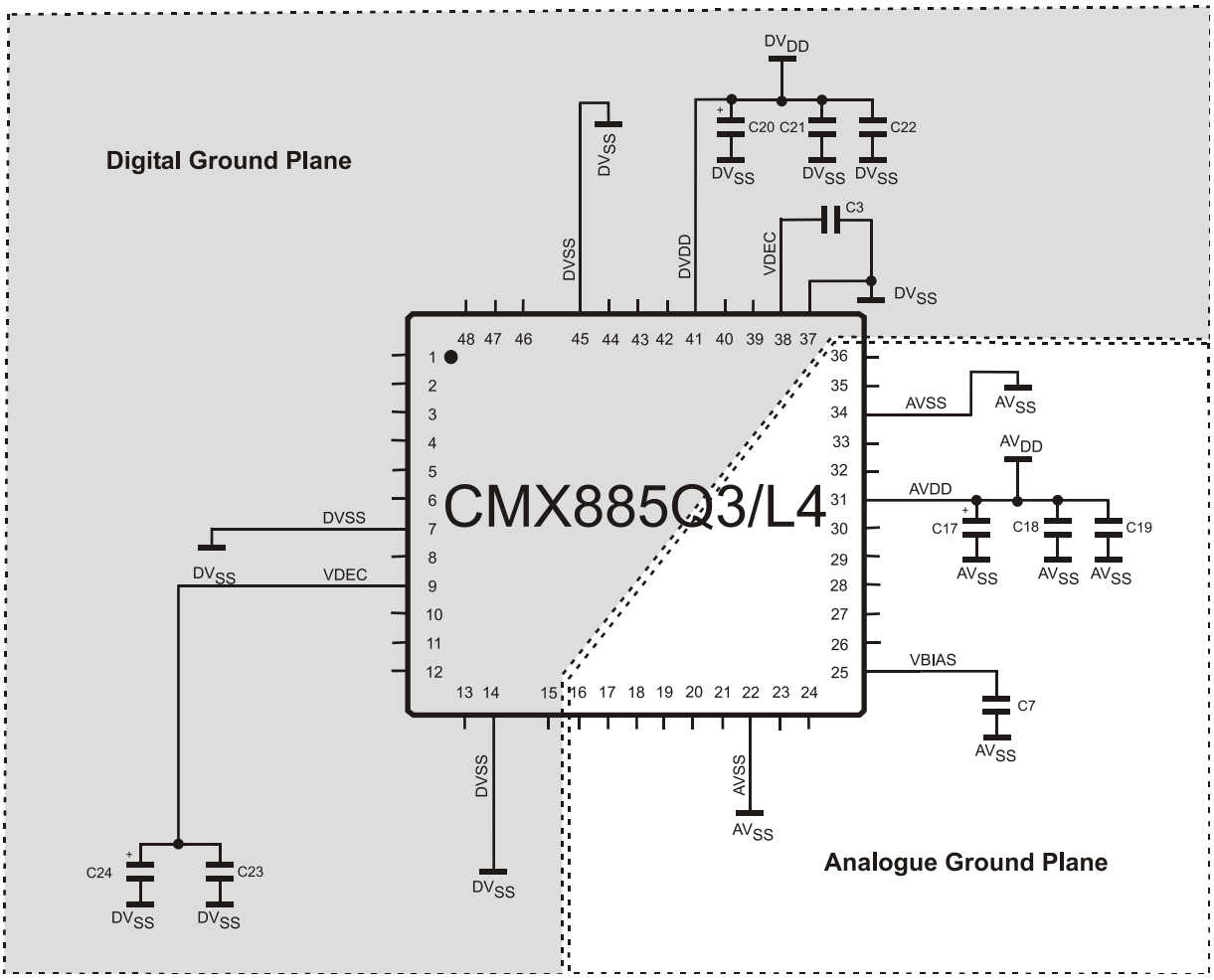


Figure 3 Power Supply and De-coupling

Component Values as per Figure 2.

Notes:

It is important to protect the analogue pins from extraneous inband noise and to minimise the impedance between the device and the supply and bias de-coupling capacitors. The de-coupling capacitors C3, C7, C18, C19, C21, C22, C24 and C25 should be as close as possible to the device. It is therefore recommended that the printed circuit board is laid out with separate ground planes for the AV_{SS} and DV_{SS} supplies in the area of the CMX885, with provision to make links between them, close to the device. Use of a multi-layer printed circuit board will facilitate the provision of ground planes on separate layers.

V_{BIAS} is used as an internal reference for detecting and generating the various analogue signals. It must be carefully decoupled, to ensure its integrity, so apart from the decoupling capacitor shown, no other loads should be connected. If V_{BIAS} needs to be used to set the discriminator mid-point reference, it must be buffered with a high input impedance buffer.

The single-ended microphone input and audio output must be ac coupled (as shown), so that their return paths can be connected to AV_{SS} without introducing dc offsets. Further buffering of the audio output is advised.

The crystal X1 may be replaced with an external clock source.

6 General Description

The CMX885 is intended for use in half duplex analogue two-way mobile radio equipment and is particularly suited to the Marine VHF band. The CMX885 provides signal filtering, encoder and decoder functions for audio, inband tones, DTMF, NWR and DSC/ATIS, permitting simple to sophisticated levels of tone control and data transfer. A flexible power control facility allows the device to be placed in its optimum powersave mode when not actively processing signals.

The CMX885 includes a crystal clock generator, with a buffered output, to provide a common system clock if required. A block diagram of the CMX885 is shown in Figure 1.

The signal processing blocks can be individually assigned to either of two signal processing paths, which in turn, can be routed from any of the three audio/discriminator input pins. This allows for a very flexible routing architecture and allows the facility for different processing blocks to act on different analogue inputs.

For Marine use, it would be typical to route Rx Audio from the working channel receiver through from the DISCN input, while at the same time routing the DSC/ATIS FSK modem from the DSC channel 70 receiver from the ALTN input.

Tx Functions:

- Single/dual microphone inputs with input amplifier and programmable gain adjustment
- Filtering selectable for 12.5kHz and 25kHz channels
- Selectable pre-emphasis
- Selectable frequency inversion voice scrambling
- Selectable audio processing order
- Two-point modulation outputs with programmable level adjustment
- Programmable audio tone generator (for custom audio tones)
- Programmable DTMF generator
- Tx Enable output
- 1200bps FSK modem for DSC/ATIS use (to ITU-R M.493-11)

Rx Functions:

- Single/dual demodulator inputs with input amplifier and programmable gain adjustment
- Audio-band and sub-audio rejection filtering
- Selectable de-emphasis
- Selectable frequency inversion voice de-scrambling
- Selectable audio processing order
- Software volume control
- DTMF decoder
- Rx Enable output
- 1200bps FSK modem for DSC/ATIS use (to ITU-R M.493-11)
- NWR SAME and WAT detector

Auxiliary Functions:

- 2 programmable system clock outputs
- 2 auxiliary ADCs with selectable input paths
- 4 auxiliary DACs, one with built-in programmable RAMDAC

Interface:

- C-BUS, 4 wire high speed synchronous serial command/data bus
- Open drain IRQ to host

7 Detailed Descriptions

7.1 Device Ident Code

Following a Power-on or Reset (see section 8.1.1), the device will report the Device Ident Code ($8850) in the Tone Status register ($CC) to indicate that it is operational.

7.2 Xtal Frequency

The CMX885 is designed to work with a Xtal of 3.6864MHz. If this default configuration is not used, then Program Block 3 (see section 8.2.4) should be loaded with the correct values to ensure that the device will work to specification with the user specified clock frequency. A table of common values can be found in Table 2. Note the maximum Xtal frequency is 12.288MHz, although an external clock source of up to 24.576MHz can be used.

The register values in Table 1 are shown in hex (however only the lower 10 bits are relevant), the default settings are shown in bold, and the settings which do not give an exact setting (but are within acceptable limits) are in italics. The new P3.2-3 settings take effect following the write to P3.3 (the settings in P3.4-7 are implemented on a change to Rx or Tx mode).

Table 2 Xtal/clock Frequency Settings for Program Block 3

Program Block			External Frequency Source (MHz)							
			3.6864	6.144	9.216	12.0	12.8	16.368	16.8	19.2
P3.2	Idle	GP Timer	**$01C**	$018	$018	$019	$019	*$018*	$019	$018
P3.3		VCO output and AUX clk divide	**$084**	$088	$08C	*$10F*	*$110*	*$095*	*$115*	$099
P3.4	Rx or Tx	Ref clk divide	**$030**	$040	$060	$07D	$0C8	$155	$15E	$0C8
P3.5		PLL clk divide	**$280**	$200	$200	$200	$300	$400	$400	$200
P3.6		VCO output and AUX clk divide	**$13C**	$140	$140	$140	$140	$140	$140	$140
P3.7		Internal ADC / DAC clk divide	**$008**	$008	$008	$008	$008	$008	$008	$008

7.3 Host Interface

A serial data interface (C-BUS) is used for command, status and data transfers between the CMX885 and the host µC; this interface is compatible with Microwire and SPI. Interrupt signals notify the host µC when a change in status has occurred and the µC should read the status register across the C-BUS and respond accordingly. Interrupts only occur if the appropriate mask bit has been set. See section 7.14.1.

The CMX885 will monitor the state of the C-BUS registers that the host has written to every 250µs (the C-BUS latency period) hence it is not advisable for the host to make successive writes to the same C-BUS register within this period.

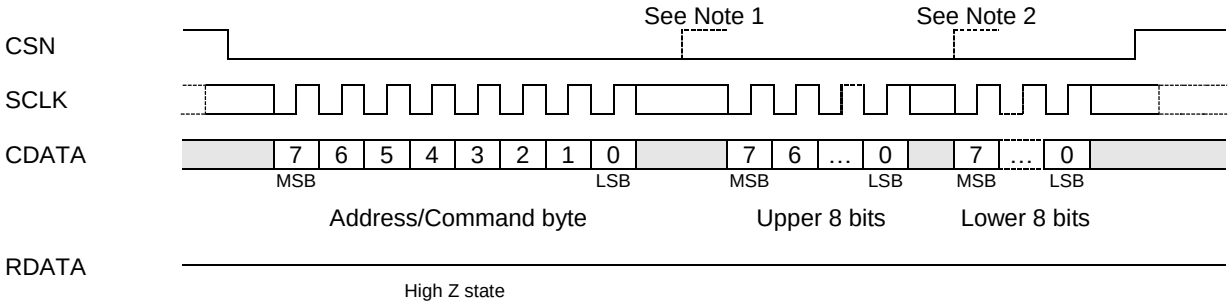
To minimise activity on the C-BUS interface, optimise response times and ensure reliable data transfers, it is advised that the IRQ facility be utilised (using the IRQ mask register, $CE). It is permissible for the host to poll the IRQ pin if the host µC does not support a fully interrupt-driven architecture. This removes the need to continually poll the C-BUS status register ($C6) for status changes.

The C-BUS block provides for the transfer of data and control or status information between the CMX885's internal registers and the host µC over the C-BUS serial interface. Each transaction consists of a single Address byte sent from the µC which may be followed by one or more Data byte(s) sent from the µC to be written into one of the CMX885's Write Only Registers, or one or more data byte(s) read out from one of the CMX885's Read Only Registers, as illustrated in Figure 4.

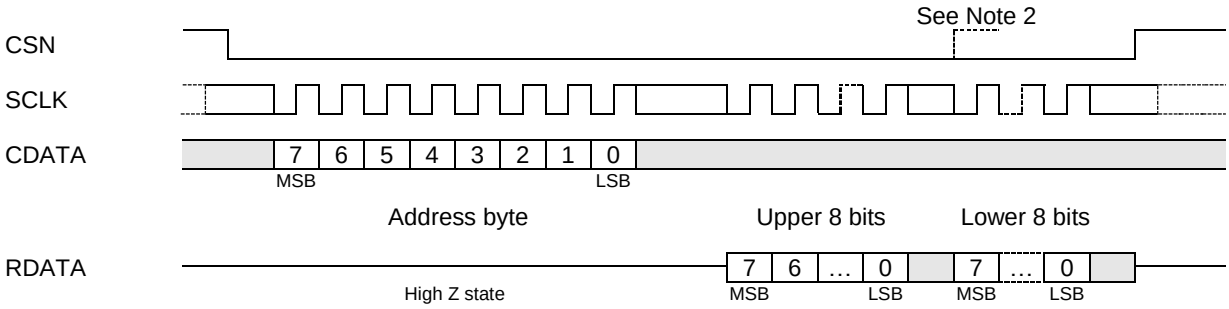
Data sent from the µC on the CDATA line is clocked into the CMX885 on the rising edge of the SCLK input. RDATA sent from the CMX885 to the µC is valid when SCLK is high. The CSN line must be held low during a data transfer and kept high between transfers. The C-BUS interface is compatible with most common µC serial interfaces and may also be easily implemented with general purpose µC I/O pins controlled by a simple software routine.

The number of data bytes following an Address byte is dependent on the value of the Address byte. The most significant bits of the address or data are sent first. For detailed timings see section 9.2. Note that, due to internal timing constraints, there may be a delay of up to 250µs between the end of a C-BUS write operation and the device reading the data from its internal register. Ensure that this C-BUS latency time (up to 250µs) is observed when writing multiple commands to the same C-BUS register.

C-BUS Write:



C-BUS Read:



Data value unimportant

Repeated cycles

Either logic level valid (and may change)

Either logic level valid (but must not change from low to high)

Figure 4 C-BUS Transactions

Notes:

1. For Command byte transfers only the first 8 bits are transferred ($01 = Reset).
2. For single byte data transfers only the first 8 bits of the data are transferred.
3. The CDATA and RDATA lines are never active at the same time. The Address byte determines the data direction for each C-BUS transfer.
4. The SCLK input can be high or low at the start and end of each C-BUS transaction.
5. The gaps shown between each byte on the CDATA and RDATA lines in the above diagram are optional, the host may insert gaps or concatenate the data as required.

7.4 Device Control

The CMX885 can be set into many modes to suit the environment in which it is to be used. These modes are described in the following sections and are programmed over the C-BUS: either directly to operational registers or, for parameters that are not likely to change during operation, via the Programming register ($C8).

For basic operation:

1. Enable the relevant hardware sections via the Power Down Control register
2. Set the appropriate mode registers to the desired state (Audio, Inband, Data, etc.)
3. Select the required Signal Routing and Gain
4. Use the Mode Control register to place the device into Rx or Tx mode

To conserve power when the device is not actively processing an analogue signal, place the device into Idle mode. Additional powersaving can be achieved by disabling the unused hardware blocks, however, care must be taken not to disturb any sections that are automatically controlled.

See:
- Powerdown Control – $C0 write
- Mode Control – $C1 write

7.4.1 Signal Routing

The CMX885 offers a very flexible routing architecture, with three signal inputs, two separate signal processing paths and two modulator outputs (to suit 2-point modulation schemes) and a single audio output. Each of the signalling processing blocks can be independently routed from either of the Input blocks, which can be routed from any of the three input signal pins. The audio/voice processing blocks are always routed from Input 1. The outputs from signal processing blocks are determined by the settings of the AuxADC and Tx MOD mode register in Tx mode.

See:
- Input Gain and Output Signal Routing – $B1 write
- AuxADC and Tx MOD Mode – $A7 write
- Mode Control – $C1 write

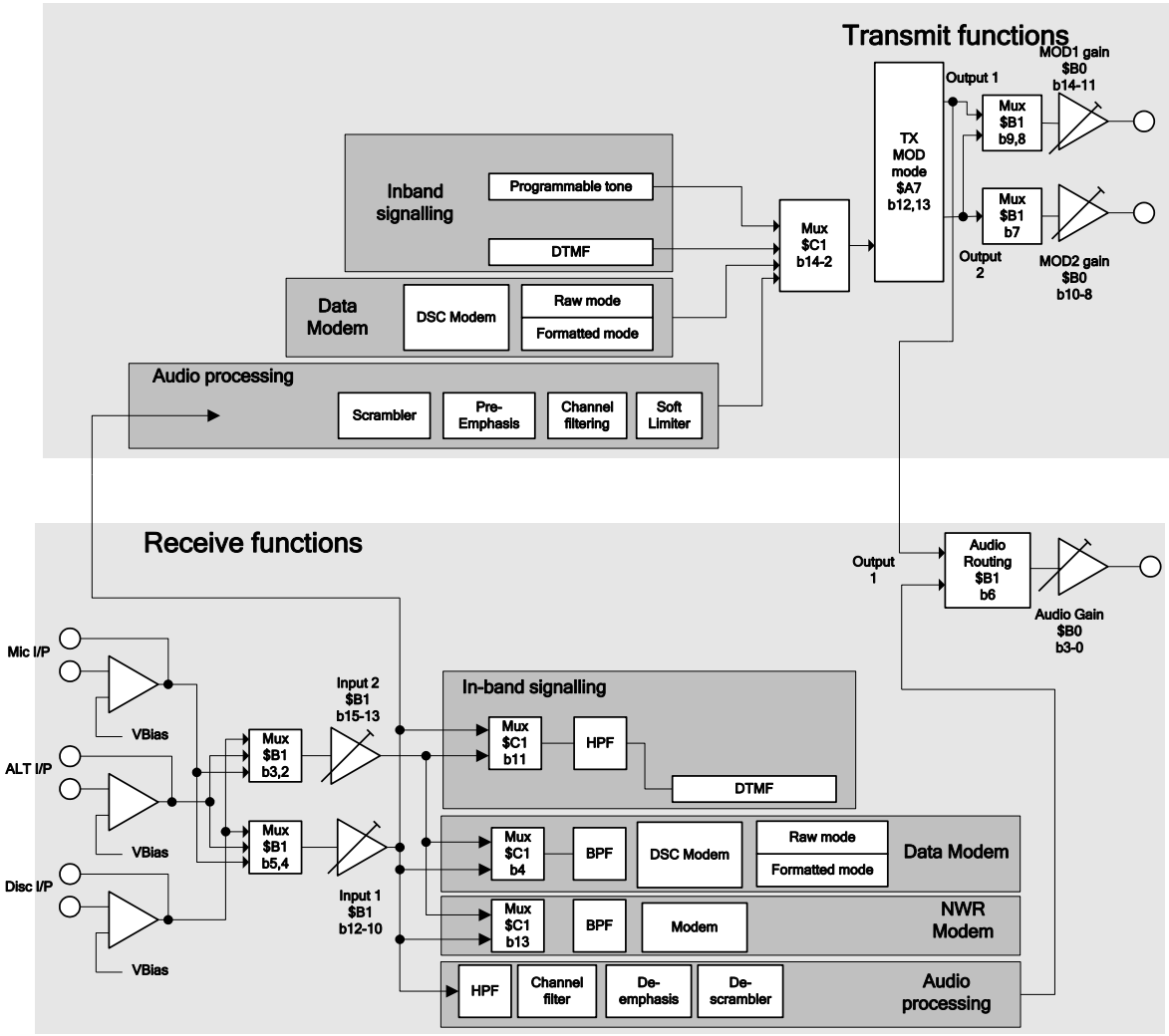


Figure 5 Signal Routing

The analogue gain/attenuation of each input and output can be set individually, with additional fine gain control available via the Programming register.

See:

- Analogue Output Gain – $B0 write
- Input Gain and Output Signal Routing – $B1 write

7.4.2 Mode Control

The CMX885 operates in one of three modes:

- Idle
- Rx
- Tx

At power-on or following a Reset, the device will automatically enter Idle mode, which allows for the maximum powersaving whilst still retaining the capability of monitoring the four ADC inputs (if enabled). It is only possible to write to the Programming register whilst in Idle mode.

See:

- Mode Control – $C1 write

7.5 Audio Functions

The audio signal can be processed in several ways, depending on the implementation required, by selecting the relevant bits in the Audio Control – $C2 write register. In both Rx and Tx modes, a selectable channel filter to suit either the 12.5kHz or 25kHz TIA/ETSI channel mask can be selected. This filter also incorporates a soft limiter to reduce the effects of over-modulation. Other features include pre- and de-emphasis, 300Hz HPF and frequency inversion scrambling, all of which may be individually enabled[1],[2]. The order in which these features are executed is selectable to ensure compatibility with existing implementations and provide optimal performance (see section 8.2.5).

7.5.1 Audio Receive Mode

The CMX885 operates in half duplex, so whilst in receive mode the transmit path (microphone input and modulator output amplifiers) can be disabled and powered down if required. The AUDIO output signal level is equalised (to V_{BIAS}) before switching between the audio port and the modulator ports, to minimise unwanted audible transients. The Off/Powersave level of the modulator outputs is the same as the VBIAS pin, so the audio output level must also be at this level before switching.

See:

- Audio Control – $C2 write

Receiving Audio Band Signals

When a voice-based signal is being received, it is up to the host µC, in response to signal status information provided by the CMX885, to control muting/enabling of the audio signal to the AUDIO output.

The discriminator path through the device has a programmable gain stage. Whilst in receive mode this should normally be set to 0dB (the default) gain.

Receive Filtering

The incoming signal is filtered, as shown in Figure 6 (with the 300Hz HPF also active), to remove sub-audio components and to minimise high frequency noise. When appropriate, the audio signal can then be routed to the AUDIO output. Separate selectable filters are available for:

- 300Hz High Pass
- 2.55kHz Low Pass (for 12.5kHz channel operation)
- 3.0kHz Low Pass (for 25kHz channel operation)

Note that with no filters selected, the low frequency response extends to below 5Hz at the low end but still rolls off above 3.3kHz at the top end. In Figure 6 and Figure 7, the template shows the +1 and -3dB limits.

[1] Use of an audio scrambler is not considered in the TIA/EIA standards and therefore this is regarded as an external process.

[2] The typical responses shown in Figure 6, Figure 7, Figure 8, Figure 9 were recorded using the PE0201 Evkit, DISC to AUDIO and MOD1 out.

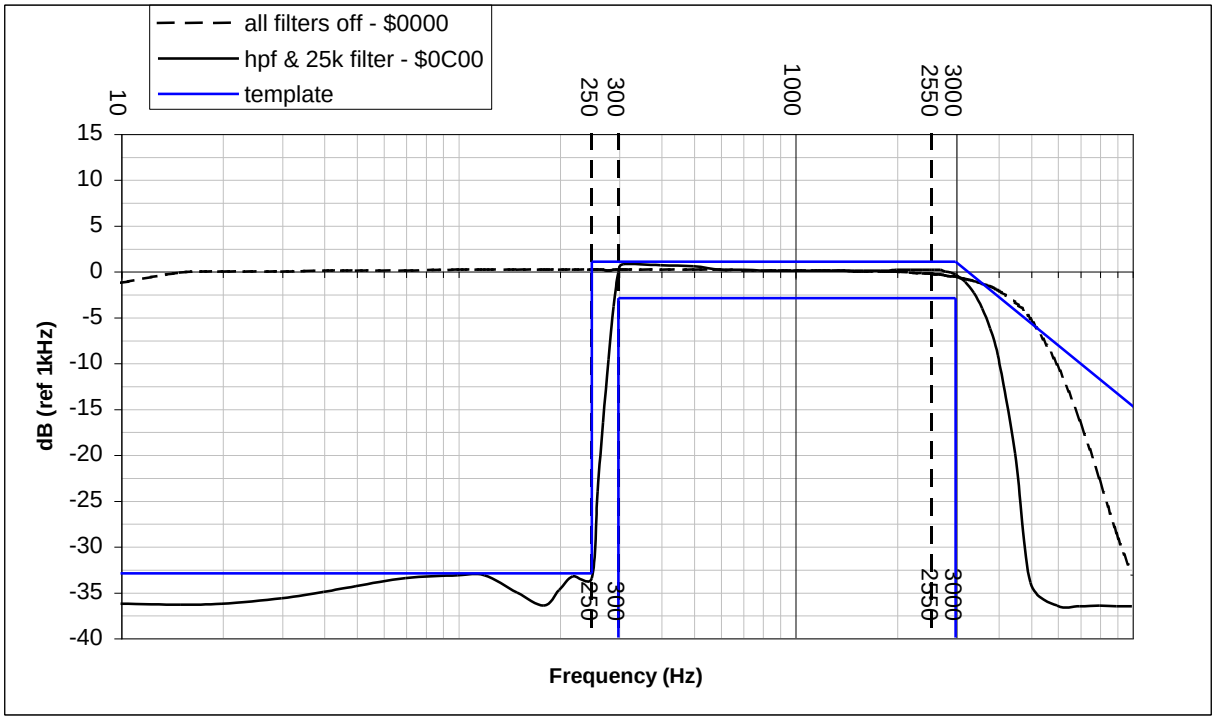


Figure 6 Rx 25kHz Channel Audio Filter Frequency Response

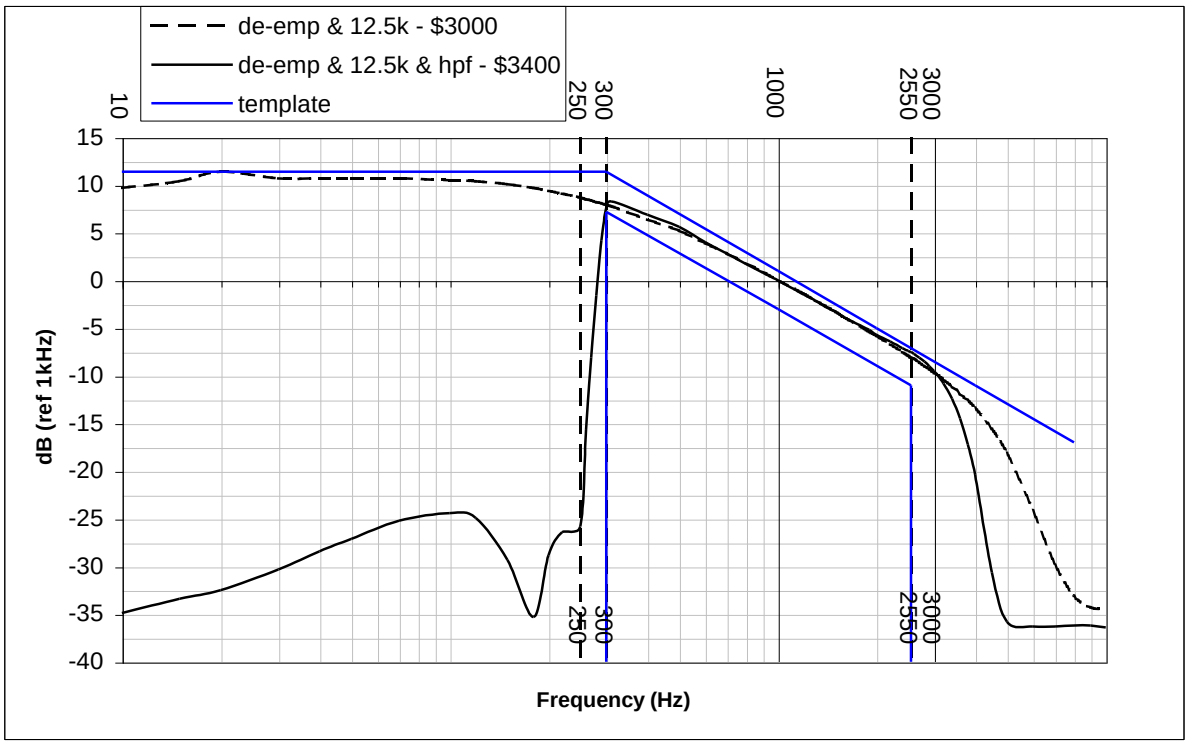


Figure 7 De-emphasis Curve for TIA/EIA-603 Compliance

De-emphasis
Optional de-emphasis at -6dB per octave from 300Hz to 3000Hz (shown in Figure 7) can be selected, to facilitate compliance with TIA/EIA-603, EN 300 086, EN 301 025.

Audio De-scrambling
The CMX885 incorporates an optional frequency inversion de-scrambler in receive mode. This de-scrambles received audio band signals that have been scrambled in the transmitter. The inversion frequency defaults to 3300Hz, but may be modified by writing to P4.8.
See:

- Audio Control – $C2 write

7.5.2 Audio Transmit Mode

The device operates in half duplex, so when in transmit mode the receive path (discriminator and audio output amplifiers) should be disabled, and can be powered down, by the host µC.

Two modulator outputs with independently programmable gains are provided to facilitate single or two-point modulation. If one of the modulator outputs is not used it can be disabled to conserve power.

To avoid spurious transmissions when changing from Rx to Tx, the MOD1 and MOD2 outputs are ramped to the quiescent modulator output level, V_{BIAS} before switching (if enabled by b7 of the Analogue Gain register, $B0). Similarly, when starting a transmission, the transmitted signal is ramped up from the quiescent V_{BIAS} level and when ending a transmission the transmitted signal is ramped down to the quiescent V_{BIAS} level. The ramp rates are set in the Program Block P4.6. When the modulator outputs are disabled, their outputs will be set to V_{BIAS}. When the modulator output drivers are powered down, their outputs will be floating (high impedance), so the RF modulator will need to be turned off.

For all transmissions, the host µC must only enable signals after the appropriate data and settings for those signals are loaded into the C-BUS registers. As soon as any signalling is enabled the CMX885 will use the settings to control the way information is transmitted.

A programmable gain stage in the microphone input path facilitates a host controlled VOGAD capability, or an internal AGC function may be used.

See:

- Audio Control – $C2 write
- AuxADC and Tx MOD Mode – $A7 write
- Input Gain and Output Signal Routing – $B1 write

Processing Audio Signals for Transmission over Analogue Channels
The microphone input(s), with programmable gain, can be selected as the audio input source. Pre-emphasis is selectable with either of the two analogue Tx audio filters (for 12.5kHz and 25kHz channel spacing). These are designed for use in EN 300 086, TIA/EIA-603 or EN 301 025 compliant applications. When the 300Hz HPF is enabled, it will attenuate frequencies below 250Hz by more than 33dB with respect to the signal level at 1kHz. In Figure 8, Figure 9 and Figure 10, the template shows the +1 and -3dB limits.

These filters, together with a built in limiter, help ensure compliance with EN 300 086 and EN 301 025 (25kHz and 12.5kHz channel spacing) when levels and gain settings are set up correctly in the target system.

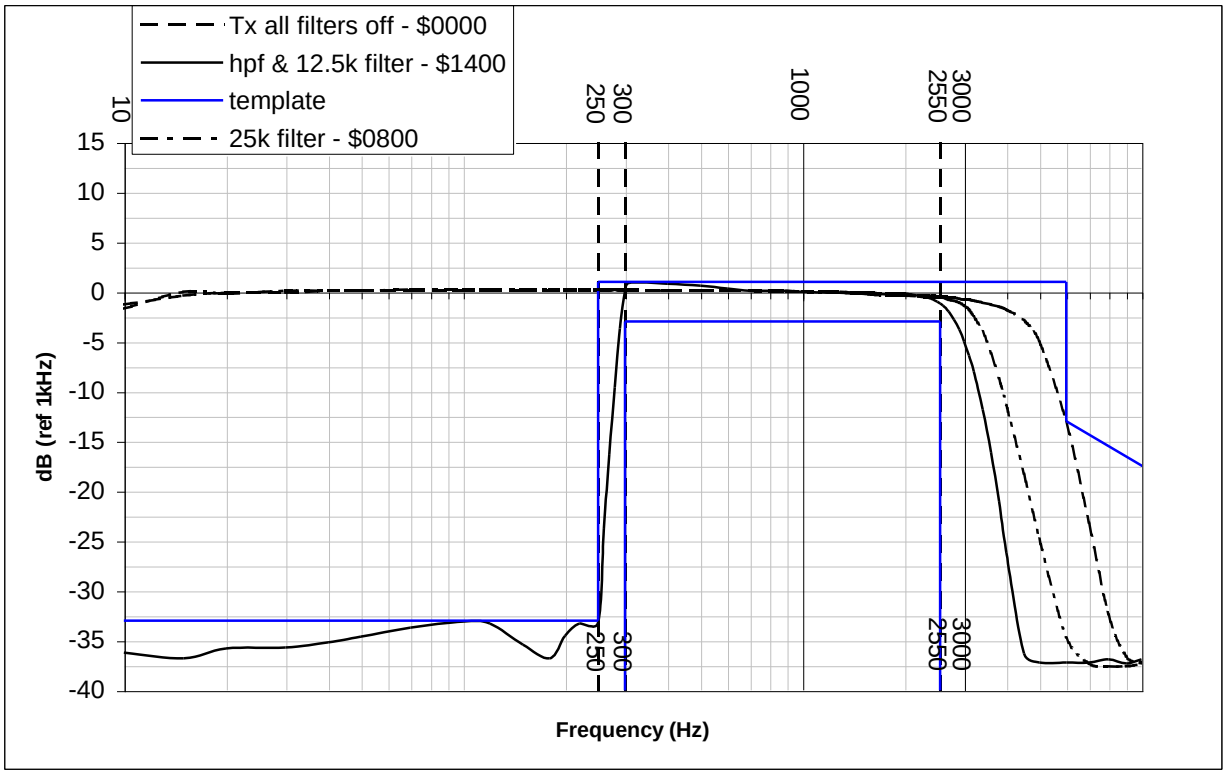


Figure 8 Tx Channel Audio Filter Response and Template (ETSI)

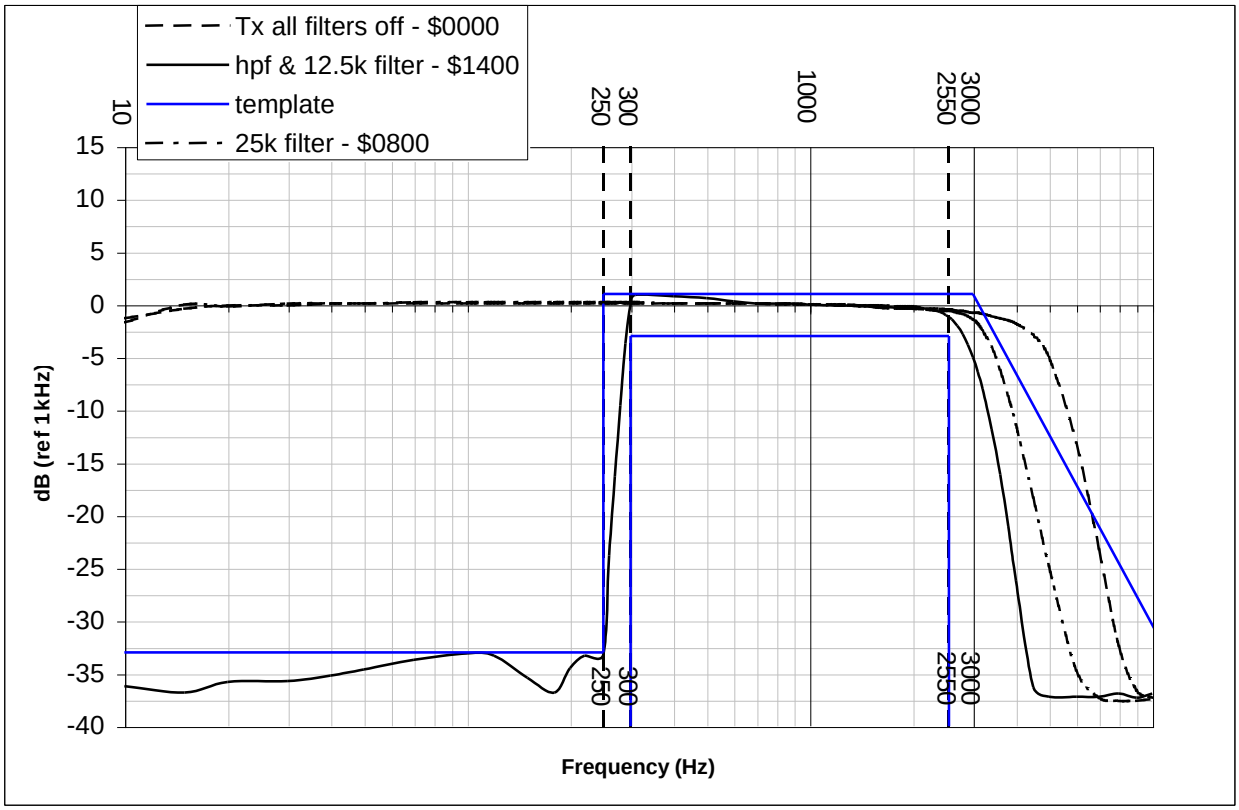


Figure 9 Tx Channel Audio Filter Response and Template (TIA)

The characteristics of the 12.5kHz channel filter fit the template shown in Figure 8 and Figure 9. This filter also facilitates implementation of systems compliant with TIA/EIA-603 'A' , 'B' and 'C' bands .

The CMX885 provides selectable pre-emphasis filtering of +6dB per octave from 300Hz to 3000Hz, matching the template shown in Figure 10.

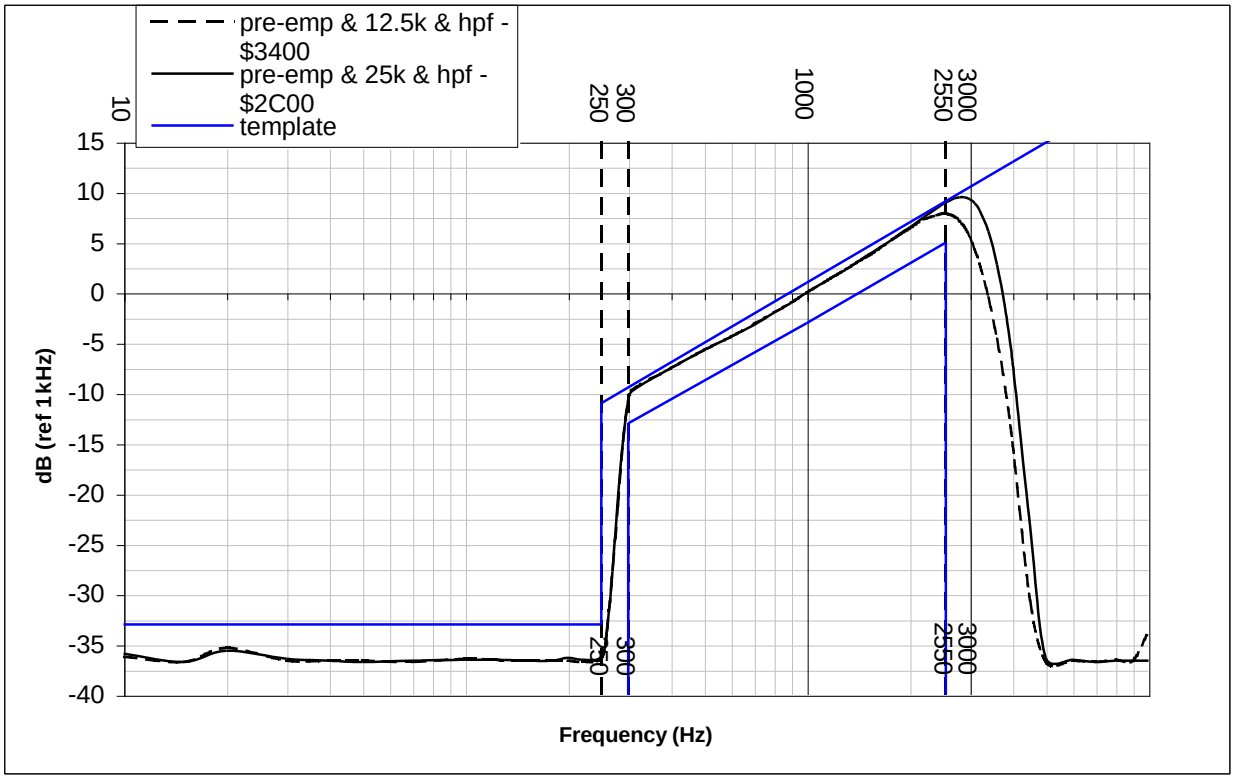


Figure 10 Audio Frequency Pre-emphasis

Modulator Output Routing

The Tx signal can be routed to both MOD1 and MOD2 outputs in accordance with the settings of:

- AuxADC and Tx MOD Mode – $A7 write
- Input Gain and Output Signal Routing – $B1 write

Input AGC

An Automatic Gain Control system can be enabled by setting the relevant bits of the Program Block P4.9. The setting of the Input 1 Gain stage is recorded when the device enters Tx mode and if the signal exceeds the pre-set threshold, the Input 1 Gain is automatically reduced in 3.2dB steps until it falls within the operational levels or the range of the gain stage is exhausted. When the signal level drops, the gain will be automatically increased in 3.2dB steps at the rate set in P4.9 until the initial value has been reached. For maximum effect the system should be designed such that the +22.4dB setting of the Input 1 Gain stage achieves the nominal levels. To ensure consistent operation, it is recommended that the Input 1 Gain stage value be re-initialised before entering Tx mode. The signal that is used as an input to this process can be selected to be either the:

- Output of Input1 Gain Stage
- Output of the Pre-emphasis Filter

by selecting the relevant bit in P4.9. The pre-emphasis option should only be chosen if this block is actually in use.

- Input Gain and Output Signal Routing – $B1 write
-
- Program Block 4 – Gain and Offset Setup

Audio Scrambling
The CMX885 incorporates an optional frequency inversion scrambler in transmit mode. This scrambles audio band signals, to be de-scrambled in the receiver. The inversion frequency defaults to 3300Hz, but maybe modified by writing to P4.8.
See:
- Audio Control – $C2 write

7.6 Inband Signalling
The CMX885 supports DSC, NWR (Rx only) and DTMF signalling and a user-programmable audio tone generator (288Hz to 3000Hz). Note that if tones below 400Hz are used, the 300Hz HPF should be disabled.

Selection of the Inband signalling mode is performed by bits 11-8 of the Mode register ($C1). Detection of the selected Inband signalling mode can be performed in parallel with voice or data reception.

See:
- Mode Control – $C1 write
- Tx Inband Tones – $C3 write
- Tone Status – $CC read
- Audio Tone – $CD write

7.6.1 Receiving DTMF Tones
DTMF Tone detection may be enabled in the Mode register ($C1) in parallel with other inband tone modes (however, this is not recommended due to the increased likelihood of false detects). When a DTMF tone has been detected, b10 of the Tone Status register ($CC) and b12 of the IRQ Status register, $C6, will be set. This value will overwrite any existing inband tone value that may be present. The DTMF detector returns the values shown below in Table 3.

7.6.2 Transmitting DTMF Tones
The DTMF signals to be generated are defined in the TxTONE register ($C3). Single tones and twist (lower frequency tone reduced by 2dB) can be enabled by setting the appropriate bit in the $C3 register to 1. The DTMF level is set in Program Block P1.0. The DTMF tones must be transmitted on their own, the host µC must disable audio band signals prior to initiating transmission of the DTMF tones and (if required) restore the audio band signals after the DTMF transmission is complete. Table 3 shows the DTMF tone pairs, together with the values for programming the 'Tone Pair' field of the TxTONE register.

Table 3 DTMF Tone Pairs

Tone Code (Hex)	Key Pad Position	Low Tone (Hz)	High Tone (Hz)
1	1	697	1209
2	2	697	1336
3	3	697	1477
4	4	770	1209
5	5	770	1336
6	6	770	1477
7	7	852	1209
8	8	852	1336
9	9	852	1477
A	0	941	1336
B	*	941	1209
C	#	941	1477
D	A	697	1633
E	B	770	1633
F	C	852	1633
0	D	941	1633

Note: Only the underlined tone is generated when the 'Single Tone' bit is enabled.

7.7 DSC modem - (FSK 1200bps)

The device can implement a 1200 bps DSC (Digital Selective Call) modem conforming to the requirements of ITU-R M.493-11 for use in Marine VHF band radio equipment. This modem uses tones at 1300Hz and 2100Hz to represent binary 1's and 0's respectively, with 6dB/octave pre-emphasis in Tx.

See:

- Mode Control – $C1 write
- Modem Configuration – $C7 write
- Rx Data 1 – $C5
- Tx Data 1 – $CA write

	DX/RX	A	B	C	D	E	F	G	H	I
Dot Pattern	Phasing Sequence	Format Specifier	Called Party Address	Category	Self-identification	Tele-command Message	Frequency Message	Frequency Message	End of Sequence	Error-check Character
		2 Identical characters	5 characters	1 character	5 characters	2 characters	3 characters	3 characters	3 identical DX characters 1 RX character	1 character

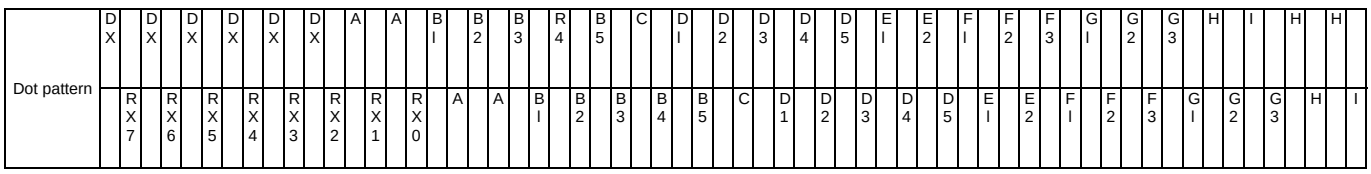


Figure 11 DSC format

To enable this mode, the En_DSC bit of the Modem Configuration register $C7:b11 must be set. The DSC modem itself can then be controlled by setting or clearing the Modem Enable bit $C1:b2, after selecting the appropriate source with $C1:b4. Note that, due to the C-BUS latency times, there should be a delay after clearing this bit, before re-enabling it again.

With DSC mode selected $C7:b8 to b3 and $C7:b1 to b0 are ignored.

Two modes of operation are provided:

- Raw Mode
- Formatted Mode

Symbol No.	Emitted signal and bit position 12345678910	Symbol No.	Emitted signal and bit position 12345678910	Symbol No.	Emitted signal and bit position 12345678910
00	BBBBBBBYYY	43	YYBYBYBBYY	86	BYYBYBYBYY
01	YBBBBBBYYB	44	BBYYBYBYBB	87	YYYBYBYBYB
02	BYBBBBBYYB	45	YBYYBYBBYY	88	BBBYYBYYBB
03	YYBBBBBYBY	46	BYYYBYBBYY	89	YBBYYBYBYY
04	BBYBBBBYYB	47	YYYYBYBBYB	90	BYBYYBYBYY
05	YBYBBBBYBY	48	BBBBYYBYBY	91	YYBYYBYBYB
06	BYYBBBBYBY	49	YBBBYYBYBB	92	BBYYYBYBYY
07	YYYBBBBYBB	50	BYBBYYBYBB	93	YBYYYBYBYB
08	BBBYBBBYYB	51	YYBBYYBBYY	94	BYYYYBYBYB
09	YBBYBBBYBY	52	BBYBYYBYBB	95	YYYYYBYBBY
10	BYBYBBBYBY	53	YBYBYYBBYY	96	BBBBBYYYBY
11	YYBYBBBYBB	54	BYYBYYBBYY	97	YBBBBYYYBB
12	BBYYBBBYBY	55	YYYBYYBBYB	98	BYBBBYYYBB
13	YBYYBBBYBB	56	BBBYYYBYBB	99	YYBBBYYBYY
14	BYYYBBBYBB	57	YBBYYYBBYY	100	BBYBBYYYBB
15	YYYYBBBBYY	58	BYBYYYBBYY	101	YBYBBYYBYY
16	BBBBYBBYYB	59	YYBYYYBBYB	102	BYYBBYYBYY
17	YBBBYBBYBY	60	BBYYYYBBYY	103	YYYBBYYBYB
18	BYBBYBBYBY	61	YBYYYYBBYB	104	BBBYBYYYBB
19	YYBBYBBYBB	62	BYYYYYBBYB	105	YBBYBYYBYY
20	BBYBYBBYBY	63	YYYYYYBBBY	106	BYBYBYYBYY
21	YBYBYBBYBB	64	BBBBBBYYYB	107	YYBYBYYBYB
22	BYYBYBBYBB	65	YBBBBBYYBY	108	BBYYBYYBYY
23	YYYBYBBBYY	66	BYBBBBYYBY	109	YBYYBYYBYB
24	BBBYYBBYBY	67	YYBBBBYYBB	110	BYYYBYYBYB
25	YBBYYBBYBB	68	BBYBBBYYBY	111	YYYYBYYBBY
26	BYBYYBBYBB	69	YBYBBBYYBB	112	BBBBYYYYBB
27	YYBYYBBBYY	70	BYYBBBYYBB	113	YBBBYYYBYY
28	BBYYYBBYBB	71	YYYBBBYBYY	114	BYBBYYYBYY
29	YBYYYBBBYY	72	BBBYBBYYBY	115	YYBBYYYBYB
30	BYYYYBBBYY	73	YBBYBBYYBB	116	BBYBYYYBYY
31	YYYYYBBBYB	74	BYBYBBYYBB	117	YBYBYYYBYB
32	BBBBBYBYYB	75	YYBYBBYBYY	118	BYYBYYYBYB
33	YBBBBYBYBY	76	BBYYBBYYBB	119	YYYBYYYBBY
34	BYBBBYBYBY	77	YBYYBBYBYY	120	BBBYYYYBYY
35	YYBBBYBYBB	78	BYYYBBYBYY	121	YBBYYYYBYB
36	BBYBBYBYBY	79	YYYYBBYBYB	122	BYBYYYYBYB
37	YBYBBYBYBB	80	BBBBYBYYBY	123	YYBYYYYBBY
38	BYYBBYBYBB	81	YBBBYBYYBB	124	BBYYYYYBYB
39	YYYBBYBBYY	82	BYBBYBYYBB	125	YBYYYYYBBY
40	BBBYBYBYBY	83	YYBBYBYBYY	126	BYYYYYYBBY
41	YBBYBYBYBB	84	BBYBYBYYBB	127	YYYYYYYBBB
42	BYBYBYBYBB	85	YBYBYBYBYY		

B = 0
Y = 1
Order of transmitted bits: bit 1 first

Figure 12 DSC character format

7.7.1 Receiving DSC Signals

The received signal is filtered and data is extracted with the aid of a PLL to recover the clock from the serial data stream. The recovered data is stored in a 2-byte buffer (grouped into 16-bit words) and an interrupt issued to indicate received data is ready. Data is transferred over the C-BUS under host µC control. If this data is not read before the next data is decoded it will be overwritten and it is up to the user to ensure that the data is transferred at an adequate rate following data ready being flagged. The DSC bit clock is not output externally.

The extracted data is compared with the 16-bit programmed Frame Sync pattern (preset to $CB23 following a RESET command). An interrupt will be flagged when the programmed Frame Sync pattern is detected. The host µC may stop the frame sync search by disabling the DSC demodulator ($C1:b2 cleared to 0). Once a valid Frame Sync pattern has been detected, the frame sync search algorithm is

disabled; it may be re-started by the host disabling the Modem Enable bit of the Mode Control register ($C1:b2) and then re-enabling it (taking note of the C-BUS latency time).

In Rx Raw mode (En_RAW=1) the modem will report back all data received as soon as it is enabled. (Note: If a valid DSC signal is not present when the modem is first enabled, it will still attempt to demodulate the input signal and output data. The host must determine if the data is valid or not. It is possible to use the SynC facility to reduce the amount of invalid data presented to the host, but this may also lead to DSC calls with errors in the SynC pattern being missed).

As soon as the Modem Enable bit has been asserted, the modem will attempt to demodulate the input signal. Data bits will then be delivered to the Rx Data 1 register, $C5 as they are demodulated, indicated by the Data_RDY bit. It is up to the host to align, decode and validate the data and to subsequently switch the modem off once an EOS (End of Sequence) has been detected (by clearing $C1:b2 to 0). In this mode, the device does not perform byte alignment or phasing (synchronisation) detection[3].

The host must read the RxData 1 register before the next 16 bits of data have been received, otherwise the data will be lost.

If the SynC facility is used in Raw mode, then the value of SynC must be programmed by the host to a suitable value via the Program Blocks, P0.0 and P0.1. The values $5555 or $AAAA are suggested for this setting, however, this will not completely remove false detections and the following received data must be analysed before assuming that a valid call is in progress (see ITU-R M.493-11 for details). The SynC enable bit $C7:b15 must be asserted. Setting the Modem Enable bit $C1:b2 will activate the DSC modem, which will then attempt to decode the signal at its input. Acquisition of the SynC data pattern will be reported to the host by the setting of the DSC bit $C6:b3.

In Rx Formatted mode, (En_Raw=0) the modem will check the incoming bit stream for a valid sequence of phasing characters (3x Rx, 2x Dx+ Rx or Dx + 2 x Rx) and then report any correctly decoded characters in the RxData1 ($C5) register. The characters are packed into the 16-bit register as two 7-bit characters and an additional error indication bit (bits 15 and 7). In the case where an odd number of characters has been received, the unused field will be reported as 0000000. This mechanism significantly reduces the amount of data transferred to the host and the host processing requirements.

The decoded 7-bit characters will be delivered to the RxData1 register, $C5, as indicated by the Data_RDY bit. The modem will not report valid data until it has correctly received the initial phasing sequence. Once the Phasing sequence has been detected, the modem's internal DPLL bandwidth will be automatically reduced to improve the error performance. If one of the time-diversity received characters is in error, only the correct one will be reported. If both characters have errors, the last one received will be reported, with bit 7 (MSB) set. The characters reported back will correspond to the data sequence (see Figure 11)[4]:

```
A A B1 B2 B3 B4 B5 C D1 D2 D3 D4 D5 E1 E2 F1 F2 F3 G1 G2 G3 H I
```

Once the H and I fields have been received by the host, it should shut the DSC modem down by clearing the Modem Enable bit in the Mode Control register $C1:b2.

7.7.2 Transmitting DSC Signals

The DSC encoding operates in accordance with the bit settings in the Modem Configuration register ($C7). When enabled the modulator will begin transmitting data using the settings and values in Program Block 0 (bit sync and frame sync patterns), the Modem Configuration register and the Tx Data registers. Therefore, these registers should be programmed to the required values before transmission is enabled.

The CMX885 generates its own internal data clock and converts the binary data into the appropriately phased frequencies. The binary data is taken from Tx DATA 1 register ($CA), most significant bit first.

In Tx Raw mode (En_RAW=1) the host must supply all data to be transmitted by the modem via the TxData register ($CA) in the correct order and format to conform to the DSC standards.

[3] This is similar to the FX604, CMX910 and CMX7032 operation.

[4] This particular sequence corresponds to the example given in ITU-R M493-11. Different Telecommands will produce different sequences of varying lengths.

Setting the Modem Enable bit $C1:b2, will enable the DSC modem, which will then transmit the data supplied by the host through the Tx Data 1 register, $CA. The Modem Configuration register $C7:b10 should also be set to enable/disable Raw data mode, as appropriate.

In Tx Formatted mode (En_RAW=0), the modem will automatically transmit the dotting pattern followed by the phasing sequence and then encode the data presented at the Tx Data 1 register ($CA) with the correct checksum bits and then transmit it in the correct position with automatic repetition to conform to the time diversity requirements of the standard. Data in the Tx Data 1 register is presented as two 7-bit characters, in the case where an odd number of characters needs to be sent, then the un-used character should be set to 0000000 and b7 set to 1. The final characters sent by the host should be a valid “End-of-Sequence” character followed by the “Error Check” character.

Valid DSC characters should be supplied by the host through the Tx Data 1 register, $CA. Two characters can be loaded in the same C-BUS write operation. The modem will begin transmitting the dotting sequence followed by the phasing sequence as soon as the Modem Enable bit $C1:b2 is set. The format of the data supplied by the host is similar to the Rx format:

```
A A B1 B2 B3 B4 B5 C D1 D2 D3 D4 D5 E1 E2 F1 F2 F3 G1 G2 G3 H I
```

There is no facility for automatically generating continuous dotting (preamble), Y data (all 1’s), B data (all 0’s) or phasing (synchronisation) sequences internally, however, the modem will continue to transmit the last data loaded into the TxData1 register, so only a single data load is required.

7.8 NOAA/NWR SAME and WAT Decoding

A data decoder and tone detector suitable for use with the NOAA’s NWR (NOAA Weather Radio) system is provided in the device. Full details of the system are publicly available from the NOAA website at http://www.nws.noaa.gov/nwr/ and the CMX885 provides support for the WAT detection and SAME decoding. It is possible to route the signal input to either Input 1 or Input 2 so that NWR monitoring can be performed in parallel with existing radio operations (subject to suitable RF sections being provided externally).

See:

- NWR Status and Data – $BB read
- Mode Control – $C1 write
- Status – $C6 read
- Modem Configuration – $C7 write
- Interrupt Mask – $CE

The NWR SAME data message consists of six possible elements in the following sequence:

1. Preamble
2. Header Code
3. Warning Alarm Tone/Attention Signal
4. Voice Message
5. Preamble
6. End Of Message (EOM)

Elements 1, 2, 5 and 6 will always be transmitted in an NWR SAME message and repeated three times. Elements 3 and 4 may or may not be transmitted depending on the specific type of message or its application.

The coded message is transmitted, using Frequency Shift Keying (FSK), in the NWR audio channel. In this application and the implementation currently used by the FCC EAS, it is more accurate to refer to the code format as Audio Frequency Shift Keying (AFSK). It is transmitted at no less than 80% modulation (± 4.0kHz deviation minimum, ± 5.0kHz deviation maximum).

The coded message and voice message is transmitted over the NWR transmitter network using standard pre-emphasis for narrow band VHF Frequency Modulation (FM) of 6dB per octave increasing slope from 300Hz to 3,000Hz applied to the modulator.

Preamble. The preamble and header code are transmitted three times with a one second pause (± 5%) between each coded message burst prior to the broadcast of the actual voice message. Then the

preamble and End Of Message (EOM) code are transmitted three times with a one second pause (± 5%) between each EOM burst.

Preamble Byte. The first 16 bytes (prior to the header code and EOM) of the data transmission constitute a preamble with each byte having the value $AB (8 bit byte [10101011]). For all bytes, the least significant bit (LSB) is sent first. The bytes following the preamble constitute the actual message data transmission.

NOTE: For NWR system maintenance, NWS will occasionally send a continuous string of preamble code, $AB or a continuous tone through its communications links to the NWR transmitters, for several seconds up to around one minute.

Bit Definition. The following definitions of a bit are based on a bit period equaling 1920 microseconds (± one microsecond).

- The data rate is 520.83 bits per second
- Logic zero is 1562.5 Hz.
- Logic one is 2083.3 Hz
- Mark and space bit periods are equal at 1.92 milliseconds.

Header. Bit and byte synchronization is attained by the preamble code at the beginning of each header code or EOM data transmission. The message data (header) code is transmitted using American Standard Code for Information Interchange (ASCII) characters as defined in ANSI INCITS 4 (rev 86, 2002), with the eighth bit always set to zero. Each separate header code data transmission should not exceed a total of 268 bytes if the maximum allowable geographic locations (31) are included.

Warning Alarm Tone. The Warning Alarm Tone (WAT), if transmitted, is sent within one to three seconds following the third header code burst. The frequency of the WAT is 1050Hz (±0.3%) for 8 to 10 seconds at no less than 80% modulation (±4.0 kHz deviation minimum, ±5.0 kHz deviation maximum).

Voice Message. If transmitted, the actual voiced message begins within three to five seconds following the last NWR SAME code burst or WAT, whichever is last. The voice audio ranges between 20% modulation (± 1 kHz deviation) and 90% modulation (± 4.5 kHz deviation) with occasional lulls near zero and peaks as high as, but not exceeding, 100% modulation (± 5.0 kHz deviation). Total length of the voice message should not exceed two minutes.

Preamble. A repeat of above.

End Of Message. EOM is identified by the use of “NNNN.”

7.8.1 Message Code Format

(Preamble) ZCZC-ORG-EEE-PSSCCC-PSSCCC+TTTT-JJJHHMM-LLLLLLLL- (1 second pause)

(Preamble) ZCZC-ORG-EEE-PSSCCC-PSSCCC+TTTT-JJJHHMM-LLLLLLLL- (1 second pause)

(Preamble) ZCZC-ORG-EEE-PSSCCC-PSSCCC+TTTT-JJJHHMM-LLLLLLLL- (1 to 3 second pause)

1050 Hz Warning Alarm Tone for 8 to 10 seconds – (if transmitted) (3 to 5 second pause)

Voice /spoken oral text of message – (if transmitted) (1 to 3 second pause)

(Preamble) NNNN (1 second pause)

(Preamble) NNNN (1 second pause)

(Preamble) NNNN

7.8.2 WAT Detection

The WAT detector is enabled by setting the NWR bit $C1:b12 and indicated by setting b15 of the NWRData register ($BB). If enabled, the NWR IRQ bit in the Status register $C6:b14 will also be set. The detector will be reset after 500ms, so multiple detections may be indicated on long WAT tones.

7.8.3 SAME Decoding

The SAME data is received at 520.83bps and decoded by the CMX885 whenever the NWR bit $C1:b12 is set. Internally, the CMX885 monitors the selected input until it detects the preamble sequence and then passes the subsequently recovered data to the host uC via the NWR Data register ($BB). The decoder will detect the data header and determine if it is “ZCZC” indicating that data follows or “NNNN” indicating the end of a transmission and report these states in bits 13 and 14 of the NWR Data register ($BB) respectively). If enabled, the NWR IRQ bit in the Status register $C6:b14 will also be set following the detection of the preamble and on every subsequently received byte.

When the En_NWR_data bit is set, the receiver outputs the received bitstream. The host is allowed to set this bit at any time to get "raw mode" data output with no preamble/header detection and no guarantee of byte alignment.

When the En_NWR_data bit is clear, the receiver searches for a valid SAME transmission but does not output data. If it sees a preamble followed by the data header ("ZCZC"), it raises an IRQ and *automatically* sets the En_NWR_data bit to put itself into data-output mode. It is then up to the host to decide when to clear the En_NWR_data bit to put the receiver back into sync-search mode (thus "re-arming" it).

If the receiver sees a preamble followed by the end-of-message header ("NNNN") while doing sync-search, it informs the host [2] and then continues the search without putting itself into data-output mode.

It is the responsibility of the host to shut the decoder down at the end of a received burst by clearing the En_NWR_data bit $C7:b12 to 0.

7.9 Auxiliary ADC Operation

The input to the Auxiliary ADCs can be independently routed to any of the signal input pins under control of the AuxADC and Tx MOD mode register, $A7. Conversions will be performed as long as a valid input source is selected; to stop the ADC, the input source should be set to “none”. Register $C0:b6, BIAS, must be enabled for Auxiliary ADC operation.

Averaging can be applied to the ADC readings by selecting the relevant bits in the AuxADC and Tx MOD mode register, $A7, the length of the averaging is determined by the value in the Program Blocks P3.0 and P3.1, and defaults to a value of 0. This is a rolling average system such that a proportion of the current data will be added to the last value. The proportion is determined by the value of the average counter in P3.0 and P3.1. For an average value of 0; 50% of the current value will be applied, for a value of 1 = 25%, 2 = 12.5% etc. The maximum useful value of this field is 8. Averaging will begin with the current value of the AuxADC, therefore it is recommended that the AuxADC be enabled for at least one sample (250µs) before starting the average process to ensure that its initial value is as expected, otherwise the initial value will default to zero.

High and low thresholds may be independently applied to both ADC channels (the comparison is applied after averaging, if this is enabled) and an IRQ generated when either the high threshold is crossed by a rising edge signal or the low threshold is passed by a falling edge signal, which allows the user to implement a selectable degree of hysterisis. The thresholds are programmed via the AuxADC Threshold register, $B5.

Auxiliary ADC data is read back in the AuxADC Data register ($A9) and includes the threshold status as well as the actual conversion data (subject to averaging, if enabled).

See:

- AuxADC and Tx MOD Mode – $A7 write
- AuxADC1 Data – $A9 read
- AuxADC2 Data – $AA read
- AuxADC Threshold Data – $B5 write

7.10 Auxiliary DAC/RAMDAC Operation

The four Auxiliary DAC channels are programmed via the AuxDAC Control register, $A8. AuxDAC channel 1 may also be programmed to operate as a RAMDAC which will automatically output a pre-programmed profile at a programmed rate. The AuxDAC Control register, $A8, with b12 set, controls this mode of operation. The default profile is a raised cosine (see Table 8), but this may be over-written with a user defined profile by writing to Program Block P3.11. The RAMDAC operation is only available in Tx mode and, to avoid glitches in the ramp profile, it is important not to change to Idle or Rx mode whilst the RAMDAC is still ramping. The AuxDAC outputs (available on their respective DAC pins) hold the user-programmed level during a powersave operation if left enabled, otherwise they will return to zero. Note that access to all four AuxDACs is controlled by the AuxDAC Control register, $A8, and therefore to update all AuxDACs requires four writes to this register. It is not possible to simultaneously update all four AuxDACs.

See:

- AuxDAC Control/Data – $A8 write

7.11 Digital System Clock Generator

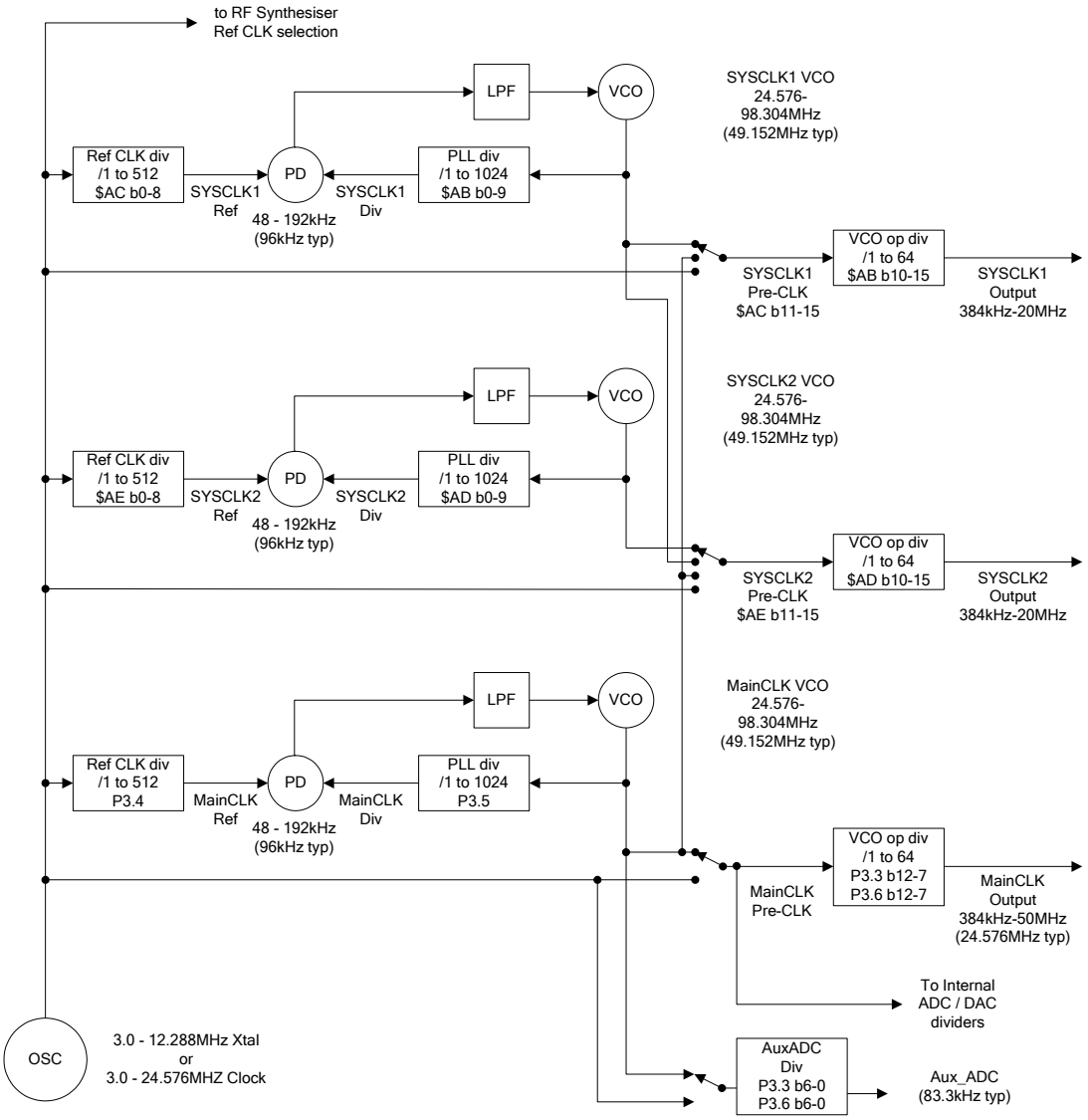


Figure 13 Digital Clock Generation Schemes

The CMX885 includes a 2-pin crystal oscillator circuit. This can either be configured as an oscillator, as shown in section 5, or the XTAL input can be driven by an externally generated clock. The crystal (Xtal) source frequency can go up to 12.288MHz (clock source frequency up to 24.576MHz), but by default, a 3.6864MHz Xtal is assumed for the functionality provided in the CMX885.

7.11.1 Main Clock Operation

A PLL is used to create the main clock (MainCLK - nominally 24.576MHz) for the internal sections of the CMX885. At the same time, other internal clocks are generated by division of either the Xtal Reference Clock or the Main Clock. These internal clocks are used for determining the sample rates and conversion times of A-to-D and D-to-A converters, running a General Purpose Timer, the signal processing block. In particular, it should be noted that in Idle mode the setting of the GP Timer divider directly affects the C-BUS latency (with the default values this is nominally 250µs).

The CMX885 defaults to the settings appropriate for a 3.6864MHz Xtal, however if other frequencies are to be used (to facilitate commonality of Xtals between external RF synthesizers and the CMX885 for

instance) then the Program Block registers P3.2 to P3.7 will need to be programmed appropriately at power-on. A table of common values is provided in Table 2.

See:
- Program Block 3 – AuxDAC, RAMDAC and Clock Control

7.11.2 System Clock Operation

Two System Clock outputs, SYSCLK1 and SYSCLK2, are available to drive additional circuits, as required. These are phase locked loop (PLL) clocks that can be programmed via the System Clock registers with suitable values chosen by the user. The System Clock PLL Configure registers ($AB and $AD) control the values of the VCO Output divider and Main Divide registers, while the System Clock Ref. Configure registers ($AC and $AE) control the values of the Reference Divider and signal routing configurations. The PLLs are designed for a reference frequency of 96kHz. If not required, these clocks can be independently powersaved. The clock generation scheme is shown in the block diagram of Figure 13. Note that at power-on, these outputs are disabled.

See:
- SYSCLK1 and SYSCLK2 PLL Data – $AB, $AD write
- SYSCLK1 and SYSCLK2 REF – $AC and $AE write

7.12 GPIO

Two pins are provided for control of external hardware. RXENA and TXENA are driven by the device to follow the state of the Rx and Tx Mode bits in the Mode register, $C1:

$C1 Mode:	b1	b0	TXENA	RXENA
Idle	0	0	1	1
Rx	0	1	1	0
Tx	1	0	0	1
reserved	1	1	1	1

7.13 Signal Level Optimisation

The internal signal processing of the CMX885 will operate with wide dynamic range and low distortion only if the signal level at all stages in the signal processing chain is kept within the recommended limits. For a device working from a 3.3V ±10% supply, the maximum signal level which can be accommodated without distortion is [(3.3 x 90%) – (2 x 0.3V)] Volts pk-pk = 838mVrms, assuming a sine wave signal. Compared to the reference level of 308mVrms, this is a signal of +8.69dB. This level should not be exceeded at any stage.

7.13.1 Transmit Path Levels

For the maximum signal out of the MOD1 and MOD2 attenuators, the signal level at the output of the Analogue Routing block should not exceed +8.69dB, assuming both fine and coarse output attenuators are set to a gain of 0dB. This means that the output from the soft limiter must not exceed 838mVrms. If pre-emphasis is used, an output signal at 3000Hz will have three times the amplitude of a signal at 1000Hz, so the signal level before pre-emphasis should not exceed 279mVrms. The Fine Input Gain adjustment has a maximum attenuation of 3.5dB and no gain, whereas the Coarse Input Gain adjustment has a variable gain of up to +22.4dB and no attenuation. If the highest gain setting were used, then the maximum allowable input signal level at the MICFB pin would be 54mV pk-pk. With the lowest gain setting (0dB), the maximum allowable input signal level at the MICFB pin would be 718mVrms.

7.13.2 Receive Path Levels

For the maximum signal out of the AUDIO attenuator, the signal level at the output of the Analogue Routing block should not exceed +8.69dB, assuming both fine and coarse output attenuators are set to a gain of 0dB. That is a signal level of 838mVrms. If de-emphasis is used, an output signal at 300Hz will have three and one third times the amplitude of a signal at 1000Hz, so the signal level before de-emphasis should not exceed 251mVrms. The Fine Input Gain adjustment has a maximum attenuation of 3.5dB and no gain, whereas the Coarse Input Gain adjustment has a variable gain of up to +22.4dB and no attenuation. If the highest gain setting were used, then the maximum allowable input signal level at the

DISCFB pin would be 12.0mVrms. With the lowest gain setting (0dB), the maximum allowable input signal level at the DISCFB pin would be 158mVrms. The signal level of +8.69dB (838mVrms) is an absolute maximum, which should not be exceeded anywhere in the signal processing chain if severe distortion is to be avoided.

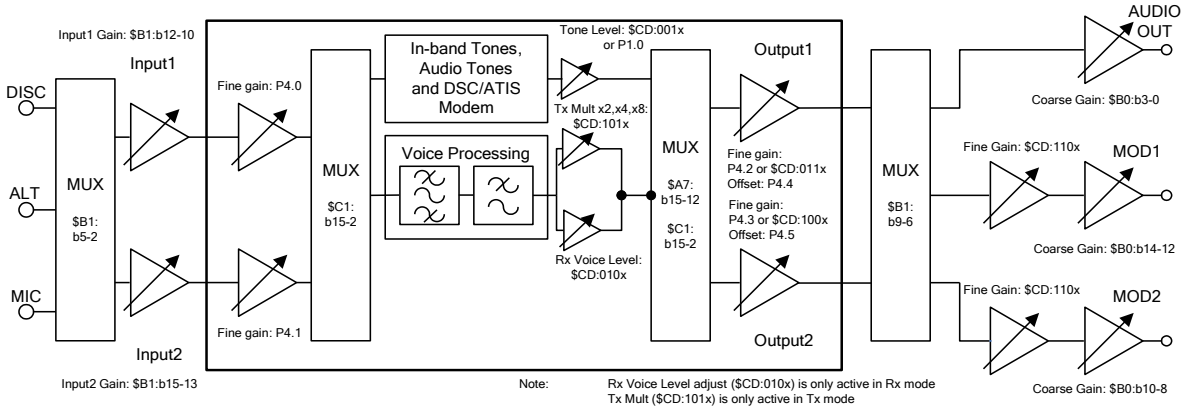


Figure 14 Level Adjustments

7.14 C-BUS Interface

7.14.1 Interrupt Operation

The CMX885 will issue an interrupt on the IRQN line when the IRQ bit (bit 15) of the Status register and the IRQ Mask bit (bit 15) are both set to 1. The IRQ bit is set when the state of the interrupt flag bits in the Status register change from a 0 to 1 and the corresponding mask bit(s) in the Interrupt Mask register is(are) set. Enabling an interrupt by setting a mask bit (0→1) after the corresponding Status register bit has already been set to 1 will also cause the IRQ bit to be set.

All interrupt flag bits in the Status register, except the PRG flag (bit 0), are cleared and the interrupt request is cleared following the command/address phase of a C-BUS read of the Status register. The PRG flag bit is set to 1 only when it is permissible to write a new word to the Programming register.
See:

- Status – $C6 read
- Interrupt Mask – $CE

7.14.2 General Notes

In normal operation, the most significant registers are:

- Mode Control – $C1 write
- Status – $C6 read
- Analogue Output Gain – $B0 write
- Input Gain and Output Signal Routing – $B1 write
- Audio Control – $C2 write

Setting the Mode Control register to either Rx or Tx will automatically increase the internal clock speed to its operational rate, whilst setting the Mode Control register to Idle will automatically return the internal clock to a lower (powersaving) rate. To access the Program Blocks (through the Programming register, $C8) the device MUST be in Idle mode.

Under normal circumstances, the CMX885 manages the main clock control automatically, using the default values loaded in Program Block 3.

8 Configuration Guide

8.1 C-BUS Register Summary

ADDR. (hex)		REGISTER	Word Size (bits)
$01	W	C-BUS RESET	0
$A7	W	AuxADC and Tx MOD Mode	16
$A8	W	AuxDAC Control/Data	16
$A9	R	AuxADC1 Data	16
$AA	R	AuxADC2 Data	16
$AB	W	SYSCLK1 PLL Data	16
$AC	W	SYSCLK1 REF	16
$AD	W	SYSCLK2 PLL Data	16
$AE	W	SYSCLK2 REF	16
$AF		*reserved*	
$B0	W	Analogue Output Gain	16
$B1	W	Input Gain and Output Signal Routing	16
$B2		*reserved*	
$B3		*reserved*	
$B4		*reserved*	
$B5	W	AuxADC Threshold Data	16
$B6		*reserved*	
$B7		*reserved*	
$B8		*reserved*	
$B9		*reserved*	
$BA		*reserved*	
$BB	R	NWR Status and Data	16
$BC		*reserved*	
$BD		*reserved*	
$BE		*reserved*	
$BF		*reserved*	
$C0	W	Power-Down Control	16
$C1	W	Mode Control	16
$C2	W	Audio Control	16
$C3	W	Tx Inband Tones	16
$C4		*reserved*	
$C5	R	Rx Data 1	16
$C6	R	Status	16
$C7	W	Modem Configuration	16
$C8	W	Programming	16
$C9		*reserved*	
$CA	W	Tx Data 1	16
$CB		*reserved*	
$CC	R	Tone Status / Device Ident Code	16
$CD	W	Audio Tone	16
$CE	W	Interrupt Mask	16
$CF		*reserved*	

The detailed descriptions of the C-BUS registers are presented in numerical order and should be read in conjunction with the relevant functional descriptions in the Datasheet.

All other C-BUS addresses (including those not listed above) are either reserved for future use or allocated for production testing and must not be accessed in normal operation.

8.1.1 Reset Operations

A reset is automatically performed when power is applied to the CMX885. A reset can be issued as a C-BUS command, either as a General Reset command ($01), or by setting the appropriate bit (b5) in the Powerdown Control register ($C0). In the latter case, an option exists to protect the values held in the Program Block (which is accessed via the Programming register, $C8). The action of each reset type is shown in the table below:

Table 4 Reset Operations

	Reset Type	Protect Bit ($C0 b4) State	Program Block State
1	Power on	cleared by h/w	default
2	General Reset (C-BUS $01)	cleared by h/w	default
3	Reset (C-BUS $C0 b5)	0	default
4	Reset (C-BUS $C0 b5)	1	protected

8.1.2 General Reset – $01 write

The General Reset command has no data attached to it. It sets all operational C-BUS registers to $0000, (apart from the registers marked as *reserved*). Note that some transient data may appear in the following registers during the reset and power-up processes – this should be ignored:

Aux ADC 1 Data	$A9	Aux ADC 2 Data	$AA
NWR Status and Data	$BB	Rx Data 1	$C5
Status	$C6	Tone Status / Ident	$CC

8.1.3 AuxADC and Tx MOD Mode – $A7 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Tx Mod Mode				Aux ADC2 AV Mode		Aux ADC2 I/P Select			Aux ADC1 AV Mode		Aux ADC1 I/P Select			0	0

				Tx MOD Mode	
b15	**b14**	**b13**	**b12**	**Output1**	**Output2**
0	0	1	1	Inband	Inband
0	0	1	0	Inband	Bias
0	0	0	1	Inband	Bias
0	0	0	0	Bias	Bias

To select the routing between the Output1, Output2 and MOD1, MOD2 and AUDIO, see section 8.1.10

		AuxADC Averaging Mode
b11	**b10**	**AuxADC2**
b6	**b5**	**AuxADC1**
1	1	reserved
1	0	reserved
0	1	rolling average, uses Program Block 3.0/3.1 value
0	0	No averaging

			AuxADC Input Select
b9	**b8**	**b7**	**AuxADC2**
b4	**b3**	**b2**	**AuxADC1**
1	1	1	ADC4
1	1	0	ADC3
1	0	1	ADC2
1	0	0	ADC1
0	1	1	MICN
0	1	0	ALTN
0	0	1	DISCN
0	0	0	off

8.1.4 AuxDAC Control/Data – $A8 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENA	0	0	RAM DAC	DAC Sel		Aux DAC Data/RAMDAC Control									

b15 enable selected Aux DAC 0 = disable 1 = enable
b14 *reserved*
b13 *reserved*
b12 RAMDAC enable 0 = AuxDAC1 operates normally
1 = AuxDAC1 operates as a RAMDAC[5]. Data in b0-6 controls the RAMDAC functions.

b11-b10 Select the AuxDAC that b9-b0 data will be written to
00 = AuxDAC1
01 = AuxDAC2
10 = AuxDAC3
11 = AuxDAC4
b9-b0 AuxDAC data (unsigned)

Note: the C-BUS latency period (250µs) should be observed between successive writes to this register.

Note: when $A8 b12 is set to 1, writing data to this register controls the RAMDAC settings. Writing to AuxDAC1 whilst the RAMDAC is still ramping may cause un-intended operation. In this mode b10 and b11 are ignored and b9 to b0 perform the following functions:

b9 *reserved*, clear to 0
b8 *reserved*, clear to 0
b7 *reserved*, clear to 0
b6 RAMDAC RAM access, 0 resets the internal RAMDAC address pointer

			RAMDAC Scan Time	
b5	b4	b3	Divider	Time (ms)
0	0	0	1024	10.50
0	0	1	512	5.25
0	1	0	256	2.63
0	1	1	128	1.31
1	0	0	64	0.66
1	0	1	32	0.33
1	1	0	16	0.16
1	1	1	8	0.08

b2 Scan direction: 0 = ramp down 1 = ramp up
b1 Autocycle 0 = disable 1 = continuous ramp up/down
b0 RAMDAC start 0 = stop 1 = start RAMDAC ramping

To initiate a RAMDAC ramp up write: $9005
To initiate a RAMDAC ramp down, write: $9001

Note that initiating a RAMDAC scan will automatically bring AuxDAC1 out of powersave. To place AuxDAC1 back into powersave, it must be written to explicitly. Do NOT change Idle/Rx/Tx mode whilst the RAMDAC is still ramping.

[5] Do NOT write to directly to AuxDAC1 whilst the RAMDAC is in operation. RAMDAC is only available when in Tx mode.

8.1.5 AuxADC1 Data – $A9 read

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Threshold Status		x	x	x	x	Aux ADC 1 Data									

b15-14 Threshold Status

b15 = 1 signal is above the high threshold
= 0 signal is below the high threshold
b14 = 1 signal is below the low threshold
= 0 signal is above the low threshold

b13 *reserved*
b12 *reserved*
b11 *reserved*
b10 *reserved*
b9–0 AuxADC1 data or last reading (unsigned)

8.1.6 AuxADC2 Data – $AA read

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Threshold Status		x	x	x	x	Aux ADC 2 Data									

b15-14 Threshold Status

b15 = 1 signal is above the high threshold
= 0 signal is below the high threshold
b14 = 1 signal is below the low threshold
= 0 signal is above the low threshold

b13 *reserved*
b12 *reserved*
b11 *reserved*
b10 *reserved*
b9-0 AuxADC2 data or last reading (unsigned)

8.1.7 SYSCLK1 and SYSCLK2 PLL Data – $AB, $AD write
C-BUS address: $AB – SYSCLK1 PLL
C-BUS address: $AD – SYSCLK2 PLL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VCO Op Divide Ratio <5-0>						PLL Feedback Divide Ratio <9-0>									

b15-10 divide the selected output clock source by the value in these bits, to generate the System Clock output. Divide by 64 is selected by setting these bits to 0.

b9-0 divide System Clock PLL VCO clock by value set in these bits as feedback to the PLL phase detector (PD); when the PLL is stable, this will be the same frequency as the internal reference as set by b8-b0 of the System Clock Reference and Source Configuration register ($AC). Divide by 1024 is selected by setting these bits to 0.

8.1.8 SYSCLK1 and SYSCLK2 REF – $AC and $AE write
C-BUS address: $AC – SYSCLK1 Ref
C-BUS address: $AE – SYSCLK2 Ref

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Select & PS Clock Sources					O/P Slew		Ref Clock Divide Ratio <8-0>								

b15,12,11 Clock output divider source

SYSCLK1 Source	b15	b12	b11
Xtal	0	x	x
SYSCLK1 PLL	1	0	0
Main PLL	1	0	1
Test	1	1	x

SYSCLK2 Source	b15	b12	b11
Xtal	0	x	x
SYSCKL2 PLL	1	0	0
Main PLL	1	0	1
SYSCLK1 PLL	1	1	0
Test	1	1	1

b14 Powersave PLL 0 = powersave 1 = enabled
b13 Powersave Output Divider 0 = powersave / bypass 1 = enabled
b10-9 Output Slew Rate

b10	b9	Output Slew Rate
0	0	normal
0	1	slow
1	0	fast
1	1	fast

b8-b0 Reference Clk divide value. Divide by 512 function is selected by setting these bits to 0.

Note that after a General Reset, there will be no signal present on the SYSCLK1 and SYSCLK2 pins.

8.1.9 Analogue Output Gain – $B0 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Inv_1	MOD1 Attenuation			Inv_2	MOD2 Attenuation			Ramp Up/Dn	0	0	0	Audio Output Attenuation			

b15 Output1 polarity 0 = true 1 = inverted
b11 Output2 polarity 0 = true 1 = inverted
Used when interfacing with RF. Any change will take place immediately (within the C-BUS latency period) after these bits are changed.

b14	b13	b12	MOD1 Output Attenuation
b10	b9	b8	MOD2 Output Attenuation
0	0	0	>40dB (default)
0	0	1	12dB
0	1	0	10dB
0	1	1	8dB
1	0	0	6dB
1	0	1	4dB
1	1	0	2dB
1	1	1	0dB

b7 Ramp Up/Down enable 0 = off 1 = on
When bit 7 is set to 1 the MOD output signals are ramped to reduce transients in the transmitted signal. The ramp up/down time is set in the 'Ramp Rate Control' section of the Programming register (P4.6).

Bits 6 to 4 are reserved - set to 0.

b3	b2	b1	b0	Audio Output Attenuation
0	0	0	0	>60dB (default)
0	0	0	1	44.8dB
0	0	1	0	41.6dB
0	0	1	1	38.4dB
0	1	0	0	35.2dB
0	1	0	1	32.0dB
0	1	1	0	28.8dB
0	1	1	1	25.6dB
1	0	0	0	22.4dB
1	0	0	1	19.2dB
1	0	1	0	16.0dB
1	0	1	1	12.8dB
1	1	0	0	9.6dB
1	1	0	1	6.4dB
1	1	1	0	3.2dB
1	1	1	1	0dB

Note that fine level control of Output 1 and Output 2 can be achieved with the FINE OUTPUT GAIN 1 and FINE OUTPUT GAIN 2 registers (P4.2-3). These affect the MOD1, MOD2 and AUDIO outputs according to the routing set in registers $A7 and $B1.

8.1.10 Input Gain and Output Signal Routing – $B1 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Input 2 Gain			Input 1 Gain			MOD1 Source		MOD2 Source	AUDIO Source	Input 1 Routing		Input 2 Routing		0	0

b12	b11	b10	Input 1 Gain
b15	b14	b13	Input 2 Gain
0	0	0	0dB (default)
0	0	1	3.2dB
0	1	0	6.4dB
0	1	1	9.6dB
1	0	0	12.8dB
1	0	1	16.0dB
1	1	0	19.2dB
1	1	1	22.4dB

b7	MOD2 Source
0	bias -> MOD2 (default)
1	Output 2 -> MOD2

b6	AUDIO Source
0	bias -> AUDIO (default)
1	Output 1 -> AUDIO

b9	b8	MOD1 Source
0	0	bias (default)
0	1	bias
1	0	Output 1 -> MOD1
1	1	Output 2 -> MOD1

b5	b4	Input 1 Signal Routing
b3	b2	Input 2 Signal Routing
0	0	bias (default)
0	1	DISCN
1	0	ALTN
1	1	MICN

Output 1 and Output 2 signal sources are also defined in section 8.1.3.
Bits 1, 0 are reserved – clear to 0.

There are a number of applications where it may be desirable to split the processing across both inputs, such as monitoring two RF receivers, in which case, Input 1 could be routed from the DISCN input with voice and DSC or NWR processing set to Input 2 from the ALTN input.

Similarly, for the output routing, under normal operation, In Tx Mode, Output 1 would be routed to MOD1 and Output 2 to MOD2. The signals that appear on Output 1 and Output 2 are defined in the Tx MOD Mode register, $A7:b14 to b12.

If the AUDIO output is selected in Tx mode (using b6) it will present the signal that has been routed to Output 1. This can be used for “sidetone” when transmitting Inband signalling in 1 or 2-point modulation modes. In Rx mode, the Audio Process is automatically routed to Output 1.

An audio output is only available when in Rx or Tx Mode.

Note: Output 1 and Output 2 may show a transient when switched from Idle to Rx or Tx mode as they power on. It is therefore recommended that the MOD1, MOD2 or AUDIO output routing be set to V_{BIAS} for a short period before implementing the operational routing and enabling the signalling. For Tx operation, the following sequence has been used successfully:

$C1 – currently in Idle mode
Enable Tx mode:
$B1 - Mod1/2 set to V_{BIAS} (b9-b7 = 000_b)
$C1 - Tx Mode Enabled
Delay of > 700µs
$C1 - Tx Function Enabled (e.g., DSC)
$B1 - Output1/2 routed to MOD1, MOD2

8.1.11 Reserved – $B2 write

8.1.12 Reserved – $B3 write

8.1.13 Reserved – $B4 8-bit read

8.1.14 AuxADC Threshold Data – $B5 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADC Sel	High /Low	0	0	0	0	Aux ADC Threshold Data									

b15 AuxADC select 0 = AuxADC1 1 = AuxADC2
b14 high/low select 0 = low threshold 1 = high threshold
b13 *reserved* 0
b12 *reserved* 0
b11 *reserved* 0
b10 *reserved* 0
b9-0 Threshold Data

8.1.15 Reserved – $B6 write

8.1.16 NWR Status and Data – $BB read

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NWR Status				x	x	x	x	NWR SAME Data							

b15 NWR WAT tone status 0 = no tone 1 = WAT tone detected
b14 NWR SAME data terminator 0 = no data 1 = data terminator NNNN detected
b13 NWR SAME data header 0 = no data 1 = data header ZCZC detected
b12 NWR SAME data status 0 = no data 1 = data available
b11 *reserved*
b10 *reserved*
b9 *reserved*
b8 *reserved*
b7–0 NWR SAME data

8.1.17 Powerdown Control – $C0 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALT Amp	MIC Amp	DISC Amp	IP1 ENA	OP1 ENA	OP2 ENA	MOD1 ENA	MOD2 ENA	AUDIO ENA	BIAS	Reset	Protect	XTAL DIS	IP2 ENA	0	0

b15 ALT Amp Enable 0 = off 1 = enabled
b14 MIC Amp Enable 0 = off 1 = enabled
b13 DISC Amp Enable 0 = off 1 = enabled
b12 Input 1 Enable 0 = off 1 = enabled
b11 Output 1 Enable 0 = off 1 = enabled
b10 Output 2 Enable 0 = off 1 = enabled
b9 MOD1 Enable 0 = off 1 = enabled
b8 MOD2 Enable 0 = off 1 = enabled
b7 AUDIO Enable 0 = off 1 = enabled
b6 BIAS Block Enable 0 = off 1 = enabled
b5 Reset 0 = normal 1 = reset/powersave
b4 Program Block Protect 0 = normal 1 = protected
If cleared, the Program Blocks will be initialised on Power on or Reset. If set, then the Program Blocks will retain their previous contents.
b3 XTAL Disable 0 = enabled 1 = disabled / powersave
Setting this bit effectively stops all signal processing within the device.
b2 Input 2 Enable 0 = off 1 = enabled
b1 reserved 0 1 = DO NOT USE

b0 reserved 0 1 = DO NOT USE

Note: Care should be taken when writing to b5 and b3. These are automatically programmed to an operational state following a power-on (ie: all 0s). Writing a 1 to either b5 or b3 will effectively cause the device to cease all processing activity, including responding to other C-BUS commands (except General Reset, $01).

When b5 is set, the device will be held in reset and all signal processing will cease (including AuxADC operation.

When b3 is set the Xtal is disabled. When b3 is subsequently cleared, it may take some time for the clock signal to become stable, hence care should be taken in using this feature.

8.1.18 Mode Control – $C1 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Audio	NWR		Inband Modes				0	0	0	Data Mode			Idle/Rx/Tx	

b15	*reserved*	0	
b14	Audio Enable	0 = off	1 = enabled (uses Input 1 source)
b13	NWR Source	0 = Input 1	1 = Input 2
b12	NWR Enable	0 = off	1 = enabled (enables both WAT and SAME)
b11	Inband Source	0 = Input 1	1 = Input 2
b10	Audio Generator Enable	0 = off	1 = enabled
b9	*reserved*	0	
b8	DTMF Enable	0 = off	1 = enabled
b7	*reserved*	0	
b6	*reserved*	0	
b5	*reserved*	0	
b4	Modem Source	0 = Input 1	1 = Input 2
b3	*reserved*	0	
b2	Modem Enable	0 = off	1 = enabled
b1-0	Operational mode	00 Idle 01 Rx 10 Tx 11 *reserved*	

Changes to the settings of the bits in this register are implemented as soon as they are received over the C-BUS (note that the C-BUS has a potential latency of up to 250µs).

In Tx mode, it is only permissible to select ONE of the following at any time:

Audio
Inband Signalling
DSC Signalling

Note that if the Audio Processing bit (b14) is set at the same time as an Inband signalling bit in Tx mode, the Inband signal will be subjected to a 6dB gain.

It is essential that changes to the Programming register and the Audio Control register are completed before entering Rx or Tx mode.

The following other registers or bits can be changed as appropriate (Note: not all possible changes are appropriate), whilst the device is in Tx or Rx mode:

- Analogue Output Gain register ($B0)
- AuxADC and Tx MOD Mode register ($A7)
- Input Gain and Signal Routing register ($B1)
- Power Down Control register ($C0)
- Tx Inband Tones register ($C3)
- Tx Data registers ($CA & $CB)
- Audio Tone register ($CD)
- Interrupt Mask register ($CE)

8.1.19 Audio Control – $C2 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Scra-mble	0	Emph	12k5	25k	HPF	0	0	0	0	0	0	0	0	0	0

b15 Audio Scrambling Enable 0 = off 1 = enabled
b14 *reserved*
b13 Audio Pre/De-emphasis 0 = off 1 = enabled[6]
b12 Audio 12.5kHz Filter Enable 0 = off 1 = enabled
b11 Audio 25kHz Filter Enable 0 = off 1 = enabled
b10 Audio 300Hz HPF Enable 0 = off 1 = enabled

b9-0 reserved

8.1.20 Tx Inband Tones – $C3 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	twist	sgl	Tx DTMF Tone			

b15-6 reserved, clear to 0.
b5 DTMF Twist 0 = normal 1 = -2dB of twist applied to the lower DTMF tone.
b4 DTMF Single Tone 0 = normal 1 = Single Tone, see Table 3 DTMF Tone Pairs
b3-0 DTMF tone value – see Table 3 DTMF Tone Pairs

See section 8.1.21.

8.1.21 Rx Data 1 – $C5 read

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$C5	flag	DSC Character 0							flag	DSC Character 1						

This word holds the most recent bytes (Byte 0 and 1) of DSC data decoded. Received data is continuous, if the data is not read before the next data is received the current data will be over-written.
In DSC Formatted mode, if the flag bit (b15 or b7) is set, then the accompanying character has been received with an error detected.

[6] In order to pre-emphasise the FSK data, Program Block P0.0 bit 11 should be set.

8.1.22 Status – $C6 read

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IRQ	NWR	res	DTMF	res	res	Aux ADC2	Aux ADC1	Data End	Data RDY	res	res	DSC	res	res	PRG

b15 IRQ

Changes in the Status register will cause this bit to be set to 1 if the corresponding interrupt mask bit is enabled. An interrupt request is issued on the IRQN pin when this bit is 1 and the IRQ MASK bit (b15 of Interrupt Mask register, $CE) is set to 1.

b14 NWR status change

The NOAA Weather Receiver has detected a change in the status of the WAT tone or SAME data. The NWR data/status register $BB should be read to determine the exact cause.

b13 reserved

b12 DTMF event

A valid DTMF tone has been detected and can be read from the Tone Status register, $CC.

b11 *reserved*

b10 *reserved*

b9 AuxADC2 Threshold change

AUX ADC2 signal has just gone above the high threshold or has just gone below the low threshold. The AuxADC2 data register $AA should be read to determine the exact cause.

b8 AuxADC1 Threshold change

AUX ADC1 signal has just gone above the high threshold or has just gone below the low threshold The AuxADC1 data register $A9 should be read to determine the exact cause.

b7 Data End

Rx mode: this bit is not used, so its value should be ignored. See section 7.7.1.

Tx mode: this will be set when the last bit of DSC data has been transmitted. After allowing a short time delay associated with the external components and radio circuitry, the host may power down the CMX885 and transmitter or set the CMX885 to transmit or receive new information as appropriate.

b6 Data Ready

Tx mode: indicates that new transmit data is required.

Rx mode: received data is ready to be read.

For continuous transmission or reception of information, a data transfer should be completed within the time appropriate for that data.

b5 *reserved*

b4 *reserved*

b3 DSC

When set to 1, this bit indicates that a valid DSC data sequence has been received.

b2 *reserved*

b1 *reserved*

b0 PRG

When set to 1, this bit indicates that the Programming register, $C8 is available for the host to write to it. Cleared by writing to the Programming register, $C8

Bits 2 to 15 of the Status register are cleared to 0 after the Status register is read.

The data in this register is not valid if bit 5 of the Power Down Control register, $C0 is set to 1.

8.1.23 Modem Configuration – $C7 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SynC	SynD	SynT	En NWR Data	En DSC	En RAW	Last Tx Data	0	0	0	0	0	0	User Bit	0	0

This register configures the way the CMX885 handles DSC data in Tx and Rx modes.

b15 SynC detect 0 = off 1 = enabled
b14 SynD detect 0 = off 1 = enabled
b13 SynT detect 0 = off 1 = enabled
note: SynC, SynD and SynT patterns are defined in Program Blocks P0.0-3
b12 En_NWR_data 0 = disabled 1 = enabled
The En_NWR_data bit is required to disable the NWR SAME data decoder at the end of a data frame. The decoder will detect and respond to the arrival of a sync signal (if $C1:b12 is set to 1), and report any following data, however the host will need to decode the data from the CMX885, recognise the end of data and then disable the SAME decoder through this bit. Setting this bit to 1 will disable the sync search and output data immediately.
b11 En_DSC data mode 0 = disabled 1 = enabled
Setting this bit selects DSC modem operation. The Modem Enable bit $C1:b2 will start/stop the modem.
b10 En_RAW: 0 = data packetising on 1 = raw data mode
This bit selects the raw or formatted (data packetising) mode for DSC data.
DSC Receive mode:
b10 = 1: device will look for the programmed Frame Sync. pattern, raise an interrupt (if enabled) and decode the following data 16 bits at a time, making them available in Rx Data 1 register ($C5).
DSC Transmit mode:
b10 = 1: device will transmit data 16 bits at a time from Tx Data 1 register ($CA). Bit and frame sync pattern generation and all formatting of the data have to be performed by the host in this case.
b9 Last Tx data:
This is only valid when transmitting data in DSC formatted mode and indicates to the CMX885 that it can cease modulation. The host must set this bit to 1 immediately after the interrupt for 'load more data' occurs $C6:b6. In receive, or when transmitting other message formats, this bit must be cleared to 0.

b8-3 reserved, clear to 0

b2 User bit.
May be freely used by the host in DSC modes. This bit has no effect on the message format or encoding and will be reported in the Rx Data 1 register for the receiving host to use as appropriate. This bit could be used to indicate a special message, e.g. one containing handset or channel set-up information.
b1-0 reserved, clear to 0

8.1.24 Programming Register – $C8 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Program Block Address				Program Block Data											

See section 8.2 for a definition of program block operation.

8.1.25 Tx Data 1 – $CA write

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$CA	flag	DSC Character 0							flag	DSC Character 1						

This word holds the next 2 bytes (Byte 0 and 1) of DSC data to be transmitted. Outgoing data is continuous, if new data is not provided before the current data has been transmitted the current data will be re-transmitted, until new data is provided. Transmission of current data will be completed before transmission of newly loaded data begins. See section 7.7.2.

In DSC Formatted mode, if the flag bit (b15 or b7) is set, then the accompanying character is ignored.

8.1.26 Tone Status – $CC read

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Device Ident Code															
x	DTMF Tone Detected				DT	x	x	x	x	x	x	x	x	x	x

After power-on or General Reset, this register will contain the Device Ident code related to this particular device. The host µC may use this to confirm that the device is in its correct operational mode before attempting to actively use the device.

In normal operation, this word holds the current status of the CMX885 DTMF detector. This word should be read by the host after an interrupt caused by a DTMF event. In Tx mode this register will be cleared to 0.

b15 *reserved* – ignore this bit.

b10 set if b14-11 represent DTMF tone.

b14-11 Detected inband frequency; identifies the frequency by its position in Table 3 DTMF Tone Pairs. A change in the state of bits 14 to 10 will cause the Status register $C6:b12, to be set to 1.

b9-0 *reserved* – ignore these bits.

8.1.27 Audio Tone – $CD write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	Audio Tone Frequency											
0	0	1	0	Audio Tone Level											
0	1	0	0	Rx Voice Level											
0	1	1	0	Output1 Fine Gain (also see P4.2)											
1	0	0	0	Output2 Fine Gain (also see P4.3)											
1	0	1	0	Tx Voice Level Multiplier											
1	0	1	1	reserved											
1	1	0	0	MOD1 and MOD2 Fine Attenuation											
1	1	0	1	*reserved*											
1	1	1	0	*reserved*											
1	1	1	1	*reserved*											
				All other values reserved											

Bits 15-12 determine how the remaining bit fields will be interpreted:

0000_2:

When the appropriate bit of the Mode Control register $C1:b10 is set, an audio tone will be generated with the frequency set by bits (11-0) of the Audio Tone register in accordance with the formula below. If bits 11-0 are programmed with 0, no tone (i.e. V_{BIAS}) will be generated when the Audio Tone is enabled.

Frequency = Audio Tone (i.e. 1Hz per LSB)

The Audio Tone frequency should only be set to generate frequencies from 288Hz to 3000Hz.

The host should disable other audio band signalling and set the correct audio routing before generating an audio tone and re-enable signalling and audio routing on completion of the audio tone. The timing of intervals between these actions is controlled by the host µC.

This register may be written to whilst the audio tone is being generated, any change in frequency will take place after the end of the C-BUS write to this register. This allows complex sequences (e.g. ring or alert tunes) to be generated for the local speaker (Tx or Rx via the AUDIO pin) or transmitted signal (Tx via the MOD1/MOD2 pins).

0010_2:

The Audio Tone Level may be attenuated by the value written to b11-0. The default value of $FFF is equivalent to x1. Note that this adjustment will affect ALL signals generated by the In-Band signalling block (DTMF, FSK, Audio Tone). This register operates in parallel with P1.0 so that the last register written ($CD with value $2xxx or $C8 P1.0 with value $Dxxx) will set the attenuation. Note that successive writes to $CD register will only be actioned if the data values are different, even if another register is accessed in between.

Example:

The writes $CD=$2123, $C8=$D456, $C3=2123 will result in the last write to $CD being ignored, whereas the writes $CD=$2123, $C8=$D456, $CD=2124 will result in the last write to $CD being actioned.

0100_2:

In Rx mode, the voice level may be attenuated by the value written to b11-0. The default value of $FFF is equivalent to x1. Note that this adjustment will only affect signals in the voice processing path as enabled by the Mode Control register $C1:b14. This allows the voice level to be adjusted “on-the-fly” and in conjunction with the Audio Output attenuator $B0:b3 to b0, offers a “fine gain” volume control. Approximate values for 0.2dB steps are shown in Table 5.

b11-0 Value (hex)	Attenuation (dB)	b11-0 Value (hex)	Attenuation (dB)
FFF	0	D50	1.6
F90	0.2	CF0	1.8
F40	0.4	CB0	2.0
EE0	0.6	C60	2.2
EA0	0.8	C20	2.4
E50	1.0	BF0	2.6
DE0	1.2	BA0	2.8
DA0	1.4	B60	3.0

Table 5 Voice Level Attenuation

0110_2:

The Output 1 level may be attenuated by the value written to b11-0. The default value of $FFF is equivalent to x1. This register operates in parallel with P4.2, but allows the level to be adjusted “on-the-fly” without needing to drop back into Idle mode. Approximate values are shown in Table 6.

1000_2:

The Output 2 level may be attenuated by the value written to b11-0. The default value of $FFF is equivalent to x1. This register operates in parallel with P4.4, but allows the level to be adjusted “on-the-fly” without needing to drop back into Idle mode. Approximate values are shown in Table 6.

b11-0 Value (hex)	Attenuation (dB)	b11-0 Value (hex)	Attenuation (dB)
FFF	0	CB5	2.0
FA2	0.2	C6B	2.2
F47	0.4	C22	2.4
EEE	0.6	BDC	2.6
E97	0.8	B97	2.8
E42	1.0	B53	3.0
DEF	1.2	B11	3.2
D9D	1.4	AD1	3.4
D4E	1.6	AB1	3.5
D01	1.8		

Table 6 Output 1 and 2 Level Attenuation

Gain = 20 x log(OG / 4095)dB. OG is the unsigned integer value in the ‘Fine Output Gain’ field.

Please note that differences between the calculated values and measured levels is due to truncation of the programmed values.

1010_2:

This sets the value of the Tx Voice Level Multiplier at the output of the Tx limiter stage. This can be useful in situations where it has been necessary to use a small limiting threshold and still maintain an acceptable level at the MOD outputs. The default state is x1.

b2	b1	b0	Tx Voice Level Multiplier
0	0	0	x1
0	0	1	x2
0	1	0	x4
0	1	1	x8
1	0	0	x16
1	0	1	x32

1100_2:

MOD1 and MOD2 fine attenuator controls. In conjunction with the coarse attenuator register ($B0), these bits allow fine control over the MOD1 and MOD2 levels in 0.2dB steps. Additional gain and offset control of Output 1 and Output 2 is also provided in register $CD:0111 and $CD:1000 settings as well as Program Blocks P4.2 – 4.5. These bits may be changed whilst the device is in Tx or Rx modes.

b3	b2	b1	b0	MOD1 Fine Output Attenuation
b7	**b6**	**b5**	**b4**	**MOD2 Fine Output Attenuation**
0	0	0	0	0dB
0	0	0	1	0.2dB
0	0	1	0	0.4dB
0	0	1	1	0.6dB
0	1	0	0	0.8dB
0	1	0	1	1.0dB
0	1	1	0	1.2dB
0	1	1	1	1.4dB
1	0	0	0	1.6dB
1	0	0	1	1.8dB

8.1.28 Interrupt Mask – $CE write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IRQ	NWR	0	DTMF	0	0	Aux ADC2	Aux ADC1	Data End	Data RDY	0	0	DSC	0	0	PRG

Bit	Value	Function
15	1	Enable selected interrupts
	0	Disable all interrupts (IRQN pin not activated)
14	1	Enable NWR detection
	0	Disabled
13	0	*reserved*
12	1	Enable interrupt when a valid DTMF tone is detected
	0	Disabled
11	0	*reserved*
10	0	*reserved*
9	1	Enable interrupt when the Aux ADC 2 status bit changes
	0	Disabled
8	1	Enable interrupt when the Aux ADC 1 status bit changes
	0	Disabled
7	1	Enable interrupt when DSC data transmission has ended
	0	Disabled
6	1	Enable interrupt when a DSC data transfer is required
	0	Disabled
5	0	*reserved*
4	0	*reserved*
3	1	Enable interrupt when valid DSC data is detected
	0	Disabled
2	0	*reserved*
1	0	*reserved*
0	1	Enable interrupt when Prog Flag bit of the Status register changes from 0 to 1 (see Programming register $C8)
	0	Disabled

8.1.29 Reserved – $CF write

This C-BUS address is allocated for production testing and must not be accessed in normal operation.

8.2 Programming Register Operation

In order to support radio systems that may not comply with the default settings of the CMX885, a set of Program Blocks is available to customise the features of the device. It is envisaged that these blocks will usually only be written to following a power-on of the device and hence can only be accessed while the device is in Idle mode. Access to these blocks is via the Programming register ($C8).

All other interrupt sources should be disabled and the AuxADCs switched off while loading the Program Blocks.

The Programming register should only be written to when the PRG flag in the Status register $C8:b0 is set to 1 and the Rx and Tx modes are disabled (bits 0 and 1 of the Mode Control register both 0) and the AuxADC is disabled.

The PRG flag is cleared when the Programming register is written to by the host. When the corresponding programming action has been completed (normally within the C-BUS latency period, 250µs) the CMX885 will set the flag back to 1 to indicate that it is now safe to write the next programming value. The Programming register must not be written to while the PRG flag bit is 0. Programming is performed by writing a sequence of 16-bit words to the Programming register in the order shown in the following tables. Writing data to the Programming register MUST be performed in the order shown for each of the blocks, however the order in which the blocks are written is not critical. If later words in a block do not require updating the user may stop programming that block when the last change has been performed. e.g. If only 'Fine output Atten 1' needs to be changed the host will need to write to P4.0, P4.1 and P4.2 only.

The user must not exceed the defined word counts for each block.

The internal pointer for each Program block write is initialised by setting bit 15 to 1. Bits 14-12 are then used to select the particular Program block in use as shown in Table 7. Subsequent writes to the Program Register (with b15 cleared to 0) will increment the pointer until the end of the Program Block is reached. Program Block 3 has an additional feature to facilitate RAMDAC programming, where the first eleven entries of the block may be skipped by setting both b15 and b10 to 1 to initialise the pointer directly to the start of the RAMDAC table.

Table 7 Program Block Selection

b15	b14	b13	b12		Bit Field (max)
1	0	x	x	Select Block 4	14
1	1	0	0	Select Block 0	12
1	1	0	1	Select Block 1	12
1	1	1	0	Select Block 2	12
1	1	1	1	Select Block 3	12

Once the final write to the Programming register has been executed, a final check of the PRG flag should be performed before returning to normal operation.

8.2.1 Program Block 0 – Modem Configuration

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P0.0	1	1	0	0	Pre	0			DSC Frame SynC LSB							
P0.1	0	1	0	0	0				DSC Frame SynC MSB							
P0.2	0	1	0	0	0				DSC Frame SynD LSB							
P0.3	0	1	0	0	0				DSC Frame SynD MSB							
P0.4	0	1	0	0	0				*reserved*							
P0.5	0	1	0	0	0				*reserved*							
P0.6	0	1	0	0	0				*reserved*							
P0.7	0	1	0	0	0				*reserved*							
P0.8	0	1	0	0	0				DSC Bit Sync LSB							
P0.9	0	1	0	0	0				DSC Bit Sync MSB							

Default values:

P0.0	$23	P0.5	$00
P0.1	$CB	P0.6	$00
P0.2	$33	P0.7	$00
P0.3	$B4	P0.8	$55
P0.4	$00	P0.9	$55

This initiates the device with the DSC frame sync pattern of $CB23 and bit sync of alternate 1s and 0s.

$C8 (P0.0-3) DSC Frame Sync

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P0.0	1	1	0	0	Pre	0			DSC Frame SynC LSB							
P0.1	0	1	0	0	0				DSC Frame SynC MSB							
P0.2	0	1	0	0	0				DSC Frame SynD LSB							
P0.3	0	1	0	0	0				DSC Frame SynD MSB							

Bits 7 to 0 set the Frame Sync pattern used in Tx and Rx DSC data. Bit 7 of the MSB is compared to the earliest received data. Note that SynT is the inverse pattern of SynC.

Bit 11 enables pre-emphasis on DSC transmission.

$C8 (P0.4-7) reserved

$C8 (P0.8-9) DSC Bit Sync

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P0.8	0	1	0	0	0				DSC Bit Sync LSB							
P0.9	0	1	0	0	0				DSC Bit Sync MSB							

This bit pattern is used when transmitting the bit sync.

8.2.2 Program Block 1 – Inband Tone Setup

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1.0	1	1	0	1	Audio Band Tones/Data Tx Level											0

Default values: P1.0: $800

$C8 (P1.0) Audio Band Tones Tx Level

Bits 11 (MSB) to 1 (LSB) set the transmitted DTMF, Audio Tone and FSK signal level (pk-pk) with a resolution of AV_{DD}/2048 per LSB (1.611mV per LSB at AV_{DD}=3.3V). Valid range for this value is 0 to 1536 – use with care as higher values may result in signal "clipping".
Bit 0 reserved

8.2.3 Program Block 2 – reserved

8.2.4 Program Block 3 – AuxDAC, RAMDAC and Clock Control

This block is divided into two sub-blocks to facilitate loading the RAMDAC buffer. Set bit 15 to restart a loading sequence. If bit 10 is set then loading the first ten locations will be skipped. If bit 10 is clear, the first ten locations must be loaded before continuing to the RAMDAC load.

The internal clock dividers only require modification if a non-standard XTAL frequency is used (see Table 2).

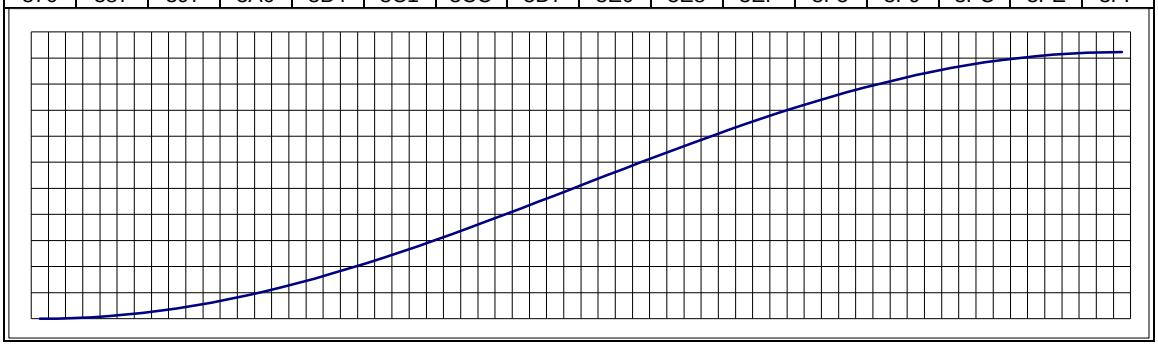
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P3.0	1	1	1	1	0	0	0	0	AuxADC1 Average Counter							
P3.1	0	1	1	1	0	0	0	0	*reserved*							
P3.2	0	1	1	1	GP Timer value in Idle mode											
P3.3	0	1	1	1	VCO output and AUX clk divide in Idle mode											
P3.4	0	1	1	1	Ref clk divide in Rx or Tx mode											
P3.5	0	1	1	1	PLL clk divide in Rx or Tx mode											
P3.6	0	1	1	1	VCO output and AUX clk divide in Rx or Tx mode											
P3.7	0	1	1	1	0	0	0	0	Internal ADC/DAC clk divide in Rx or Tx mode							
P3.8	0	1	1	1	0	0	0	0	ADC Internal Control 1							
P3.9	0	1	1	1	0	0	0	0	ADC Internal Control 2							
P3.10	0	1	1	1	0	0	0	0	0	0	0	0	ADC Internal Control 3			
P3.11	1	1	1	1	0	1	User Defined RAMDAC Data 0									
P3.xx	0	1	1	1	0	1	User Defined RAMDAC Data xx									
P3.74	0	1	1	1	0	1	User Defined RAMDAC Data 63									

Default Values:

P3.0	$000
P3.1	$000
P3.2 - P3.7:	see Table 2
P3.8	$000 – reserved, do not change
P3.9	$101 – reserved, do not change
P3.10	$002 – reserved, do not change
P3.11 - P3.74:	see Table 8

Table 8 RAMDAC Values

Default RAMDAC Contents After Reset (hex)															
0 000	1 001	2 003	3 006	4 00A	5 010	6 017	7 01F	8 028	9 033	10 03E	11 04B	12 059	13 068	14 078	15 089
16 09A	17 0AD	18 0C1	19 0D5	20 0EA	21 100	22 116	23 12D	24 145	25 15D	26 175	27 18E	28 1A7	29 1C0	30 1D9	31 1F3
32 20C	33 226	34 23F	35 258	36 271	37 28A	38 2A2	39 2BA	40 2D2	41 2E9	42 2FF	43 315	44 32A	45 33E	46 352	47 365
48 376	49 387	50 397	51 3A6	52 3B4	53 3C1	54 3CC	55 3D7	56 3E0	57 3E8	58 3EF	59 3F5	60 3F9	61 3FC	62 3FE	63 3FF



8.2.5 Program Block 4 – Gain and Offset Setup

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.0	1	0	Fine Input Gain 1													
P4.1	0	0	Fine Input Gain 2													
P4.2	0	0	Fine Output Gain 1													
P4.3	0	0	Fine Output Gain 2													
P4.4	0	0	Output 1 Offset Control													
P4.5	0	0	Output 2 Offset Control													
P4.6	0	0	Ramp Rate Control													
P4.7	0	0	Limiter Setting													
P4.8	0	0	Scrambler Inversion Frequency													
P4.9	0	0	Audio Filter Sequence													
P4.10	0	0	*reserved*													
P4.11	0	0	Input AGC Threshold Level													

Default values:

P4.0	$8000	P4.6	$0000
P4.1	$0000	P4.7	$3FFF
P4.2	$0000	P4.8	$119A
P4.3	$0000	P4.9	$001B
P4.4	$0000	P4.10	$0608
P4.5	$0000	P4.11	$0FFF

$C8 (P4.0) Fine Input Gain 1 and Fine Input Gain 2

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.0	1	0	Fine Input Gain 1 (unsigned integer)													
P4.1	0	0	Fine Input Gain 2 (unsigned integer)													

Gain = 20 × log([32768-IG]/32768)dB. IG is the unsigned integer value in the 'Fine Input Gain' field.

Fine input gain adjustment should be kept within the range 0 to -3.5dB. This adjustment occurs after the coarse input gain adjustment (register $B1)

$C8 (P4.2-3) Fine Output Gain 1 and Fine Output Gain 2

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.2	0	0	Fine Output Gain 1 (unsigned integer)													
P4.3	0	0	Fine Output Gain 2 (unsigned integer)													

Approximate values are shown in Table 9:

b13-0 Value (hex)	Attenuation (dB)	b13-0 Value (hex)	Attenuation (dB)
0	0	1A53	2.0
2EA	0.2	1CA4	2.2
5C3	0.4	1EE7	2.4
88B	0.6	211D	2.6
B43	0.8	2346	2.8
DEB	1.0	2562	3.0
1084	1.2	2772	3.2
130E	1.4	2976	3.4
1589	1.6	2A74	3.5
17F5	1.8		

Table 9 Output 1 and 2 Level Attenuation

Gain = 20 × log([32768-OG]/32768)dB. OG is the unsigned integer value in the 'Fine Output Gain' field. Note that differences between the calculated values and measured levels is due to truncation of the programmed values.

Fine output gain adjustment should be kept within the range 0dB to -3.5dB. This adjustment occurs before the coarse output gain adjustment (register $B0). Alteration of Fine Output Gain 1 will affect the gain of both MOD1 and AUDIO outputs.

$C8 (P4.4-5) Output 1 Offset and Output 2 Offset

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.4	0	0	2's complement Offset for MOD1, resolution = AV_{DD} / 65536 per LSB													
P4.5	0	0	2's complement Offset for MOD2, resolution = AV_{DD} / 65536 per LSB													

The programmed value is subtracted from the output signal. Can be used to compensate for inherent offsets in the output path via MOD1 (Output 1 Offset) and MOD2 (Output 2 Offset). It is recommended that the offset correction is kept within the range +/-50mV. This adjustment occurs before the coarse output gain adjustment (register $B0), therefore an alteration to the latter register will require a compensation to be made to the output offsets.

$C8 (P4.6) Ramp Rate Control

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.6	0	0	Ramp Rate Up Control (RRU)							Ramp Rate Down Control (RRD)						

The ramp-up and ramp-down rates can be independently programmed. The ramp rates apply to all the analogue output ports. They only affect those ports being turned on (ramp-up) or turned off (ramp down). The ramp rates should be programmed before ramping any outputs.

Time to ramp-up to full gain = (1 + RRU) × 1.333ms
Time to ramp down to zero gain = (1 + RRD) × 1.333ms

Ramp up starts from when the transmit mode starts (Mode Control Register $C1:b1 set to 1). Ramp down starts from when transmit mode is turned off (Mode Control Register $C1:b1 cleared to 0).

$C8 (P4.7) Transmit Limiter Control

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.7	0	0	Limiter Setting													

This unsigned number sets the clipping point (maximum deviation from the centre value) for the MOD1 and MOD2 pins. The maximum setting ($3FFF) is $V_{BIAS} \pm (AV_{DD}/2)$ i.e. output limited from 0 to AV_{DD}.

For an AV_{DD} of 3.3V, the resolution is approx. 0.3mV per LSB.

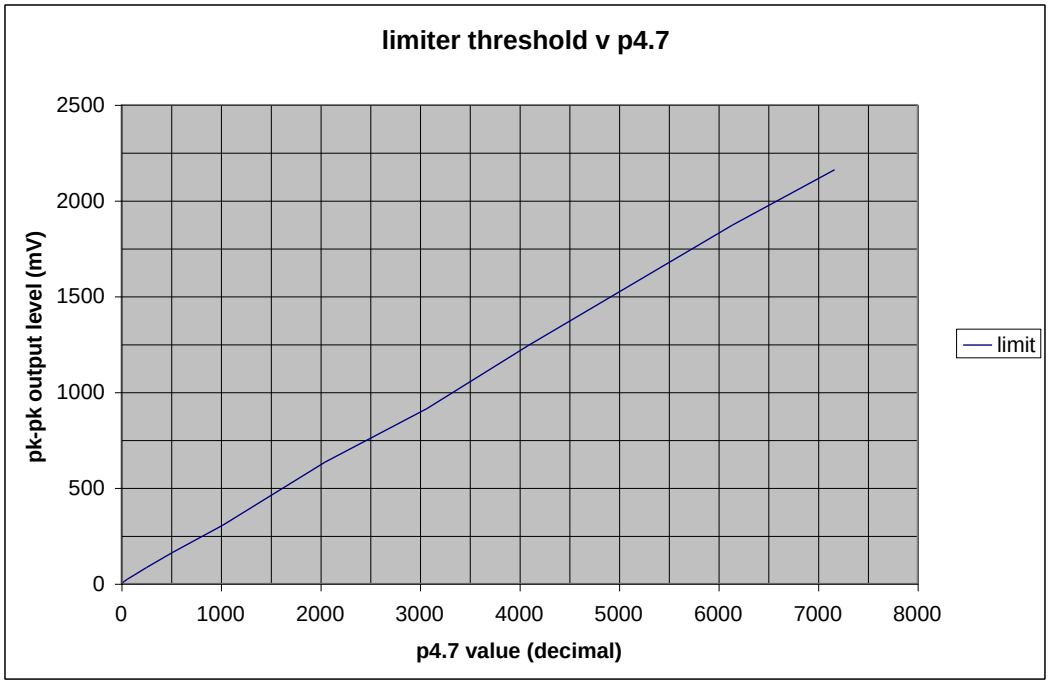


Figure 15 Limiter Values

The limiter is set to maximum following a C-BUS Reset or a Power-up Reset. The levels of internally generated signals may need to be adjusted by setting appropriate transmit levels to avoid unintentional limiting.

$C8 (P4.8) Scrambler Inversion Frequency

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.8	0	0	Scrambler Inversion Frequency = f / 0.7324													

This unsigned hex number sets the inversion frequency for the Voice Scrambler and de-Scrambler (Default is 3300Hz).

$C8 (P4.9) Audio Filter Sequence

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.9	0	0	Limit	src	Input AGC				Pre-emp		0	1	Scramble		300Hz	

b13 sets the position of the limiter in the Audio Processing chain. The default is a soft limiter function; setting this bit provides a hard limiter function (placing the limiter at the output of the channel filter).

b12 sets the source of the reference signal when InputAGC function is active.

0 = Audio Input
1 = Pre-emphasis output

b11-8 control the hardware InputAGC function and its release timer for Voice / Audio signals on Input 1 in 64ms steps:

0000	InputAGC off
0001	InputAGC on, release time = 64ms
0010	InputAGC on, release time = 128ms
0011	InputAGC on, release time = 196ms
0100	InputAGC on, release time = 256ms
0101	InputAGC on, release time = 320ms
- - - -	- -
1111	InputAGC on, release time = 960ms

b7-0 set the order of the Audio Filter processing. This feature can be used to optimise the signal to noise performance of particular radio hardware designs. Each filter/process block can be specified in any order. Each two-bit field specifies the order in which the process will be executed in Tx mode, therefore it is imperative that each set of bit fields be different. The reverse sequence is used in Rx mode. The Voice Filter and Soft Limiter will always be implemented as the final block in the Tx sequence.

The default settings (P4.9 = $001B) are:

- Pre-emph: 00
- Dummy: 01
- Scramble: 10
- 300Hz HPF: 11

which will implement the line-up as shown below:

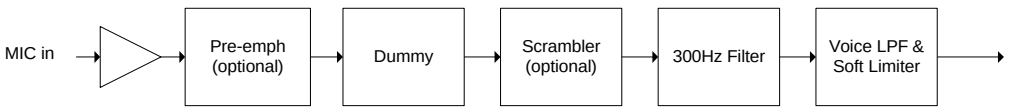


Figure 16 Default Tx Audio Filter Line-up

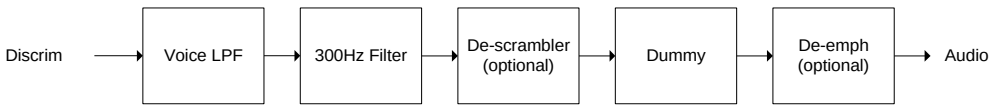


Figure 17 Default Rx Audio Filter Line-up

An alternative, preferred, line-up is shown below for the following settings (P4.9 = $004B):

- Dummy: 01
- Pre-emph: 00
- Scramble: 10
- 300Hz HPF: 11

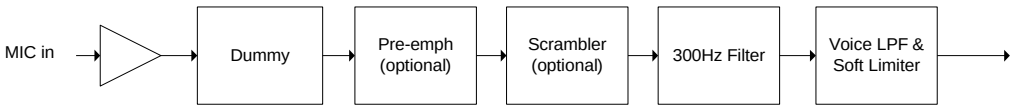


Figure 18 Preferred Tx Audio Filter Line-up

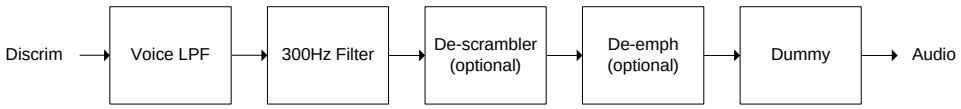


Figure 19 Preferred Rx Audio Filter Line-up

$C8 (P4.10) Reserved – do not use

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.10	0	0	*reserved* – set to $0608													

Reserved – set to $0608

$C8 (P4.11) Input AGC Threshold Level

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.11	0	0	Threshold Setting, resolution = AV_{DD}/16384 per LSB													

This unsigned number sets the threshold point (maximum deviation from the centre value) for the Input AGC function, where the input gain will be stepped to avoid exceeding the specification limits.

The threshold is set to half of full-scale ($0FFF = $V_{BIAS} \pm (AV_{DD}/4)$) following a C-BUS Reset or a Power-Up Reset.

8.2.6 Initialisation of the Program Blocks

Removal of the Signal Processing block from reset (Power Down register, $C0:b5 1→ 0 transition), with b4 kept low (= 0), will cause all of the Program Blocks (P0 – P4) to be reset to their default values.

9 Performance Specification

9.1 Electrical Performance

9.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Unit
Supply: DV_{DD}- DV_{SS}	–0.3	4.5	V
AV_{DD}- AV_{SS}	–0.3	4.5	V
Voltage on any pin to DV_{SS}	–0.3	DV_{DD} + 0.3	V
Voltage on any pin to AV_{SS}	–0.3	AV_{DD} + 0.3	V
Current into or out of any power supply pin (excluding VBIAS) (i.e. VDEC, AVDD, AVSS, DVDD, $DVSS_)$	–30	+30	mA
Current into or out of any other pin	–20	+20	mA
Voltage differential between power supplies:			
DV_{DD} and AV_{DD}	0	0.3	V
DV_{SS} and AV_{SS}	0	50	mV

Q3 Package (48-pin VQFN)	Min.	Max.	Unit
Total Allowable Power Dissipation at Tamb = 25°C	–	1750	mW
... Derating	–	17.5	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

L4 Package (48-pin LQFP)	Min.	Max.	Unit
Total Allowable Power Dissipation at Tamb = 25°C	–	1600	mW
... Derating	–	16	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

9.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Unit
Supply Voltage:				
DV_{DD} – DV_{SS}		3.0	3.6	V
AV_{DD} – AV_{SS}		3.0	3.6	V
V_{DEC} – DV_{SS}	12	2.25	2.75	V
Operating Temperature		–40	+85	°C
XTAL/CLK Frequency (using a Xtal)	11	3.0	12.288	MHz
XTAL/CLK Frequency (using an external clock)	11	3.0	24.576	MHz

Notes: 11 Nominal XTAL/CLK frequency is 3.6864MHz.
12 The V_{DEC} supply is automatically created from DV_{DD} by the on-chip voltage regulator.

9.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

External components as recommended in Figure 2.
Maximum load on digital outputs = 30pF.
Xtal Frequency = 3.6864MHz ±0.01% (100ppm); Tamb = –40°C to +85°C.
AV_{DD} = DV_{DD} = 3.0V to 3.6V.
Reference Signal Level = 308mV rms at 1kHz with AV_{DD} = 3.3V.
Signal levels track with supply voltage, so scale accordingly.
Signal to Noise Ratio (SNR) in bit rate bandwidth.
Input stage gain = 0dB. Output stage attenuation = 0dB.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Supply Current	21				
All Powersaved					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	8	100	µA
AI_{DD} (AV_{DD} = 3.3V)		–	4	20	µA
Idle Mode	22				
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	1.12	–	mA
AI_{DD} (AV_{DD} = 3.3V)		–	50	–	µA
Rx Mode	22				
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	5.00	–	mA
AI_{DD} (AV_{DD} = 3.3V)		–	3.20	–	mA
Tx Mode	22				
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	5.75	–	mA
AI_{DD} (AV_{DD} = 3.3V)	24	–	3.20	–	mA
Additional current for Auxiliary ADC					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	50	–	µA
Additional current for each Auxiliary DAC					
AI_{DD} (AV_{DD} = 3.3V)		–	200	–	µA

Notes: 21 Tamb = 25°C. Not including any current drawn from the device pins by external circuitry.
22 Auxiliary circuits disabled, Bias enabled.
24 Single MOD output enabled.

DC Parameters (continued)	Notes	Min.	Typ.	Max.	Unit
XTAL/CLK	25				
Input Logic 1		70%	–	–	DV_{DD}
Input Logic 0		–	–	30%	DV_{DD}
Input Current (Vin = DV_{DD})		–	–	40	µA
Input Current (Vin = DV_{SS})		–40	–	–	µA
C-BUS Interface and Logic Inputs					
Input Logic 1		70%	–	–	DV_{DD}
Input Logic 0		–	–	30%	DV_{DD}
Input Leakage Current (Logic 1 or 0)	21	–1.0	–	1.0	µA
Input Capacitance		–	–	7.5	pF
C-BUS Interface and Logic Outputs					
Output Logic 1 (I_{OH} = 120µA)		90%	–	–	DV_{DD}
(I_{OH} = 1mA)		80%	–	–	DV_{DD}
Output Logic 0 (I_{OL} = 360µA)		–	–	10%	DV_{DD}
(I_{OL} = -1.5mA)		–	–	15%	DV_{DD}
"Off" State Leakage Current	21	–	–	10	µA
IRQN (Vout = DV_{DD})		–1.0	–	+1.0	µA
RDATA (output HiZ)		–1.0	–	+1.0	µA
V_{BIAS}	26				
Output Voltage Offset wrt $AV_{DD}/2$ (I_{OL} < 1µA)		–	±2%	–	AV_{DD}
Output Impedance		–	22	–	kΩ

Notes: 25 Characteristics when driving the XTAL/CLK pin with an external clock source.

26 Applies when utilising V_{BIAS} to provide a reference voltage to other parts of the system. When using V_{BIAS} as a reference, V_{BIAS} must be buffered. V_{BIAS} must always be decoupled with a capacitor as shown in Figure 2.

AC Parameters (continued)	Notes	Min.	Typ.	Max.	Unit
XTAL/CLK Input					
'High' Pulse Width	31	15	–	–	ns
'Low' Pulse Width	31	15	–	–	ns
Input Impedance (measured at 6.144MHz)					
Powered-up Resistance		–	150	–	kΩ
Capacitance		–	20	–	pF
Powered-down Resistance		–	300	–	kΩ
Capacitance		–	20	–	pF
Xtal Start Up (from powersave)		–	400	–	ms
Auxiliary SYSCLK1/2 Outputs					
XTAL/CLK Input to CLOCK_OUT Timing:					
(in high to out high)	32	–	15	–	ns
(in low to out low)	32	–	15	–	ns
'High' pulse width	33	127	135.63	144	ns
'Low' pulse width	33	127	135.63	144	ns
V_{BIAS}					
Start up time (from powersave)		–	30	–	ms
Microphone, Alternative and Discriminator Inputs (MICN, ALTN, DISCN)					
Input impedance	34	–	1	–	MΩ
Maximum Input Level (pk-pk)	35	–	–	80%	AV_{DD}
Load Resistance (feedback pins)		80	–	–	kΩ
Amplifier Open Loop Voltage Gain (I/P = 1mV rms at 100Hz)		–	60	–	dB
Unity Gain Bandwidth		–	1.0	–	MHz
Programmable Input Gain Stage	36				
Gain (at 0dB)	37	−0.5	0	+0.5	dB
Cumulative Gain Error (wrt attenuation at 0dB)	37	−1.0	0	+1.0	dB

Notes:

31 Timing for an external input to the XTAL/CLK pin.

32 XTAL/CLK input driven by an external source

33 3.6864MHz XTAL .

34 With no external components connected.

35 Centred about $AV_{DD}/2$; after multiplying by the gain of input circuit (with external components connected).

36 Gain applied to signal at output of buffer amplifier: DISCFB, ALTFB OR MICFB

37 Design value for this block only in test mode. Overall attenuation input to output has a tolerance of 0dB ±1.0dB.

AC Parameters (continued)	Notes	Min.	Typ.	Max.	Unit
Modulator Outputs 1/2 and Audio Output (MOD1, MOD2, AUDIO)					
Power-up to Output Stable	41	–	50	100	µs
Modulator Attenuators					
Attenuation (at 0dB)	43	−1.0	0	+1.0	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)		−0.6	0	+0.6	dB
Output Impedance Enabled	42	–	600	–	Ω
Output Impedance Disabled	42	–	500	–	kΩ
Output Current Range (AV_{DD} = 3.3V)		–	–	±125	µA
Output Voltage Range	44	0.5	–	AV_{DD} –0.5	V
Load Resistance		20	–	–	kΩ
Audio Attenuator					
Attenuation (at 0dB)	43	−1.0	0	+1.0	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)		−1.0	0	+1.0	dB
Output Impedance Enabled	42	–	600	–	Ω
Output Impedance Disabled	42	–	500	–	kΩ
Output Current Range (AV_{DD} = 3.3V)		–	–	±125	µA
Output Voltage Range	44	0.5	–	AV_{DD} –0.5	V
Load Resistance		20	–	–	kΩ

Notes:

41 Power-up refers to issuing a C-BUS command to turn on an output. These limits apply only if V_{BIAS} is on and stable. At power supply switch-on, the default state is for all blocks, except the XTAL and C-BUS interface, to be placed in powersave mode.

42 Small signal impedance, at AV_{DD} = 3.3V and Tamb = 25°C.

43 With respect to the signal at the feedback pin of the selected input port.

44 Centred about $AV_{DD}/2$; with respect to the output driving a 20kΩ load to $AV_{DD}/2$.

AC Parameters (continued)	Notes	Min.	Typ.	Max.	Unit
Auxiliary Signal Inputs (Aux ADC 1)					
Source Output Impedance	51	–	–	24	kΩ
Auxiliary 10 Bit ADC					
Resolution		–	10	–	Bits
Maximum Input Level (pk-pk)	54	–	–	80%	AV_{DD}
Conversion Time	52	–	250	–	µs
Input Impedance					
Resistance		–	10	–	MΩ
Capacitance		–	5	–	pF
Zero Error (input offset to give ADC output = 0)		0	–	±10	mV
Integral Non-linearity		–	–	±3	LSBs
Differential Non-linearity	53	–	–	±1	LSBs
Auxiliary 10 Bit DACs					
Resolution		–	10	–	Bits
Maximum Output Level (pk-pk), no load	54	80%	–	–	AV_{DD}
Zero Error (output offset from a DAC input = 0)		0	–	±10	mV
Resistive Load		5	–	–	kΩ
Integral Non-linearity		–	–	±4	LSBs
Differential Non-linearity	53	–	–	±1	LSBs

Notes:

51 Denotes output impedance of the driver of the auxiliary input signal, to ensure < 1 bit additional error under nominal conditions.

52 With an auxiliary clock frequency of 3.6864MHz.

53 Guaranteed monotonic with no missing codes.

54 Level centered about $AV_{DD}/2$.

9.1.4 Parametric Performance

For the following conditions unless otherwise specified:

External components as recommended in Figure 2.
Maximum load on digital outputs = 30pF.
Xtal Frequency = 3.6864MHz±0.003% (30ppm)[§]; Tamb = –40°C to +85°C.
AV_{DD} = DV_{DD} = 3.0V to 3.6V.
Reference Signal Level = 308mVrms at 1kHz with AV_{DD} = 3.3V.
Signal levels track with supply voltage, so scale accordingly.
Signal to Noise Ratio (SNR) in bit rate bandwidth.
Input stage gain = 0dB, Output stage attenuation = 0dB.

AC Parameters	Notes	Min.	Typ.	Max.	Unit
DSC Decoder					
Signal Input Dynamic Range	81	100	–	800	mVrms
Bit Error Rate (SNR = 8dB)	81	–	<1	–	10^{-2}
Co-channel Rejection		–	10	–	dB
Bit Rate Sync Time		–	2	–	edges
DTMF Decoder					
Sensitivity		–	–22	+3	dB
Response Time		–	35	–	ms
De-response Time		–	–	45	ms
Falsing Rate (per 30min voice input)		–	10	–	
Frequency Tolerance		–	±2.5	–	%
Twist		–10	–	+10	dB
NWR Decoder					
Sensitivity		–	TBD	–	dB
Inband Tone Encoder					
Frequency Range		288	–	3000	Hz
Tone Frequency Accuracy		–	–	±0.3	%
Tone Amplitude Tolerance	83	–1.0	0	+1.0	dB
Total Harmonic Distortion	82	–	2.0	4.0	%
DTMF Encoder					
Output Signal Level	84	–	775	–	mVrms
Output Level Variation		–	± 0.5	–	dB
Output Distortion		–	–	5	%
DSC Encoder					
Output Signal Level		–	775	–	mVrms
Output Distortion		–	–	5	%
3rd Harmonic Distortion		–	–	3	%
Logic 1 Frequency		–	1300	–	Hz
Logic 0 Frequency		–	2100	–	Hz
Baud Rate		–	1200	–	bps
Pre-emphasis (per octave)		–	6	–	dB

Notes:

§ To meet DSC specifications, a 30ppm xtal, or better, is required.

81 AV_{DD} = 3.3V, for a "101010101 … 01" pattern measured at the input amplifier feedback pin. Signal level scales with AV_{DD}.

82 Measured at MOD1 or MOD2 output.

83 AV_{DD} = 3.3V and Tx Audio Level set to 871mV p-p (308mVrms).

84 AV_{DD} = 3.3V. Measured in single tone mode, P1.0 set to $DFFE.

AC Parameters (continued)	Notes	Min.	Typ.	Max.	Unit
Analogue Channel Audio Filtering					
Pass-band (nominal bandwidth):					
Received Audio	91	300	–	3300	Hz
12.5kHz Channel Transmitted Audio	92	300	–	2550	Hz
25kHz Channel Transmitted Audio	93	300	–	3000	Hz
Pass-band Gain (at 1.0kHz)		–	0	–	dB
Pass-band Ripple (wrt gain at 1.0kHz)		−2.0	0	+0.5	dB
Stop-band Attenuation		33.0	–	–	dB
Residual Hum and Noise Tx	96	–	−47	–	dBm
Residual Hum and Noise Rx	96	–	−74	–	dBm
Pre-emphasis	94	–	+6	–	dB/oct
De-emphasis	95	–	−6	–	dB/oct
Audio Scrambler					
Inversion Frequency		–	3300	–	Hz
Passband		300	–	3000	Hz

Notes:

91 The receiver audio filter complies with the characteristic shown in Figure 6. The high pass filtering removes sub-audio components from the audio signal.

92 The 12.5kHz channel filter complies with the characteristic shown in Figure 9.

93 The 25kHz channel filter complies with the characteristic shown in Figure 8.

94 The pre-emphasis filter complies with the characteristic shown in Figure 10.

95 The de-emphasis filter complies with the characteristic shown in Figure 7.

96 Psophometrically weighted. Pre/de-emphasis and 25kHz channel filter selected.

9.2 C-BUS Timing

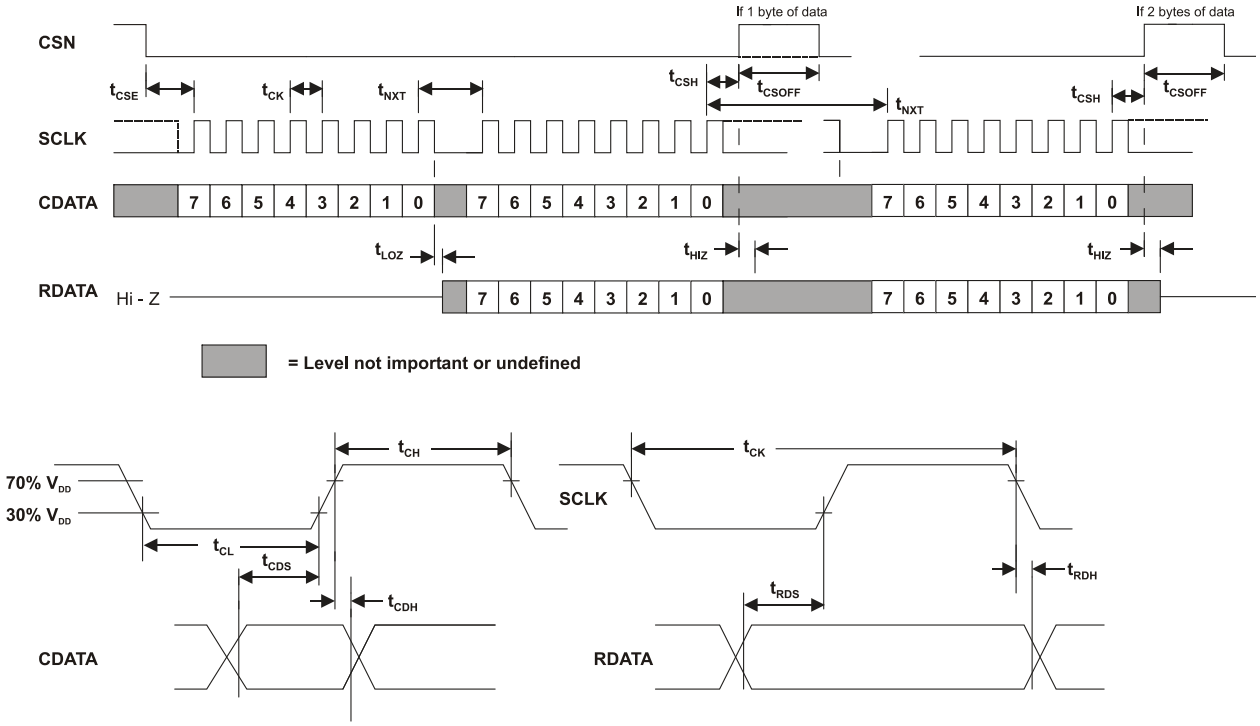


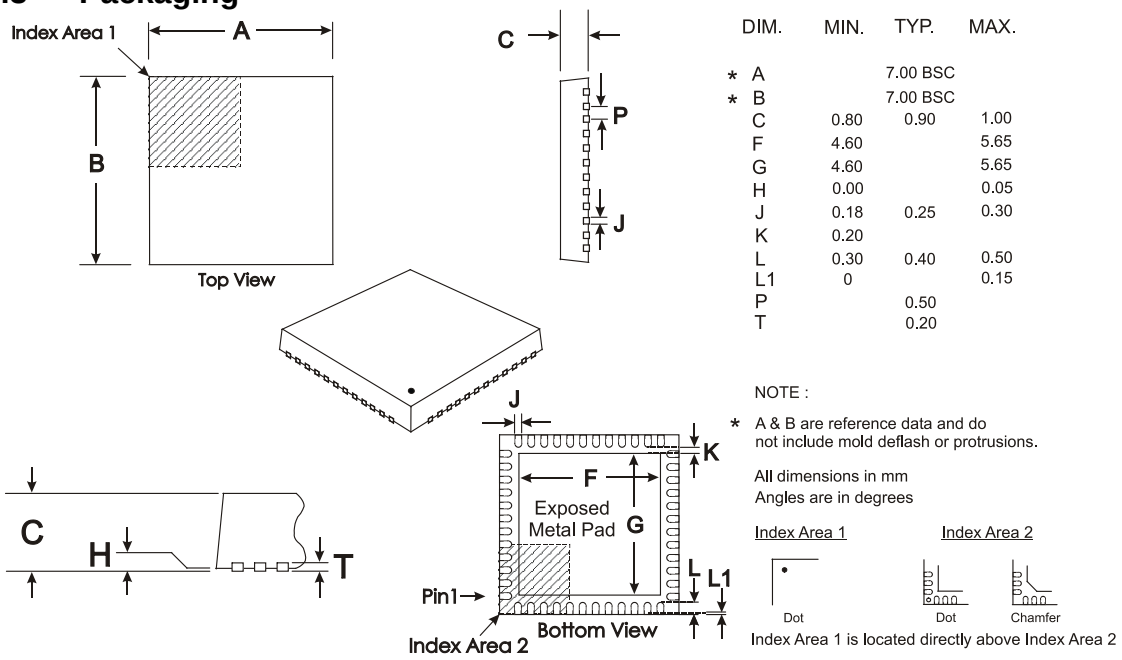
Figure 20 C-BUS Timing

C-BUS Timing		Notes	Min.	Typ.	Max.	Unit
t_{CSE}	CSN Enable to SCLK high time		100	–	–	ns
t_{CSH}	Last SCLK high to CSN high time		100	–	–	ns
t_{LOZ}	SCLK low to RDATA Output Enable time		0.0	–	–	ns
t_{HIZ}	CSN high to RDATA high impedance		–	–	1.0	µs
t_{CSOFF}	CSN high time between transactions		1.0	–	–	µs
t_{NXT}	Inter-byte time		200	–	–	ns
t_{CK}	SCLK cycle time		200	–	–	ns
t_{CH}	SCLK high time		100	–	–	ns
t_{CL}	SCLK low time		100	–	–	ns
t_{CDS}	CDATA setup time		75	–	–	ns
t_{CDH}	CDATA hold time		25	–	–	ns
t_{RDS}	RDATA setup time		50	–	–	ns
t_{RDH}	RDATA hold time		0	–	–	ns

Notes:
1. Depending on the command, 1 or 2 bytes of CDATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. RDATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
2. Data is clocked into the peripheral on the rising SCLK edge.
3. Commands are acted upon at the end of each command (rising edge of CSN).
4. To allow for differing µC serial interface formats, C-BUS compatible ICs are able to work with SCLK pulses starting and ending at either polarity.
5. Maximum 30pF load on IRQN pin and each C-BUS interface line.

These timings are for the latest version of C-BUS and allow faster transfers than the original C-BUS timing specification. The CMX885 can be used in conjunction with devices that comply with the slower timings, subject to system throughput constraints.

9.3 Packaging



	DIM.	MIN.	TYP.	MAX.
*	A		7.00 BSC	
*	B		7.00 BSC	
	C	0.80	0.90	1.00
	F	4.60		5.65
	G	4.60		5.65
	H	0.00		0.05
	J	0.18	0.25	0.30
	K	0.20		
	L	0.30	0.40	0.50
	L1	0		0.15
	P		0.50	
	T		0.20	

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

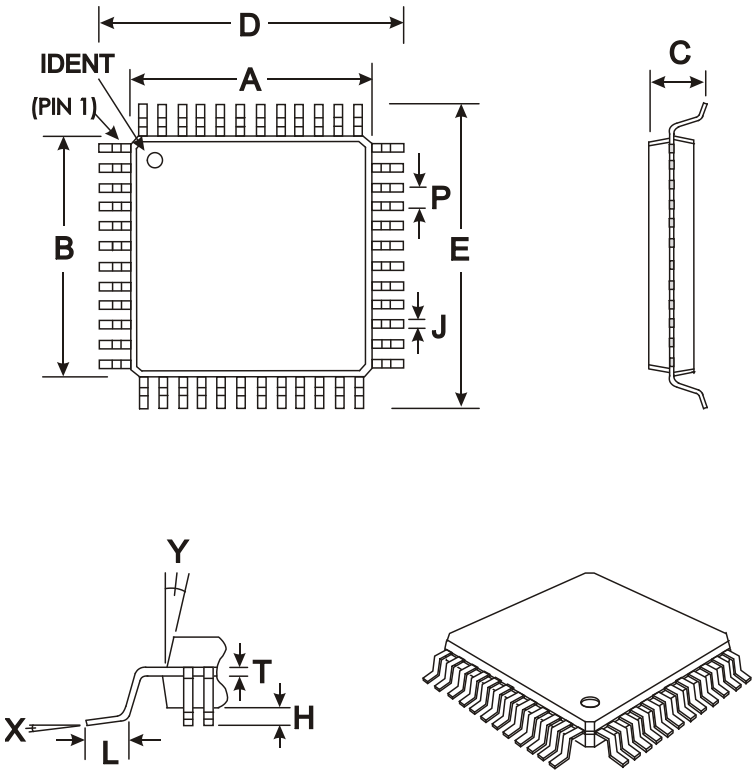
All dimensions in mm
Angles are in degrees

Index Area 1 is located directly above Index Area 2

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 21 Mechanical Outline of 48-pin VQFN (Q3)

Order as part no. CMX885Q3



	DIM.	MIN.	TYP.	MAX.
*	A	6.91		7.11
*	B	6.91		7.11
	C	1.40		1.60
	D	8.74		9.25
	E	8.74		9.25
	H	0.05		0.15
	J	0.10		0.28
	L	0.35		0.76
	P		0.50	
	T		0.13	
	X	0°		7°
	Y	11°		13°

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees
Co-Planarity of leads within 0.1mm

Figure 22 Mechanical Outline of 48-pin LQFP (L4)

Order as part no. CMX885L4

As package dimensions may change after publication of this datasheet, it is recommended that you check for the latest Packaging Information from the Datasheet page of the CML website: [www.cmlmicro.com].

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