CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CMX991/CMX992

RF Quadrature Transmitter and RF Quadrature/Low IF Receiver

D/991_992/22 May 2017 Provisional Issue

This document describes two separate, high performance, RF ICs covering the range: 100MHz[1] to 1GHz. The CMX991 is an RF Quadrature Transceiver and the CMX992 is an RF Quadrature Receiver.

Features

- **Rx (CMX991 and CMX992)**
  - **RF mixer with output select**
  - **1st IF input select**
  - **Selectable low IF outputs (450kHz/455kHz)**
  - **1st IF Variable Gain Amplifier (VGA)**
  - **1st IF Signal Level Indicator (SLI)**
  - **Two-mode demodulator**
  - **I/Q Zero-IF with differential outputs**
- **Tx (CMX991 only)**
  - **I/Q modulator to IF**
  - **Image-reject up-converter**
  - **IF and RF outputs**
- **IF (CMX991 and CMX992)**
  - **IF LO synthesiser**
  - **IF VCO negative resistance amplifier**
- **3.3V low power operation**

Applications

- **Analogue/digital multimode radio**
- **Software Defined Radio (SDR)**
- **Portable, mobile and base station terminals**
- **Data telemetry modems**
- **TETRA (CMX992)**
- **ETSI: EN 300 113, EN 301 166, EN 302 561, EN 300 220, TS 102 361 (DMR)**
- **Automatic Identification System (AIS) transponders**
- **Constant envelope and linear modulation**
- **Compatible with CMX998 (CMX992 only)**
- **Narrowband: e.g. 25kHz, 12.5kHz, 6.25kHz**
- **Wideband: up to 2MHz**
- **APCO Project 25 (P25) Phase 1 and Phase 2 TDMA: TIA-102.CAAB**
- **Satellite communications**

1 Brief Description

The CMX991 is a single-chip, high performance, RF transceiver that provides the core functions required to implement a full-featured radio transmitter and receiver. It operates from 100MHz to 1GHz and its I/Q architecture supports multiple modulation types and bandwidths with a single radio design. The half-duplex CMX991 integrates Tx modulators, Rx demodulators, IF PLL and IF VCO subsystems to minimise the external circuits needed when implementing a complete transceiver. User-selected modes suit different application requirements.

The Tx path includes an I/Q modulator to accurately generate modulation at the IF frequency, which may then be translated to the final RF frequency by an integrated image-reject up-converter system. The I/Q modulator IF output is also made available for conversion to RF via external circuits, if desired.

The Rx path includes an integrated 1st Rx mixer having two outputs to support two external 1st IF filter choices, then an integrated 2:1 input mux followed by VGA and wideband signal level measurement functions, to support AGC implementation. The 1st IF signal is then either I/Q demodulated to Zero-IF or mixed to a Low IF output. The CMX991 provides differential and single-ended Rx output options and differential amplifiers for flexible signal conditioning.

The CMX992 is a single-chip, high performance, RF receiver that includes the core RF and IF receive functions of the CMX991 above and can be used in a wide range of narrowband and wideband wireless products, including multi-mode analogue/digital terminals.

The CMX992 can be used where highly linear modulations are being used, e.g. for applications such as TETRA, where a typical transmitter solution would include the CMX998 Cartesian Feedback Transmitter.

Both devices operate from a single 3.3V supply over a temperature range of -40°C to +85°C and are available in 48-pin VQFN (Q3) packages.

[1] The CMX991/CMX992 may be used at lower frequencies by using appropriate external components. Use below 100MHz is covered in a separate application note available from the CML website.

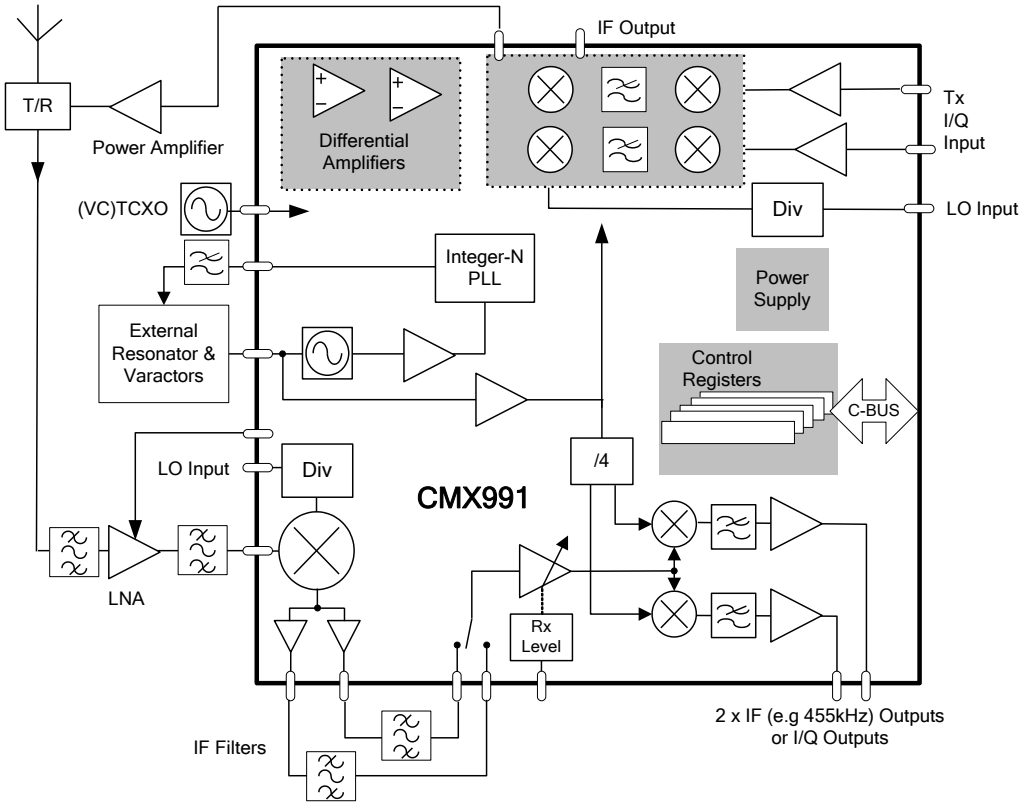

Figure 1 CMX991 – RF Quadrature Transceiver

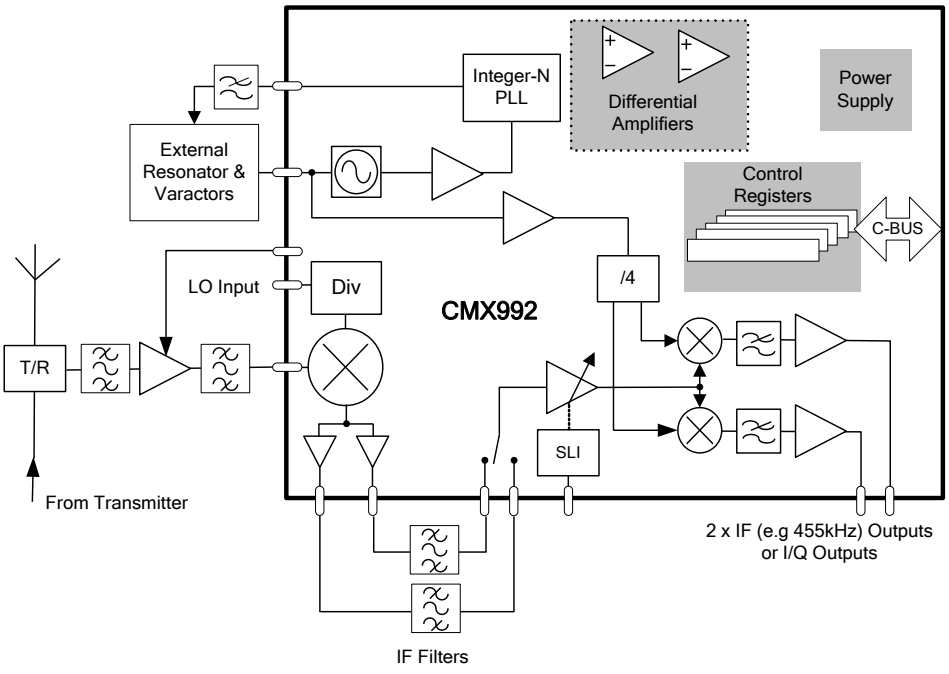

Figure 2 CMX992 – RF Quadrature/Low IF Receiver

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1.1 History

Version	Changes	Date
22	• For clarification changed Typical Gain Distribution to 7.3.1 System Gain with reference made to evaluation board documentation for more technical details. • Clarified description of RF mixer input impedance • Typos corrected, clarifications made	May 2017
21	• Correct typos in Table 19. • Figure 3, Figure 4 and Section 7.8: clarified position of SLI circuit. • New data in section 7.7.2 on noise figure of the IF stages. • New information on IF gain compression in section 7.3.3 and 7.7.3.	Jun 2016
20	• 1S305 (typo) corrected to 1SV305; SMV1279 (typo) corrected to SMV1249 • Typo in note to section 4.5 corrected, 'b1' corrected to 'b7' Information added on Rx dc offset variation with temperature (section 7.13)	Feb 2015
19	• Receiver IF section 1 dB Compression point changed to typical; measurement method clarified (section 8.1.3.2). • Half IF specification changed to reflect production test limit (section 8.1.3.2). JDV2S08S replaced with 1S305FCT in Table 14 as JDV diode is obsolete.	Oct 2012
18	• Various editorial corrections. Alternative diodes added in Table 11.	May 2012
17	• VCO N divider start-up issue when using an external VCO (section 4.5)	Feb 2012
16	• Clarification of gain and noise of IF stage in 'Straight in' case (section 7.7) • Editorial changes for consistency of table header format • Update of receiver gain partition (section 7.3.1)	Jun 2011
15	• Details of receiver gain switching added (Section 7.3.2) • PLL frequency formula added (section 5.4.1) • Phase noise formula typo corrected (M not N) (section 8.1.3.2 Note 94)	Mar 2011
14	• CMX991: Transmitter LO Leakage specification clarified and limits adjusted • CMX991: Transmitter LO Image typical value updated	Dec 2010
13	• Transmitter I and Q channels shown in error causing a spectrum inversion in Tx path. Pins TXQN and TXQP swapped (Table 1) • Editorial error in **Error! Reference source not found.** corrected.	Sep 2010
12	• Rx IMD minimum specification improved after evaluation of production test fixture (section 8.1.3.2)	Jun 2010
11	• Redundant series capacitor deleted and separate capacitors shown for C3 in Figure 7 and Table 5 • Extra information on Mixer Output Impedance added (section 7.6). • **Error! Reference source not found.** updated. • Extra information added on IF gain measurement conditions in (section 7.7). • Extra information added on Rx I/Q Filter, (section 7.10). • Extra information added on Tx Filter, (section 7.12). • Maximum limits added for 'Total Current Consumption' figures', (Section 8.1.3.1) • LO Leakage performance specification updated; clarification of Note 7 and 7a; new Note 7b; reference corrected in Note 11; test frequency of 45MHz moved from Note 17 to Note 10; Gain of I/Q Filter moved to overall IF Amplifier and I/Q Demodulator table (Section 8.1.3.2).	Mar 2010
10	• PLL Phase noise specification corrected and definition added • I/Q Bandwidth clarified in section 4.2.3.2.	Jan 2010

9	• VCO specification corrected. It should be 400MHz (max). • dBV/V terminology clarified. It should be dB(V/V) • Clarification of Rx 1st Mixer Input 3rd order Intercept Point measurement • Correction to C5 in Figure 7, the circuit referenced in IIP3 measurement	Nov 2009
8	• Updated with further application information (e.g. IF VCO options).	July 2009
7	• Updated with enhanced application information.	May 2009
6	• Original published document for both the CMX991 and CMX992 devices.	Mar 2009

It is always recommended that you check for the latest product datasheet version from the CML website: [www.cmlmicro.com].

2 Block Diagrams

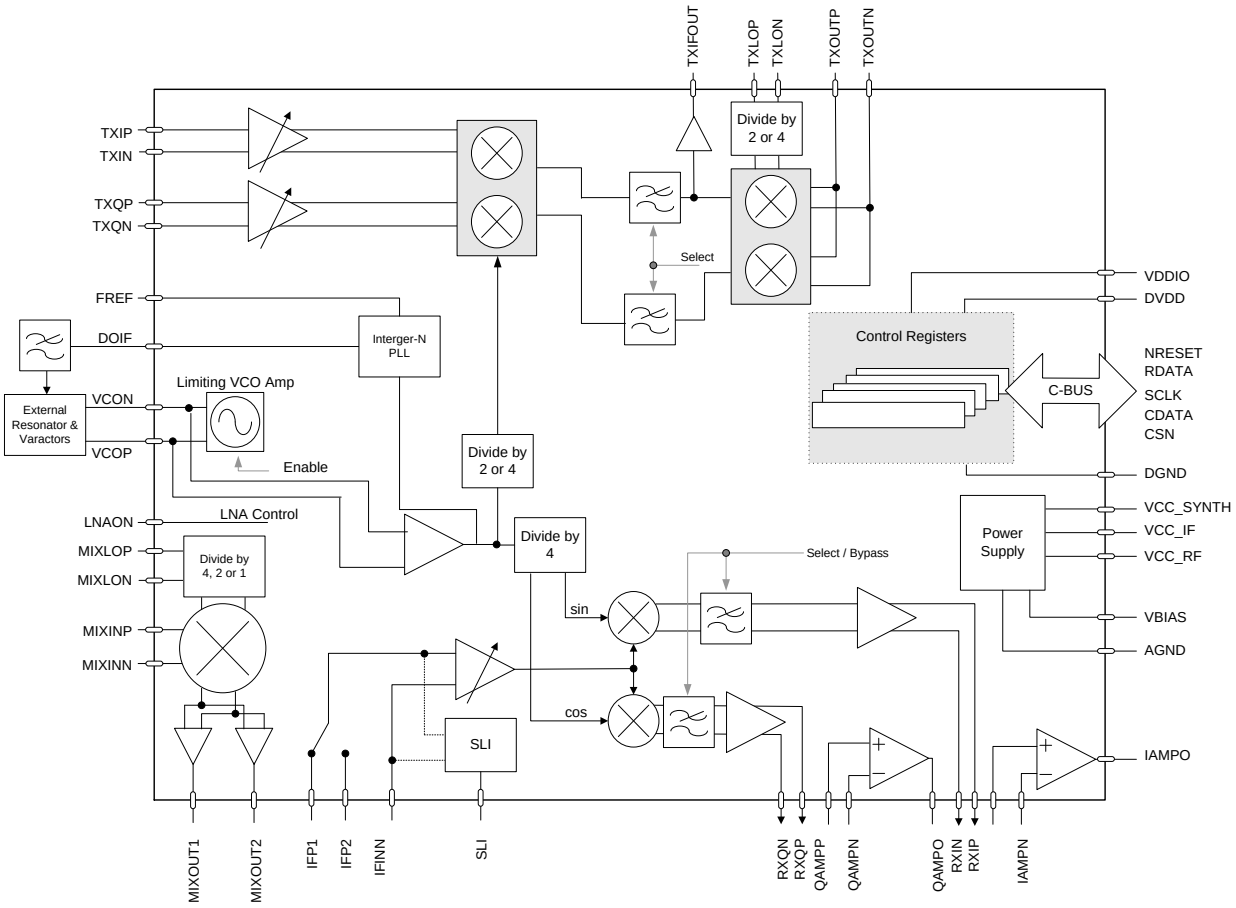


Figure 3 CMX991 Block Diagram

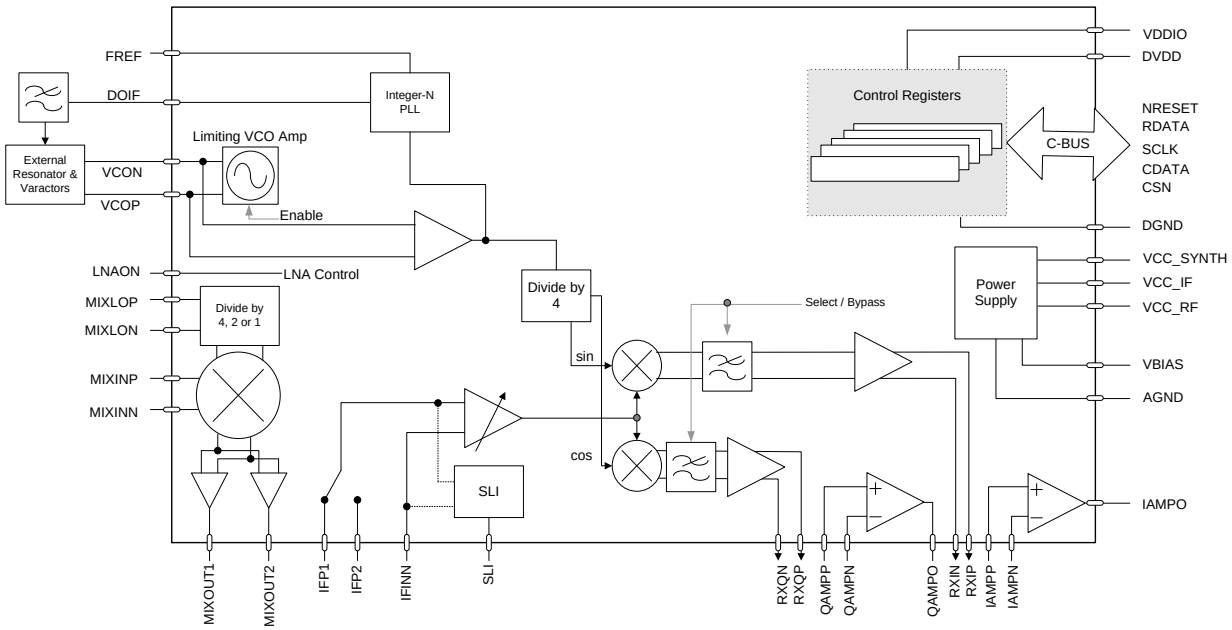


Figure 4 CMX992 Block Diagram

3 Pin List

Package Q3 Pin No.	Pin Name (CMX991)	Pin Name (CMX992)	Signal Type	Description
1	VCCIF	VCCIF	Power	Supply for IF circuits
2	TXOUTP	NC	O/P	CMX991: Tx section positive output
			NC	CMX992: Do not connect to this pin, reserved for future use
3	TXOUTN	NC	O/P	CMX991: Tx section positive output
			NC	CMX992: Do not connect to this pin, reserved for future use
4	NC	NC	NC	Do not connect to this pin, reserved for future use
5	NC	NC	NC	Do not connect to this pin, reserved for future use
6	TXLON	NC	I/P	CMX991: Tx local oscillator negative input
			NC	CMX992: Do not connect to this pin, reserved for future use
7	TXLOP	NC	I/P	CMX991: Tx local oscillator positive input
			NC	CMX992: Do not connect to this pin, reserved for future use
8	MIXINN	MIXINN	I/P	Rx mixer negative input
9	MIXINP	MIXINP	I/P	Rx mixer positive input
10	MIXLON	MIXLON	I/P	Rx mixer local oscillator negative input
11	MIXLOP	MIXLOP	I/P	Rx mixer local oscillator positive input
12	VCCRF	VCCRF	Power	Supply for RF circuits
13	MIXOUT1	MIXOUT1	O/P	Rx mixer output 1
14	MIXOUT2	MIXOUT2	O/P	Rx mixer output 2
15	IFIP1	IFIP1	I/P	Rx IF positive input 1
16	IFIP2	IFIP2	I/P	Rx IF positive input 2
17	IFINN	IFINN	I/P	Rx IF negative input
18	SLI	SLI	O/P	Receiver Signal Level Indicator (SLI) output
19	RXQN	RXQN	O/P	RxQ negative output
20	RXQP	RXQP	O/P	RxQ positive output
21	QAMPP	QAMPP	I/P	RxQ amplifier positive input
22	QAMPN	QAMPN	I/P	RxQ amplifier negative input
23	QAMPO	QAMPO	O/P	Low IF output or RxQ amp output
24	RXIN	RXIN	O/P	RxI negative output
25	RXIP	RXIP	O/P	RxI positive output
26	IAMPP	IAMPP	I/P	RxI amplifier positive input
27	IAMPN	IAMPN	I/P	RxI amplifier negative input
28	IAMPO	IAMPO	O/P	RxI amplifier output
29	DGND	DGND	Power	Digital ground
30	CSN	CSN	I/P	C-BUS chip select (active low), used to enable a C-BUS data read or write operation on the chip
31	RDATA	RDATA	T/S	C-BUS serial data 3-state output (reply data) to host
32	SCLK	SCLK	I/P	C-BUS clock input from the host
33	CDATA	CDATA	I/P	C-BUS serial data input (command data) from the host
34	RESETN	RESETN	I/P	C-BUS reset (low for reset condition)
35	DVDD	DVDD	Power	Supply to digital circuits

Package Q3 Pin No.	Pin Name (CMX991)	Pin Name (CMX992)	Signal Type	Description
36	VDDIO	VDDIO	Power	Supply to C-BUS circuits
37	LNAON	LNAON	O/P	Control line to enable/disable Rx LNA
38	VCCSYNTH	VCCSYNTH	Power	Supply to IF integer N PLL
39	FREF	FREF	I/P	Reference frequency input
40	DOIF	DOIF	O/P	IF PLL charge pump output
41	VCOP	VCOP	I/P	IF PLL VCO positive input
42	VCON	VCON	I/P	IF PLL VCO negative input
43	VBIAS	VBIAS	O/P	Bandgap generated bias voltage – measurement output
44	TXQP (Note 2)	NC	I/P	CMX991: TxQ positive input
			NC	CMX992: Do not connect to this pin, reserved for future use
45	TXQN (Note 2)	NC	I/P	CMX991: TxQ negative input
			NC	CMX992: Do not connect to this pin, reserved for future use
46	TXIN	NC	I/P	CMX991: TxI negative input
			NC	CMX992: Do not connect to this pin, reserved for future use
47	TXIP	NC	I/P	CMX991: TxI positive input
			NC	CMX992: Do not connect to this pin, reserved for future use
48	TXIFOUT	NC	O/P	CMX991: Tx IF output
			NC	CMX992: Do not connect to this pin, reserved for future use
EXPOSED METAL PAD	AGND	AGND	Power	The exposed metal pad must be electrically connected to analogue ground

Total = 49 Pins (48 pins and central, exposed metal ground pad)

Table 1 Pin List

Notes:
1) I/P = Input T/S = 3-state
   O/P = Output NC = Not Connected
2) In versions of the datasheet before D/991_992/13 these pins were incorrectly referenced as pin 44 = TXQN and pin 45 = TXQP causing a spectrum inversion at the modulator output.

3.1 Signal Definitions

Signal Name	Pins	Usage
AV_{DD}	VCCIF, VCCRF, VCCSYNTH	Power supply for analogue circuits.
DV_{DD}	DVDD	Power supply for digital circuits.
$V_{DD}IO$	VDDIO	Power supply voltage for digital interface (C-BUS).
V_{BIAS}	VBIAS	Bandgap generated bias voltage used as a reference for differential amplifier stages. Decoupling is optional but, if used, a capacitor of >200nF should be connected between V_{BIAS} and AV_{SS}.
DV_{SS}	DGND	Ground for digital circuits.
AV_{SS}	AGND	Ground for analogue circuits.

Table 2 Definition of Power Supply and Reference Voltages

4 External Components

4.1 Power Supply Decoupling

The CMX991/CMX992 has separate supply pins for the analogue and digital circuitry: a 3.3V nominal supply is recommended for all circuits but a different voltage for V_{DD}IO may be used (see section 5.6).

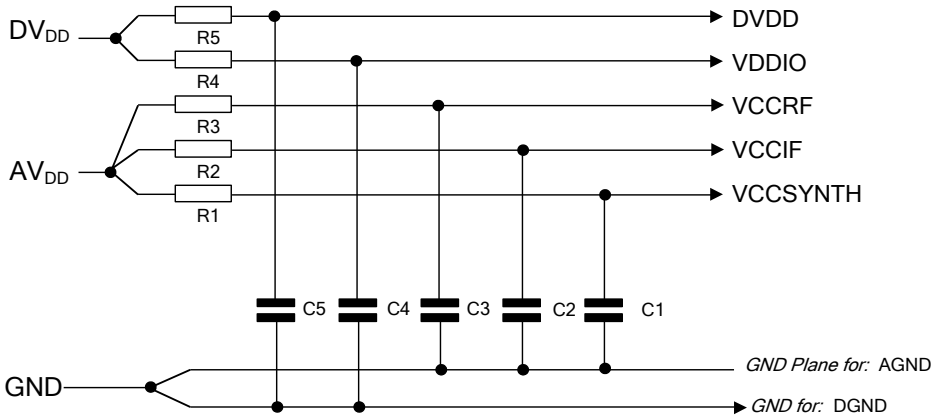


Figure 5 Recommended Power Supply Connections and Decoupling

C1	10nF	R1	3.3 Ω
C2	10nF	R2	3.3 Ω
C3	10nF	R3	3.3 Ω
C4	10nF	R4	10 Ω
C5	10nF	R5	10 Ω

Table 3 Decoupling Components

Notes:

1. Maximum Tolerances: Resistors ±5%, capacitors ±20% unless otherwise stated
2. It is expected that any low frequency interference on the 3.3 Volt supply will be removed by active regulation; a large capacitor is an alternative but may require more board space and so may not be preferred. It is particularly important to ensure that there is no interference from the V_{DD}IO (which supplies the digital I/O) or from any other circuit that may use the DV_{DD} supply (such as a microprocessor), to sensitive analogue supplies (AV_{DD}). It is therefore advisable to use separate power supplies for the digital and analogue circuitry.
3. The supply decoupling shown is intended for RF noise suppression. It is necessary to have a small series impedance prior to the decoupling capacitor for the decoupling to work well; this may be cost effectively done with the resistor and capacitor values shown. The use of resistors results in small dc voltage drops (up to approx 0.1V). Choosing resistor values approximately inversely proportional to the dc current requirements of each supply ensures the dc voltage drop on each supply are reasonably matched. In any case, the dc voltage change that results is well within the design tolerance of the device. If higher impedance resistors are used (not recommended) then greater care will be needed to ensure the supply voltages are maintained within tolerance, even when parts of the device are enabled or disabled.
4. It is advisable to have separate ground planes for the analogue and digital circuits.

4.2 Receiver (CMX991 and CMX992)

The receiver relies on an external LNA, filtering and a transmit/receive switch; details can be found in section 5.2.

4.2.1 Rx 1st Mixer

The Rx 1st Mixer has a differential input. To ensure optimum performance a balun is required when driving from typical single-ended (un-balanced) LNAs or filters. The balun may be a transformer type or implemented using LC networks. A typical matching circuit to the Rx 1st Mixer is shown in Figure 6. In a particular implementation the shunt resistors R1 and R2 may be replaced by a single component across the balun T1 output. The blocking capacitors C3 and C4 may be omitted if the input signals are 0V dc biased. DC should not be applied to the input pins, otherwise damage to the internal protection diodes may result.

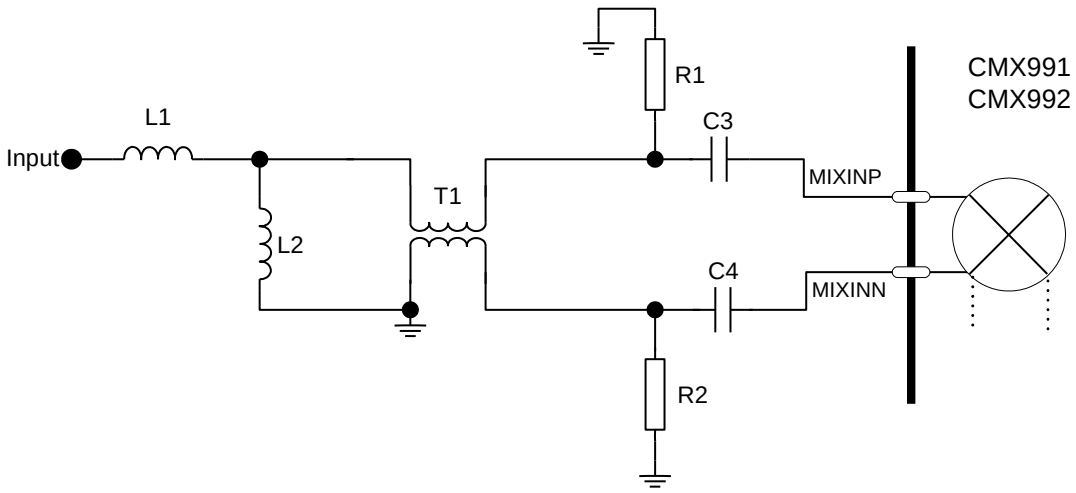


Figure 6 Example External Components – Receive 1st Mixer Input

L1	27nH	L2	33nH
C3	1nF	T1	TC1-1-13M+
C4	1nF	R1 and R2	NF

Table 4 Typical Rx 1st Mixer Input Matching Components for 455MHz

4.2.2 Rx 1st IF Filtering

The output of the CMX991/CMX992 first receive mixer can be switched between MIXOUT1 and MIXOUT2 to support two different external 1st IF filters for different receiver operating modes. The IF output should be in the range 10MHz to 150MHz. The integrated IF amplifier that follows external 1st IF filters has two switchable inputs. It is recommended that an IF filter (e.g. crystal or SAW type) be placed between the mixer output and IF amplifier input stages to protect the IF amplifier and subsequent stages from off-channel signals. Matching arrangements will vary with the particular filter used, however an example of a typical configuration for a 45MHz IF is given in Figure 7. The configuration shown only utilises one possible combination of the two 1st Mixer outputs and two IF amplifier inputs; the other input and output (IFIP2 and MIXOUT2 respectively) could be configured to use a SAW filter or operate with a different IF frequency or bandwidth, for example. The MIXEROUT1 and MIXEROUT2 pins should have a dc blocking capacitor, as should the IF amplifier inputs IFIP1 and IFIP2. IFINN should be ac coupled to the IF filter ground.

For additional information see sections 5.2.2 and 7.6.

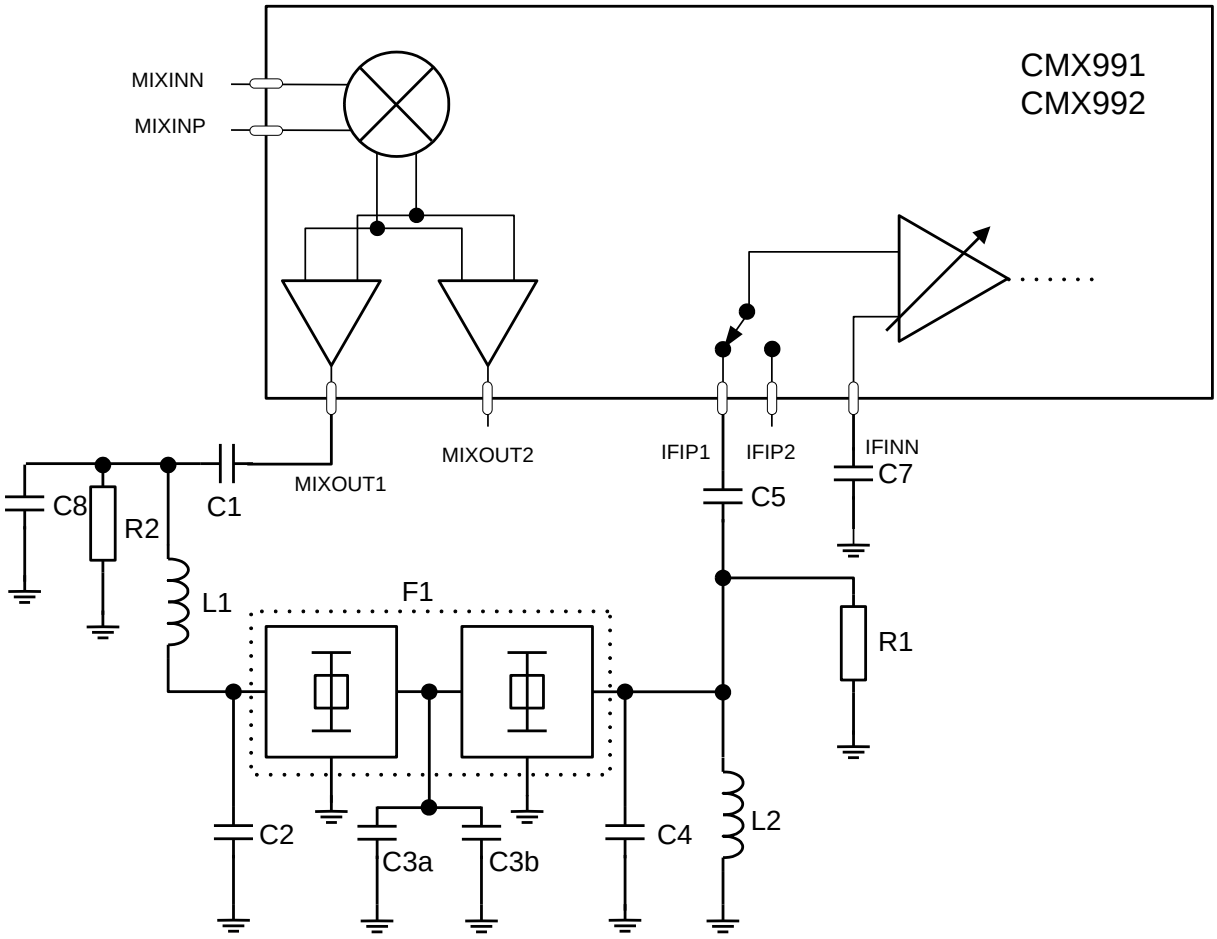


Figure 7 Example External Components – Receive 1st IF Section

C1	1nF	C7	1nF
C2	15pF	C8	18pF
C3a	3.9pF	L1	1µH
C3b	4.7pF	L2	1µH
C4	4.7pF	R1	1200Ω
C5	1nF	R2	220Ω
		F1	45G15B1

Table 5 1st IF Filtering Components for 45MHz

4.2.3 Rx Output

4.2.3.1 I/Q Output Amplifiers

The CMX991/CMX992 includes uncommitted differential amplifiers, which may be used to convert the differential I and Q output signals to a single ended output. A typical configuration of the amplifier on the Q channel (the I channel is identical) is shown in Figure 8. This circuit has a linear gain of 1.5 and is not optimum for rejection of common mode signals, however in practice performance is generally satisfactory. Users should note that the gain and bandwidth of this stage can be adjusted by altering the component values and should be configured to suite a particular application.

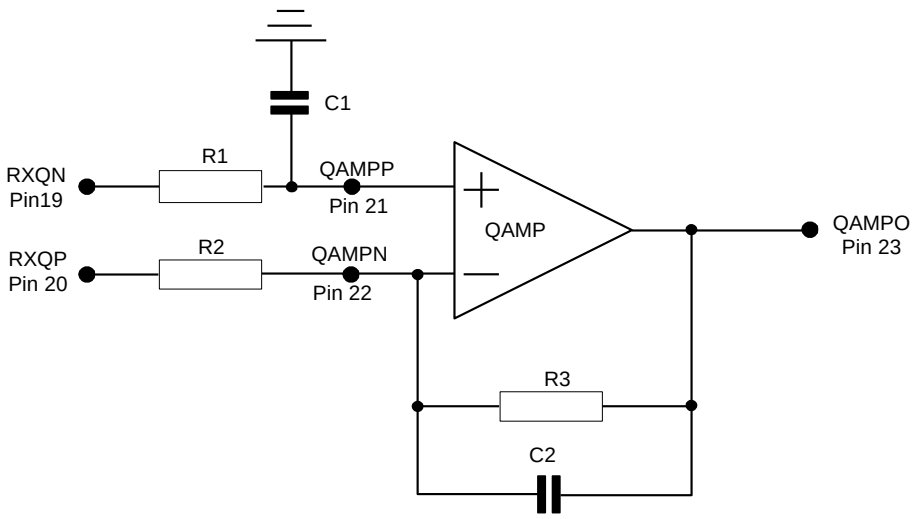


Figure 8 Example External Components – Receive I/Q Output

C1	NF	R1	10kΩ
C2	NF	R2	10kΩ
		R3	10kΩ

Table 6 Rx I/Q Differential to Single Ended Amplifier Components

4.2.3.2 Low IF Output

The I/Q demodulator output bandwidth has a minimum of 1MHz, typically 1.4MHz (see section 8.1.3.2), so the output of each I and Q demodulator mixer can be configured to mix down to a low 2nd IF and use a demodulator output amplifier to provide gain. A typical configuration for the Q channel is shown in Figure 9.

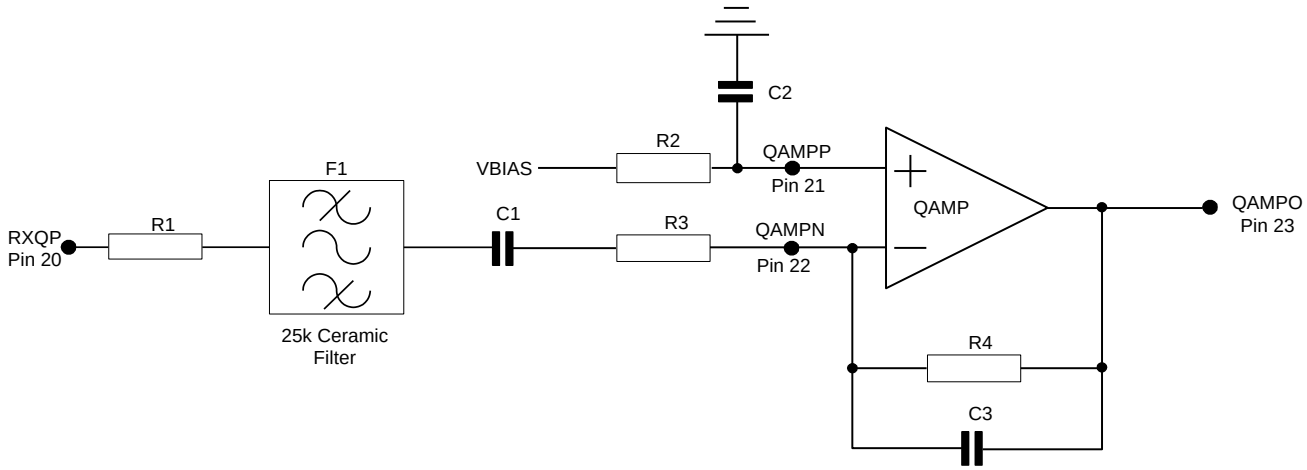


Figure 9 Example External Components – Receive Low IF Output

C1	100nF	R1	1.5kΩ
C2	47nF	R2	1.5kΩ
C3	33pF	R3	1.5kΩ
F1	CFWLA455KEFA-B0	R4	4.7kΩ

Table 7 Rx Low IF (455kHz) Components

The components above specify, as an example, a particular ceramic filter (F1) that would typically be used in a 25kHz channel application in a system with an IF frequency of 455kHz. The other component values specified (e.g. R1, R3) are determined by the input/output impedance of the filter used. The filter and other components can be easily changed to allow for other bandwidths or any 2nd IF output up to 1MHz.

A different external 2nd IF filter, of different bandwidth, could similarly be connected to the I channel output to support a second modulation bandwidth mode, e.g. to receive a 6.25kHz channel signal. The channel to be used is selectable via the general control register ($11), section 6.2, the unused channel being powered-down.

4.3 Transmitter (CMX991 only)

4.3.1 Transmitter

Details of the transmitter are contained in the Transmitter description, section 5.3. The components used around the CMX991 will depend on application requirements, however a typical configuration is shown in Figure 10.

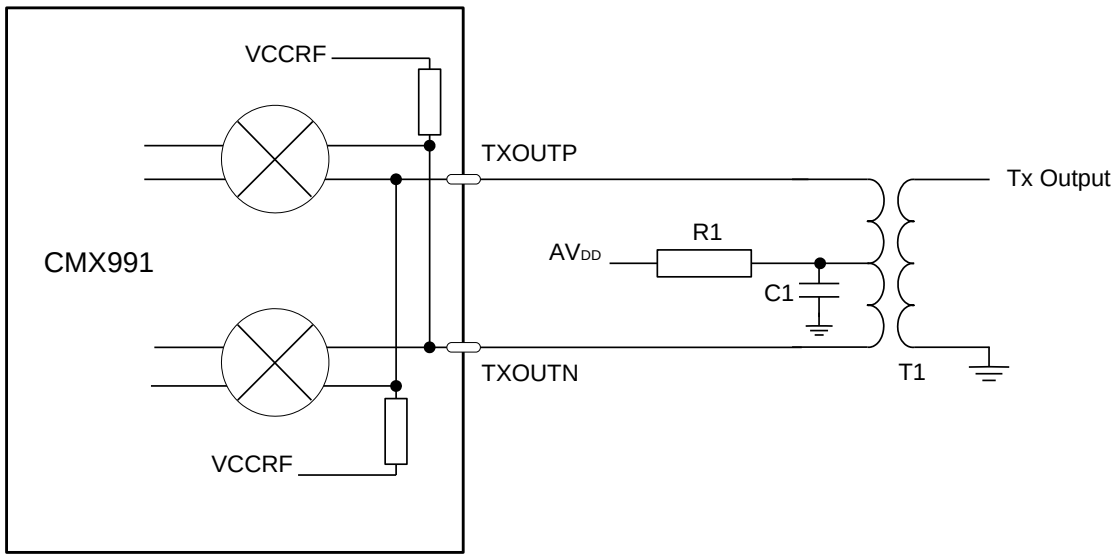


Figure 10 Example External Components – Transmitter

C1	10nF (note 1)	T1	4:1 balun with centre tap (note 2)
R1	3.3Ω		

Table 8 Transmitter Components

Notes:
1. Value of C1 is dependant on frequency of operation. At higher frequencies an additional low value decoupling capacitor in parallel (e.g. 33pF) may be required for optimum performance. C1 should be located as close to the centre tap of T1 as possible.
2. Example component for T1 is Mini-Circuits TC4-14+.
3. Additional components may be required at the T1 output for optimum match to 50Ω.

4.3.2 IF I/Q Modulator Output

The I/Q modulator can be used on its own, without the up-conversion mixers, by switching the I/Q modulator output to the output pin, TXIFOUT (pin 48) – see section 6.5. A typical configuration for this output is shown in Figure 11.

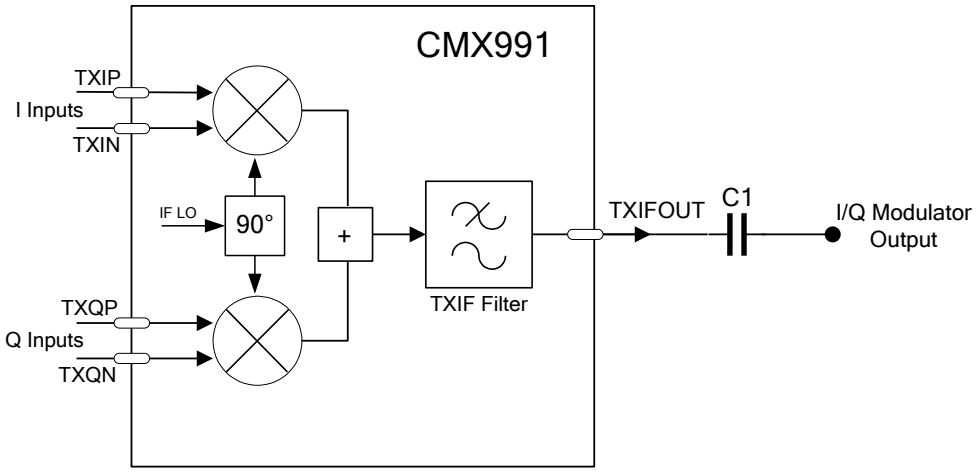


Figure 11 Example External Components – I/Q Modulator Output

C1	1nF

Table 9 I/Q Modulator Output Matching Components

4.4 Main Local Oscillator

4.4.1 Receiver LO Input (CMX991 and CMX992)

The main local oscillator input is differential, but the normal configuration will be single ended, with the other input ac coupled to ground as shown in Figure 12. To prevent signals present on the local ground affecting the LO, the ground associated with capacitor C2 should be the same ground that is used for the LO source. In this way any ground noise will be common mode at the inputs A and B and will be rejected.

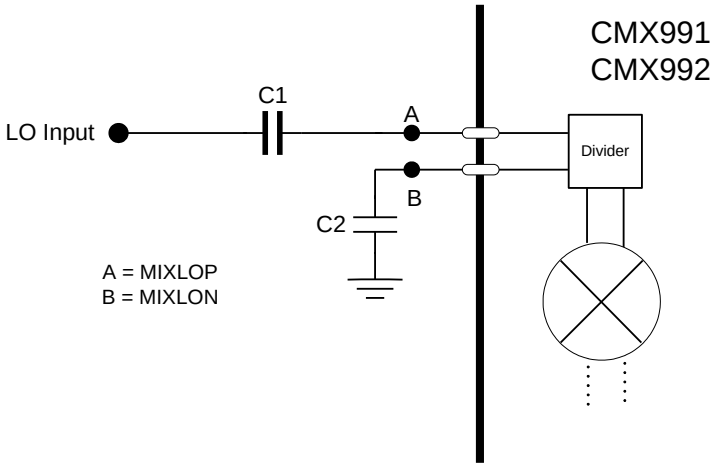


Figure 12 Example External Components – Rx LO Input

C1	1nF	C2	1nF

Table 10 Rx LO Input Components

The blocking capacitors C1 and C2 may be omitted (i.e. point B connected to ground) if the input signals are 0V dc biased. DC should not be applied to the input pins, otherwise damage to the internal protection diodes may result.

4.4.2 Transmitter LO Input (CMX991 only)

Exactly the same configuration can be used for the CMX991 Tx LO input as for the receiver (Figure 12, Table 10). For the transmitter, 'A' in the diagram is pin TXLOP and 'B' is pin TXLON.

4.5 IF Local Oscillator (CMX991 and CMX992)

A typical configuration for using the internal VCO negative resistance amplifier at 180MHz is shown in Figure 13. The other external components required to complete the PLL are the loop filter components, see Figure 14 – which shows a 3rd order loop filter; typical values for a 1kHz bandwidth are given in Table 12.

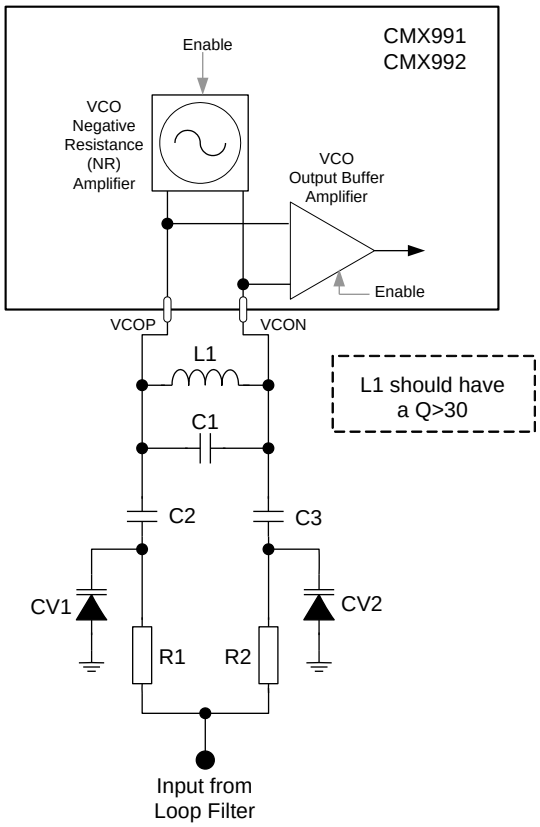


Figure 13 Example External Components – IF LO VCO External Tank Circuit

L1	33nH (Note 1)	CV1	1SV305 (Note 3)
C1	6.8 pF (Note 2)	CV2	1SV305 (Note 3)
C2	27 pF	R1	10kΩ
C3	27 pF	R2	10kΩ

Note 1: Tolerance of 2% or better recommended
Note 2: Tolerance of 5% or better recommended
Note 3: Alternatives are SMV1705-079LF or JDV2S08S (obsolete); SMV1249-079LF gives increased tuning range and slightly degraded phase noise.

Table 11 IF VCO LO Internal VCO Amplifier Tank Circuit for 180MHz Operation

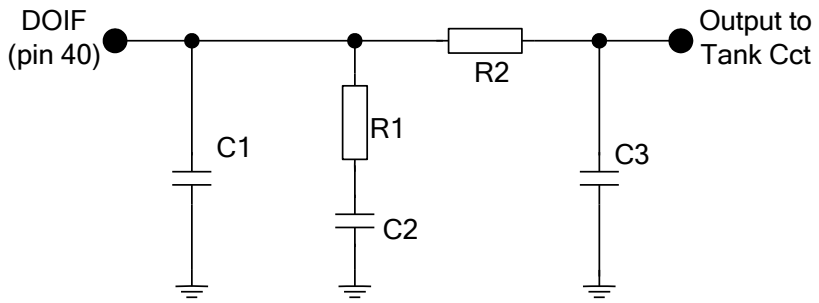


Figure 14 Example External Components – IF LO Loop Filter

C1	22nF	R1	430Ω
C2	470nF	R2	12kΩ
C3	1nF		

Table 12 IF LO 3rd Order Loop Filter Circuit for 180MHz Operation

To inject an external IF LO signal, the negative resistance amplifier should be disabled, with the VCON input decoupled to ground with a 1nF capacitor. The signal is then applied to VCOP via a dc blocking capacitor (e.g. 1nF). Other circuitry shown above, such as the tank circuit, should be not fitted.

Note: When using an external IF VCO the N divider can experience a transient during start up that will cause incorrect operation (charge pump always 'high'). To avoid this situation either the value of the PLL N divider should be an integer multiple of 4 or it is necessary to ensure that the external VCO is powered-up before the PLL is enabled (register $21, b7).

5 General Description

5.1 Overview

The CMX991/CMX992 are RF Quadrature Transceiver and Receiver ICs respectively. Each incorporates a superheterodyne receiver section along with IF local oscillator circuits. The CMX991 has an I/Q modulator with image-rejecting up-converter. The CMX991/CMX992 I/Q architecture supports a wide range of modulation types and various selectable functions maintain the performance across multiple modulations and bandwidths. The demodulator outputs are analogue signals with a quadrature (I/Q) Zero-IF signal format that simplifies connection to external ADCs. The receiver analogue signal interface also supports a low IF output mode. The transmitter interface is analogue I/Q format. Control of the CMX991/CMX992 is via the serial C-BUS (see section 6).

5.2 Receiver

The CMX991/CMX992 has a flexible multi-standard receiver designed to support multiple digital and analogue radio systems of both constant envelope and linear modulation types. It is expected that the applied input signal will have been amplified by an external Low Noise Amplifier (LNA). The user must determine the need for, and design of, any external image reject filtering. The CMX991/CMX992 design is optimised for an LNA gain of about 13dB[2]. It is assumed there is some insertion loss prior to the LNA but an overall noise figure of 4dB and gain of 8dB (approx.) should be provided by the circuits preceding the CMX991/CMX992. A digital control signal is available from the chip, which can be used to enable/disable the LNA. Use of this signal is recommended as it simplifies I/Q calibration of dc-offsets. A differential input signal to the first mixer on the chip is recommended.

The receiver architecture is a superheterodyne type with a 1st IF allowed in the range 10MHz to 150MHz, some typical 1st IFs being 10.7MHz, 21.4MHz, 45MHz, 70MHz and 150MHz. The CMX991/CMX992 provides a 1st down converter mixer with excellent linearity and noise figure. The design is intended to meet the challenging requirements of typical PMR/LMR radio systems.

5.2.1 Rx 1st Mixer and IF Filtering

The Rx 1st Mixer has a differential input and selectable LO input dividers (/1, /2 and /4) to allow common LO structures with the various Tx architectures, including use of the CMX992 with a CMX998-based transmitter. The mixer RF LO input is differential but the normal configuration is single ended with the other input ac coupled to ground (see section 4.4.1).

The mixer has two selectable outputs to allow the connection of two different 1st IF filters, crystal or SAW type, that may be separately enabled under host control. The type of filter used is dependent on the application. The filter should provide rejection of blocking and intermodulation test tones for the subsequent IF stages. This 1st IF filter may also provide some useful adjacent channel filtering but it is likely that the majority of the adjacent channel rejection will come in subsequent stages.

5.2.2 IF Variable Gain Amplifier (VGA) and I/Q Down-converter Mixer

There are two selectable inputs to the IF amplifier, which is low noise and controlled through the C-BUS serial interface (See section 6). The inputs are differential with a common inverting input (pin IFINN) which should be decoupled locally to the ground plane used for the external IF elements. The IF inputs are high impedance (see section 8.1.3.2) and this allows straightforward matching to IF filter components. A typical configuration is shown in section 4.2.2, Figure 7 where the resistor R1 is used to define the resistive load

[2] The precise gain will depend on application and is often a trade-off between intermodulation performance and receiver noise figure. See also section 7.3.1.

for the filter. The suggested value of 1200Ω can be varied depending on requirements, noting the trade-off between voltage gain and Q of the matching arrangements. The input impedance varies slightly with VGA setting but the effect of this is minimised by use of the terminating resistor R1.

The variable gain may be adjusted by a host processor based on the measured Signal Level Indicator (SLI) value or on other criteria such as I/Q vector magnitude. The SLI output is an analogue output which is single ended and referenced to ground. Following the IF amplifier there is a pair of mixers that perform the final down-conversion either to an I/Q or low IF output. The I/Q demodulator has an output bandwidth of 1MHz which allows a low IF output of up to 1MHz; typical values may be 450kHz, 455kHz or 465kHz.

5.2.3 I/Q Filters

The I/Q outputs include two filters that provide continuous time rejection to serve as anti-alias filters for external ADCs. The default filter will give an I/Q bandwidth of 1MHz. A narrower filter of 100kHz bandwidth is selectable to improve analogue rejection for narrow-band systems and guarantees image rejection for typical (e.g. sigma-delta) ADC solutions.

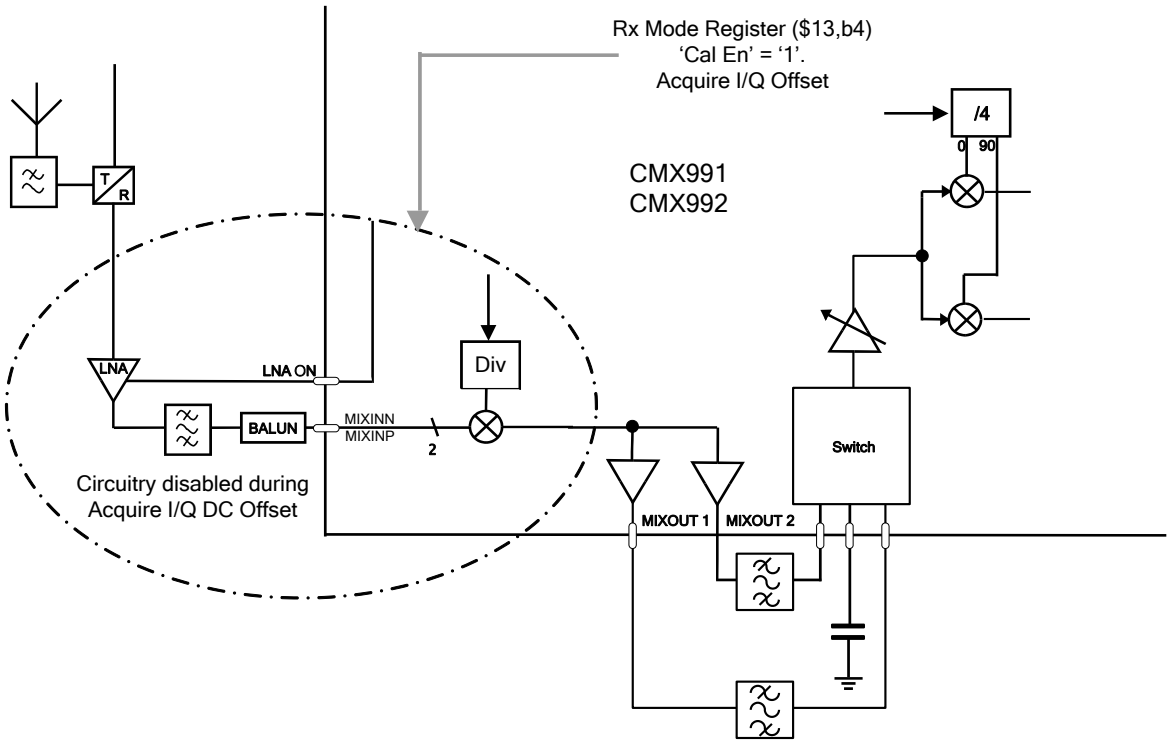


Figure 15 DC Offset Calibration Mode

5.2.4 DC Offset Correction

The CMX991/CMX992 does not provide direct compensation of dc offsets in the I/Q outputs from the receiver, however it does provide a mode that allows the I/Q signals to be measured externally to support easy compensation. To allow optimum measurement of dc offsets it is desirable to remove the input signal to allow fast averaging of the output i.e. without the need to consider the possibility of modulation being present. In this mode the areas of the CMX991/CMX992 that can generate dc offsets remain enabled.

The CMX991/CMX992 'Cal En' mode (Rx Mode register $13, b4, see section 6.4.1) disables the early stages of the receiver, as shown in Figure 15.

5.3 Transmitter (CMX991 only)

The transmitter requires analogue I and Q (baseband) signal inputs. This I/Q input is up-converted by quadrature modulator(s) to a suitable IF (TxIF). This is the modulated signal with the desired modulation, but at an IF of typically 45MHz or 90MHz, i.e. typically lower than the final desired (RF) transmit frequency. The TxIF signal is available at the TXIFOUT pin or can be up (or down) converted to final frequency using the CMX991 image reject up-mixer.

The TxIF signal can be optimised by selecting the correct setting of the IFH bit (register $11, b5 see section 6.2.1) for IFs above or below 75MHz.

The IF LO input applied to the IF I/Q modulator(s) is generally developed internally (see section 5.4). The LO is divided by either 2 or 4 to generate the quadrature signals used in the modulator. The main LO, used in image-reject up-converter, is generated off-chip.

5.3.1 Image-Reject Up-converter

The CMX991 transmitter architecture is shown in Figure 16. The image rejection process involves generating TxIF signals with a quadrature phase relationship. The TxIF signals pass through filters to remove harmonic content – this substantially reduces the spurious content of the final output. The bandwidth of the filters is selectable as 45MHz, 60MHz, 90MHz or 120MHz (see also section 7.12). The signals are then used in a modulator stage which converts to the final frequency. The process results in image cancellation of the unwanted mixing sideband with default operation being high side mixing as follows:

$$f_{rf} = f_{lo} - f_{TxIf} \quad \text{(wanted)}$$
$$f_{image} = f_{lo} + f_{TxIF} \quad \text{(rejected)}$$

Which mixing product is the wanted and which the unwanted image can be selected, see section 6.6.

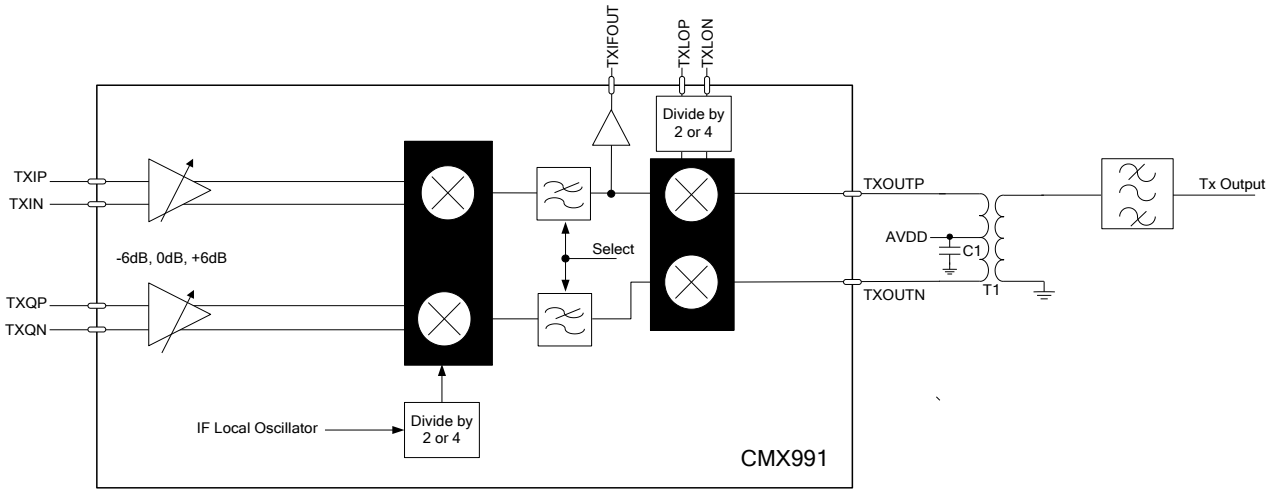


Figure 16 CMX991 Transmitter Architecture

The image-reject function reduces the need for filtering following the modulator to remove spurious products, however it is likely that some filtering will still be required to meet spurious emissions limits, hence the additional filter as shown in Figure 16.

5.3.2 Direct I/Q IF Output Tx Mode

As shown in Figure 16, the filtered TxIF output from the I/Q modulator can be made available on the TXIFOUT pin. This can then be translated up to RF frequency via user-supplied external circuits or in some cases used directly for VHF operation. When this mode is selected the image-reject up-converter should be powersaved (register $14, b6 – see section 6.5.1): this disables unused circuits and saves power.

5.4 Local Oscillators

5.4.1 IF Local Oscillator

The CMX991/CMX992 provides an integer-N PLL that can be used to create the IF Local oscillator, see Figure 17. The CMX991/CMX992 provides a VCO negative resistance amplifier, so only a tank circuit needs to be implemented externally. Alternatively, this amplifier can be bypassed and an external VCO can be used in the range 40 to 600 MHz (NB: see note at end of section 4.5).

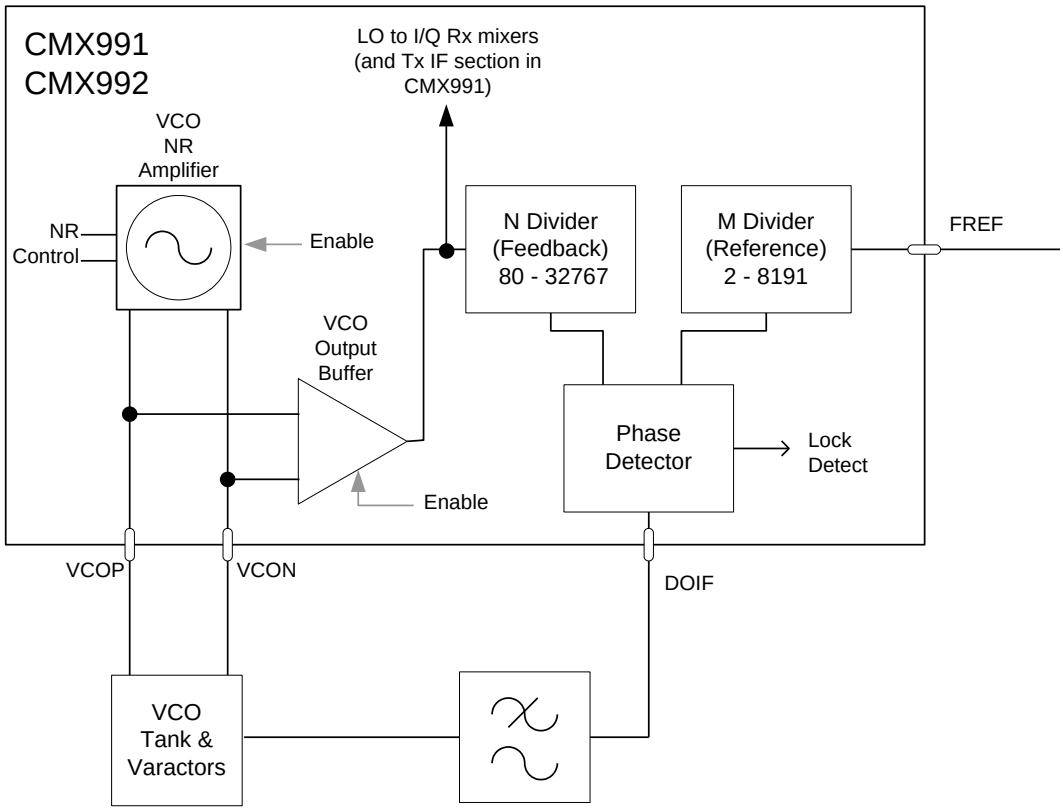


Figure 17 CMX991/CMX992 IF Local Oscillator

The integer-n PLL has programmable M and N dividers as shown in Figure 17. The phase detector provides a charge pump output which requires a suitable loop filter to convert this signal into a control voltage for a VCO. The phase detector can be turned off (high impedance mode) and the PLL section disabled if an external LO is to be used, see section 6.8 for control details. In the case of an external LO it is necessary for the VCO Output buffer to remain enabled (section 6.2, register $11, b1) however the VCO amplifier must be disabled (Register $11, b0).

The output frequency of the PLL is set by the following calculation:

$$f_{out} = f_{ref} \times (N / M)$$

where

f_{out} = The desired output frequency in MHz
f_{ref} = The reference frequency supplied to the PLL on pin FREF in MHz
N = Divider value programmed in the N divider register (see section 6.9.1)
M = Divider value programmed in the M divider register (see section 6.8.1)

The PLL only supports VCOs with a positive tuning slope, i.e. a high tuning voltage from DO results in a higher oscillation frequency from the VCO.

The PLL has a lock-detect function that can be evaluated using register $21, b6 (section 6.8.2).

The VCO amplifier is a negative resistance amplifier requiring an external tank circuit (see section 4.5). The amplifier has two control bits available in the general control register (section 6.2, register $11, b2 - b3). These bits can be used to optimise performance for a particular tank circuit depending on its Q value.

5.4.2 RF Local Oscillator

The main LO for both the transmitter and the receiver are not provided on the CMX991/CMX992 and must be supplied from an external source (see section 4.4). Independent selectable internal dividers for Tx and Rx sections are provided to work with the external source, see Figure 3 or Figure 4. The input impedance is nominally 300Ω differential with a series capacitance of 6pF to each pin.

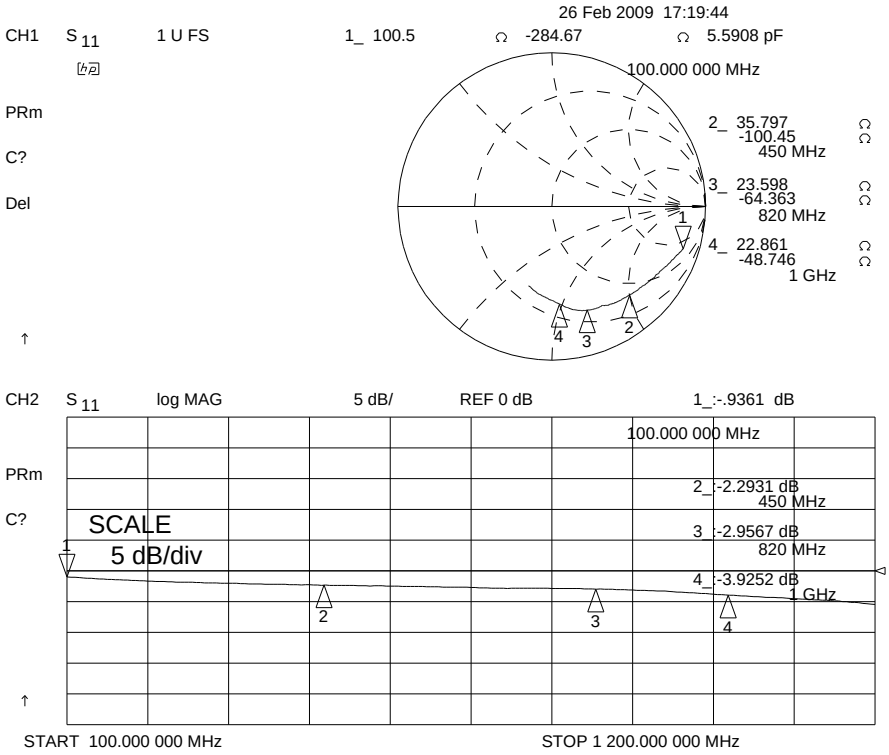


Figure 18 Typical LO Input Impedance

5.5 V_{BIAS}

The VBIAS pin provides a 1.6V bandgap reference-derived bias voltage (V_{BIAS}) that may be used as a reference voltage for differential amplifier stages (e.g. in the receiver output). The VBIAS pin can be decoupled to ground but a capacitor greater than 200nF should be used to ensure stability.

5.6 Data Interface

The CMX991/CMX992 is controlled via a three wire C-BUS. A fourth pin (RDATA) is required if register read-back is to be used. A further pin (RESETN) is provided which, when 'low', generates a reset signal (see section for 6.1 further details). The pin should be pulled to the V_{DD}IO supply with a suitable resistor if not used.

The data interface can run at a lower voltage than the rest of the IC by setting the V_{DD}IO supply to the required interface voltage, in the range 1.6V to 3.6V.

Full details of the control register structure are given in section 6.

6 C-BUS Interface and Register Description

The C-BUS serial interface supports the transfer of control or status information between the CMX991/CMX992s' internal registers and an external host. Each C-BUS transaction consists of the host sending a single Register Address byte, which may then be followed by zero or more data bytes that are written into the corresponding CMX991/CMX992 register, as illustrated in Figure 19.

Data sent from the host to the Command Data (CDATA) pin is clocked into the CMX991/CMX992 on the rising edge of the Serial Clock (SCLK) input. The C-BUS interface is compatible with common µC/DSP serial interfaces and may also be easily implemented with general purpose I/O pins controlled by a simple software routine. Section 8.1.3.5 gives the detailed C-BUS timing requirements.

Whether a C-BUS register is of a read or write type is fixed for a given C-BUS register address, thus one cannot both read and write the same C-BUS register address.

In order to provide ease of addressing when using this device with the CMX998, the C-BUS addresses shown below are arranged so as not to overlap those used on the CMX998. Thus, a common Chip Select (CSN) signal can be used, as well as common CDATA, RDATA and SCLK signals. Also note that the General Reset ($10) command on the CMX991/CMX992 differs from other CML devices (such as CMX998), which use $01 for this General Reset function.

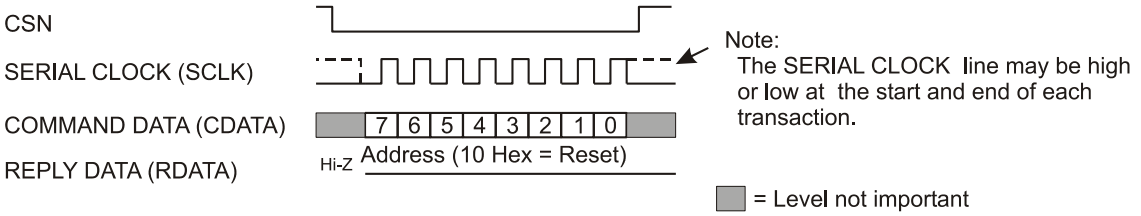
The following C-BUS register addresses are used in the CMX991/CMX992:

Write Only register;	
General Reset Register (Address only, no data)	Address $10
General Control Register, 8-bit write only.	Address $11
Rx Control Register, 8-bit write only.	Address $12
Rx Mode Register, 8-bit write only.	Address $13
Tx Control Register, 8-bit write only.	Address $14
Tx Mode Register, 8-bit write only.	Address $15
Tx Gain Register, 8-bit write only	Address $16
IF PLL M Divider Register, 8-bit write only	Address $20-$21
IF PLL N Divider Register, 8-bit write only	Address $22-$23
Read Only register;	
General Control Register, 8-bit read only.	Address $E1
Rx Control Register, 8-bit read only.	Address $E2
Rx Mode Register, 8-bit read only.	Address $E3
Tx Control Register, 8-bit read only.	Address $E4
Tx Mode Register, 8-bit read only.	Address $E5
Tx Gain Register, 8-bit read only	Address $E6
IF PLL M Divider Register, 8-bit read only	Address $D0-$D1
IF PLL N Divider Register, 8-bit read only	Address $D2-$D3

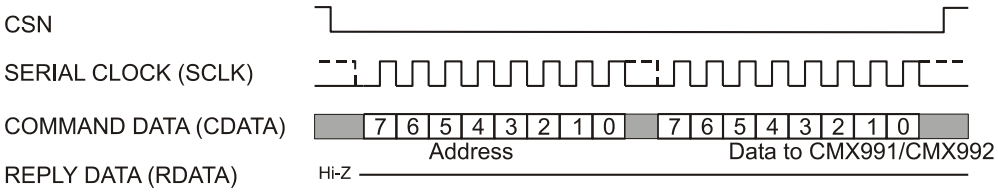
Notes:

- All registers will retain data if DVDD and VDDIO pins are held high, even if all other power supply pins are disconnected.
- If clock and data lines are shared with other devices, DV_{DD} and $V_{DD}IO$ must be maintained in their normal operating ranges otherwise ESD protection diodes may cause a problem with loading signals connected to SCLK, RDATA and CDATA pins, preventing correct programming of other devices. Other supplies may be turned off and all circuits on the device may be powered down without causing this problem.

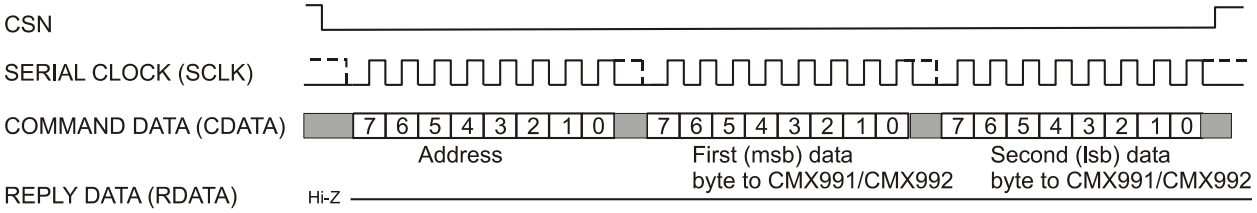
a) Single byte from µC (General Reset command)



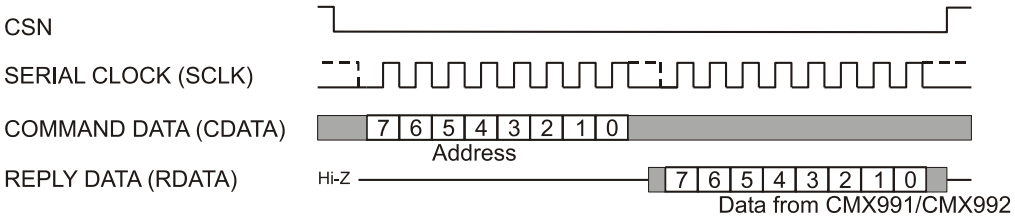
b) One Address and one Data byte from µC to CMX991/CMX992



c) One Address and 2 Data bytes from µC to CMX991/CMX992



d) One Address byte from µC and one Reply byte from CMX991/CMX992



e) One Address byte from µC and 2 Reply bytes from CMX991/CMX992

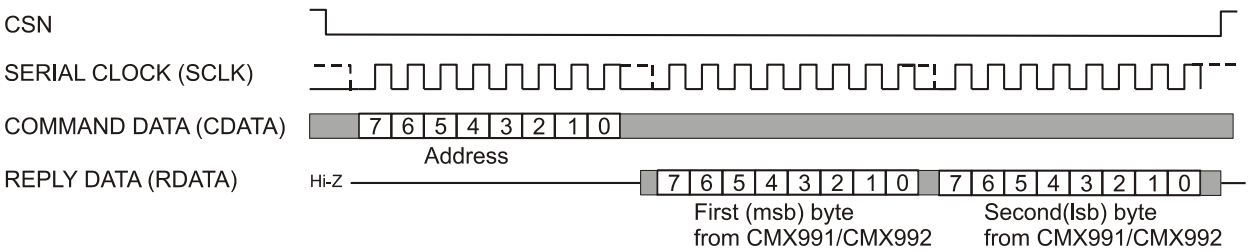


Figure 19 C-BUS Transactions

6.1 General Reset Command (CMX991/CMX992)

6.1.1 General Reset Command C-BUS address $10
(no data)

This command resets the device and clears all bits of all registers. The General Reset command places the device into powersave mode.

Whenever power is applied to the DVDD pin, a built in power-on-reset circuit ensures that the device powers up into the same state as follows a General Reset command. The RESETN pin on the device will also reset the device to the same state.

6.2 General Control Register (CMX991/CMX992)

6.2.1 General Control Register: C-BUS address $11
8-bit write-only

This register controls general features of the device.
All bits of this register are cleared to '0' by a General Reset command.

Bit:	7	6	5	4	3	2	1	0
	En Bias	IFH	Chan Sel	Rx Mode	VCO_NR2	VCO_NR1	VCO_Buff En	VCO_NR En

General Control Register b7, b1 and b0

These bits control power up/power down of the various blocks of the IC.
In all cases '1' = power up, '0' = power down.

b7	Enable bias generator.
b1	Enable VCO buffer
b0	Enable VCO NR amplifier. (When disabled the amplifier is bypassed to support the application of an external IF LO signal.)

General Control Register b6

IF Control bit, this applies to Tx and Rx intermediate frequencies:
for IF > 75MHz then set IFH = '1', for IF < 75MHz use IFH = '0'.

General Control Register b5 and b4

Output Mode Control

These bits control the output mode of the receiver. The Rx Mode bit determines if the output mode is I/Q or IF. In I/Q mode both receiver output channels are enabled and the Chan Sel bit has no effect. In IF mode only one of the receiver output channels is enabled, as selected by the Chan Sel bit.

NOTE: In IF Mode the I or Q baseband amplifier is also selected by the Chan Sel bit, i.e. only one of the baseband differential amplifiers can be powered up using the Amp Pwr bit in the Rx Control Register.

b5	b4	
x	0	I/Q Mode: I and Q channel can be enabled by bits in Rx Control Register.
0	1	IF Mode: only the I channel output and I channel differential amplifier can be powered up using the Rx Control Register.
1	1	IF Mode: only the Q channel output and Q channel differential amplifier can be powered up using the Rx Control Register.

General Control Register b3 and b2

VCO amplifier Negative Resistance (NR) control for optimum phase noise performance. These bits control the NR (magnitude of the negative transconductance) of the on-chip VCO NR amplifier. The NR minimum mode would thus be used with the lowest Q external tank circuit and NR maximum with the highest Q one.

b3	b2	
0	0	NR maximum
0	1	NR intermediate value
1	0	NR intermediate value
1	1	NR minimum

6.2.2 General Control Register C-BUS address $E1 8-bit read-only

This register reads the value in register $11, see section 6.2.1 for details of bit functions.

6.3 Rx Control Register (CMX991/CMX992)

6.3.1 Rx Control Register: C-BUS address $12 8-bit write-only

This register controls general features of the receiver such as Powersave.
All bits of this register are cleared to '0' by a General Reset command.

Bit:	7	6	5	4	3	2	1	0
	Mix Pwr	I/Q Pwr	Amp Pwr	SLI Pwr	LNA	DIV2	DIV1	VBIAS

Rx Control Register b7 - b3 and b0

These bits control power up/power down of the various blocks of the IC.
In all cases '1' = power up, '0' = power down.

b7	Enable receiver 1st mixer
b6	Enable IF amplifier/VGA stage, I/Q mixers, baseband filters
b5	Enable baseband differential amplifiers
b4	Enable SLI amplifier
b3	Enable LNA control signal (output pin LNAON)
b0	Enable V_{BIAS} (bias voltage on pin 43)

Rx Control Register b2 and b1
RF LO Divider control.

b2	b1	
0	0	RF MIXLO input divide by 2
0	1	RF MIXLO input no division
1	0	RF MIXLO input divide by 4
1	1	reserved – do not use

6.3.2 Rx Control Register C-BUS address $E2 8-bit read-only

This read-only register mirrors the value in register $12; see section 6.3.1 for details of bit functions.

6.4 Rx Mode Register (CMX991/CMX992)

6.4.1 Rx Mode Register: C-BUS address $13 8-bit write-only

This register controls operational modes of the receiver such as gain setting.
All bits of this register are cleared to '0' by a General Reset command.

Bit:	7	6	5	4	3	2	1	0
	IFin	Mix Out	I/Q Filter	Cal En	VGA4	VGA 3	VGA 2	VGA 1

Rx Mode Register b7 and b6
Mixer and IF Amplifier signal routing. b7 selects the IF input, b7 = '0' selects IFIP1 and b7 = '1' selects IFIP2. b6 selects the IF output of the Rx 1st Mixer, b6 = '0' selects MIXOUT1 and b6 = '1' selects MIXOUT2.

b7	b6	
0	0	Mixer output on MIXOUT1; IF input on IFIP1 and IFINN
0	1	Mixer output on MIXOUT2; IF input on IFIP1 and IFINN
1	0	Mixer output on MIXOUT1; IF input on IFIP2 and IFINN
1	1	Mixer output on MIXOUT2; IF input on IFIP2 and IFINN

Rx Mode Register b5
Writing b5 = '1' I/Q Filter BW = 1MHz; Writing b5 = '0' I/Q Filter BW = 100kHz.

Rx Mode Register b4
Enable Calibration Mode: disable LNA and 1st Mixer when b4 = '1'; normal operation when b4 = '0'. For further details see section 5.2.4.

Rx Mode Register b3 - b0
VGA Control. For further details see section 7.3.2.

b3	b2	b1	b0	
1	0	0	0	VGA= -48dB
0	1	1	1	VGA = -42dB
0	1	1	0	VGA = -36dB
0	1	0	1	VGA = -30dB
0	1	0	0	VGA = -24dB
0	0	1	1	VGA = -18dB

b3	b2	b1	b0	
0	0	1	0	VGA = -12dB
0	0	0	1	VGA = -6dB
0	0	0	0	VGA = 0dB (Maximum gain)

6.4.2 Rx Mode Register: C-BUS address $E3
8-bit read-only

This read-only register mirrors the value in register $13; see section 6.4.1 for details of bit functions.

6.5 Tx Control Register (CMX991 only)

6.5.1 Tx Control Register: C-BUS address $14
8-bit write-only

This register controls transmitter features including Powersave modes.
All bits of this register are cleared to '0' by a General Reset command.

Bit:	7	6	5	4	3	2	1	0
	0	TxMix Pwr	0	I/Q Mod Pwr	0	0	Freq	I/Q Out

Tx Control Register b7 - b4
These bits control power up/power down of the various blocks of the IC.
In all cases '1' = power up, '0' = power down.

b7	Reserved set to '0'
b6	Enable image-reject up-converter
b5	Reserved set to '0'
b4	Enable I/Q modulator, filters and its input circuits

Tx Control Register b3 and b2
Reserved set to '0'.

Tx Control Register b1
Controls internal operating mode for LO circuits, set b1 = '0' for frequency below 600MHz; set b1 = '1' for frequencies above 600MHz.

Tx Control Register b0
With b0 = '0' the output of the I/Q modulator is connected to the image-reject up-converter; with b0 = '1' the output of the I/Q modulator is connected to the TXIFOUT output pin.

6.5.2 Tx Control Register C-BUS address $E4
8-bit read-only

This read-only register mirrors the value in register $14; see section 6.5.1 for details of bit functions.

6.6 Tx Mode Register (CMX991 only)

6.6.1 Tx Mode Register: C-BUS address $15
8-bit write-only

This register controls transmitter features.
All bits of this register are cleared to '0' by a General Reset command.

Bit:	7	6	5	4	3	2	1	0
	0	0	IF_Filter BW2	IF_Filter BW1	0	HiLo	TxRFDiv	TxIFDiv

Tx Mode Register b7 and b6
Reserved set to '0'.

Tx Mode Register b5 and b4
These bits select the Tx IF filter bandwidth:

b5	b4	Tx IF filter bandwidth
0	0	45MHz
0	1	60MHz
1	0	90MHz
1	1	120MHz

For further information see section 7.12.

Tx Mode Register b3
Reserved set to '0'.

Tx Mode Register b2
This bit controls the mixing arrangements in the image-reject up-converter as follows:

b2 = '0' $f_{rf} = f_{lo} - f_{if}$
b2 = '1' $f_{rf} = f_{lo} + f_{if}$

Tx Mode Register b1
Controls the divider for the RF Local Oscillator: b1 = '0' selects RF LO divided by 2 mode and b1 = '1' selects RF LO divided by 4 mode.

Tx Mode Register b0
Controls the divider for the IF Local Oscillator: b0 = '0' selects IF LO divided by 4 mode and b0 = '1' selects IF LO divided by 2 mode.

6.6.2 Tx Mode Register C-BUS address $E5
8-bit read-only

This read-only register mirrors the value in register $15; see section 6.6.1 for details of bit functions.

6.7 Tx Gain Register (CMX991 only)

6.7.1 Tx Gain Register: C-BUS address $16
8-bit write-only

This register controls transmitter gain features.

All bits of this register are cleared to '0' by a General Reset command.

Bit:	7	6	5	4	3	2	1	0
	Gain2	Gain1	0	0	0	0	0	0

Tx Gain Register b7 and b6
I/Q Input Gain Control: These bits control the internal gain applied to input I/Q signals before they are sent to the I/Q modulator.

b7	B6	
0	0	I/Q input gain = 0dB
0	1	I/Q input gain = -6dB
1	0	I/Q input gain = +6dB
1	1	reserved, do not use

Tx Gain Register b5 - b0
Reserved set to '0'.

6.7.2 Tx Gain Register C-BUS address $E6
8-bit read-only

This read-only register mirrors the value in register $16, see section 6.7.1 for details of bit functions.

6.8 IF PLL M Divider (CMX991/CMX992)

6.8.1 PLL M Divider C-BUS Addresses $21 and $20
8-bit write-only

These registers set the M divider value for the PLL (Reference divider – see Figure 17). The PLL dividers are not updated until both registers ($21 and $20) have been written. The order of writing these registers is not important. Bits also control the enable of the PLL and charge-pump blocks and these control bits are active as soon as $21 is written.

	$21								**$20**							
Bit:	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	E	LD_Synth	CP	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0

M12 - M0
Phase Locked Loop M divider value.
CP
$21, b5 = '1' enables the Charge Pump, $21 b5 = '0' puts the Charge Pump into high impedance mode.

LD_Synth
Only write '0' to b6 of $21 (when read, this shows the integer N PLL lock status).

E
$21, b7 = '1' enables the PLL; b7 = '0' disables the PLL – in this mode an external local oscillator can be supplied to the IC.

6.8.2 PLL M Divider C-BUS Addresses $D1 and $D0
8-bit read-only

These registers read the respective values in registers $20 and $21 ($D0 reads back $20 and $D1 reads back $21), see section 6.8.1 for details of bit functions.

NOTE: $21 b6 indicates the lock status. If set to '1' then the PLL is locked.

6.9 PLL N Divider (CMX991/CMX992)

6.9.1 PLL N Divider C-BUS Addresses $23 and $22
8-bit write-only

These registers set the N divider value for the PLL (Feedback divider – see Figure 17). The PLL dividers are not updated until both registers ($23 and $22) have been written. The order of writing these registers is not important.

	$23								$22							
Bit:	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	0	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0

N14 - N0
Phase Locked Loop N divider value.
(NB: when using an external VCO see the note at the end of section 4.5).

$23, b7
Reserved, set to '0'.

6.9.2 PLL N Divider C-BUS Addresses $D3 and $D2
8-bit read-only

These registers read the respective values in registers $22 and $23 ($D2 reads back $22 and $D3 reads back $23), see section 6.9.1 for details of bit functions.

7 Application Notes

7.1 General

The CMX991/CMX992 chips are RF systems designed for digital wireless applications. These devices address the needs of various data systems, both product standards and regulatory requirements, including TETRA (EN 300 392-2, EN 300 394-1, EN 302 561) and DMR (EN 300 113). APCO Project 25 (TIA-102.CAAB).

7.2 Using the CMX992 with the CMX998

The CMX998 device linearises an external RF PA and is an ideal complement to the CMX992.

To simplify CMX992+CMX998 designs the CMX992 uses the same physical interface architecture as the CMX998 (SDI is equivalent to CDATA, SDO to RDATA). The C-BUS registers of the two devices are also compatible and allow the CMX992 and CMX998 to be connected to the same C-BUS interface pins, including Chip Select (CSN), assuming the drive capabilities of the host are adequate.

7.3 Receiver Gain Issues

7.3.1 System Gain

The CMX991/CMX992 receiver section provides exposed interfaces for external filters and matching networks to support a flexible range of user-specific configurations. The total gain of a specific receiver design will be influenced by specific external IF filter and matching circuits.

EV9910B/EV9920B evaluation boards provide a complete receiver design (from external LNA input to baseband output, including external filters and matching networks) that provides ~61 dB total system gain. Their documentation provides specific design and performance details.

7.3.2 Gain Adjustment

The adjustment of the receiver gain is controlled by b3 – b0 of the Rx Mode Register ($13), see section 6.4.1. The switching of gain during reception of data should be avoided as phase discontinuities will occur at transitions from –18dB to –24dB and –24dB to –18dB. The architecture of the gain control is shown in Figure 20.

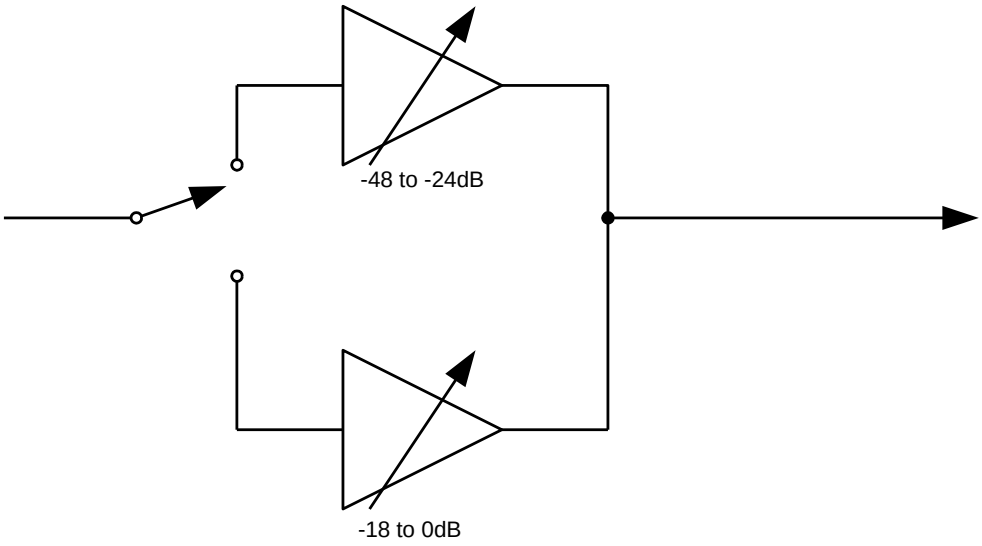


Figure 20 Receiver Gain Control

7.3.3 Gain Compression

Typical IF gain compression is shown for the different gain control settings in Figure 21 and summarised in Table 13, the measurements use a 50Ω terminating resistor at pin IFIN1 and are for a 45MHz IF signal. See also section 7.7.3.

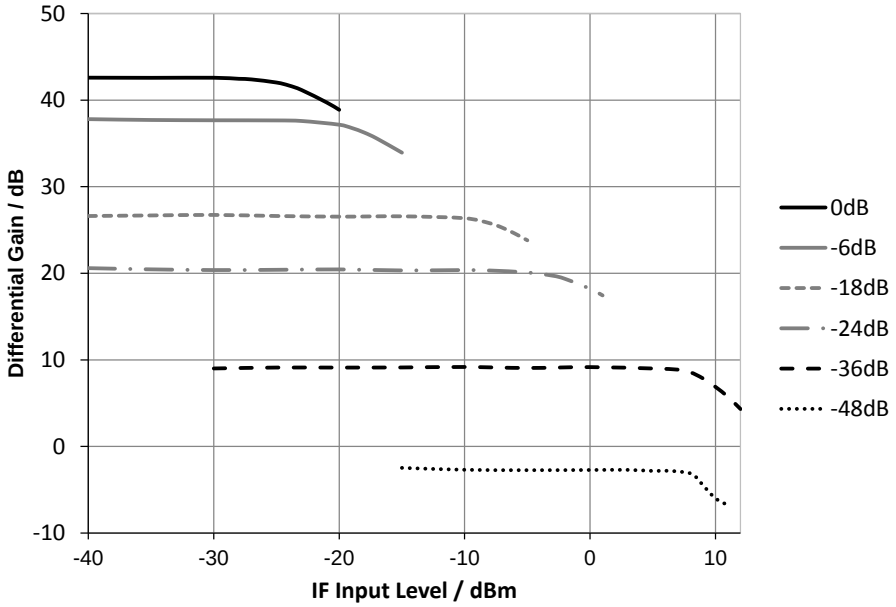


Figure 21 Typical IF Gain Compression at 45MHz with Gain Control Setting

VGA Setting (dB)	Input 1dB Compression Point / dBm
0	-25
-6	-19
-12	-13
-18	-8
-24	-3
-30	3
-36	9
-48	8.5

Table 13 Typical IF Gain Compression

7.4 Oscillator Components for Alternative Intermediate Frequencies.

Table 11 shows the tank circuit values for operating the internal IF local oscillator and negative resistance amplifier at 180MHz (45MHz receive IF). With reference to Figure 13, typical values for other common intermediate frequencies are shown below.

Receive IF Frequency /MHz	NR Value	VCO Frequency /MHz	L1 Value /nH (Coilcraft Type)	C1 Value	C2 and C3 Value	CV1 and CV2 Type	MHz/V
10.7	00	42.8	220 (0805CS)	47pF	47pF	SMV1255-079LF	1.25
21.4	00	85.6	100 (0805CS)	18pF	47pF	1SV305	2.0
70	00	280	18 (0805CS)	1.2pF	18pF	1SV305	6.3
90	00	360	10 (0805CS)	0.8pF	15pF	1SV305	5.9
110.5	01	442 §	5.6 (0805CS)	0.5pF	15pF	1SV305	5.5
§ NOTE: Above 400MHz reliability of operation under all conditions cannot be guaranteed.							

Table 14 Typical IF VCO Circuit Values for a Variety of IF Frequencies

7.5 RF Mixer Input Matching

With reference to Figure 22 and Table 15 below, the receiver input can be matched to alternative frequencies, with typical values shown. In all cases, R1, R2 = not fitted and C3, C4 = 1nF.

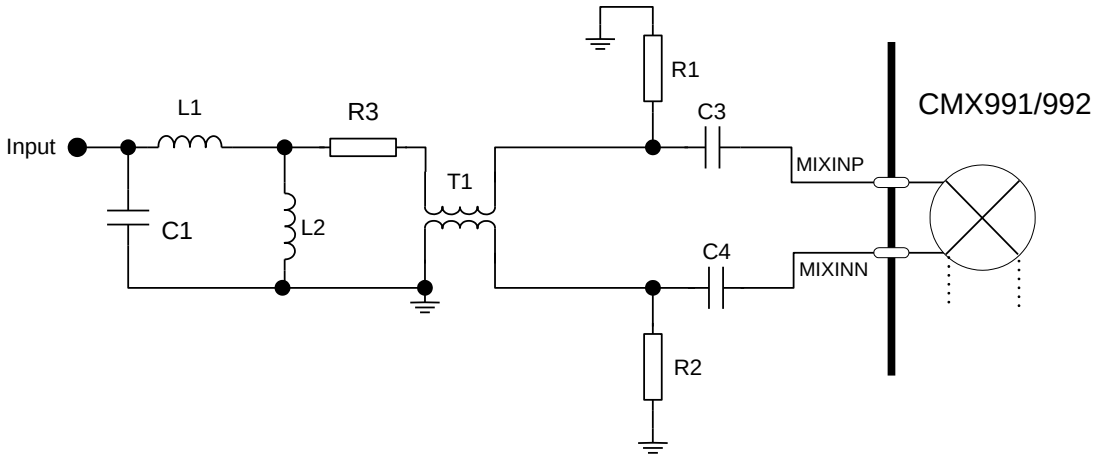


Figure 22 Receiver Matching Components

Component	100MHz	155MHz	850MHz	950MHz
L1	220nH	150nH	0R	0R
L2	2.7pF	Not fitted	4.7nH (0603)	6.8nH (0603)
R3	0R	0R	6.8pF	3.9pF
C1	Not fitted	4.7pF	Not fitted	Not fitted

Table 15 Receiver Input Match Circuit for Other Operating Frequencies

7.6 RF Mixer IF Output Matching

In a typical implementation, the MIXOUT pin(s) will require matching from around 500Ω ‖ 4pF to the input of a crystal filter. The impedance of such a filter will often only be specified within the passband; it will be very different outside the passband. Careful broad band termination of the MIXOUT port is therefore critical in achieving the optimum intermodulation and spurious response performance from the system. The use of a shunt resistive element at MIXOUT is a compromise between system gain and intermodulation. Values between 1,000ohms and 120ohms can be used in practice. Some shunt capacitance at MIXOUT also helps in suppressing harmonics of the RF and LO inputs that may appear at the port, so a Pi network is recommended.

With the matching network of Figure 7, the rejection of the half IF response has been found to be optimum using high side mixing.

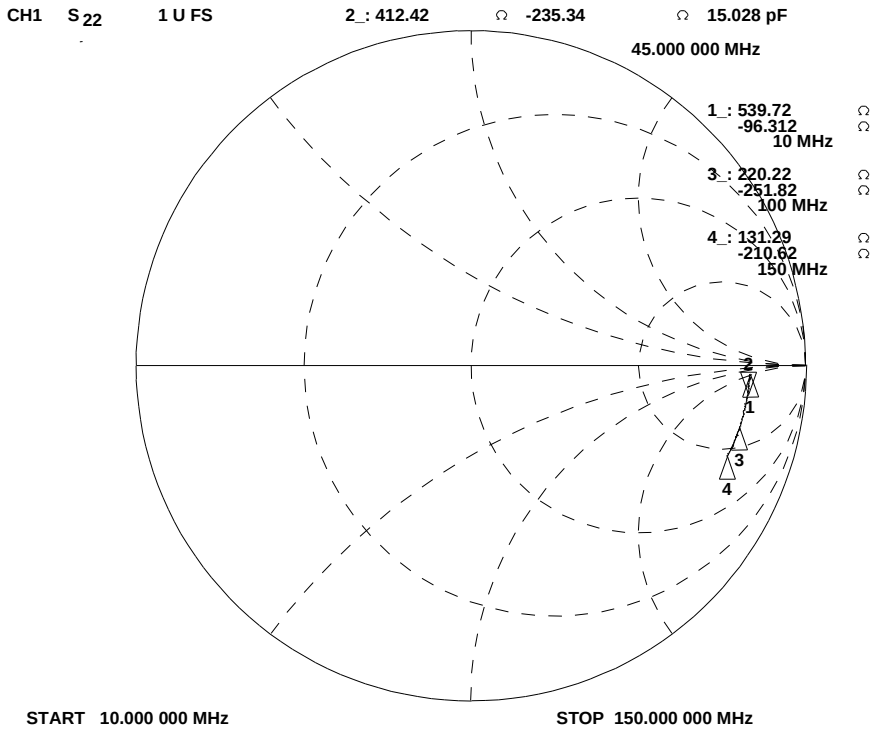


Figure 23 MIXOUT1 Port Impedance (unmatched)

Frequency / MHz	Series Impedance / Ω	Parallel Equivalent
10	540 – j 96	557Ω // 5.1pF
45	412 - j 235	547Ω // 3.7pF
100	220 – j 252	508Ω // 3.6pF
150	131 – j 211	469Ω // 3.6pF

Table 16 MIXOUT Equivalent Impedances

7.7 IF Input Matching

7.7.1 IF Input Matching Options

The configuration of the IF input has a significant effect on the measured performance. This is demonstrated in Table 17, where the receiver is measured with a 50 ohm source and three different input conditions. The typical input impedance of the IFIP1 or IFIP2 port is shown in Figure 24, the impedance does not change much with attenuation setting (Table 18). A matched network provides the best noise figure and maximum gain, however intermodulation will be degraded in this condition due to the larger signal levels indicated by the extra gain. The ‘Straight in’ condition means that the 50 ohm signal source was connected directly to either IFIP1 or IFIP2 input via a dc blocking capacitor.

Input Condition	Noise Figure /dB	Gain /dB
50R shunt resistor	13	43
matched network	5	61
straight in	8	49

Table 17 Noise Figure and Gain of IF Amp, VGA, I/Q Mixer and Baseband Filters

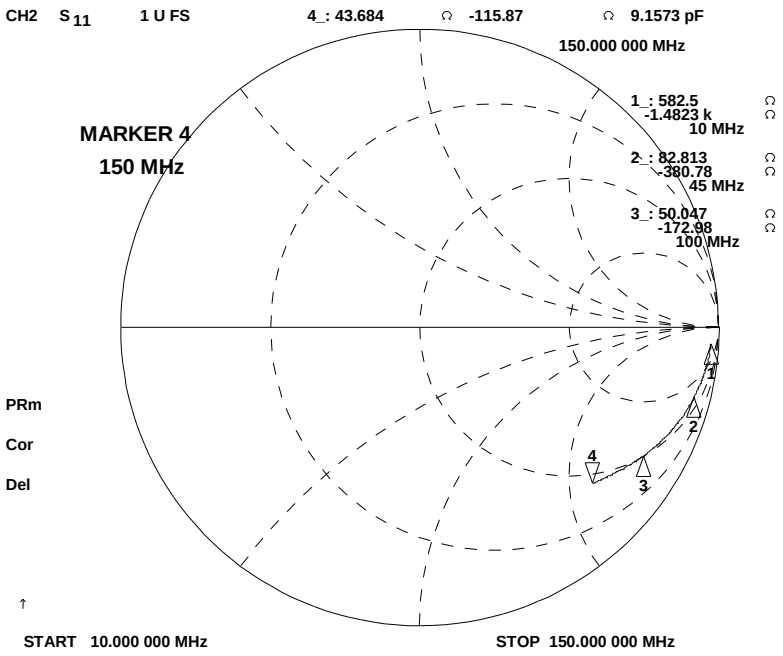


Figure 24 IFIP1 Input Impedance at 0dB attenuation

Freq (MHz)	0dB Setting	6dB Setting	12dB Setting	18dB Setting	24dB Setting
10	4.35kΩ//9.3pF	4.61kΩ//9.2pF	4.80kΩ//8.2pF	6.63kΩ//8.3pF	4.75kΩ//8.8pF
45	1.836kΩ//8.9pF	1.97kΩ//8.4pF	2.3kΩ//7.9pF	2.21kΩ//8.2pF	1.96kΩ//8.8pF
100	648Ω//8.5pF	744Ω//8.0pF	776Ω//7.6pF	723Ω//7.8pF	633Ω//8.3pF
150	351Ω//8.0pF	402Ω//7.6pF	390Ω//7.3pF	365Ω//7.3pF	326Ω//7.8pF

Table 18 IFIP1 Port Impedance (Parallel Equivalent Circuit Models)

The gain calculated in the 'Straight in' case is based on direct conversion of the signal generator power to a voltage and calculating the gain based on the output voltage. The output signal is the differential signal at RXIN / RXIP (or RXQN and RXQP) so if the voltage is measured at a single pin the signal level must be doubled to get the appropriate differential signal level. Also it should be noted that making a simple conversion of the power in the 'Straight in' case is erroneous as the voltage calculated will be a potential difference. As the circuit is un-matched an e.m.f. would be more appropriate (i.e. twice the p.d. value).

The ‘straight in’ value is useful in calculating overall circuit gain, as in section 7.3.1, but it is necessary to correct for the difference between e.m.f. and p.d. i.e. reduce the gain by 6dB, also the noise figure must be degraded by 6dB. To exemplify this some typical measurements are shown in Table 19. The theoretical correction of 6 dB was actually measured at 5.4 dB (which is reasonable as the 6 dB figure would only be measured without any load applied to the source). The slightly positive figure for the 50 ohms is because the IFIP1 pin presents an impedance that reduces the effective input impedance slightly below 50 ohms.

	SNR for -100dBm input signal / dB	NF / dB	Gain / dB	Gain correction based on measure input voltage of 45MHz signal at IFIP1 compared to the source operated into 50 ohms / dB	Corrected gain / dB	Corrected NF / dB
Straight in	63	8	48.9	-5.4	43.5	13.4
50R shunt resistor	58	13	43.9	+0.2	44.1	12.8
Matched	65.5	5.5	61.4	-0.6	60.8	6.1

Table 19 IF Noise Figure Measurements at 45 MHz

7.7.2 Variations in IF Noise Figure with Matching and Gain

The noise figure of the IF section varies with gain control setting and matching arrangement, typical performance is shown in Figure 25.

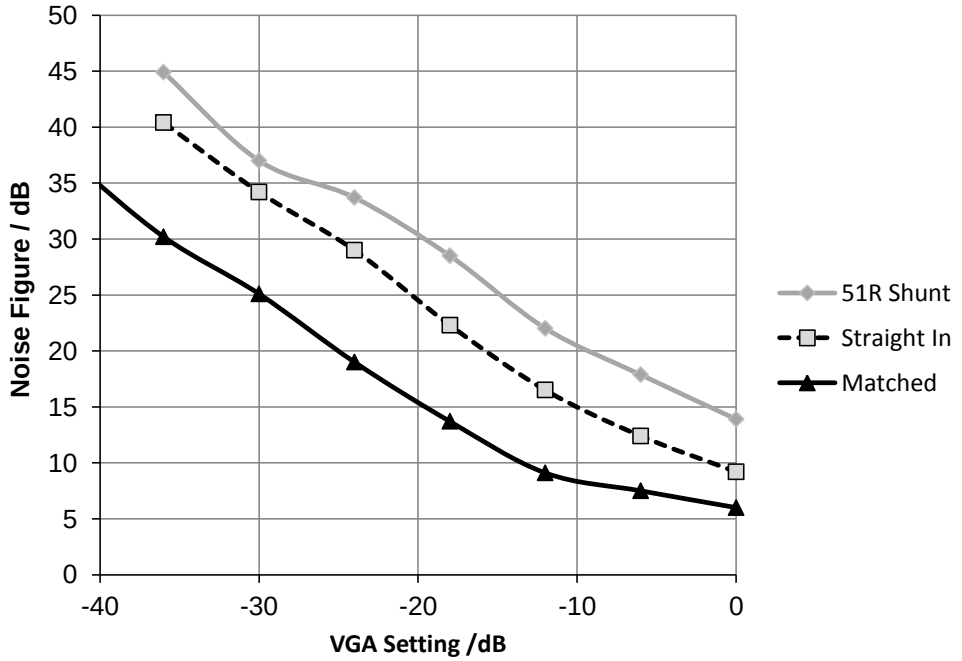


Figure 25 Typical Variation in IF Noise Figure

7.7.3 Variations in Gain Compression with IF Matching

The gain compression of the IF section varies with matching arrangement, typical performance is shown in Figure 26.

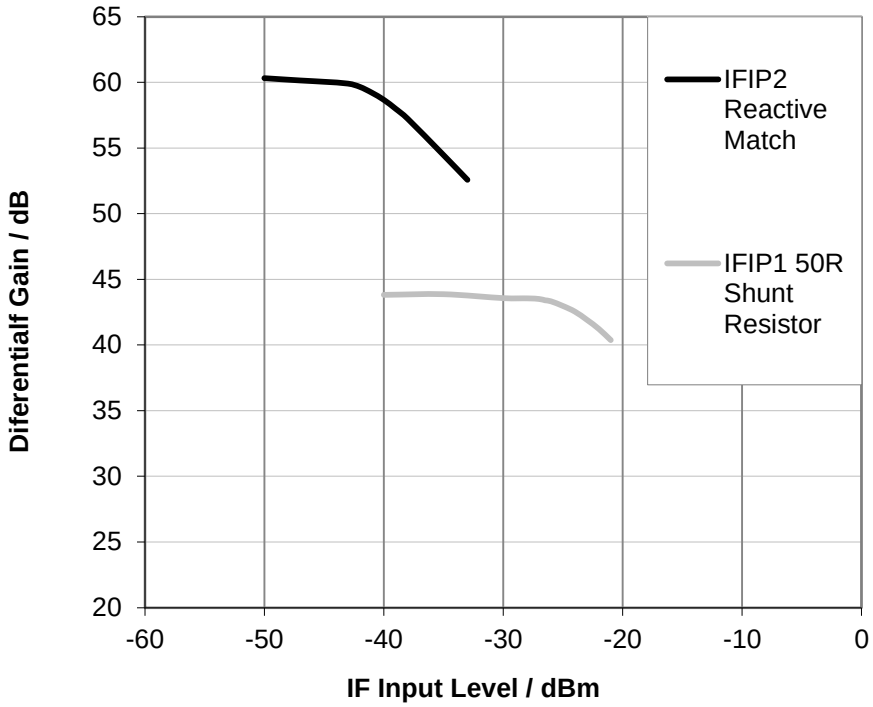


Figure 26 Typical Variation in IF Gain Compression

7.8 Signal Level Indicator (SLI)

The SLI output is an analogue output which gives an indication of the signal level in the receiver IF input prior to the IF variable gain amplifier stage. A typical use of this signal would be to allow a host to control the receiver gain settings in the CMX991/CMX992. In such an application the SLI pin would be connected to an analogue-to-digital converter which would sample the level at which the host would then base the choice of gain setting on. The host would then set the appropriate gain value via C-BUS (see section 6.4). When SLI is enabled there is a degradation in the noise figure of the IF stages. In many application circuits this degradation does not cause a significant reduction in overall receiver sensitivity as earlier stages dominate the system noise figure. Typical performance is shown in Figure 27 for the IC alone (IF input) and Figure 28 for a typical CMX991/CMX992 receiver system, measured using the EV9910B/EV9920B evaluation PCB.

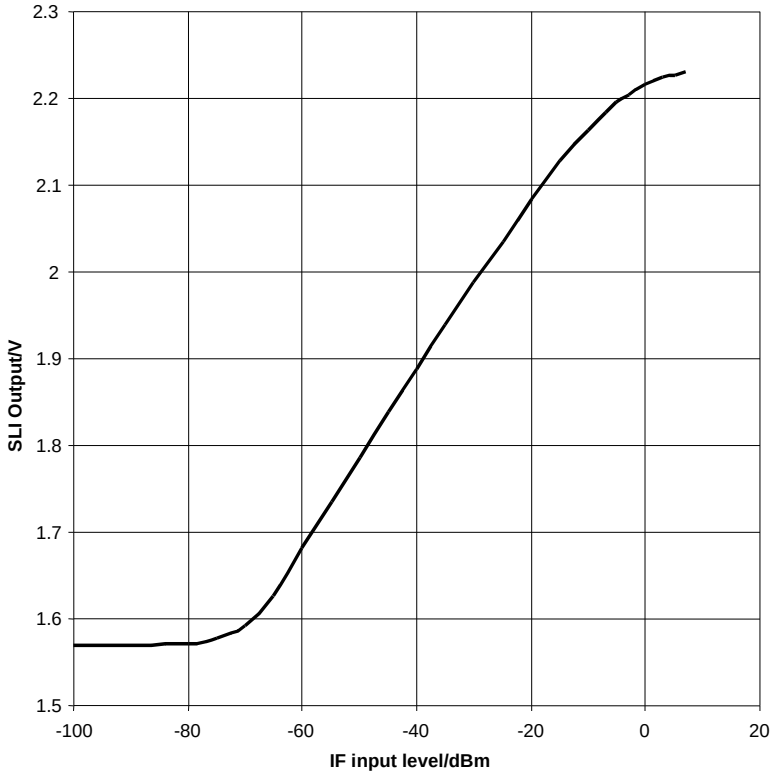


Figure 27 Typical SLI Performance

(with the signal applied to IFIP1 or IFIP2 and terminated with a 50ohm resistor)

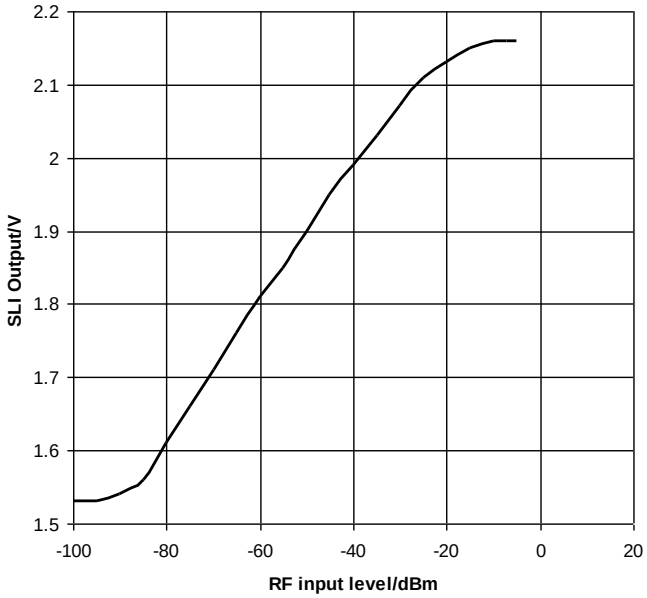


Figure 28 Typical SLI Performance in an Application Circuit (EV9920B)

(Input 460MHz, 25kHz IF crystal filter: 45G15B1)

7.9 Receiver Spurious Rejection Performance

The immunity of a receiver to signals away from the wanted channel is an important factor in the overall quality of a radio receiver. Receivers may suffer interference due to off-channel signals due to a variety of mechanisms including intermodulation, blocking and receiver spurious responses.

7.9.1 Blocking

The CMX991/CMX992 blocking performance can be evaluated by injecting an unwanted signal at a 1MHz offset and observing the IF output response with the unwanted signal present or not present, as shown in Figure 29. The channel filtering was used at the IF output of the CMX991 1st mixer to ensure the spectrum analyser was capable of measuring the low levels and a LNA was before the spectrum analyser to ensure the measurement was above the analyser noise floor. The results were taken with the LO path in /2 mode, LO at 820MHz. The wanted signal was at 455MHz @-110dBm and the unwanted was –18dBm at 455.9MHz. The plot in Figure 29 shows the output response with (upper trace) and without (lower trace) the unwanted signal present. The noise floor rises by 3.6dB when the blocker is present; note that the scale is 5dB/div on plot.

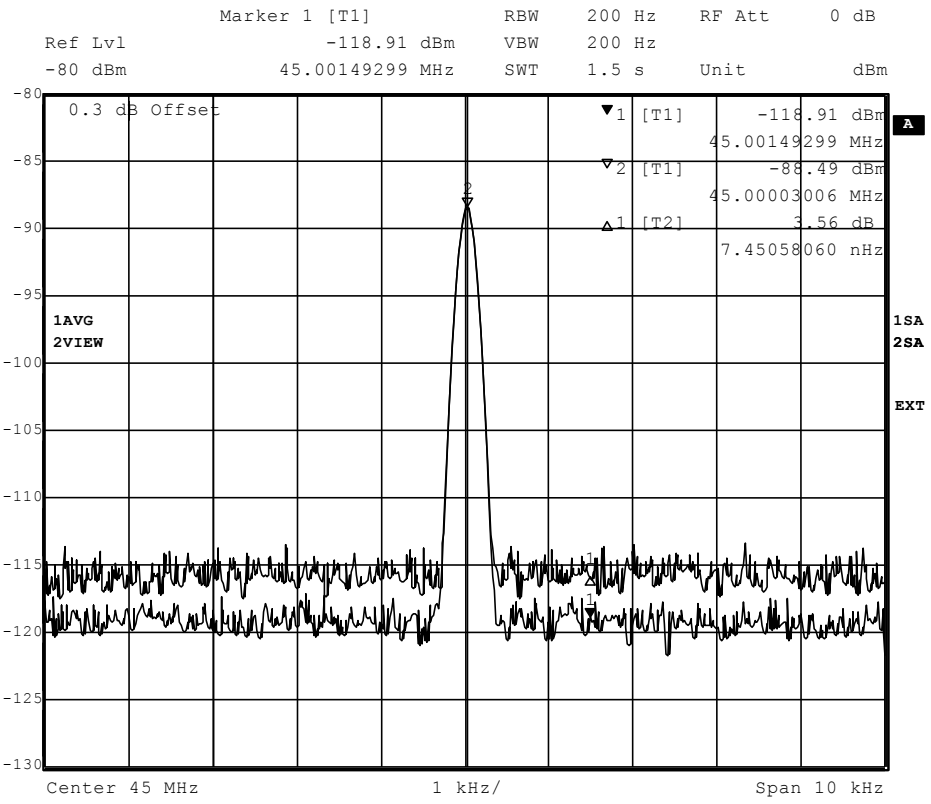


Figure 29 IF Output Response with and without Blocking Signal Present

7.9.2 Half IF Response

The half IF response occurs at a frequency half the 1st IF frequency away from the wanted signal is a 2nd order product. For example if receiving at 455MHz with a 1st IF of 45MHz and 'low side' LO at 410MHz the half IF response is at 455MHz – (45/2)MHz = 432.5MHz.

The half IF response of the CMX991/CMX992 is dependent on the output matching of the 1st mixer. The arrangements described in 7.4 should be applied and matching can be optimised for a particular design. The half IF performance has some variability between devices and care needs to be taken to ensure sufficient margin exits for device variations, a standard deviation of 1.9 may be used for such calculations.

7.10 Receiver I/Q Filters

Two filtering modes are selectable using the 'I/Q Filter' bit (b5 of the Rx Mode Register, $13). The default setting of the 'I/Q Filter' bit is '0' and in this case the I/Q output bandwidth is limited to about 100kHz. With the 'I/Q Filter' bit set to '1' the I/Q output has a bandwidth of approximately 1MHz. Typical frequency responses for the two modes are shown in Figure 30.

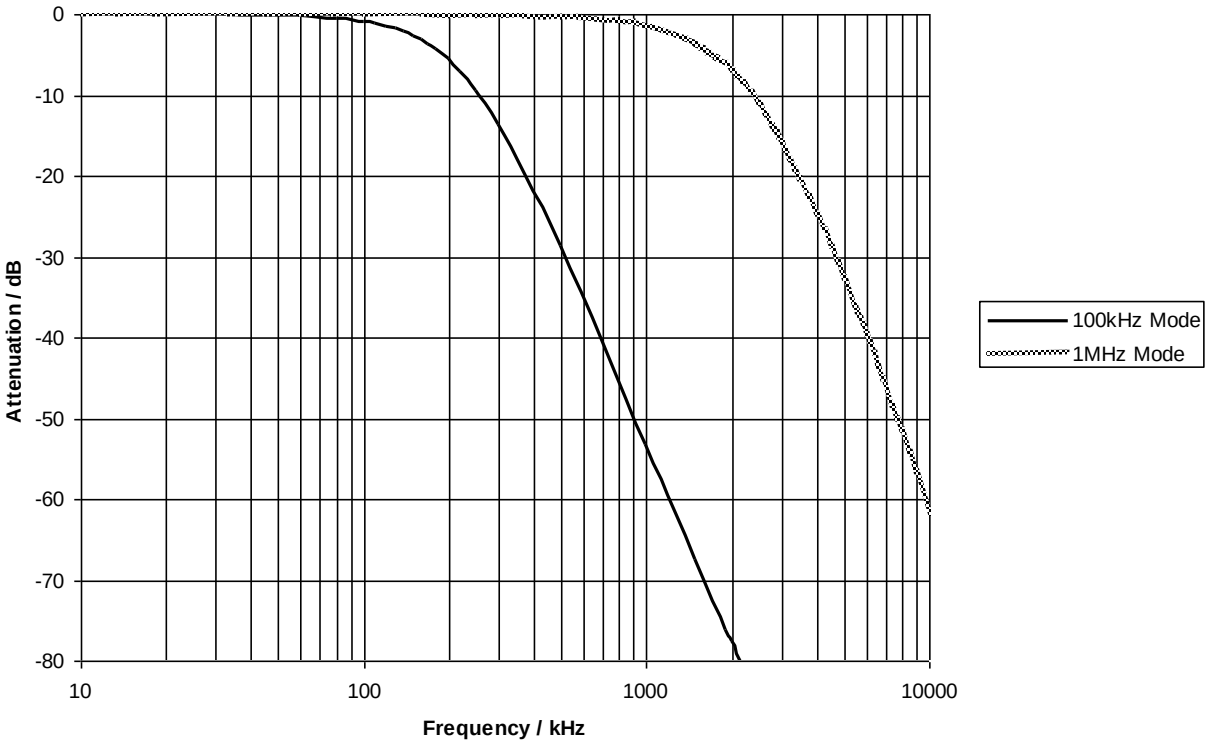


Figure 30 Typical Receiver I/Q Frequency Response

7.11 Modulation Accuracy

Note: This section applies only to the CMX991.

To check the phase error of the transmitter, a CMX910 Evaluation Kit (EV9100) was used to drive the Tx I/Q modulator differentially with GMSK. This setup tested 9.6kbps GMSK with a BT of 0.4, to fit in a 25kHz channel. The plot in Figure 31 shows the Tx Output ACP performance as ~77dBc and Table 20 shows the RMS phase error as being less than 1 degree (~0.8 degrees). The differential output level from the EV9100 is 2Vp-p, therefore the 0dB I/Q gain setting was used.

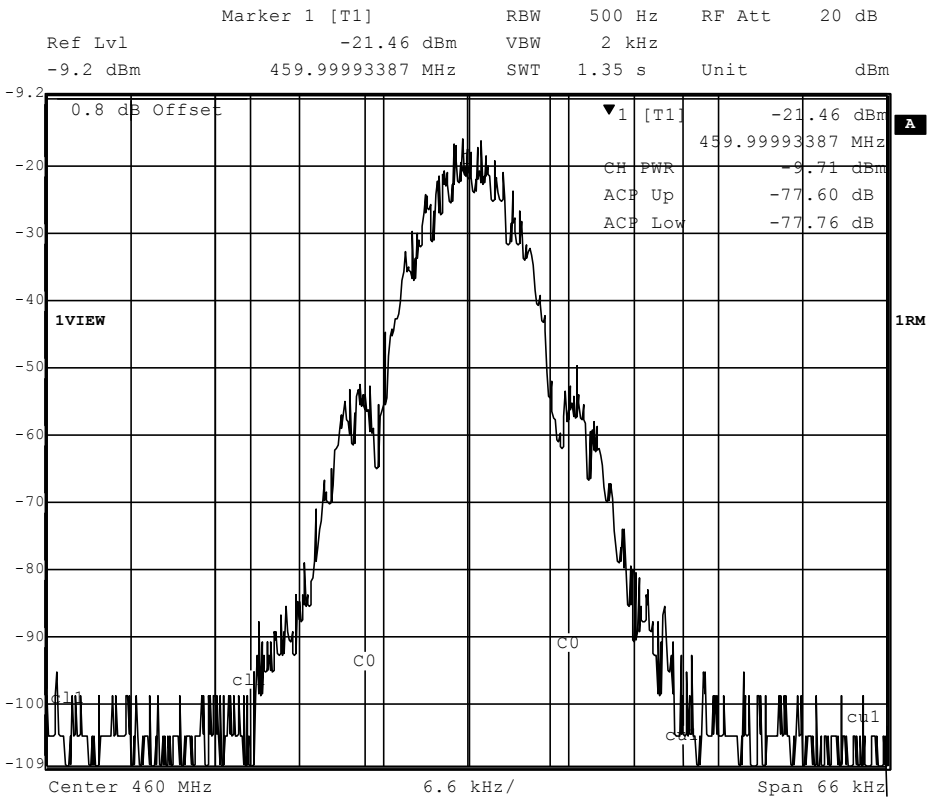


Figure 31 Tx Output with 9.6kbps GMSK from an EV9100
(TxIF = 90MHz, ACP ~ 77dBc)

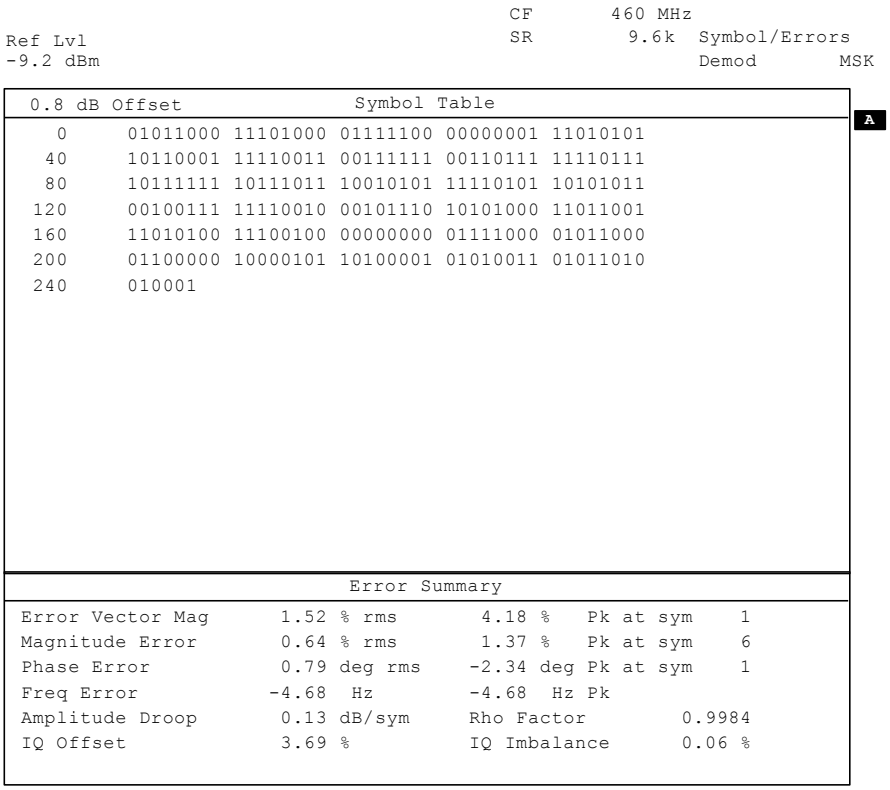


Table 20 Symbol/Error Table for the Tx with 9.6kbps GMSK from an EV9100

7.12 Post I/Q Modulator Filter

Note: This section applies only to the CMX991.

The filters following the I/Q modulation process (see Figure 16) are designed to reduce harmonic content of the signal. The bandwidth of the filters is selectable using b4, b5 of the Tx Mode register ($15), see section 6.6.1. Four modes are supported 45MHz, 60MHz, 90MHz and 120MHz; these frequencies do not specify the cut-off of the filters but are intended as a guide to the IF frequency to be used with each filter. Note however that other IF frequencies may also be used.

The internal filter responses are shown in Figure 32. In practice the filter responses are slightly modified by the internal circuits and the response at the TXIFOUT pin is shown in Figure 33.

It is also important to note that the IFH bit (b6, General Control Register $11, see section 6.2.1) has an effect on the response. IFH = ‘0’ is recommended for IF frequencies below 75MHz and IFH = ‘1’ for IF frequencies above 75MHz. The effect is shown in Figure 34. Note that 90MHz and 120MHz modes are not recommended with IFH = ‘0’.

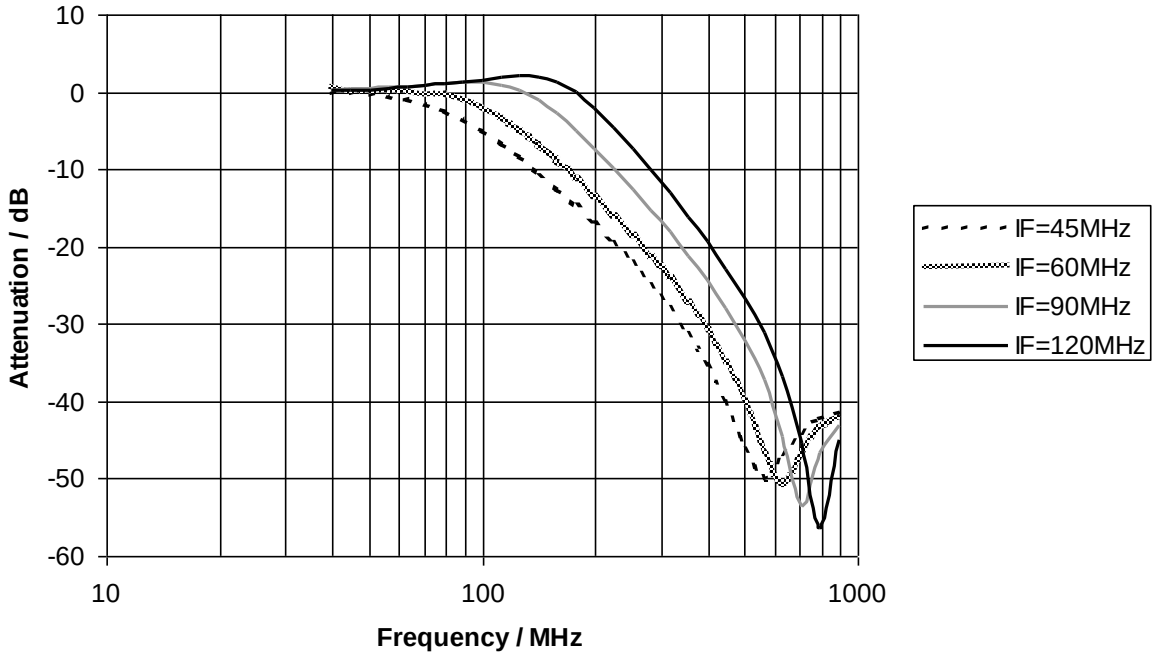


Figure 32 Transmitter Path IF Filters

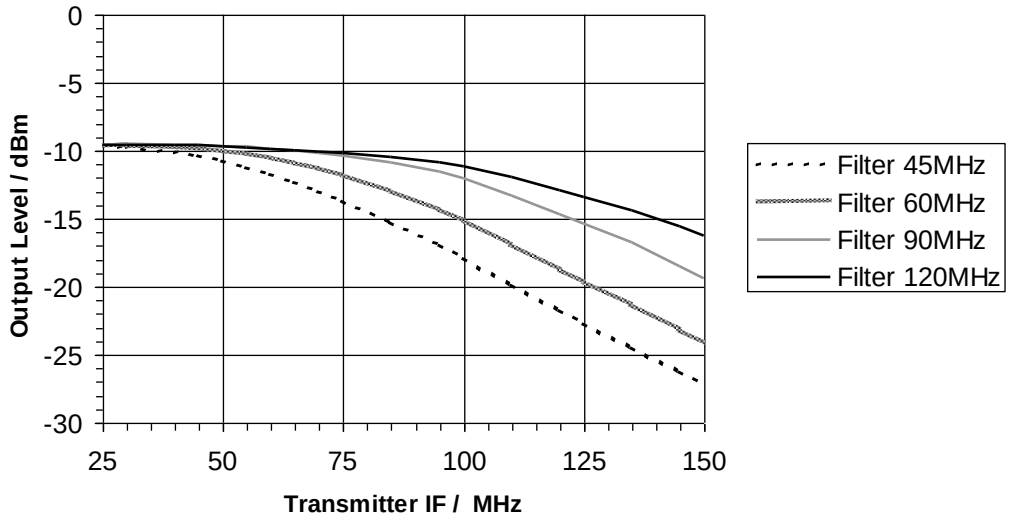


Figure 33 Transmitter IF Output Showing Filter Responses with IFH bit = '1'

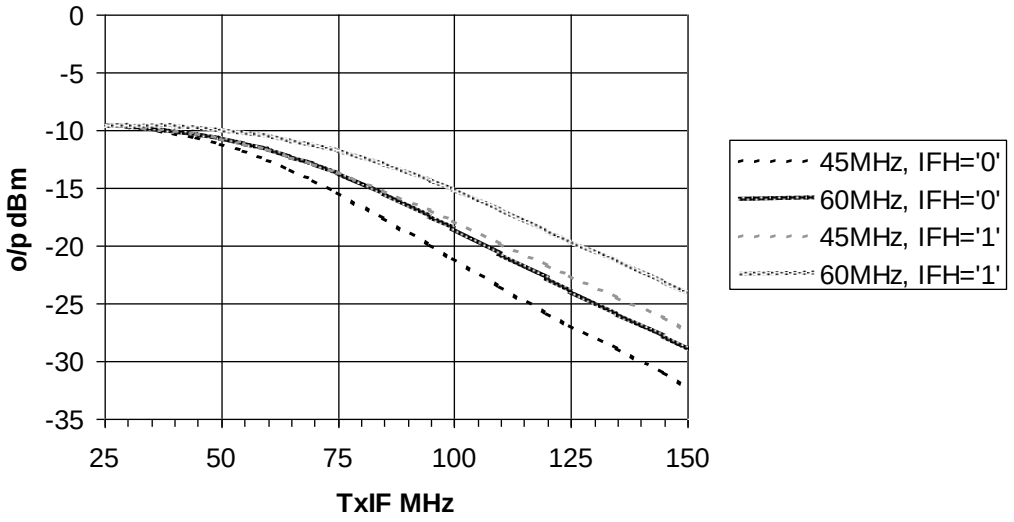


Figure 34 Effect of IFH on 45MHz and 60MHz Transmitter IF Filters

7.13 Variation in I/Q dc Offset with Temperature

7.13.1 Overview

All I/Q RF mixer designs exhibit dc offset generation in receivers and LO leakage resulting from dc offsets in transmitters. Such dc offsets, if not properly compensated, can reduce the effective dynamic range of a receiver and degrade modulation accuracy in transmitters. Receiver offsets are caused by a range of effects including nonlinear mixing of unwanted frequencies leaking into the mixer via the RF input or other routes (e.g. PCB ground plane, on-chip leakage paths, etc.), LO leakage and transistor matching effects. Additionally, wider system level issues can be a cause where the presence of unwanted signals can generate dc offsets as a result of finite second order intermodulation performance of the mixer.

Due to this complexity and the associated costs of a hardware solution to remove dc offsets from an I/Q mixer design it is usual to apply a dc offset compensation process in host software which allows the radio system engineer to maximise radio performance. Software is also preferred because dc offset mitigation strategies are typically optimised for a particular RF system (i.e. dependent on the air-interface characteristics). In a receiver this process typically involves measuring the dc offset at the baseband I/Q signal pins and applying a suitable offset compensation during the subsequent signal processing. For further information see also section 5.2.4.

7.13.2 Variation of Receiver I/Q Offsets

The change in the I/Q dc offset over temperature can be an important parameter for the operation of a correction scheme. Assuming the absolute offset is normalised at +20°C then the offset variation over the full operating temperature range (-40°C to +85°C) is typically only a few mV however designers are recommended to assume a maximum variation of up to ±10mV. The slope of the variation is not guaranteed as it varies between devices and between I and Q channels on a particular device. The variation over -10°C to +55°C is typically half the variation over the full temperature range.

8 Performance Specification

8.1 Electrical Performance

For definition of voltage and reference signal, see Table 2.

8.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

ESD Warning: This high performance RF integrated circuit is an ESD sensitive device which has unprotected inputs and outputs. Handling and assembly of this device should only be carried out at an ESD protected workstation.

	Min.	Max.	Units
Supply (AV_{DD} – AV_{SS}) or (DV_{DD} – DV_{SS})	-0.3	+4.0	V
Voltage between AV_{SS} and DV_{SS}	-50	+50	mV
Voltage between AV_{DD} and DV_{DD}	-0.3	+0.3	V
Current into or out of DGND, any AV_{DD} pin or DVDD	-75	+75	mA
Current into or out of AGND (exposed metal pad)	-200	+200	mA
Current into or out of any other pin	-20	+20	mA

Q3 Package	Min.	Max.	Units
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	1750	mW
... De-rating	–	17.5	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

8.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

Notes	Min.	Max.	Units
Supply (AV_{DD} – AV_{SS}) and (DV_{DD} – DV_{SS})	3.0	3.6	V
IO Supply (V_{DD}IO – DV_{SS})	1.6	3.6	V
Operating Temperature	-40	+85	°C

8.1.3 Operating Characteristics

The following conditions apply unless otherwise specified:
V_{DD} = AV_{DD} = DV_{DD} = 3.0V to 3.6V; V_{SS} = AV_{SS} = $DV_{SS,}$ T_{AMB} = -40°C to +85°C, SLI disabled.

8.1.3.1 DC Parameters

DC Parameters	Notes	Min.	Typ.	Max.	Units
Total Current Consumption					
Powersave Mode	A, F	–	10	60	µA
V_{BIAS} Only	C	–	2.1	2.6	mA
Operating Currents	J				
Rx Only (with SLI)	D	–	58	75	mA
Rx Only (SLI Disabled)	D	–	52	–	mA
Rx IF and PLL Only	H	–	37	–	mA
Synth Only	D	–	14	20	mA
Tx Only (RF Output)	G	–	82	108	mA
Tx Only (IF Output)	G	–	61	76	mA
Current from V_{DD}IO	B	–	0.3	600	µA
Logic '1' Input Level		70%	–	–	V_{DD}IO
Logic '0' Input Level		–	–	30%	V_{DD}IO
Output Logic '1' Level (I_{OH} = 0.6 mA)		80%	–	–	V_{DD}IO
Output Logic '0' Level (I_{OL} = -1.0 mA)		–	–	+0.4	V
Power-up Time					
Reference Voltage	E	–	–	0.5	ms
All Blocks Except Reference Voltage	E	–	–	10	µs
Internal Bandgap Voltage (V_{BG})		1.06	1.13	1.2	V
External Bias Voltage (V_{BIAS}) – derived from V_{BG}		1.45	1.6	1.75	V

Notes:
A. Powersave mode includes the state after General Reset with all analogue and digital supplies applied and also the case with V_{DD} applied but with all analogue supplies disconnected (i.e. in this later scenario, power from V_{DD} will not exceed the specified value whatever the state of the registers).
B. Assumes 30pF on each C-BUS interface line and an operating serial clock frequency of 5MHz.
C. The stated current drawn here is with the bandgap reference and accompanying bias current generators enabled only (register $11, b7), all other circuitry is disabled.
D. Not including any current drawn from the device pins by external circuitry:
Rx only – All Rx circuitry including SLI , synthesiser and bias generator.
Synth only – Synthesiser, NR Amplifier, VCO Buffer and bias generator.
E. As measured from the rising edge of CSN.
F. At T_{AMB} = 25ºC, not including any current drawn from the CMX991/CMX992 pins by external circuitry.
G. Tx only – Tx circuitry plus synthesiser, VCO, buffer and bias generator. IF output excludes the Tx Image Reject Mixer, but includes the IF Output buffer.
H. Rx IF and PLL – IF amplifier and I/Q mixers plus synthesiser, VCO, buffer and bias generator
J. Total current from $AV_{DD,}$ DV_{DD} and V_{DD}IO.

8.1.3.2 AC Parameters – Receiver Sections

Rx 1st Mixer	**Notes**	**Min.**	**Typ.**	**Max.**	**Units**
Gain	1, 7, 7b	–	18	–	dB(V/V)
Noise Figure	7, 6b	–	11.5	–	dB
Input Third Order Intercept Point (IIP3)					
450MHz	7, 7a	+9.5	+11	–	dBm
950MHz	7, 7a	+8	+9.5	–	dBm
Input Frequency Range	9	100	–	1000	MHz
LO Frequency Range	3	50	–	1150	MHz
Input Impedance, each pin	8	–	150 + 8	–	Ω + pF
IF Output Frequency Range		10	–	150	MHz
IF Output Impedance		–	500 ‖ 4pF	–	Ω
LO Leakage at Input ($f_{LO}/2$)	6				
150MHz Operation	6a	–	-99	–	dB
460MHz Operation	6b	–	-92	–	dB
950MHz Operation	6c	–	-84	–	dB
1dB Compression Point (input)	1	-10	-7	–	dBm
Half IF Rejection	2, 4	55	70	–	dB
Blocking	5, 6	–	90	–	dB
LO Input					
Frequency Range		100	–	2000	MHz
Input Level		-10	–	0	dBm
Division Ratios		–	1, 2 or 4	–	

Notes:
1. Measured from a low loss matched input source to a matched output load.
2. Significant variation in half IF rejection can occur as a function of frequency and LO level/matching. Users are recommended to optimise for a particular application.
3. LO as supplied to mixer circuit block.
4. Relative level of signal at mixer IF output relative to RF signal of –30dBm; IF = 45MHz and RF = 972.5MHz, LO = 1990MHz @ -10dBm.
5. Relative to –107dBm (level from ETSI EN 300 113), based on IF = 45MHz and RF = 450MHz, to give ~3dB rise in mixer output noise floor.
6. Including operation of selectable dividers, tested in divide by 2 mode.

6a f_{LO} = 390MHz at –5dBm, 45MHz IF, Circuit matched for 155MHz input (Table 15)
6b f_{LO} = 1010MHz at –5dBm, 45MHz IF, Circuit matched for 455MHz input (Table 4)
6c f_{LO} = 1810MHz at –5dBm, 45MHz IF, Circuit matched for 950MHz input (Table 15)

7. Gain, IP3 and noise figure can be adjusted using external resistors (R1 and R2 in Figure 6).

7a. Measured as a system from mixer input to I/Q output (pins RXIN, RXIP, RXQN, RXQP) and using the circuits of Figure 6 and Figure 7.

7b. Mixer gain is the defined as $20\log_{10}(V_{out} / V_{in}) + L_{match}$, where V_{in} = voltage at 50 ohm input to mixer stage ('Input' in Figure 6); V_{out} = voltage at mixer output (MIXOUT1 or MIXOUT2); L_{match} = loss of input matching components (e.g. T1 in Figure 6).

8. The RF mixer input is 300 Ω resistive differential with 8 pF in series with each mixer pin.
9. The mixer can be used below 100MHz with reduced performance. (See separate application note available from the CML website.)

IF Amplifier and I/Q Demodulator	Notes	Min.	Typ.	Max.	Units
Gain	10, 17	–	43	–	dB(V/V)
Noise Figure	10, 11	–	13	–	dB
Third Order Intercept Point (Input)	10, 17	–	-20	–	dBm
Input Frequency Range		10	–	150	MHz
LO Frequency Range	12	40	–	600	MHz
Input Impedance	15	–	1800	–	Ω
Output Impedance		–	20	–	Ω
LO Leakage at Input		–	–	-27	dBm
1dB Compression Point	13	–	-25	–	dBm
VGA Control Range	14	–	48	–	dB
VGA Step Size		4	6	8	dB
VGA Response Time	E	–	–	10	µs
Image Rejection (I/Q Gain/Phase matching)		30	40	–	dB
I/Q Output Bandwidth (-3dB)					
1MHz Mode	16	1	1.4	–	MHz
100kHz Mode		100	135	–	kHz

Notes:
10. Measured from an un-matched 50Ω input source to a differential I or Q output voltage; test frequency = 45MHz. Note that values include combined response of IF amplifier, I/Q demodulator and I/Q filter stages; see also section 7.7 for further details.
11. At maximum VGA setting (0dB); see section 7.7 for further details.
12. LO Supplied at four times the IF frequency.
13. At maximum gain, input terminated with 50Ω resistor.
14. Eight VGA steps.
15. Based on single ended input at 45MHz.
16. In 1MHz output mode an IF output in the range 450kHz to 465kHz is supported.
17. Gain reduces at higher IFs.

I/Q Filters	Notes	Min.	Typ.	Max.	Units
Gain	20	–	N/A	–	dB(V/V)
Noise Figure	20	–	N/A	–	dB
Third Order Intercept Point (Input)	20	–	N/A	–	dBm
Output Impedance	20	–	N/A	–	Ω
Output Anti-alias Filter Stop-band		1.92	–	–	MHz
Stop-band Attenuation		55	–	–	dB
Data Filter Bandwidth (-3dB)		–	100	–	kHz
Differential Output Voltage Swing	21	–	–	4	Vp-p

Notes:
20. Performance included in overall performance of I/Q Demodulator.
21. This is the maximum swing to guarantee meeting the third order distortion characteristics under the specified conditions and is not the maximum limiting value. For clarity, this means that the device has the capability to produce +/-1V on each of the differential outputs. The outputs are capable of driving a load resistance across the differential outputs of 1kΩ. This voltage output capability provides easy interfacing to other CML devices, like the CMX981, which has a maximum input signal amplitude of 2.4Vp-p.

Differential Amplifiers	Notes	Min.	Typ.	Max.	Units
Gain Bandwidth Product	30, 33	11	14	–	MHz
Input Offset Voltage		–	1	–	mV
Input Common Mode Range	32	1.0	1.6	2.5	V
Input Bias Current		–	0.4	–	µA
Input Resistance		–	160	–	kΩ
Slew Rate	30	–	6	–	V/µs
Differential Input Voltage	31	–	–	1.2	V
Input Referred Noise at 1kHz		–	15	–	nV/√Hz
Input Referred Noise at 450kHz		–	10	–	nV/√Hz
DC Output Range		AV_{ss}+0.1	–	AV_{DD}-0.1	V

Notes:
30. With a load of 1kΩ in parallel with 100pF referenced to a virtual earth not ground.
31. The inputs are protected with diodes. These diodes prevent the inadvertent application of voltages that may cause damage to the input transistors.
32. For small signal operation. It is recommended that for this application the input levels be restricted to +/-0.4V about a defined reference voltage of 1.6V (nominal); this will allow for some tolerance in components and for the precision of the setting the reference voltage.
33. Gain Bandwidth Product typically 40MHz with 15pF load.

Auxiliary Rx Functions	Notes	Min.	Typ.	Max.	Units
LNA Control					
Enable Voltage Level		80%	–	–	V_{DD}IO
Disable Voltage Level		0	–	0.4	V
SLI Output					
Output Voltage Range		$V_{ref.}$	–	–	V
Scaling		5	10	15	mV/dB
Operating Range	35	–	50	–	dB
Rise time	36	–	0.2	–	µs
Decay time	36, 37	–	1	–	µs

Notes:
35. See section 7.8.
36. Measured with a pulsed signal applied to IFIN and terminated with 50Ω.
37. Recovery from SLI saturated (high input signal) takes typically an additional 500ns.
38. V_{ref} is the reference voltage on pin VBIAS.

8.1.3.3 AC Parameters - Transmitter

I/Q Modulator	Notes	Min.	Typ.	Max.	Units
Input Signal Level	40	–	2.0	–	Vp-p
Gain Control Steps		–	+6, 0, -6	–	dB
Input Common Mode Range	41	V_{SS}+1.0	V_{DD}/2	V_{DD}-1.0	V
Input Voltage Range (on each input)		V_{SS}+0.5	–	V_{DD}-0.5	V
Third Order IMD Products		–	–	-50	dBc
IMD Products (greater than third order)		–	–	-60	dBc
Carrier Leakage		–	-30	–	dBc
Image Suppression		–	-40	-30	dBc
I or Q Modulation Bandwidth (-3dB)	42	–	–	1	MHz

Notes: 40. The 2.0Vp-p is a differential signal. For clarity, this means +/-0.5V on each input.
41. The common mode range is based on a 2.0Vp-p differential input signal level.
42. This is the maximum modulation frequency that should be applied in the I or Q channel. The bandwidth of the modulator is much higher than this but use of higher modulation frequencies may result in an increase in distortion products.

Post Modulator Filter	Notes	Min.	Typ.	Max.	Units
Selectable Filter Bandwidth		–	45, 60, 90, 120	–	MHz
Gain		–	-2	–	dB
Stopband (45MHz Mode)					
>135MHz		–	30	–	dB
Stopband (60MHz Mode)					
>170MHz		–	30	–	dB
Stopband (90MHz Mode)					
>270MHz		–	30	–	dB
Stopband (120MHz Mode)					
>360MHz		–	30	–	dB
Tx IF Output	45				
Frequency Range		45	–	120	MHz
Output Signal Level	46	–	-10	–	dBm
Wideband Noise at 1MHz		–	-142	–	dBc/Hz
Output Impedance		–	50	–	Ω

Notes: 45. At pin TXIFOUT.
46. For specified I/Q Modulator Input Signal Level.

Image-Reject Up-Converter	Notes	Min.	Typ.	Max.	Units
Output Frequency Range		100	–	1000	MHz
Output Impedance	50	–	200	–	Ω
Output Level	46, 51	–	-10	–	dBm
Wideband Noise at 1MHz		–	-141	–	dBc/Hz
Image Suppression		–	-36	–	dBc
LO Suppression (1GHz)	53	-25	-30	–	dBc
LO Suppression (460 MHz)		–	-35	–	dBc
APCO P25 Performance					
ACPR (12.5kHz) with C4FM	52	–	70	–	dB
ACPR (12.5kHz) with H-CPM	52	–	70	–	dB
LO Input					
Frequency Range		40	–	2000	MHz
Level		-10	-5	0	dBm
Division Ratios		–	2 or 4	–	

Notes:
50. Differential output TXOUTP and TXOUTN.
51. Output via 4:1 balun (See section 4.3.1) and matching to 50Ω.
52. TxIF of 45MHz or 90MHz; ACPR measured as TIA-102.CAAB-B section 3.2.8.1.
53. Tested with 1910MHz LO and 45MHz IF, 2Vp-p differential input signal on I and Q; level at 955MHz measured relative to wanted signal at 1GHz.

8.1.3.4 AC Parameters – IF LO Integer N PLL

	Notes	Min.	Typ.	Max.	Unit
Phase Locked Loop					
Supply Current (Enabled)		–	5	–	mA
Supply Current (Standby)	1	–	1	–	µA
Reference Input					
Frequency		5	–	30	MHz
Level	90	0.5	–	–	Vp-p
Divide Ratios (M divider)		2	–	8191	
IF Synthesiser					
Comparison Frequency		–	–	500	kHz
Input Frequency Range		40	–	600	MHz
Input Level		-10	-4	–	dBm
Divide Ratios (N divider)	95	80	–	32767	
Charge Pump Current		–	±2.5	–	mA
1Hz Normalised SSB Phase Noise Floor	94	–	-198	–	dBc/Hz
VCO Negative Resistance Amplifier					
Supply Current (Enabled)		–	2	–	mA
Supply Current (Standby)	1	–	1	–	µA
Input Frequency Range	93	40	–	400	MHz
Phase Noise at 10kHz Offset	91	–	-110	–	dBc/Hz
Phase Noise at 100kHz Offset	91	–	-125	–	dBc/Hz
VCO Output Buffer					
Supply Current (Enabled)		–	4	–	mA
Supply Current (Standby)	1	–	1	–	µA
Frequency Range		40	–	600	MHz
IF LO Input	92				
Frequency Range		40	–	600	MHz
Level		-10	-5	0	dBm
Division Ratios		–	2 or 4	–	

Notes:
90. Sinewave or clipped sinewave.
91. With external components forming an 180MHz VCO, as shown in Figure 13/Table 11 and measured after the on-chip divide by 2.
92. Input to VCOP and/or VCON pins, VCO Negative Resistance amplifier disabled, see section 6.2.1).
93. Operation will depend on the choice and layout of external resonant components. Above 400MHz reliability of operation under all conditions cannot be guaranteed and it is recommended that an external VCO be used.
94. 1Hz Normalised Phase Noise Floor (PN1Hz) can be used to calculate the phase noise within the PLL loop bandwidth by: Measured Phase Noise (in 1Hz) = PN1Hz + $20\log_{10}(N)$ + $10\log_{10}(f_{comparison})$; $f_{comparison} = f_{ref} \times (1 / M)$, see also section 5.4.1.
95. When using an external VCO see the note at the end of section 4.5.

8.1.3.5 AC Parameters – C-BUS

C-BUS Timings (See *Figure 35*)		Notes	Min.	Typ.	Max.	Units
t_{CSE}	CSN-enable to clock-high time		100	–	–	ns
t_{CSH}	Last clock-high to CSN-high time		100	–	–	ns
t_{LOZ}	Clock-low to reply output enable time		0.0	–	–	ns
t_{HIZ}	CSN-high to reply output 3-state time		–	–	1.0	µs
t_{CSOFF}	CSN-high time between transactions		1.0	–	–	µs
t_{NXT}	Inter-byte time		200	–	–	ns
t_{CK}	Clock-cycle time		200	–	–	ns
t_{CH}	Serial clock-high time		100	–	–	ns
t_{CL}	Serial clock-low time		100	–	–	ns
t_{CDS}	Command data set-up time		75.0	–	–	ns
t_{CDH}	Command data hold time		25.0	–	–	ns
t_{RDS}	Reply data set-up time		50.0	–	–	ns
t_{RDH}	Reply data hold time		0.0	–	–	ns

Maximum 30pF load on each C-BUS interface line.

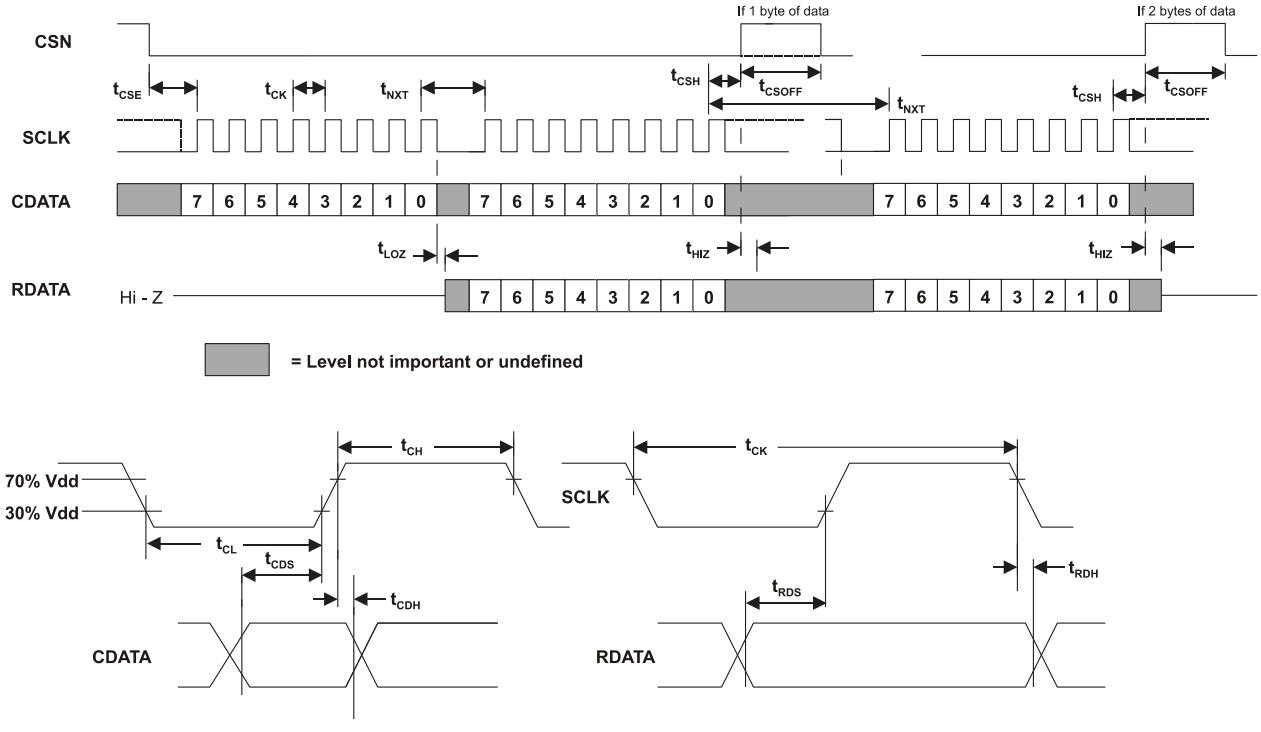
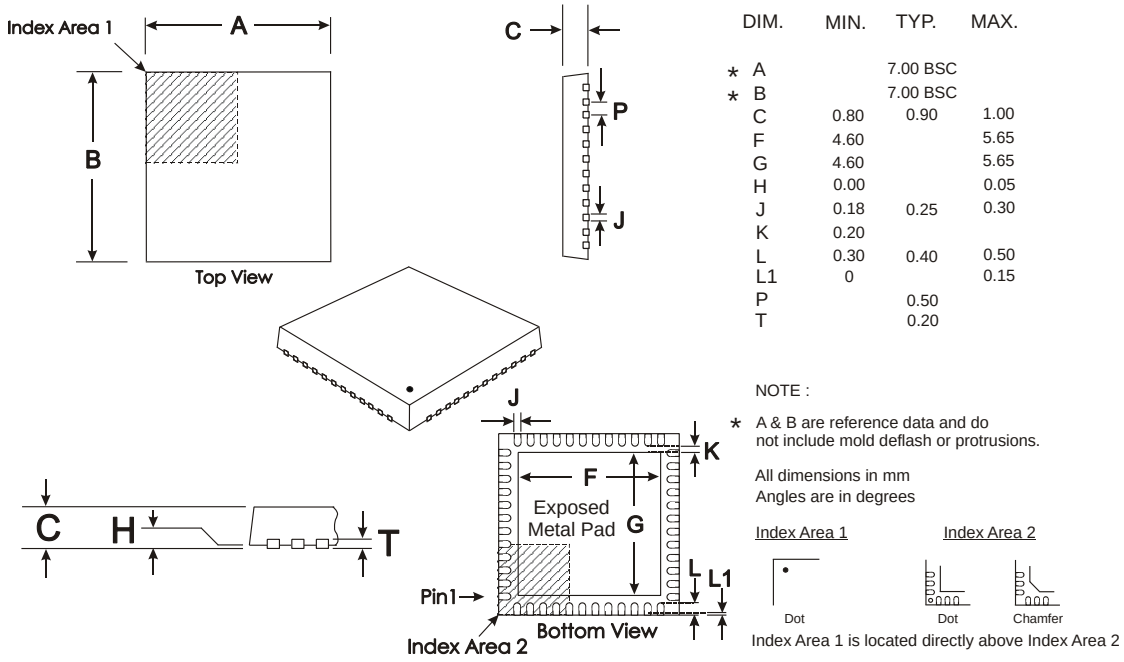


Figure 35 C-BUS Timing

8.2 Packaging



DIM.	MIN.	TYP.	MAX.
* A		7.00 BSC	
* B		7.00 BSC	
C	0.80	0.90	1.00
F	4.60		5.65
G	4.60		5.65
H	0.00		0.05
J	0.18	0.25	0.30
K	0.20		
L	0.30	0.40	0.50
L1	0		0.15
P		0.50	
T		0.20	

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Notes:

1. In this device, the underside of the Q3 package should be electrically connected to the analogue ground. The circuit board should be designed so that no unwanted short circuits can occur.
2. As package dimensions may change after publication of this datasheet, it is recommended that you check for the latest Packaging Information from the Datasheets page of the CML website: [www.cmlmicro.com].

Figure 36 Q3 Mechanical Outline:

Order as part no. CMX991Q3 or CMX992Q3

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