■ Features

- Fixed 1/4 duty mode, Up to 384 dots
- Low power consumption design, 6uA current at typical condition
- Built-in OSC Circuit
- Internal LCD Contrast control Circuit
- Integrated Power-on Reset Circuit
- No external component required
- Interface: 2 wire serial interface
- Compatable with TTL/CMOS
- High EMC immunity

■ Applications

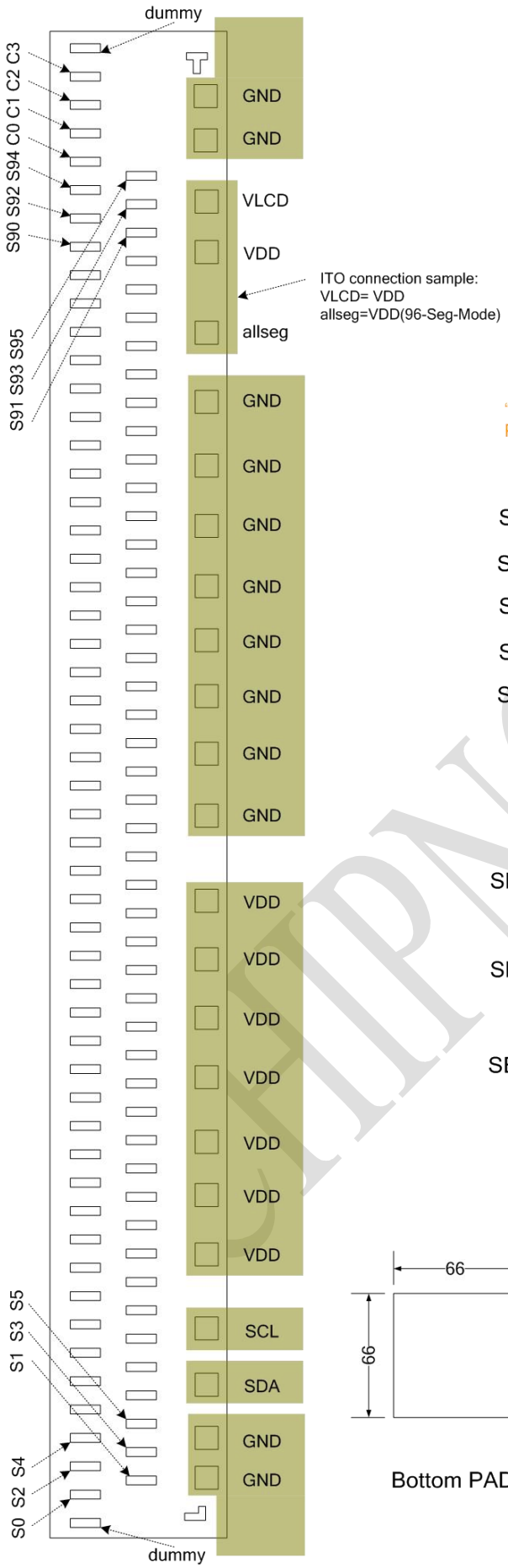
- Home electrical appliance
- Meter equipment etc.
- Toys
- PDA
- Clocks

■ Order Information

Part No.	Package Type	Tray
CN91C4S96	COG	154/Tray

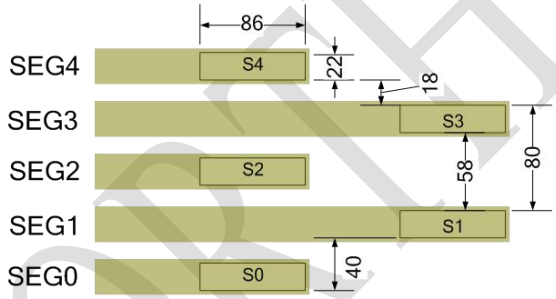
■ PAD Description

Name	I/O	Function
SDA	I/O	2-line serial data input and output. Open-Drain, and a pull-up resistor on board is needed.
SCL	I	2-line serial clock input CMOS input, do not need a pull-up resistor.
VSS	I	GND
VDD	I	Power
VLCD	I	Set LCD bias voltage. It can be directly tied to VDD, and then you can adjust the internal LCD bias voltage by setting the registor EV[3:0].
allseg	I	Seg-Mode selection 1: 96-Seg-Mode; Normal mode. 0: 48-Seg-Mode; Only outward 48 segs can be used, but ITO pitch can be double. This mode is very usefull to reduce the difficulty ot the COG process.
S0~S95	O	SEGMENT driver output for LCD
C0~C3	O	COMMON driver output for LCD

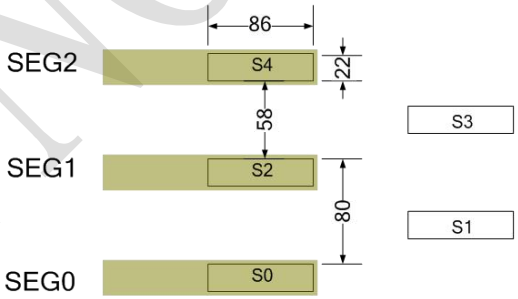


Die Thickness: 300um
Die Size: 4380 X 580 um2
Bump Hight: 9um ± 2um
SEG Bump Width: 22um
SEG Bump Space: 18um (96-Seg-Mode)
58um (48-Seg-Mode)
SEG Bump Pitch: 40um (96-Seg-Mode)
80um (48-Seg-Mode)

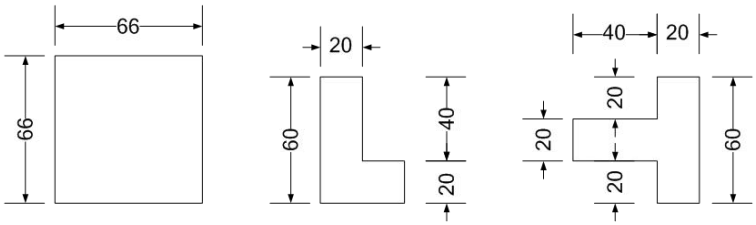
"allseg" PAD is very important, it defines the SEG ITO pitch.
Please refer to the SEG ITO samples as follows:



(allseg=VDD, 96-Seg-Mode)

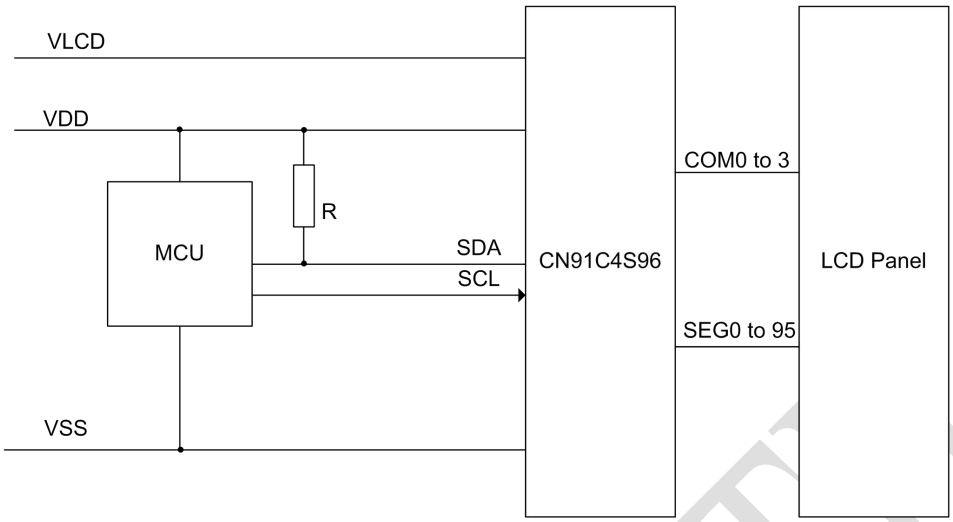


(allseg=GND, 48-Seg-Mode)

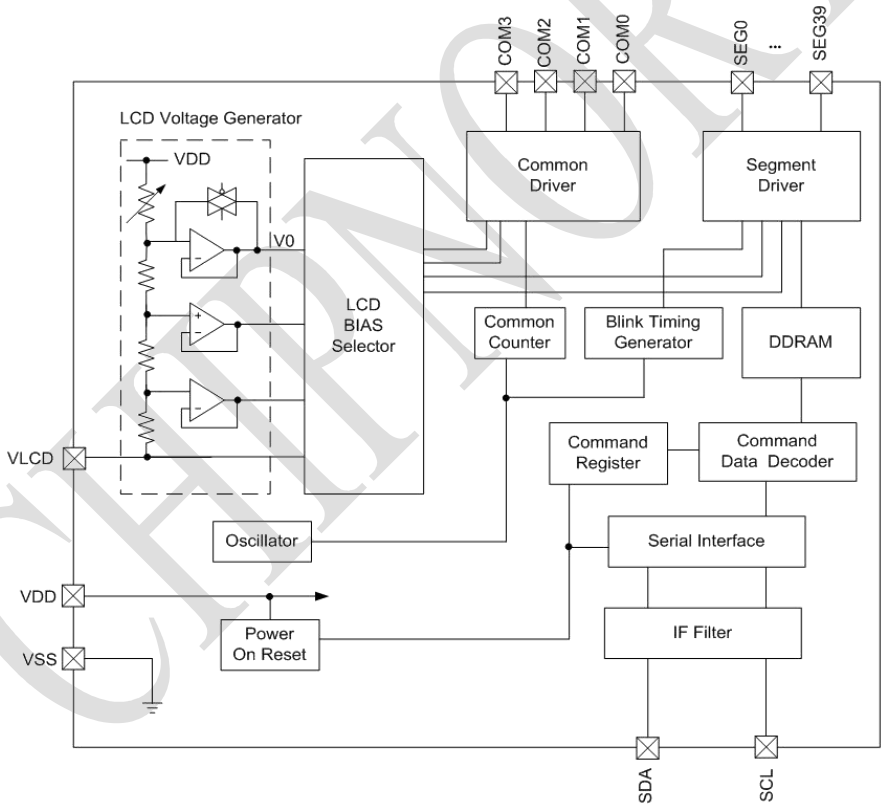


Bottom PAD Left Mark Right Mark

■ Typical Application Circuit



■ Block Diagram



■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Remarks
Power Supply Voltage1	V_{DD}	-0.5 to + 6	V	Power supply
Power Supply Voltage1	V_{LCD}	-0.5 to + 6	V	LCD drive voltage
Input voltage range	V_{IN}	-0.5 to VDD + 0.5	V	
Operational temperature range	Topr	-40 to + 85	°C	
Storage temperature range	Tstg	-55 to + 125	°C	

■ Electrical Characteristics

Test conditions: VDD=3.3V, TA = 25 °C unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
VDD Power Range	VDD	2.7	-	5.5		
VLCD Power Range	VLCD	2.7	-	5.5	V	LCD drive voltage
"H" Level Input Voltage	VIH	0.8* VDD	-	VDD	V	
"L" Level Input Voltage	VIL	VSS	-	0.2*VDD	V	
SDA "L" Level Output Voltage	VOL_sda	0	-	0.4	V	Iload=-3mA Without the consideration of ITO resistance on COG pannel.
COM/SEG ON Resistance	RON	-	3	-	kΩ	Iload=±10uA
Frame Frequency	Fclk	-	80	-	Hz	FR=80Hz setting
Standby Current	IDD1	-	-	1	uA	Display off, Oscillation off
Operating Current	IDD2	-	6	20	uA	VDD=3.3V, Ta=25, SR=Power save mode 1, FR=Power save mode1, Frame inversion, FR=80Hz, with an LCD panel load.

■ Command Registers Description

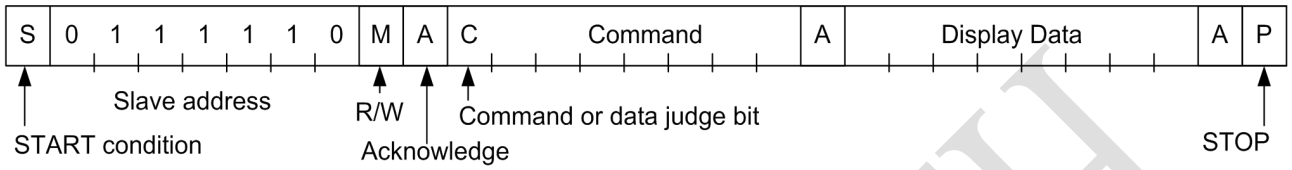
	7	6	5	4	3	2	1	0
ADSET	**C**	**0**	**0**	P[4:0]				
DISCTL	**C**	**0**	**1**	FR[1:0]		LF	SR[1:0]	
MODSET	**C**	**1**	**0**	ULP	EN	/	/	/
EVRSET	**C**	**1**	**1**	**0**	**0**	EV[2:0]		
ICSET	**C**	**1**	**1**	**0**	**1**	P[5]	RST	P[6]
BLKCTL	**C**	**1**	**1**	**1**	**0**	BF[2:0]		
APCTL	**C**	**1**	**1**	**1**	**1**	EV[3]	AON	AOF

Name	Default	Description
P[6:0]	000000	DDRAM Address. In the write mode, the range of address P [6:0] can be set as 0~5F(Hex). In the read mode, the range of address P [6:0] can be set as 0~62(Hex). Don't specify another address; otherwise address will be set to "000000". Note: The bit P[5] is in the command 'ICSET'.
FR[1:0]	00	Set Frame Frequency for Power Saving. 00, 80Hz, Normal Mode 01, 130Hz Power Save Mode1 10, 64Hz, Power Save Mode2 11, 200Hz, Power Save Mode3
LF	0	Set Line or Frame inverse mode. 0, Line inverse 1, Frame inverse
SR[1:0]	10	Set internal bias current for Power Saving. 00, *0.5, Power Save Mode 1 01, *0.67, Power Save Mode 2 10, *1.0, Normal Mode, default value. 11, *1.8, High Power Mode
ULP	0	Set '1' to enable the Ultra-Low-Power mode, which can decrease total power consumption further more along with 'SR' and 'FR' Power Save Mode.
EN	0	0: disable all blocks on-chip, all com/seg pin will be pulled to GND. 1: enable
EV[3:0]	00000	Adjust resistor divider for LCD contrast setting. 0000, 1.000 * VLCD 0001, 0.975 * VLCD 0010, 0.950 * VLCD 0011, 0.925 * VLCD 0100, 0.900 * VLCD 0101, 0.875 * VLCD 0110, 0.850 * VLCD 0111, 0.825 * VLCD 1000, 0.800 * VLCD 1001, 0.775 * VLCD 1010, 0.750 * VLCD 1011, 0.725 * VLCD 1100, 0.700 * VLCD 1101, 0.675 * VLCD 1110, 0.650 * VLCD 1111, 0.625 * VLCD Note: The bit EV[4] is in the command 'APCTL'.
RST	0	Set '1' to reset all the registers in this table, but it won't reset the display data in the DDRAM.
BF[2:0]	000	Config the blink frequency: 000, No blink. 001, 0.3Hz 010, 0.25Hz 011, 2Hz 100~111, 1Hz
AON: AOFF	00	Config the pixel display 00, All pixels are ON/OFF depending on the data in the display DDRAM. 01, All pixels are OFF regardless of DDRAM data. 10, All pixels are ON regardless of DDRAM data. 11, All pixels are OFF regardless of DDRAM data, the same as '01'.

■ Function Description

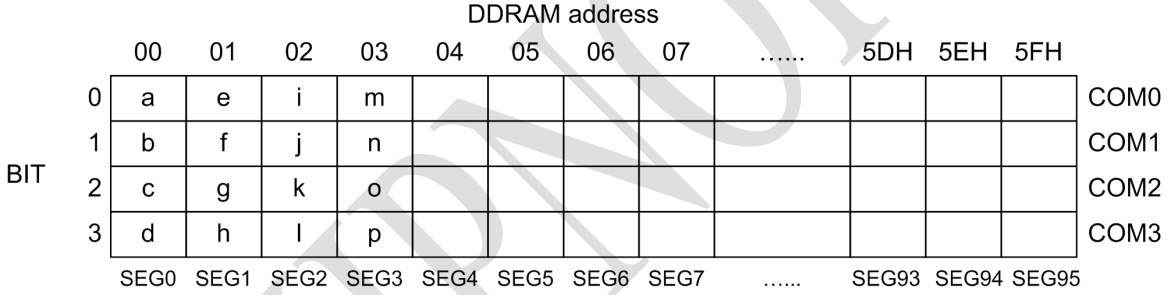
● Command and Data Transfer Method

1. Generate “START condition”.
2. Issue Slave address 7C.
3. Transfer command.
4. Transfer display data.
5. Generate “STOP condition”

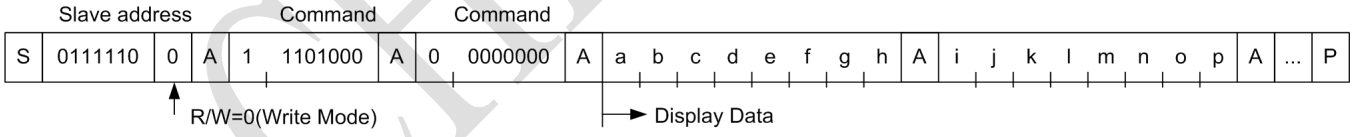


● Write Display Data and Transfer Method

Set R/W bit to ‘0’ to come into write mode.
This device has Display Data RAM (DDRAM) of 96×4=384 bit.

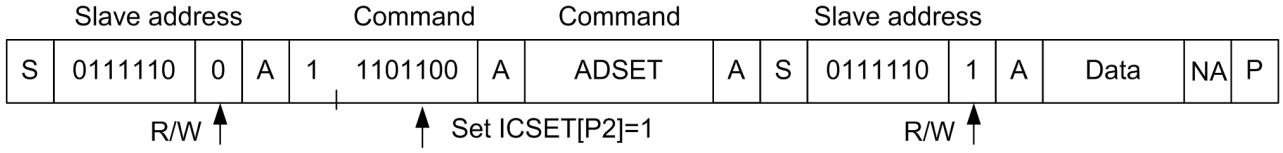


8-bit data will be stored in DDRAM. The address to be written is the address specified by Address set command, and the address is automatically incremented in every 4bit data. Data can be continuously written in DDRAM by transmitting Data continuously.



● Read Command Register and Transfer Method

The command registers can be read during read mode. The sequence for the command registers reading is shown below and is similar to the display data reading sequence.

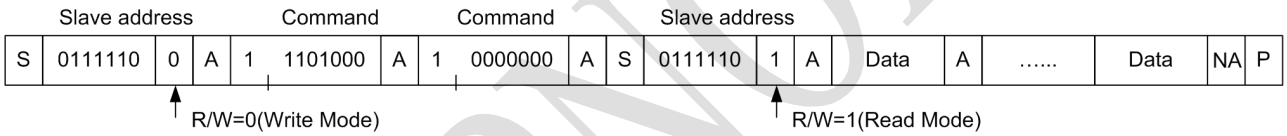


The command register addresses are described below. The following register settings can be read in this mode.

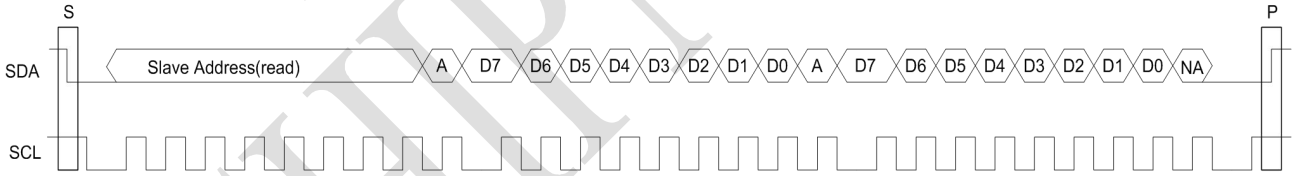
Register	D7	D6	D5	D4	D3	D2	D1	D0	Address
REG1	/	/	/	/	RST	BF[2:0]			60H
REG2	FR[1:0]		SR[1:0]		LF	EN	AON	AOF	61H
REG3	/	/	/	ULP	EV[3:0]				62H

● Read Display Data and Transfer Method

The read mode sequence is shown below



An example of the display data read sequence is shown below.



■ ORDER INFORMATION:

date	Version	Revision notes	Reviser
2020.3.9	V1.0	Initial data compilation	ZhangSongfeng