STANDARD MICROSYSTEMS CORPORATION

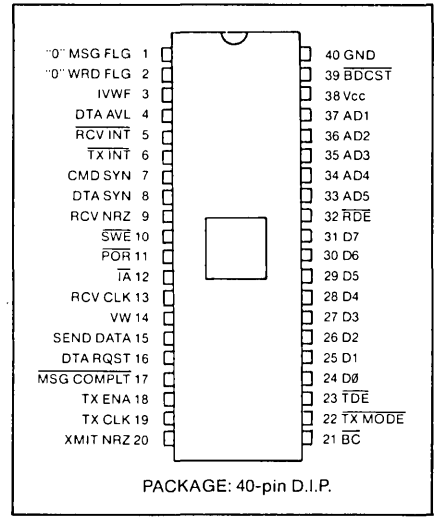
COM 1553A
μPC FAMILY

MIL-STD-1553A "SMART®"

FEATURES

- ☐ Support of MIL-STD-1553A
- ☐ Operates as a: Remote Terminal Responding
  Bus Controller Initiating
- ☐ Performs Parallel to Serial Conversion when Transmitting
- ☐ Performs Serial to Parallel Conversion when Receiving
- ☐ Compatible with HD-15531 Manchester Encoder/Decoder
- ☐ All Inputs and Outputs are TTL Compatible
- ☐ Single +5 Volt Supply
- ☐ COPLAMOS® N Channel MOS Technology
- ☐ Available in PC Board Form from Grumman Aerospace Corporation

PIN CONFIGURATION



PACKAGE: 40-pin D.I.P.

GENERAL DESCRIPTION

The COM 1553A SMART® (Synchronous Mode Avionics Receiver/Transmitter) is a special purpose COPLAMOS N-Channel MOS/LSI device designed to provide the interface between a parallel 8-bit bus and a MIL-STD-1553A serial bit stream.

The COM 1553A is a double buffered serial/parallel and parallel/serial converter providing all of the "hand shaking" required between a Manchester decoder/encoder and a microprocessor as well as the protocol handling for both a MIL-STD-1553 bus controller and remote terminal.

The COM 1553A performs the following functions in response to a 16 bit Command Word. It provides address detection for the first five bits of the serial data input. If all 1's appear in the address field, a broadcast signal is generated. The sixth bit is decoded as mode: transmit or receive. The next five bits are decoded for zero message flag and special flags in the subaddress/mode field. The last five bits (word-count field) are decoded determining the number of words to be received or transmitted.

When receiving data sync the COM 1553A performs a serial to parallel conversion, buffers the 16 bit message word, and formats it into two parallel (8 bit) bytes for presentation to the I/O bus under processor or hard wired logic control.

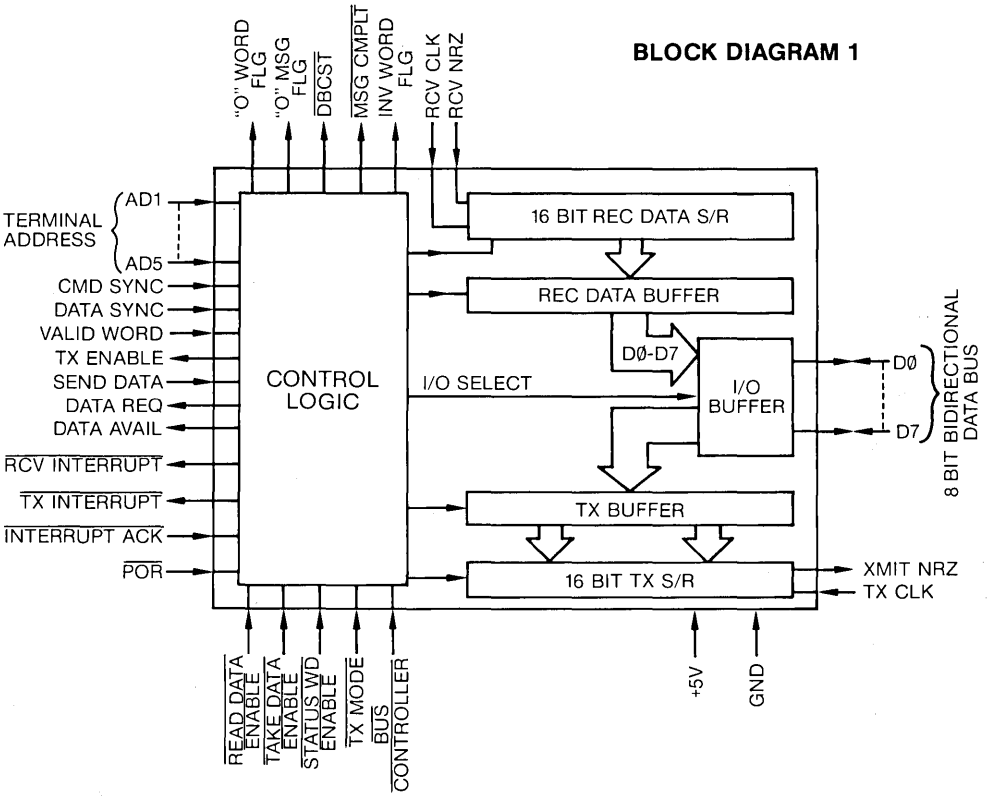
In the transmit mode the COM 1553A takes two parallel 8 bit data words from the I/O bus and serially transmits the resultant 16 bit word to the Manchester encoder. This is done under the control of Send Data. To facilitate data transfer the COM 1553A provides all necessary buffering and storage for transmitted and received data. It also provides all necessary hand shaking, control flags and interrupts to a processor or hard wired logic terminal. See block diagram 1.

The COM 1553A can be set up as either a remote terminal or a bus controller interface.

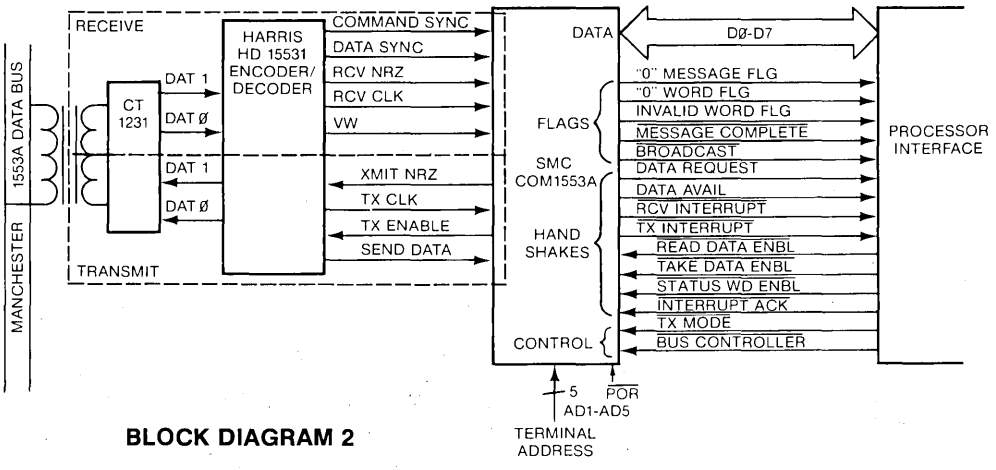
The COM 1553A is compatible with Harris' HD-15531 CMOS Manchester Encoder-Decoder chip and interfaces directly with it. A 3 device kit consisting of: SMC's COM 1553A, Harris' HD-15531 and Circuit Technology's CT1231 forms a complete system interface for the message structure of MIL-STD-1553A. See block diagram 2.

Note: All terminology utilized in this data sheet is consistent with MIL-STD-1553.

BLOCK DIAGRAM 1



BLOCK DIAGRAM 2



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1	"Ø" MESSAGE FLAG	ØMF	The ZERO MESSAGE FLAG output is set when the 7th through 11th bits of the NRZ serial input data in a command envelope (see figure 1) are zero. ØMF is an open drain output.
2	"Ø" WORD FLAG	ØWF	The ZERO WORD FLAG output is set when the 12th through 16th bits of the NRZ serial input data in a command envelope (see figure 1) are zero. ØWF is an open drain output.
3	INVALID WORD FLAG	IVWF	The INVALID WORD FLAG output is set when the word just received has an invalid parity bit or invalid format. IVWF is an open drain output.
4	DATA AVAILABLE	DTA AVL	DATA AVAILABLE is set when a word received is ready to be read. When the COM 1553A is the bus controller, DTA AVL occurs on command, status or data words. When the COM 1553A is a remote terminal, DTA AVL is set only on data words. DTA AVL is an open drain output.
5	$\overline{\text{RECEIVE INTERRUPT}}$	$\overline{\text{RCV INT}}$	$\overline{\text{RECEIVE INTERRUPT}}$ is set to zero when the 6th bit following a command sync is a zero and the first 5 bits match AD1-AD5. $\overline{\text{RCV INT}}$ is reset to one by $\overline{\text{IA}}$ or $\overline{\text{POR}}$, or if the line is not active for 32 receive clocks.
6	$\overline{\text{TRANSMIT INTERRUPT}}$	$\overline{\text{TX INT}}$	$\overline{\text{TRANSMIT INTERRUPT}}$ is set to zero when the 6th bit following a command sync is a one, and the first 5 bits match AD1-AD5. $\overline{\text{TXINT}}$ is reset to one by $\overline{\text{IA}}$ or $\overline{\text{POR}}$.
7	COMMAND SYNC	CMD SYN	COMMAND SYNC is an input from the Manchester decoder and must be high for 16 receive clocks enveloping the receive NRZ data of a command word.
8	DATA SYNC	DTA SYN	DATA SYNC is an input from the Manchester decoder and must be high for 16 receive clocks enveloping the receive NRZ data of a data word.
9	RECEIVER NRZ	RCV NRZ	Receiver serial input from Manchester decoder. Data must be stable during the rising edge of the receive clock.
10	$\overline{\text{STATUS WORD ENABLE}}$	$\overline{\text{SWE}}$	$\overline{\text{SWE}}$ is the output enable for the following open drain outputs: ØMF ØWF IVWF DTA AVL $\overline{\text{DTA RQ}}$ $\overline{\text{MSG CPLT}}$
11	$\overline{\text{POWER ON RESET}}$	$\overline{\text{POR}}$	$\overline{\text{POWER ON RESET}}$. Active low for reset.
12	$\overline{\text{INTERRUPT ACKNOWLEDGE}}$	$\overline{\text{IA}}$	$\overline{\text{IA}}$ resets $\overline{\text{TX INT}}$, $\overline{\text{REC INT}}$, ØMF, ØWF and $\overline{\text{BRD CST}}$. $\overline{\text{IA}}$ may occur between the trailing edges of receive clocks 6 and 10, or between the leading edge of receive clock 12 and the falling edge of receive clock 15, or after the falling edge of clock 17.
13	RECEIVE CLOCK	RCV CLK	The RECEIVE CLOCK is synchronous with the Receiver NRZ input during the command sync or data sync envelopes.
14	VALID WORD	VW	This input is driven by the VALID WORD output of the Manchester Decoder. VW should occur immediately after the rise of the first RCV CLK following the fall DATA SYNC or COMMAND SYNC.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
15	SEND DATA	SD	SEND DATA is a "handshake" signal received from the Manchester encoder indicating that the encoder is ready for the COM 1553A to transmit data. SD will bracket 16 transmit data clocks. The contents of the transmitter buffer will be transferred into the transmit register when SD is low.
16	DATA REQUEST	DTA RQST	DATA REQUEST is an open drain output which is set high when the transmitter holding register is ready to accept more data.
17	$\overline{\text{MESSAGE COMPLETE}}$	$\overline{\text{MSG CMPLT}}$	In the receive mode the $\overline{\text{MESSAGE COMPLETE}}$ output is set low when the appropriate number of data words have been received. In the transmit mode, $\overline{\text{MSG CMPLT}}$ indicates that the appropriate number of command, status or data words have been transmitted. When the COM 1553A is a bus controller, $\overline{\text{MSG CMPLT}}$ will be asserted low when 33 command status or data words have been transmitted. $\overline{\text{MSG CMPLT}}$ is an open drain output.
18	TRANSMIT ENABLE	TXENA	A TRANSMIT ENABLE signal will be sent to the Manchester Encoder to initiate transmission of a word. TXENA is generated under the following conditions: 1) COM 1553A is a bus controller: A $\overline{\text{TXMODE}}$ pulse will set TXENA. A second $\overline{\text{TXMODE}}$ pulse will reset TXENA. 2) COM 1553A is a remote terminal. A Transmit Command from the Controller will cause a $\overline{\text{TRANSMIT INTERRUPT}}$ (see pin 6). When this is acknowledged by a TXMODE pulse from the system, TXENA will be set. TXENA will then be reset by either A) Send Data Command associated with the last data word. B) a second TXMODE pulse. 3) COM 1553A is a remote terminal. The falling edge of a DATA SYNC associated with the last data word of a message while in the receive mode. TXENA will be reset during the next SEND DATA envelope.
19	TRANSMIT CLOCK	TXCLK	Transmitter shift clock.
20	TRANSMIT NRZ	XMIT NRZ	Serial data output to the Manchester Encoder.
21	$\overline{\text{BUS CONTROLLER}}$	$\overline{\text{BC}}$	$\overline{\text{BC}}$ determines whether the COM 1553A is acting as bus controller ($\overline{\text{BC}} = 0$) or as a remote terminal ($\overline{\text{BC}} = 1$).
22	$\overline{\text{TRANSMIT MODE}}$	$\overline{\text{TXMODE}}$	$\overline{\text{TXMODE}}$ is a system input controlling transmission. See TXENA (pin 18).
23	$\overline{\text{TAKE DATA ENABLE}}$	$\overline{\text{TDE}}$	$\overline{\text{TDE}}$ is an input from the system initiating transmission. Two $\overline{\text{TDE}}$ pulses are required for each 16 bit data word, one for each 8 data bits placed on DØ-D7.
24-31	DATA BUS	DØ-D7	Bidirectional 8 bit Data Bus to the system. DØ is the LSB. DØ-D7 present open drain outputs.
32	$\overline{\text{READ DATA ENABLE}}$	$\overline{\text{RDE}}$	$\overline{\text{RDE}}$ is an input from the system instructing the COM 1553A to place the received data onto DØ-D7. Two $\overline{\text{RDE}}$ pulses are required per 16 bit data word, one for each 8 bits.
33-37	ADDRESS	AD5-AD1	AD1-AD5 provide addressing to the COM 1553A. Each input has a pull-up resister allowing simple switching to ground to select the user address.
38	POWER SUPPLY	VCC	+5 Volt supply.
39	$\overline{\text{BROADCAST}}$	$\overline{\text{BDCST}}$	$\overline{\text{BDCST}}$ is set low when a "broadcast" command word (the address bits all set to "one") is being received. $\overline{\text{BDCST}}$ is reset by $\overline{\text{IA}}$.
40	GROUND	GND	Ground

OPERATION...RECEIVE MODE

The COM 1553A is considered in the receive mode when TXENA = 0. The most significant bit of both command and data words is received first.

Message reception is initiated when CMD SYN goes high. The next 16 receive clocks are used to shift serial data into RCV NRZ.

The first 5 bits of a command word designate a remote terminal address. These 5 bits are compared with AD1-5. Should the address bits compare, the sixth bit is examined. If it is a zero, a $\overline{\text{RECEIVE INTERRUPT}}$ is generated. If it is a one, a $\overline{\text{TRANSMIT INTERRUPT}}$ is generated.

Bit fields 7-11 and 12-16 are examined for all zeros. All zeros in bit field 7-11 denotes a "ZERO MESSAGE" and all zeros in bit field 12-16 denotes a "ZERO WORD."

Receipt of a data word is indicated when DTA SYN goes high.

When DTA SYN or CMD SYN goes low, the contents of the 16 bit receive register are loaded into the receive buffer. The buffer is organized into two groups of 8 bits each. The most significant 8 bits (byte 1) will be enabled onto the 8 bit data bus on receipt of the first $\overline{\text{RDE}}$ pulse ($\overline{\text{RDE1}}$). The second byte will be enabled on receipt of the second $\overline{\text{RDE}}$ pulse ($\overline{\text{RDE2}}$).

A DATA AVAILABLE is generated for data words only. However, data will be available on DØ-D7 for both command and data words.

If 32 clocks are received after the rising edge of CMD SYN or DTA SYN an "Idle Line Reset" condition exists. This implies that a new CMD SYN or DTA SYN has not yet been received within 16 clocks of the fall of the previous sync signal. The "Idle Line Reset" will reset the following signals:

$\overline{\text{REC INT}}$	"0" MSG FLG
$\overline{\text{TX INT}}$	"0" WRD FLG
$\overline{\text{BRD CST}}$	

When the commanded number of data words have been received, a $\overline{\text{MESSAGE COMPLETE}}$ signal is generated.

As the transmitter and receiver registers operate independently, the COM 1553A will receive its own transmission. The following signals are inhibited during transmission:

$\overline{\text{BC}} = 0$	$\overline{\text{BC}} = 1$
$\overline{\text{REC INT}}$	DAT AVL
$\overline{\text{XMT INT}}$	IVWF
$\overline{\text{BRD CST}}$	$\overline{\text{REC INT}}$
ØWF	$\overline{\text{XMT INT}}$
ØMF	ØMG
JAM MESSAGE ERROR*	ØWF
	$\overline{\text{BRD CST}}$
	JAM MESSAGE ERROR*

*JAM MESSAGE ERROR is an internal signal. See OPERATION...TRANSMIT MODE.

OPERATION...TRANSMIT MODE

The COM 1553A is considered in the transmit mode when TXENA = 1. This is caused by a $\overline{\text{TXMODE}}$ pulse (see description of pin functions, pin 18). The $\overline{\text{TXMODE}}$ pulse in turn is a system response to a transmit command from the receiver.

When the Manchester Encoder receives TXENA = 1, it will respond with SEND DATA = 1. The COM 1553A will then send the system a DATA REQUEST.

Data is loaded into the transmitter data buffer from the 8 bit data bus by pulsing $\overline{\text{TDE}}$. The 8 most significant bits are loaded in by the first $\overline{\text{TDE}}$ pulse ($\overline{\text{TDE1}}$), the 8 least significant bits by the second $\overline{\text{TDE}}$ pulse ($\overline{\text{TDE2}}$).

When SEND DATA (pin 15) is low, the transmitter shift register inputs will follow either the transmit buffer output, JAM ADDRESS or JAM MESSAGE ERROR signals. When SEND DATA is high, the shift register parallel inputs are disabled and the shift register contents are shifted out in NRZ form using the 16 negative edges in the send data envelope.

To facilitate transmission of the status word from a remote terminal, the COM 1553A will "jam" the first (most significant) 6 bits of the status word into the transmit register when $\overline{\text{BC}}$ is high. These bits will automatically be sent at the first SEND DATA pulse. In general for MIL-STD-1553A the remaining 10 bits will normally be all zeros and will automatically be sent out as such. If it is desired to send additional status information (for MIL-STD-1553B), a $\overline{\text{TDE1}}$ pulse will load the least significant 2 bits of the first 8 bit byte, and a $\overline{\text{TDE2}}$ will load all 8 bits of the second byte. Note that these TDE pulses must be sent (and data presented) before the first SD = 1 response from the Manchester Encoder.

A JAM ADDRESS occurs when 1) a transmit command is addressed to the COM 1553A 2) A $\overline{\text{TXMODE}}$ pulse is received and 3) a valid word signal is received. Upon a JAM ADDRESS the COM 1553A will load its address into the first 5 bits of the transmit register.

Alternatively, a JAM ADDRESS will also occur at the fall of the last data sync after valid receive command has been detected.

The JAM ADDRESS function will be inhibited if a "0" word and "0" message condition exists in the command word. The JAM ADDRESS will be reset by the leading edge of SEND DATA.

The JAM MESSAGE ERROR function occurs when, in the receive mode, a data word is not followed by a VALID WORD signal. JAM MESSAGE ERROR consists of loading a one in the sixth bit location of the transmit shift register (the message error location).

JAM MESSAGE ERROR is inhibited when the transmit command word contains "0" Message and "0" Word fields.

When the commanded number of data words has been transmitted a $\overline{\text{MESSAGE COMPLETE}}$ signal will be generated.

GENERAL OPERATION NOTES

1. BUS CONTROLLER. When $\overline{BC} = 0$, signifying that the COM 1553A is the bus controller the following is true:
   A. DTA AVL is generated on the rising edge of the 17th receive clock following a Command Sync or Data Sync. This allows the bus controller to receive command, status or data words regardless of their address.
   B. TXENA is contingent only on $\overline{TXMODE}$. A bus controller can therefore transmit whenever it desires.
   C. The jam functions are inhibited.

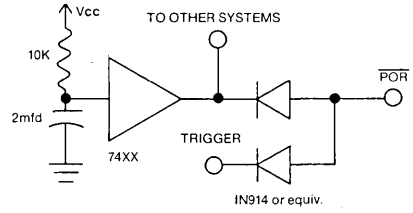
2. INVALID WORD FLAG. When $\overline{BC} = 0$, IVWF will be set if the Valid Word input (from the Manchester decorder) does not go high following receipt of all words. This includes words received from the same device's transmitter. (This provides a validity test of the controller transmission).
   When $\overline{BC} = 1$, IVWF will be set if Valid Word does not go high following receipt of all command and address words addressed to the terminal.
   IVWF will be set for the following conditions:

Message type	*Word*	*Terminal is*	*IVWF generated*
Transit Group	Transmit command	receiving	yes
	Status word	transmitting	no
	Data word	transmitting	no
Receive Group	Receive command	receiving	yes
	Data word	receiving	yes
	Status word	transmitting	no
Receive/Transmit Group (this terminal addressed to receive)	Receive command	receiving	yes
	Transmit command	receiving	no
	Status word	receiving	no
	Data word	receiving	yes
	Status word	transmitting	no
Receive/Transmit group (this terminal addressed to transmit)	Receive command	receiving	no
	Transmit command	receiving	yes
	Status word	transmitting	no
	Data word	transmitting	no
	Status word	receiving	no

3. POWER ON RESET. During power-up, $\overline{POR}$ is a low to high exponential with a minimum low time, after the supply is within specified limits, of 10 microseconds. $\overline{POR}$ may also occur asynchronously anytime after power has stabilized.
   $\overline{POR}$ initializes the following outputs:

ØMG	$\overline{REC\ INT}$	$\overline{TDE}$
ØWF	$\overline{MSG\ CMPLT}$	DTA AVL
$\overline{BRD\ CST}$	IVW	TXENA
$\overline{XMT\ INT}$	$\overline{RDE}$	DTA RQ

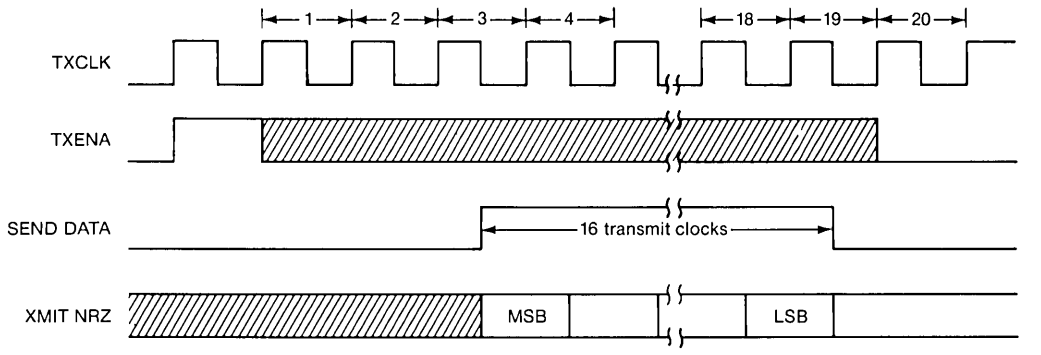
   The following circuit may be used to implement $\overline{POR}$.



4. WORD COUNT: Word count is decoded as follows:

D1	*D2*	*D3*	*D4*	*D5*	*Word Count*
0	0	0	0	1	1
0	0	0	1	0	2
1	1	1	1	1	31
0	0	0	0	0	32

TRANSMIT TIMING FIGURE 1



MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... -55°C to +125°C
Storage Temperature Range ..... -55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... -0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

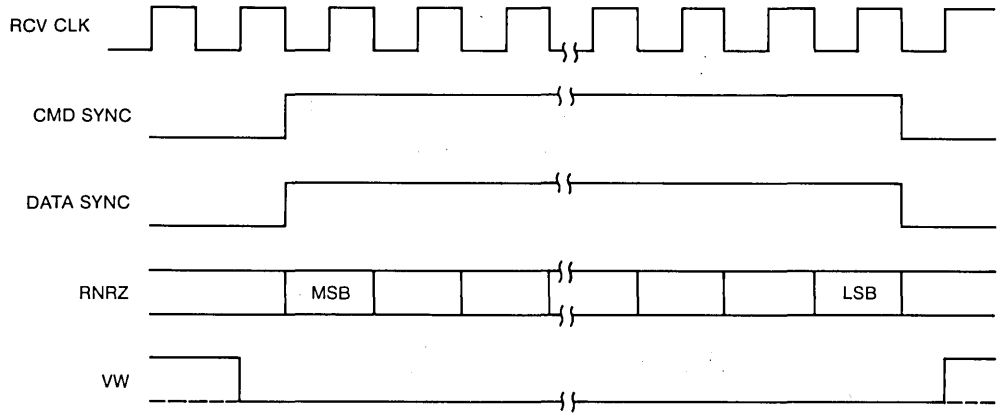
NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS (T_A = -55°C to 125°C, V_{CC} = +5 ±5%, unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
DC CHARACTERISTICS					
Input Voltage Levels					
Low Level, V_{IL}			0.8	V	
High Level, V_{IH}	3.0			V	
Output Voltage Levels					
Low Level V_{OL}			0.4	V	I_{OL} = -1.6 mA, except open drain
High Level V_{OH}	3.0	4.0		V	I_{OH} = 100 μA, except open drain
Low Level V_{OL}			0.4	V	I_{OL} = -1.6 mA, open drain output
Output Leakage, I_{LO}			10	μA	
Input Current, AD1-AD5		60		μA	V_{IN} = 0V
Output Capacitance		5	10	pf	
Input Capacitance		10	25	pf	
Power Dissipation			500	mW	

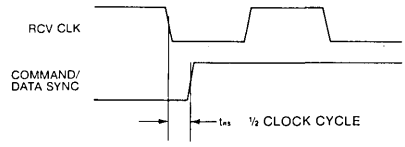
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
AC CHARACTERISTICS						
Clock Frequency	f_T, f_R	980	1000	1020	KHz	
Clock Duty Cycle		45	50	55	%	
Rise and fall times, $\overline{IA}$, $\overline{TDE}$ $\overline{TX\ MODE}$, $\overline{SWE}$, $\overline{RDE}$	t_r, t_f			20	ns	
rise and fall times, all other inputs	t_r, t_f			50	ns	
receiver clock-NRZ	t_{RN}			65	ns	figure 3B
receiver clock-sync delay	t_{SR}			85	ns	figure 3B
receiver clock-VW delay	t_{RV}			100	ns	figure 3B
VW reset delay	t_{VS}			500	ns	figure 3C
transmit clock-TX ENA delay	t_{TX}	25			ns	figure 4A
TX ENA pulse width	t_{XW}	60			ns	figure 4A
transmit clock-send data set-up	t_{TS}			40	ns	figure 4B
transmit clock-send data hold time	t_{ST}			140	ns	figure 4C
transmit clock fall to NRZ	t_{TN}	0			ns	figure 4B
transmit clock rise to NRZ	t_{NT}	95			ns	figure 4B
$\overline{TX\ MODE}$ pulse width	t_{MW}	150			ns	figure 5A
$\overline{TX\ MODE}$ to TX ENA delay	t_{MX}			750	ns	figure 5B
VALID word to TX ENA delay	t_{VX}			750	ns	figure 5B
Data sync to TX ENA delay	t_{DX}			750	ns	figure 5C
TX ENA reset delay	t_{SX}			750	ns	figure 5C
DATA SET-up time	t_{D1}	100			ns	figure 6A
$\overline{TDE}$ pulse width	t_{D2}	150			ns	figure 6A
Data Hold time	t_{D3}	100			ns	figure 6A
Cycle time	t_{D4}	450		16000	ns	figure 6A
DTA RQST Delay	t_{D5}	450			ns	figure 6A
Output Enable time	t_{D6}	100			ns	figure 6B
$\overline{RDE}$ Pulse width	t_{D7}	150			ns	figure 6B
receive cycle time	t_{D8}	450		17000	ns	figure 6B
Flag delay time	t_{D9}	450			ns	figure 6B
Output disable time	t_{D10}	100			ns	figure 6B
SEND DATA delay	t_{D11}	2.5		3.5	μs	figure 6C
$\overline{TDE}$ off delay	t_{D12}	1.5			μs	figure 6C
$\overline{TDE1}$ delay	t_{D13}	500			ns	figure 6C
SYN to $\overline{RDE}$	t_{D14}	500			ns	figure 6D
RDE to SYN	t_{D15}			2.5	μs	figure 6D
Status word Enable	t_{SE}			100	ns	figure 8A
Status word Disable	t_{SD}			100	ns	figure 8A
Flag delay time	t_{CF}			1	μs	figure 8B
VW delay time	t_{CV}			90	ns	figure 8B
IVWF delay time	t_{CI}			450	ns	figure 8B
DTA AVL delay time	t_{CD}			500	ns	figure 8B
DTA RQST delay time	t_{SR}			450	ns	figure 8C
$\overline{BRD\ CST}$ delay time	t_{RB}			2	μs	figure 8C
$\overline{BRD\ CST}$ pulse width	t_{BW}	1			μs	figure 8D
flag reset delay	t_{IB}			750	ns	figure 8D, 8E
Interrupt delay	t_{RI}			1.5	μs	figure 8D
IA pulse width	t_{IA}	150			ns	figure 8D
Interrupt pulse width	t_{IW}	1			μs	figure 8D
Flag reset time	t_{FR}			450	ns	figure 8F
DTA AVL reset delay	t_{RD}			750	ns	figure 8F
IVWF reset delay	t_{RV}			750	ns	figure 8F
$\overline{MSG\ CMPLT}$ turn-on delay	t_{MR}			1.5	μs	figure 9A, 9B
$\overline{MSG\ CMPLT}$ turn-on delay	t_{MF}			1.5	μs	figure 9A, 9C

RECEIVE TIMING FIGURE 2

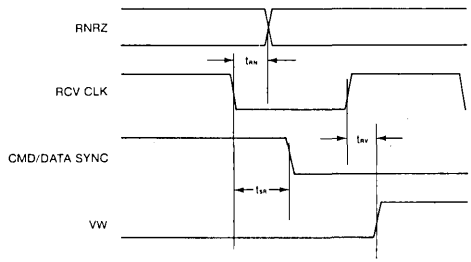


RECEIVER INPUT TIMING FIGURE 3

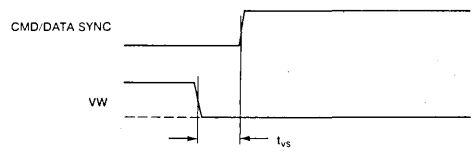
3A



3B

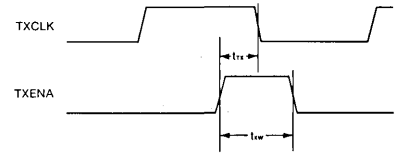


3C

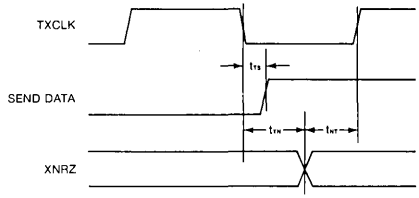


TRANSMITTER TIMING FIGURE 4

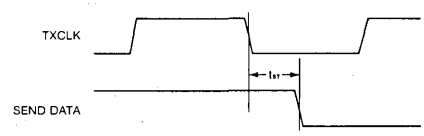
4A



4B

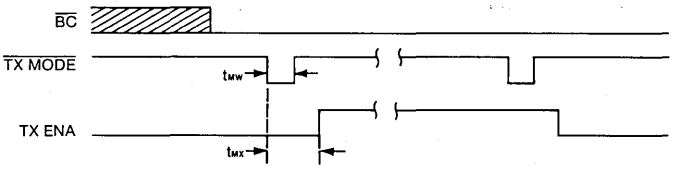


4C

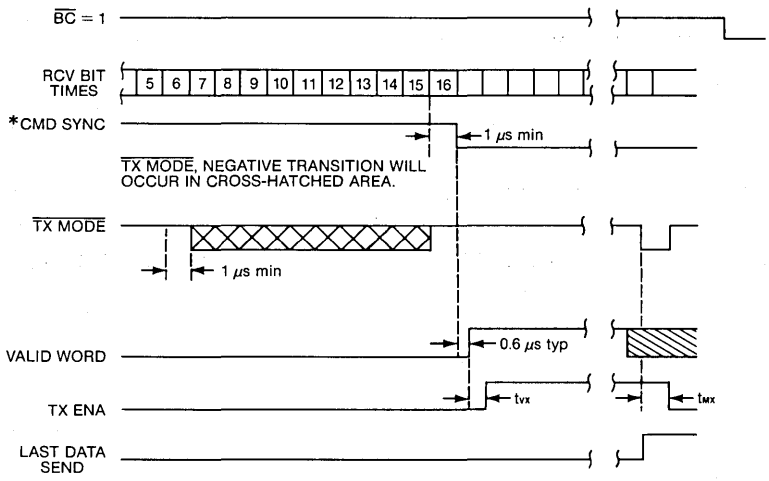


TRANSMIT ENABLE (TX ENA) TIMING FIGURE 5

5A

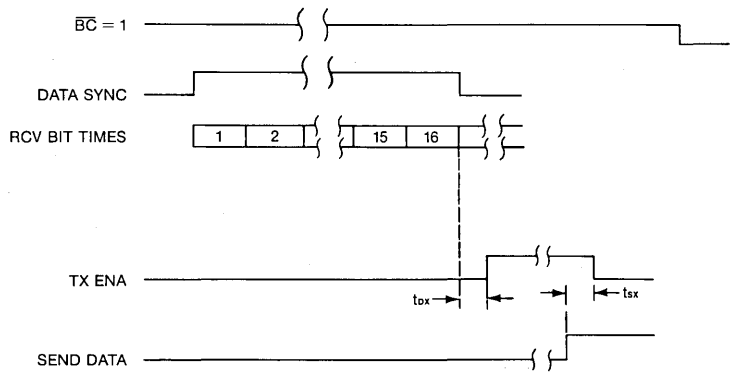


5B*



*THIS IS A CMD WORD BEING RECEIVED, IT IS ADDRESSED TO THIS BUFFER AND THE T/R BIT = 1. TX ENA IS RESET BY 2ND TX MODE NEGATIVE TRANSITION OR BY LAST SEND DATA (MESSAGE COMPLETE FUNCTION).

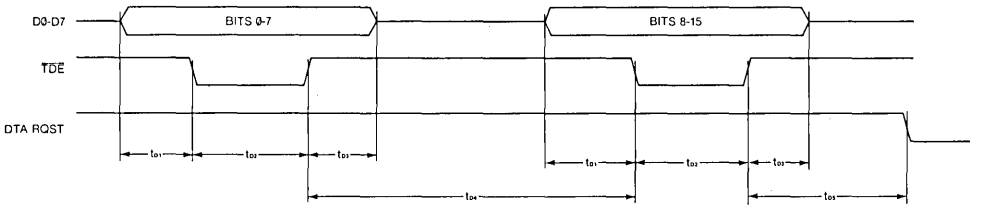
5C**



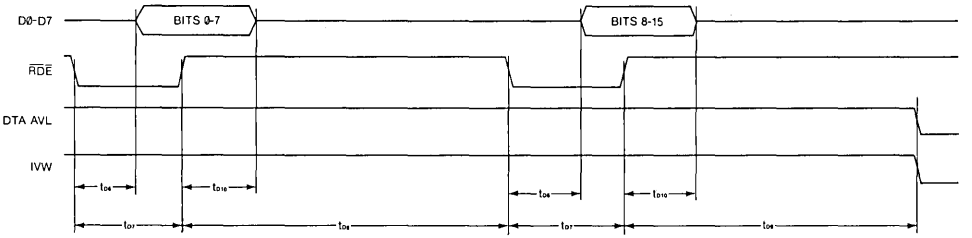
**THIS IS THE LAST DATA WORD BRING RECEIVED. THIS TERMINAL PREVIOUSLY HAD RECEIVED A REC CMD WORD WITH OUR ADDRESS AND A REC/XMIT BIT = 0 DURING THIS MESSAGE SEQUENCE. TX ENABLE IS SET BY MSG CMPLT FUNCTION AND RESET BY RECEIPT OF SEND DATA.

DATA BUS TIMING FIGURE 6

6A

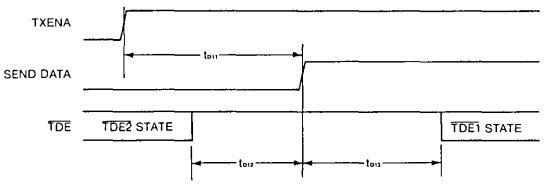


6B



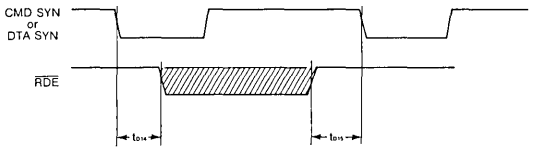
DATA BUS TIMING FIGURE 6

6C

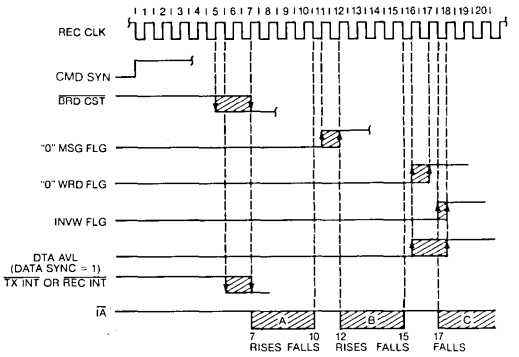


NOTE: SEND DATA RISING EDGE INITIALIZES $\overline{TDE}$ TO $\overline{TDE1}$ STATE

6D



$\overline{IA}$ RESETS FIGURE 7



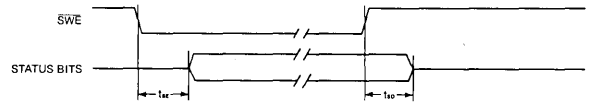
$\overline{IA}$ OCCURRING DURING ZONE A RESETS: BRD CST. TX INT. REC INT.

$\overline{IA}$ OCCURRING DURING ZONE B RESETS: BRD CST. TX INT. REC INT. "0" MSG FLG.

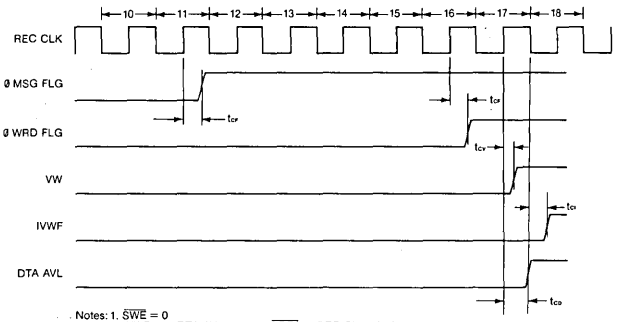
$\overline{IA}$ OCCURRING DURING ZONE C RESETS: BRD CST. TX INT. REC INT. "0" MSG FLG. "0" WRD FLG.

STATUS FLAGS FIGURE 8

8A

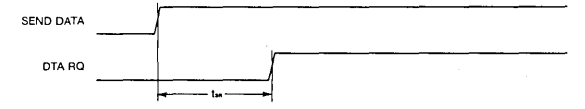


8B

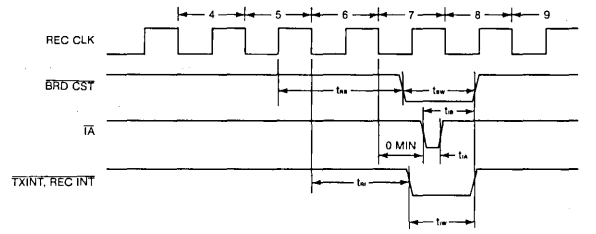


Notes: 1. $\overline{SWE} = 0$
2. IVWF and DTA AVL reset by $\overline{RDE2}$ or REC CLK 14 of the next word

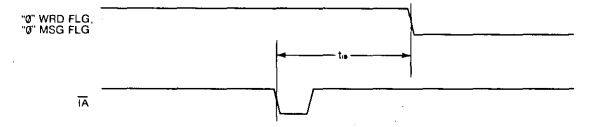
8C



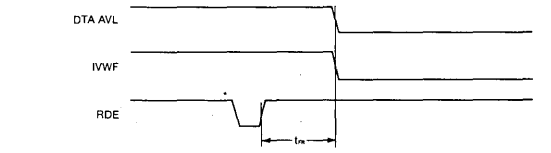
8D



8E

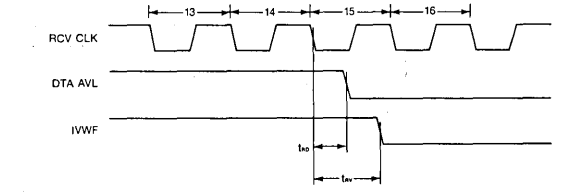


8F



*RDE 2

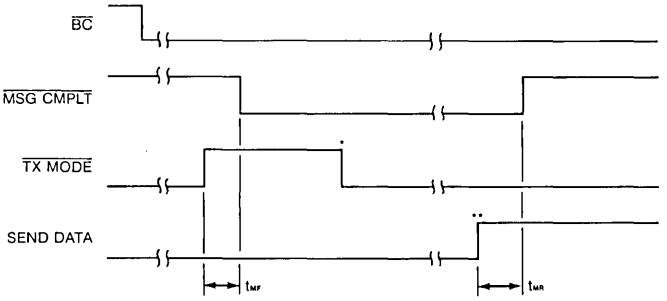
If RDE is not used to reset IVWF and RDE, then they are reset by RCV CLK 14 as shown below.



MESSAGE COMPLETE FIGURE 9

BUS CONTROLLER MODE

9A

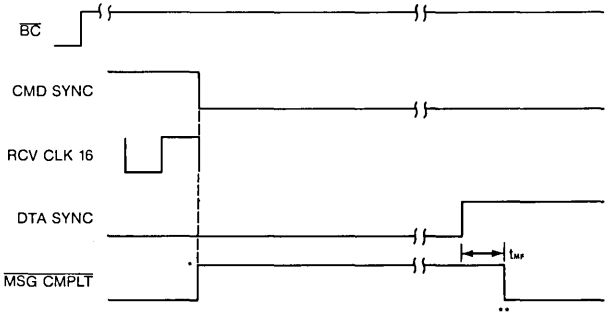


*WORD COUNTER IS PRESET TO 33

**MSG CMPLT SET t_{MR} MAX AFTER RISE OF 33RD SEND DATA PULSE

REMOTE TERMINAL, RECEIVE COMMAND RECEIVED

9B

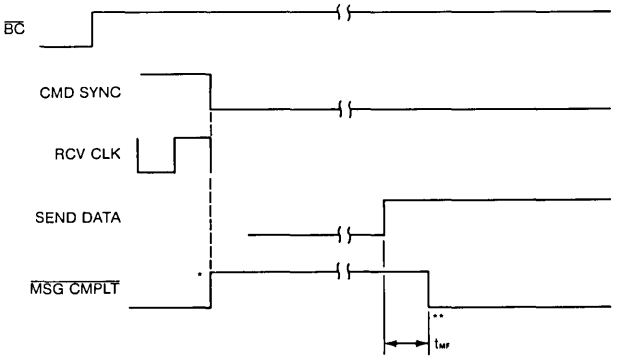


*WORD COUNTER PRESET TO COUNT IN COMMAND WORD

**MSG CMPLT GENERATED BY LAST DATA SYNC OF THE MESSAGE GROUP

REMOTE TERMINAL, TRANSMIT COMMAND RECEIVED

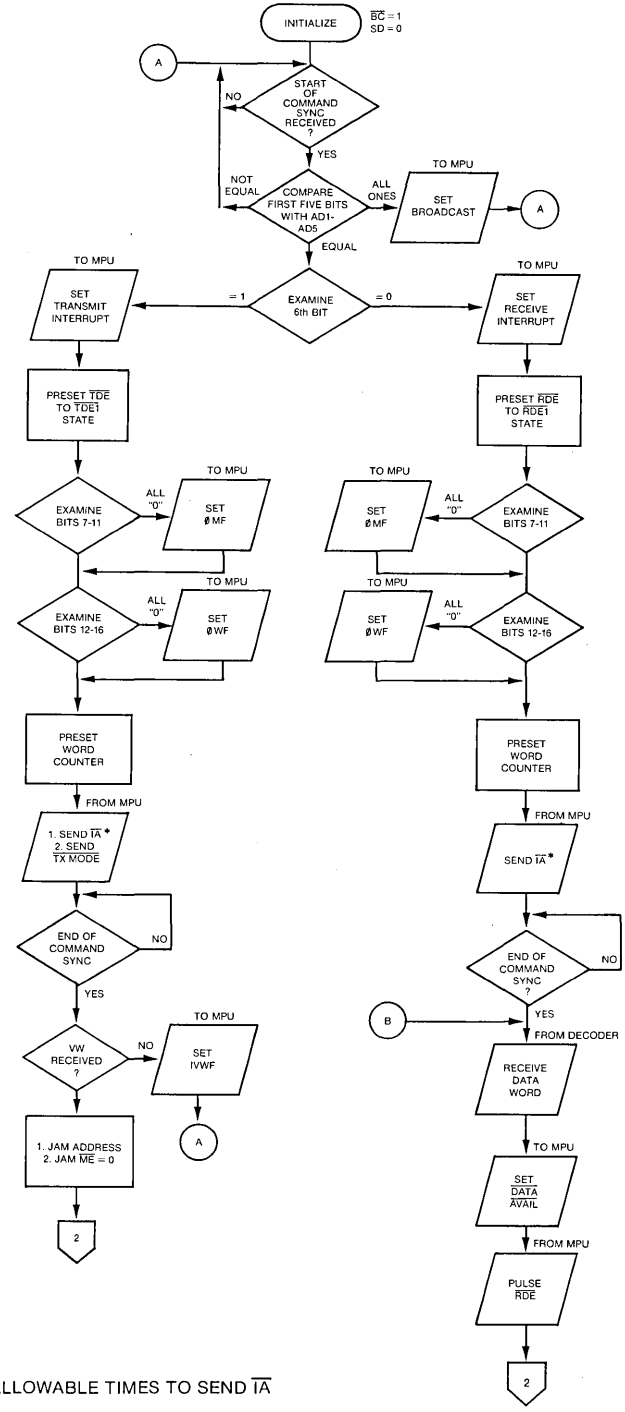
9C



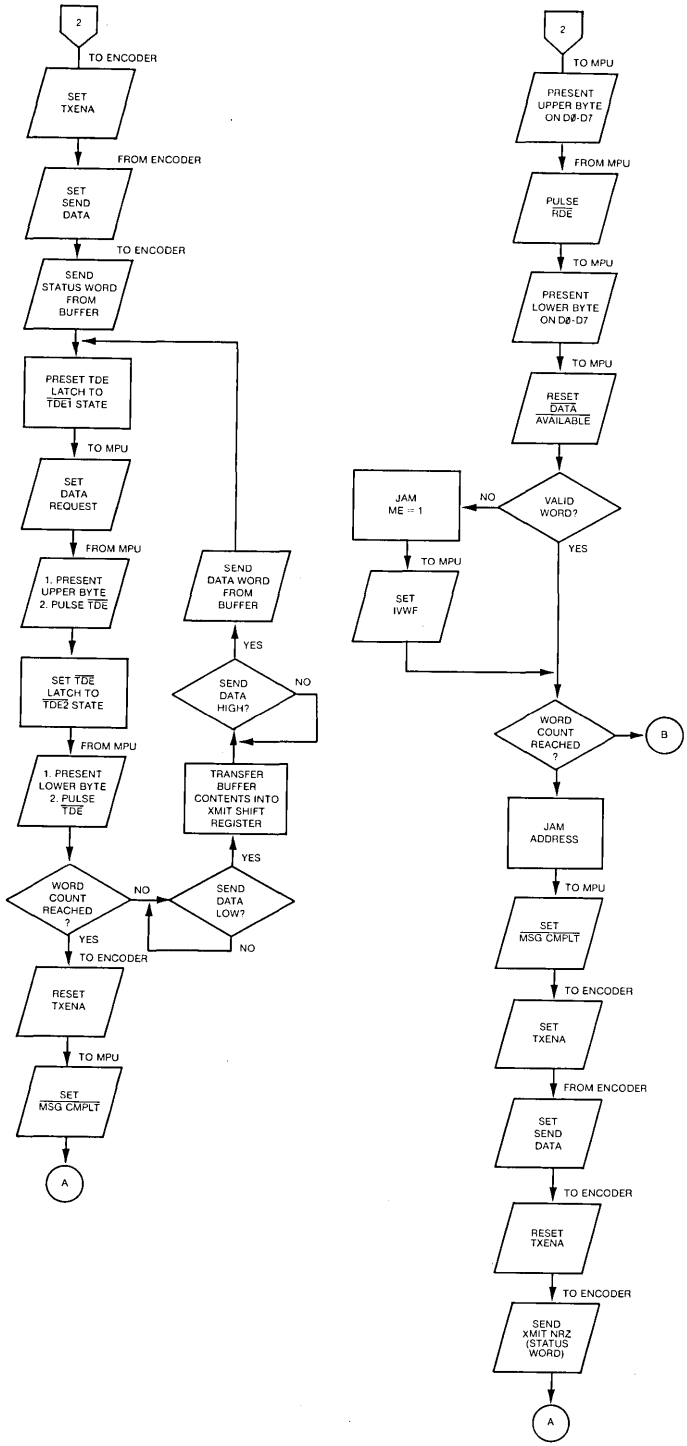
*WORD COUNTER PRESET TO TRANSMIT COMMAND WORD FIELD PLUS 1. THIS ALLOWS FOR THE STATUS WORD.

**MSG CMPLT GENERATED BY THE LAST SEND DATA OF THE TRANSMIT MESSAGE GROUP.

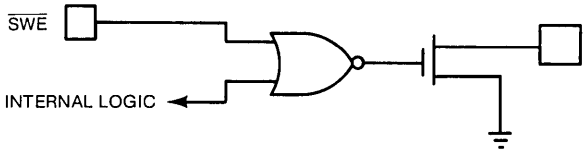
TYPICAL SYSTEM OPERATION



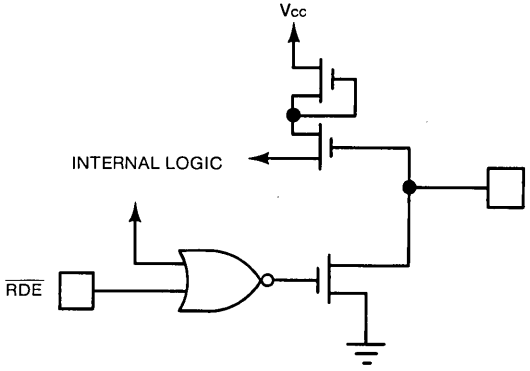
*SEE FIGURE 7 FOR ALLOWABLE TIMES TO SEND $\overline{IA}$


2
TO ENCODER
SET TXENA
FROM ENCODER
SET SEND DATA
TO ENCODER
SEND STATUS WORD FROM BUFFER
PRESET TDE LATCH TO TDE1 STATE
TO MPU
SET DATA REQUEST
FROM MPU
1. PRESENT UPPER BYTE
2. PULSE TDE
SET TDE LATCH TO TDE2 STATE
FROM MPU
1. PRESENT LOWER BYTE
2. PULSE TDE
WORD COUNT REACHED ?
NO
YES
SEND DATA LOW?
NO
YES
TRANSFER BUFFER CONTENTS INTO XMIT SHIFT REGISTER
SEND DATA HIGH?
NO
YES
SEND DATA WORD FROM BUFFER
TO ENCODER
RESET TXENA
TO MPU
SET MSG CMPLT
A
2
TO MPU
PRESENT UPPER BYTE ON DØ-D7
FROM MPU
PULSE RDE
TO MPU
PRESENT LOWER BYTE ON DØ-D7
TO MPU
RESET DATA AVAILABLE
VALID WORD?
NO
YES
JAM ME = 1
TO MPU
SET IWF
WORD COUNT REACHED ?
B
JAM ADDRESS
TO MPU
SET MSG CMPLT
TO ENCODER
SET TXENA
FROM ENCODER
SET SEND DATA
TO ENCODER
RESET TXENA
TO ENCODER
SEND XMIT NRZ (STATUS WORD)
A

OPEN DRAIN OUTPUT
FIGURE 10



DØ-D7 INPUT/OUTPUT
FIGURE 11



OTHER OUTPUTS
FIGURE 12