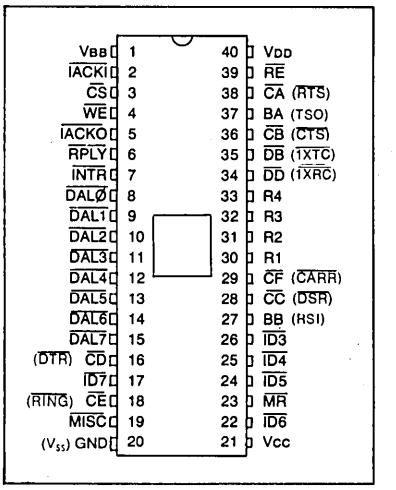
Asynchronous/Synchronous Transmitter-Receiver

ASTRO

FEATURES

- ☐ SYNCHRONOUS AND ASYNCHRONOUS
  - Full Duplex Operations
- ☐ SYNCHRONOUS MODE
  - Selectable 5-8 Bit Characters
  - Two Successive SYN Characters Sets Synchronization
  - Programmable SYN and DLE Character Stripping
  - Programmable SYN and DLE-SYN Fill
- ☐ ASYNCHRONOUS MODE
  - Selectable 5-8 Bit Characters
  - Line Break Detection and Generation
  - 1-, 1½-, or 2-Stop Bit Selection
  - Start Bit Verification
  - Automatic Serial Echo Mode
- ☐ BAUD RATE—DC TO 1M BAUD
- ☐ 8 SELECTABLE CLOCK RATES
  - Accepts 1X Clock and Up To 4 Different 32X Baud Rate Clock Inputs
  - Up to 47% Distortion Allowance With 32X Clock
- ☐ SYSTEM COMPATIBILITY
  - Double Buffering of Data
  - 8-Bit Bi-Directional Bus For Data, Status, and Control Words
  - All Inputs and Outputs TTL Compatible
  - Up To 32 ASTROS Can Be Addressed On Bus
  - On-Line Diagnostic Capability
- ☐ ERROR DETECTION
  - Parity, Overrun and Framing

PIN CONFIGURATION



- ☐ COPLAMOS® n-Channel Silicon Gate Technology
- ☐ Pin for Pin replacement for Western Digital UC1671 and National INS 1671
- ☐ Baud Rate Clocks Generated by COM5036 @ 1X and COM5016-6 @ 32X

APPLICATIONS

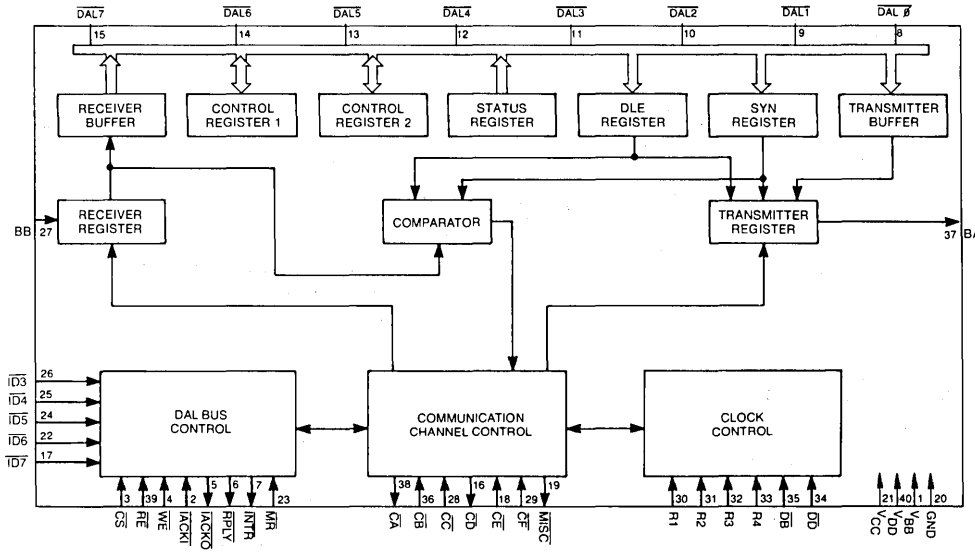
Synchronous Communications
Asynchronous Communications
Serial/Parallel Communications

General Description

The COM1671 (ASTRO) is a MOS/LSI device which performs the functions of interfacing a serial data communication channel to a parallel digital system. The device is capable of full duplex communications (receiving and transmitting) with synchronous or asynchronous systems. The ASTRO is designed to operate on a multiplexed bus with other bus-oriented devices. Its operation is programmed by a processor or controller via the bus and all parallel data transfers with these machines are accomplished over the bus lines.

The ASTRO contains several "handshaking" signals to insure easy interfacing with modems or other peripheral devices such as display terminals. In addition, a programmable diagnostic mode allows the selection of an internal looping feature which allows the device to be internally connected for processor testing.

The COM1671 provides the system communication designer with a software responsive device capable of handling complex communication formats in a variety of system applications.



Organization

Data Access Lines — The DAL bus is an 8-bit bi-directional port over which all address, data, control, and status transfers occur. In addition to transferring data and control words the DAL bus also transfers information related to addressing of the device, reading and writing requests, and interrupting information.

Receiver Buffer — This 8-bit parallel register presents assembled received characters to the DAL bus when requested through a Read operation.

Receiver Register — This 8-bit shift register inputs the received data at a clock rate determined by Control Register 2. The incoming data is assembled to the selected character length and then transferred to the Receiver Buffer with logic zeroes filling out any unused high-order bit positions.

Syn Register — This 8-bit register is loaded from the DAL bus by a Write operation and holds the synchronization code used for receiver character synchronization. It serves as a fill character when no new data is available in the Transmitter Buffer during transmission. This register cannot be read onto the DAL bus. It must be loaded with logic zeroes in all unused high-order bits.

Comparator — The 8-bit comparator is used in the Synchronous mode to compare the assembled contents of the Receiver Register and the SYN register or the DLE register. A match between the registers sets up stripping of the received character, when programmed, by preventing the data from being loaded into the Receiver Buffer. A bit in the Status Register is set when stripping is effected. The comparator output also enables character synchronization of the Receiver on two successive matches with the SYN register.

DLE Register — This 8-bit register is loaded from the DAL bus by a Write operation and holds the DLE character used in the Transparent mode of operation in which an idle transmit period is filled with the combination DLE-SYN pair of characters rather than a single SYN character. In addition the ASTRO may be programmed to force a single DLE character prior to any data character transmission while in the transmitter transparent mode.

Status Register — This 8-bit register holds information on communication errors, interface data register status, match character conditions, and communication equipment status. This register may be read onto the DAL bus by a Read operation.

Control Registers — There are two 8-bit Control Registers which hold device programming signals such as mode selection, clock selection, interface signal control, and data format. Each of the Control Registers can be loaded from the DAL bus by a Write operation or read onto the DAL bus by a Read operation. The registers are cleared by a Master Reset.

Transmitter Buffer — This 8-bit parallel register holds data transferred from the DAL bus by a Write operation. This data is transferred to the Transmitter Register when the transmitter section is enabled and the Transmitter Register is ready to send new data.

Transmitter Register — This 8-bit shift register is loaded from the Transmitter Buffer, SYN register, or DLE register. The purpose of this register is to serialize data and present it to the serial data output.

Astro Operation

Asynchronous Mode

Framing of asynchronous characters is provided by a Start bit (logic 0) at the beginning of a character and a Stop bit(s) (logic 1) at the end of a character. Reception of a character is initiated on recognition of the first Start bit by a positive transition of the receiver clock, after a preceding Stop bit(s). The Start and Stop bits are stripped off while assembling the serial input into a parallel character.

The character assembly is completed by the reception of the Stop bit(s) after reception of the last character bit (including the parity bit, if selected). If the Stop bit(s) is a logic 1, the character is determined to have correct framing and the ASTRO is prepared to receive the next character. If the Stop bit(s) is a logic 0, the Framing Error Status flag is set and the Receiver assumes this bit to be the Start bit of the next character. Character assembly continues from this point if the input is still a logic 0 when sampled at the theoretical center of the assumed Start bit. As long as the Receiver input is spacing, all zero characters are assembled and error flags and data received interrupts are generated so that line breaks can be determined. After a character of all zeroes is assembled along with a zero in the Stop bit(s) location, the first sampled logic one is determined as a Stop bit and this resets the Receiver circuit to a Ready state for assembly of the next character.

In the Asynchronous mode the character transmission occurs when information contained in the Transmitter Buffer is transferred to the Transmitter Register. Transmission is initiated by the insertion of a Start bit, followed by the serial output of the character (including the parity bit, if selected), then the insertion of a 1, 1.5, or 2 bit length Stop condition. If the Transmitter Buffer is full, the next character transmission starts after the transmission of the Stop bit(s) of the present character in the Transmitter Register. Otherwise, the Mark (logic 1) condition is continually transmitted until the Transmitter Buffer is loaded.

Synchronous Mode

Framing of characters is carried out by a special Synchronization Character Code (SYN) transmitted at the beginning of a block of characters. The Receiver, when enabled, searches for two contiguous characters matching the bit pattern contained in the SYN register. During the time the Receiver is searching, data is not transferred to the Receiver Buffer, status bits are not updated, and the Receiver interrupt is not activated. After the detection of the first SYN character, the Receiver assembles subsequent bits into characters whose length is determined by the contents of Control Register 2. If, after the first SYN character detection, a second SYN character is present, the Receiver enters the Synchronization mode until the Receiver Enable Bit is turned off. If a second successive SYN character is not found, the Receiver reverts back to the Search mode.

In the Synchronous mode a continuous stream of characters are transmitted once the Transmitter is enabled. If the Transmitter Buffer is not loaded at the time the Transmitter Register has completed transmission of a character, this idle time will be filled by a transmission of the character contained in the SYN register in the Non-transparent mode, or the characters contained in the DLE and SYN registers respectively while in the Transparent mode of operation.

Astro Operation

Receiver

The Receiver Data input is clocked into the Receiver Register by a 1X Receiver Clock from a modem Data Set, or by a local 32X bit rate clock selected from one of four externally supplied clock inputs. When using the 1X clock, the Receiver Data is sampled on the positive transition of the clock in both the Asynchronous and Synchronous modes. When using a 32X clock in the Asynchronous mode, the Receiver Sampling Clock is phased to the Mark-To-Space transition of the Received Data Start bit and defines, through clock counts, the center of each received Data bit with +0%, −3% at the positive transition 16 clock periods later.

In the Synchronous mode the Sampling Clock is phased to all Mark-To-Space transitions of the Received Data inputs when using a 32X clock. Each transition of the data causes an incremental correction of the Sampling Check by 1/32nd of a bit period. The Sampling clock can be immediately phased to every Mark-To-Space Data transition by setting Bit 4 of Control Register 1 to a logic one, while the Receiver is disabled.

When the complete character has been shifted into the Receiver Register it is transferred to the Receiver Buffer; the unused, higher order bits are filled with logic zero's. At this time the Receiver Status bits (Framing Error/Sync Detect, Parity Error/DLE Detect, Overrun Error, and Data Received) are updated in the Status Register and the Data Received interrupt is activated. Parity Error is set, if encountered while the Receiver parity check is enabled in the Control Registers. Overrun Error is set if the Data Received status bit is not cleared through a Read operation by an external device when a new character is transferred to the Receiver Buffer. This error flag indicates that a character has been lost; new data is lost while the old data and its status flags are saved.

The characters assembled in the Receiver Register that match the content of the SYN or the DLE register are not loaded into the Receiver Buffer, and the DR interrupt is not generated, if Bit 3 of Control Register 2 (CR23) or Bit 4 of Control Register 1 (CR14) are set respectively, and SYN Detect and DLE Detect are set with the next non SYN or non DLE character. When both CR23 and CR14 are set (Transparent mode), the DLE-SYN combination is stripped. The SYN comparison occurs only with the character received after the DLE character. If two successive DLE characters are received only the first DLE character is stripped. No parity check is made while in this mode.

Transmitter

Information is transferred to the Transmitter Buffer by a Write operation. Information can be loaded into this register at any time, even when the Transmitter is not enabled. Transmission of data occurs only when the Request to Send bit is set to a logic 1 in Control Register 1 and the Clear To Send input is logic 0. Information is normally transferred from the Transmitter Buffer to the Transmitter Register when the latter has completed transmission of a character. However, information in the DLE register may be transferred prior to the information contained in the Transmitter Buffer if the Force DLE signal condition is enabled (Bits 5 and 6 of Control Register 1 set to a logic 1). The control bit CR15 must be set prior to loading of a new character in the Transmitter Buffer to insure forcing the DLE character prior to transmission of the data character. The Transmitter Register output passes through a flip-flop which delays the output by one clock period. When using the 1X clock generated by the Modem Data Set, the output data changes state on the negative clock transition and the delay is one bit period. When using a local 32X clock the the transmitter section selects one of the four selected rate inputs and divides the clock down to the baud rate. This clock is phased to the Transmitter Buffer Empty Flag such that transmission of characters occurs within two clock times of the loading of the Transmitter Buffer, when the Transmitter Register is empty.

When the Transmitter is enabled, a Transmitter interrupt is generated each time the Transmitter Buffer is empty. If the Transmitter Buffer is empty, when the Transmitter Register is ready for a new character, the Transmitter enters an idle state. During this idle time a logic 1 will be presented to the Transmitted Data output in the Asynchronous mode or the contents of the SYN register will be presented in the Synchronous Non-transparent mode (CR16 = 0). In the Synchronous Transmit Transparent mode (CR16 = 1), the idle state will be filled by DLE-SYN character transmission in that order. When entering the Transparent mode DLE must precede the contents of the Transmitter Buffer. This is accomplished by setting of Bit 5 of Control Register 1.

If the transmitter section is disabled by a reset of the Request to Send, any partially transmitted character is completed before the transmitter section of the ASTRO is disabled. As soon as the Clear To Send goes high the transmitted data output will go high.

When the Transmitter parity is enabled, the selected Odd or Even parity bit is inserted into the last data bit of the character in place of the last bit of the Transmitter Register. This limits transfer of character information to a maximum of seven bits plus parity or eight bits without parity. Parity cannot be enabled in the Synchronous Transparency mode.

Input/Output Operations

All Data, Control, and Status words are transferred over the Data Access Lines (DAL 0-7). Additional input lines provide controls for addressing a particular ASTRO, and regulating all input and output operations. Other lines provide interrupt capability to indicate to a Controller that an input operation is requested by the ASTRO. All input/output terminology below is referenced to the Controller so that a Read or input takes data from the ASTRO and places it on the DAL bus, while a Write or Output places data from the DAL bus into the ASTRO.

A Read or Write operation is initiated by the placement of an eight-bit address on the DAL bus by the Controller. When the Chip Select signal goes to a logic 0 state, the ASTRO compares Bits 7-3 of the DAL bus with its hard-wired ID code (Pins 17, 22, 24, 25, and 26) and becomes selected on a Match condition. The ASTRO then sets its RPLY line low to acknowledge its readiness to transfer data. Bit 0 must be a logic O in Read or Write operation. A setup time must exist between CS and the RE or WE signals to allow chip selection prior to read/write operations.

Read

Bits 2-0 of the address are used to select ASTRO registers to read from as follows:

Bits 2-0	Selected Register
000	Control Register 1
010	Control Register 2
100	Status Register
110	Receiver Buffer

When the Read Enable (RE) line is set to a logic 0 condition by the Controller the ASTRO gates the contents of the addressed register onto the DAL bus. The Read operation terminates, and the device becomes unselected, when both the Chip Select and Read Enable return to a logic 1 condition. Reading of the Receiver Buffer clears the Data Received Status bit. The data is removed from the DAL bus when the RE signal returns to the logic high state.

Write

Bits 2-0 of the address are used to select ASTRO registers to be written into as follows:

Bits 2-0	Selected Register
000	Control Register 1
010	Control Register 2
100	SYN and DLE Register
110	Transmitter Buffer

When the Write Enable (WE) line is set to a logic 0 condition by the Controller the ASTRO gates the data from the DAL bus into the addressed register. If data is written into the Transmitter Buffer, the TBMT Status bit is cleared to a logic zero.

The 100 address loads both the SYN and DLE registers. After writing into the SYN register the device is conditioned to write into the DLE if followed by another Write pulse with the 100 address. Any intervening Read or Write operation with other addresses or other ASTROs resets this condition such that the next 100 will address the SYN register.

Interrupts

The following conditions generate interrupts:

Data Received (DR)

Indicates transfer of a new character to the Receiver Buffer while the Receiver is enabled.

Transmitter Buffer Empty (TBMT)

Indicates that the Transmitter Buffer is empty while the Transmitter is enabled. The first interrupt occurs when the Transmitter becomes enabled if there is an empty Transmitter Buffer, or after the character is transferred to the Transmitter Register making the Transmitter Buffer empty.

Carrier On

Indicates Carrier Detector input goes low and the Data Terminal Ready (DTR) bit (CR10) is high.

Carrier Off

Indicates Carrier Detector input goes high and the Data Terminal Ready (DTR) bit (CR10) is high.

Data Set Ready On

Indicates the Data Set Ready input goes low and the Data Terminal Ready (DTR) bit (CR10) is high.

Data Set Ready Off

Indicates the Data Set Ready input goes high and the Data Terminal Ready (DTR) bit (CR10) is high.

Ring On

Indicates the Ring Indicator input goes low and the Data Terminal Ready (DTR) bit (CR10) is low.

Each time an interrupt condition exists the INTR output from the ASTRO is made a logic low. The following interrupt procedure is then carried out even if the interrupt condition is removed.

The Controller acknowledges the Interrupt request by setting the Chip Select (CS) and the Interrupt Acknowledge Input (IACKI) to the ASTRO to a low state. On this transition all non-interrupting devices receiving the IACKI signal set their Interrupt Acknowledge Output (IACKO) low, enabling lower priority daisy-chained devices to respond to the interrupt request. The highest priority device that is interrupting will then set its RPLY line low. This device will place its ID code on Bit Positions 7-3 of the DAL bus when a low RE signal is received. The data is removed from the DAL bus when the Read Enable (RE) signal returns to the logic one state. To reset the Interrupt condition (INTR) Chip Select (CS) and IACKI must be received by the ASTRO.

Description of Pin Functions

Pin No.	Symbol	Pin Name	I/O	Function
1	V_{BB}	POWER SUPPLY	PS	− 5 Volts
21	V_{CC}	POWER SUPPLY	PS	+ 5 Volts
40	V_{DD}	POWER SUPPLY	PS	+ 12 Volts
20	V_{SS}	GROUND	GND	Ground
23	$\overline{MR}$	$\overline{MASTER\ RESET}$	I	The Control and Status Registers and other controls are cleared when this input is low.
8-15	$\overline{DAL0}$-$\overline{DAL7}$	$\overline{DATA\ ACCESS\ LINES}$	I/O	Eight-bit bi-directional bus used for transfer of data, control status, and address information.
17	$\overline{ID7}$	$\overline{SELECT\ CODE}$	I	Five input pins which when hard-wired assign the device a unique identification code used to select the device when addressing and used as an identification when responding to interrupts.
22	$\overline{ID6}$		I	
24	$\overline{ID5}$		I	
25	$\overline{ID4}$		I	
26	$\overline{ID3}$		I	
3	$\overline{CS}$	$\overline{CHIP\ SELECT}$	I	The low logic transition of $\overline{CS}$ identifies a valid address on the DAL bus during Read and Write operations.
39	$\overline{RE}$	$\overline{READ\ ENABLE}$	I	This input, when low, gates the contents of the addressed register from a selected ASTRO onto the DAL bus.
4	$\overline{WE}$	$\overline{WRITE\ ENABLE}$	I	This input, when low, gates the contents of the DAL bus into the addressed register of a selected ASTRO.
7	$\overline{INTR}$	$\overline{INTERRUPT}$	O	This open drain output, to facilitate WIRE-ORing, goes low when any interrupt conditions occur.
2	$\overline{IACKI}$	$\overline{INTERRUPT\ ACKNOWLEDGE\ IN}$	I	When the Controller (determining the interrupting ASTRO) makes this input low, the ASTRO places its ID code on the DAL bus and sets reply low if it is interrupting, otherwise it makes $\overline{IACKO}$ a low.
5	$\overline{IACKO}$	$\overline{INTERRUPT\ ACKNOWLEDGE\ OUT}$	O	This output goes low in response to a low $\overline{IACKI}$ if the ASTRO is not the interrupting device.
6	$\overline{RPLY}$	$\overline{REPLY}$	O	This open drain output, to facilitate WIRE-ORing, goes low when the ASTRO is responding to being selected by an address on the DAL bus or in affirming that it is the interrupting source.

Description of Pin Functions

Pin No.	Symbol	Pin Name	I/O	Function
30 31 32 33	R1 R2 R3 R4	CLOCK RATES	I I I I	These four inputs accept four different local 32X data rate Transmit and Receive clocks. The input on R4 may be divided down into a 32X clock from a 32X, 64X, 128X, or 256X clock input. The clock used in the ASTRO is selected by bits 0-2 of Control Register 2.
37	BA	TRANSMITTED DATA	O	This output is the transmitted serial data from the ASTRO. This output is held in a Marking condition when the transmitter section is not enabled.
27	BB	RECEIVED DATA	I	This input receives serial data into the ASTRO.
38	$\overline{CA}$	$\overline{\text{REQUEST TO SEND}}$	O	This output is enabled by bit 1 of Control Register 1 and remains in a low state during transmitted data from the ASTRO.
36	$\overline{CB}$	$\overline{\text{CLEAR TO SEND}}$	I	This input, when low, enables the transmitter section of the ASTRO.
28	$\overline{CC}$	$\overline{\text{DATA SET READY}}$	I	This input generates an interrupt when going ON or OFF while the Data Terminal Ready signal is ON. It appears as bit 6 in the Status Register.
16	$\overline{CD}$	$\overline{\text{DATA TERMINAL READY}}$	O	This output is generated by bit 0 in Control Register 1 and indicates Controller readiness.
18	$\overline{CE}$	$\overline{\text{RING INDICATOR}}$	I	This input from the Data Set generates an interrupt when made low with Data Terminal Ready in the OFF condition.
29	$\overline{CF}$	$\overline{\text{CARRIER DETECTOR}}$	I	This input from the Data Set generates an interrupt when going ON or OFF if Data Terminal Ready is ON. It appears as bit 5 in the Status Register.
35	$\overline{DB}$	$\overline{\text{TRANSMITTER TIMING}}$	I	This input is the Transmitter 1X Data Rate Clock. Its use is selected by bits 0-2 of Control Register 2. The transmitted data changes on the negative transition of this signal.
34	$\overline{DD}$	$\overline{\text{RECEIVER TIMING}}$	I	This input is the Receiver 1X Data Rate Clock. Its use is selected by bits 0-2 of Control Register 2. The Received Data is sampled by the ASTRO on the positive transition of this signal.
19	$\overline{MISC}$	$\overline{\text{MISCELLANEOUS}}$	O	This output is controlled by bits 4 and 5 of Control Register 1 and is used as an extra programmable signal.

Device Programming

The two 8-bit Control Registers of the ASTRO determine the operative conditions of the ASTRO chip.

Control Register 1

BIT 7	6	5	4	3	2	1	0
SYNC/ASYNC 0 – LOOP MODE 1 – NORMAL MODE	ASYNC 0 – NONBREAK MODE 1 – BREAK MODE TX SYNC 0 – TRANSMITTER NON TRANSPARENT MODE 1 – TRANSMITTER TRANSPARENT MODE	ASYNC (TRANS. ENABLED) 0 – 1½ or 2 STOP BIT SELECTION 1 – SINGLE STOP BIT SELECTION ASYNC (TRANS. DISABLED) 0 – $\overline{\text{MISC}}$ OUT = 1 1 – $\overline{\text{MISC}}$ OUT = 0 SYNC (CR16 = 0) 0 – NO PARITY GENERATED 1 – TRANSMIT PARITY ENABLED SYNC (CR16 = 1) 0 – NO FORCE DLE 1 – FORCE DLE	ASYNC 0 – NON ECHO MODE 1 – AUTO ECHO MODE SYNC (CR12 = 1) 0 – DLE STRIPPING NOT ENABLED 1 – DLE STRIPPING ENABLED SYNC (CR12 = 0) 0 – $\overline{\text{MISC}}$ OUT = 1 1 – $\overline{\text{MISC}}$ OUT = 0	ASYNC 0 – NO PARITY ENABLED 1 – PARITY CHECK ENABLED ON RECEIVER AND PARITY GENERATION ENABLED ON TRANSMITTER SYNC 0 – RECEIVER PARITY CHECK IS DISABLED 1 – RECEIVER PARITY CHECK IS ENABLED	SYNC/ASYNC 0 – RECEIVER DISABLED 1 – RECEIVER ENABLED	SYNC/ASYNC 0 – SETS $\overline{\text{RTS}}$ OUT = 1 1 – SETS $\overline{\text{RTS}}$ OUT = 0	SYNC/ASYNC 0 – SETS $\overline{\text{DTR}}$ OUT = 1 1 – SETS $\overline{\text{DTR}}$ OUT = 0

Bit 0

Controls the Data Terminal Ready output on Pin 16 to control the CD circuit of the Data Set. A logic 1 enables the Carrier and Data Set Ready interrupts. A logic 0 enables only the telephone line Ring interrupt. The $\overline{\text{DTR}}$ output is inverted from the state of CR10.

Bit 1

Controls the Request to Send output on Pin 38 to control the CA circuit of the Data Set. The $\overline{\text{RTS}}$ output is inverted from the state of CR11. A logic 1 combined with a low logic Clear to Send input enables the Transmitter and allows TBMT interrupts to be generated. A logic 0 disables the Transmitter and turns off the external Request to Send signal. Any character in the Transmitter Register will be completely transmitted before the Transmitter is turned off. The Request to Send output may be used for other functions such as Make Busy on 103 Data Sets.

Bit 2

A logic 1 enables the ASTRO to receive data into the Receiver Buffer, update Receiver Status Bits 1, 2, 3, and 4, and to generate Data Received interrupts. A logic 0 disables the Receiver and clears the Receiver Status bits.

Bit 3

Asynchronous Mode

A logic 1 enables check of parity on received characters and generation of parity for transmitted characters.

Synchronous Mode

A logic 1 bit enables check of parity on received characters only. Note: Transmitter parity enable is controlled by CR15.

Bit 4

Asynchronous Mode

A logic 1 enables the Automatic Echo mode when the receiver section is enabled. In this mode the clocked regenerated data is presented to the Transmitter Data output in place of normal transmission through the Transmitter Register. This serial method of echoing does not present any abnormal restrictions on the transmit speed of the terminal. Only the first character of a Break condition of all zeroes (null character) is echoed when a Line Break condition is detected. For all subsequent null characters, with logic zero Stop bits, a steady Marking condition is transmitted until normal character reception resumes. Echoing does not start until a character has been received and the Transmitter is idle. The Transmitter does not have to be enabled during the Echo mode.

Synchronous Mode

A logic 1, with the Receiver enabled does not allow assembled Receiver data matching the DLE register contents to be transferred to the Receiver Buffer; also, parity checking is disabled.

When the Receiver is not enabled this bit controls the Miscellaneous output on Pin 19, which may be used for New Sync on a 201 Data Set. When operating with a 32X clock and a disabled Receiver, a logic 1 on this bit also causes the Receiver timing to synchronize on Mark-To-Space transitions.

Bit 5

Asynchronous Mode

A logic 1, with the Transmitter enabled, causes a single Stop bit to be transmitted. A logic 0 causes transmission of 2 stop bits for character lengths of 6, 7, or 8 bits and one-and-a-half Stop bits for a character length of 5 bits.

With the Transmitter disabled this bit controls the Miscellaneous output on Pin 19, which may be used for Make Busy on 103 Data Sets, Secondary Transmit on 202 Data Sets, or dialing on CBS Data Couplers.

Synchronous Mode

A logic 1 combined with a logic 0 on Bit 6 of Control Register 1 enables Transmit parity; if CR15=0 or CR16=1 no parity is generated. When set to a logic 1 with Bit 6 also a logic 1, the contents of the DLE register are transmitted prior to the next character loaded in the Transmitter Buffer as part of the Transmitter Transparent mode.

Bit 6

Asynchronous Mode

A logic 1 holds the Transmitted Data output in a Spacing (Logic 0) condition, starting at the end of any current transmitted character, when the Transmitter is enabled. Normal Transmitter timing continues so that this Break condition can be timed out after the loading of new characters into the Transmitter Buffer.

Synchronous Mode

A logic 1 conditions the Transmitter to a transparent transmission which implies that idle transmitter time will be filled by DLE-SYN character transmission and a DLE character can be forced ahead of any character in the Transmitter Buffer (Bit 5 above). When forcing DLE transmission, Bit 5 should be set to a logic 1 prior to loading the Transmitter Buffer, otherwise the character in the latter register may be transferred to the Transmitter Register prior to sending the DLE character.

Bit 7

A logic 0 configures the ASTRO into an Internal Data and Control Loop mode and disables the Ring interrupt. In this diagnostic mode the following loops are connected internally:

a. The Transmit Data is connected to the Receive Data with the BA pin held in a Mark condition and the input to the BB pin disregarded.

b. With a 1X clock selected, the Transmitter Clock also becomes the Receive Clock.

c. The Data Terminal Ready (DTR) Control bit is connected to the $\overline{\text{Data Set Ready (DSR)}}$ input, with the $\overline{\text{Data Terminal Ready (DSR)}}$ output pin held in an OFF condition (logic high), and the $\overline{\text{DSR}}$ input pin is disregarded.

d. The Request to Send Control bit is connected to the $\overline{\text{Clear To Send (CTS)}}$ and $\overline{\text{Carrier Detector (CF)}}$ inputs, with the $\overline{\text{Request To Send (RTS)}}$ output pin held in an OFF condition (logic high), and the $\overline{\text{CTS}}$ and $\overline{\text{Carrier Detector}}$ input pins are disregarded.

e. The $\overline{\text{Miscellaneous}}$ pin is held in an OFF (logic high) condition.

A logic 1 on Bit 7 enables the Ring interrupt and returns the ASTRO to the normal full duplex configuration.

Control Register 2

Control Register 2, unlike Control Register 1, cannot be changed at any time. This register should be changed only while both the receiver and transmitter sections of the ASTRO are in the idle state.

BIT 7 6	5	4	3	2 1 0
SYNC/ASYNC CHARACTER LENGTH SELECT 00 = 8 BITS 01 = 7 BITS 10 = 6 BITS 11 = 5 BITS	MODE SELECT 0 – ASYNCHRONOUS MODE 1 – SYNCHRONOUS MODE	SYNC/ASYNC 0 – EVEN PARITY SELECT 1 – ODD PARITY SELECT	ASYNC 0 – RECEIVER CLK = RATE 1 1 – RECEIVER CLOCK DETERMINED BY BITS 2-0 SYNC (CR16 = 0) 0 – NO SYN STRIP 1 – SYN STRIP SYNC (CR16 = 1) 0 – NO DLE-SYN STRIP 1 – DLE-SYN STRIP	SYNC/ASYNC CLOCK SELECT 000 – 1X CLOCK 001 – RATE 1 CLOCK 010 – RATE 2 CLOCK 011 – RATE 3 CLOCK 100 – RATE 4 CLOCK 101 – RATE 4 CLOCK ÷ 2 110 – RATE 4 CLOCK ÷ 4 111 – RATE 4 CLOCK ÷ 8

Bits 0-2
These bits select the Tranmit and Receive clocks.

Bits	Clock Source	
2 1 0	Tx	Rx
0 0 0	1X Clock (Pin 35)	1X Clock (Pin 34)
0 0 1	Rate 1 32X clock (Pin 30)	
0 1 0	Rate 2 32X clock (Pin 31) *	
0 1 1	Rate 3 32X clock (Pin 32) *	
1 0 0	Rate 4 32X clock (Pin 33) *	
1 0 1	Rate 4 32X clock (Pin 33) (÷ 2) *†	
1 1 0	Rate 4 32X clock (Pin 33) (÷ 4) *†	
1 1 1	Rate 4 32X clock (Pin 33) (÷ 8) *†	

NOTES:
*Rx clock is modified by bit 3 in the asynchronous mode.
†Rate 4 is internally dividable so that the required 32X clock may be derived from an applied 64X, 128X, or 256X clock which may be available.

Bits 3

Asynchronous Mode

A logic 0 selects the Rate 1 32X clock input (Pin 30) as the Receiver clock rate and a logic 1 selects the same clock rate for the Receiver as selected by Bits 2-0 for the Transmitter. This bit must be a logic 1 for the 1X clock selection by Bits 2-0.

Synchronous Mode

A logic 1 causes all DLE-SYN combination characters in the Transparent mode when DLE strip (CR14) is a logic 1, or all SYN characters in the Non-transparent mode to be stripped out and no Data Received interrupt to be generated. The SYN Detect status bit is set with reception of the next assembled character as is transferred to the Receiver Buffer.

Bit 4
A logic 1 selects odd parity and a logic 0 selects even parity, when parity is enabled by CR13 and/or CR15.

Bit 5
A logic 1 selects the Synchronous Character mode. A logic 0 selects the Asynchronous Character mode.

Bits 6-7
These bits select the full character length (including parity, if selected) as shown above. When parity is enabled it must be considered as a bit when making character length selection (5 bits plus parity = 6 bits).

Status Register

The data contained in the Status Register define Receiver and Transmitter data conditions and status of the Data Set.

7	6	5	4	3	2	1	0
• Data Set Change	• Data Set Ready (DSR)	• Carrier Detector	• Framing Error • Syn Detect	• DLE Detect • Parity Error	• Overrun Error	• Data Received (DR)	• Transmitter Buffer Empty (TBMT)

Bit 0
A logic 1 indicates that the Transmitter Buffer may be loaded with new data. It is set to a logic 1 when the contents of the Transmitter Buffer is transferred to the Transmitter Register. It is cleared when the Transmitter Buffer is loaded from the DAL bus, or when the Transmitter is disabled.

Bit 1
A logic 1 indicates that an entire character has been received and transferred into the Receiver Buffer. It is cleared when the Receiver Buffer is read onto the DAL bus, or the Receiver is disabled.

Bit 2
A logic 1 indicates an Overrun error which occurs if the previous character in the Receiver Buffer has not been read and Data Received is not reset, at the time a new character is to be transferred to the Receiver Buffer. This bit is cleared when no Overrun condition is detected (the next character transfer time) or when the Receiver is disabled.

Bit 3
When the DLE Strip is enabled (CR14) the Receiver parity check is disabled and this bit is set to a logic 1 if the previous character to the presently assembled character matched the contents of the DLE register; otherwise it is cleared. The DLE DET remains for one character time and is reset on the next character transfer or on a Status Register Read. If DLE Strip is not enabled this bit is set to a logic 1 when the Receiver is enabled, Receiver parity (CR13) is also enabled, and the last received character has a Parity error. A logic 0 on this bit indicates correct parity. This bit is cleared in both modes when the Receiver is disabled.

Bit 4

Asynchronous Mode

A logic 1 indicates that the received data did not have a valid stop bit, while the Receiver was enabled, which indicates a Framing error. This bit is set to a logic 0 if the stop bit (logic 1) was detected.

Synchronous Mode

A logic 1 indicates that the contents of the Receiver Register matches the contents of the SYN Register. The condition of this bit remains for a full character assembly time. If SYN strip (CR23) is enabled this status bit is updated with the character received after the SYN character.

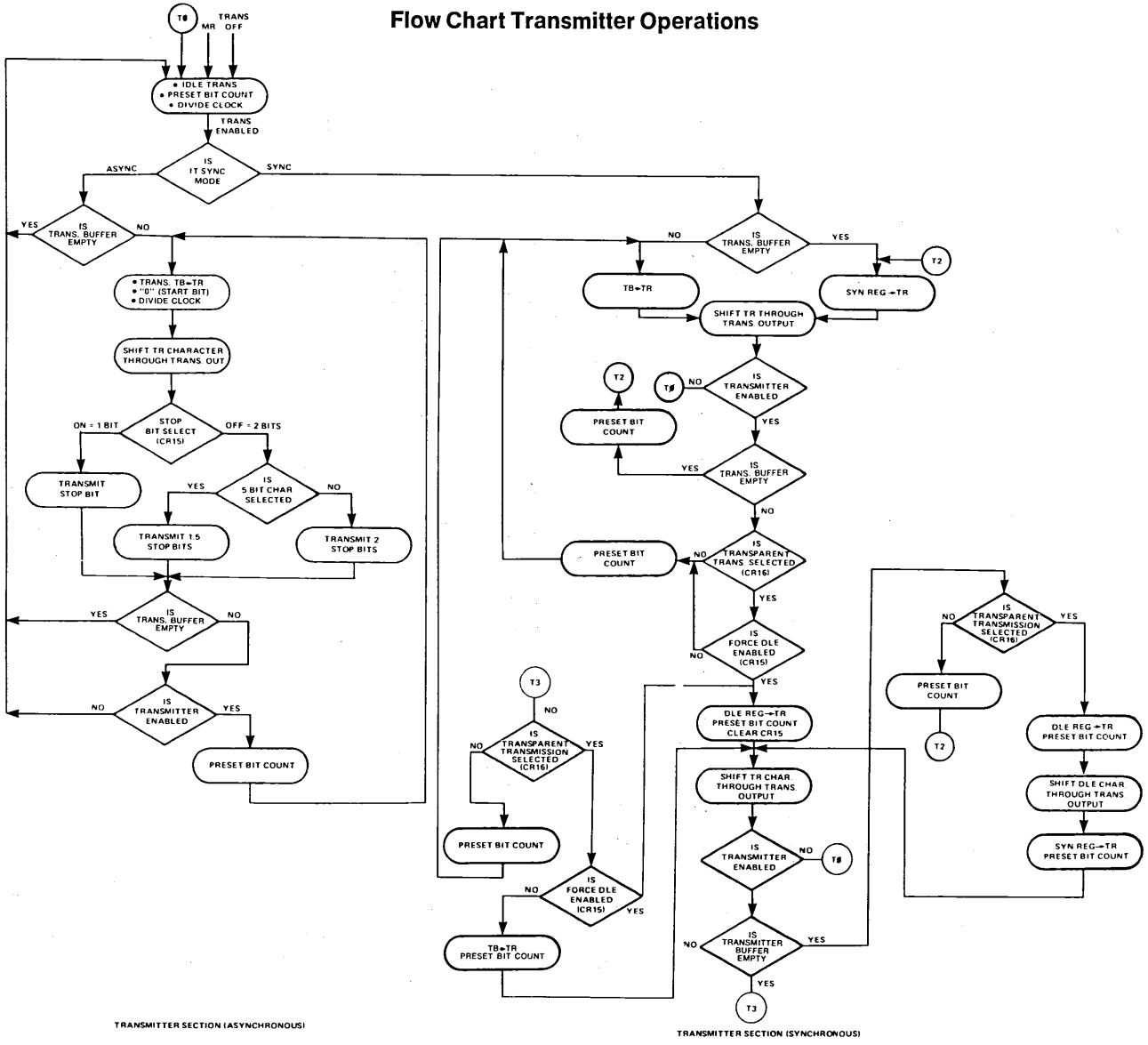
In both modes the bit is cleared when the Receiver is disabled.

Bit 5
This bit is the logic complement of the $\overline{\text{Carrier Detector}}$ input on Pin 29.

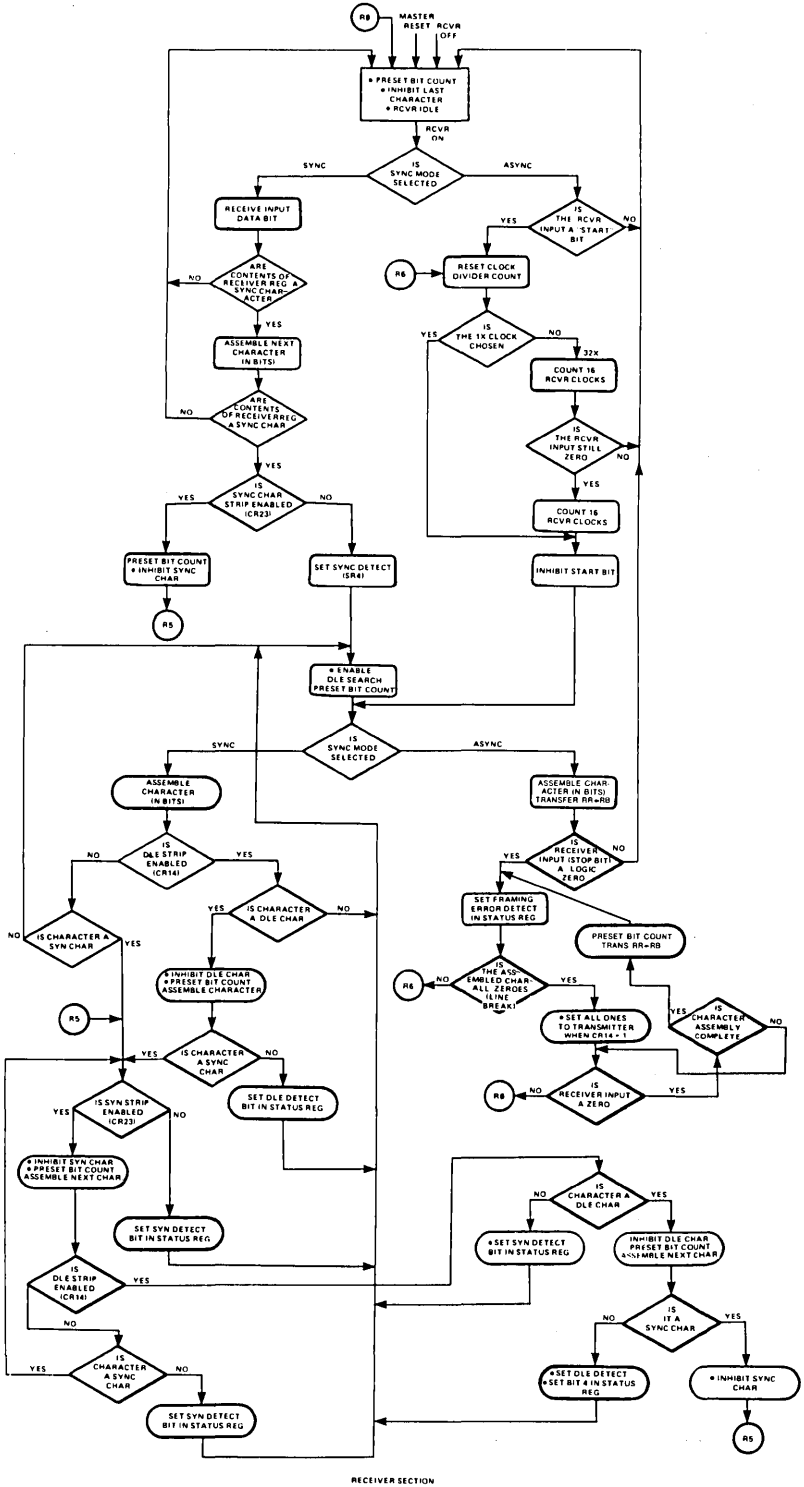
Bit 6
This bit is the logic complement of the $\overline{\text{Data Set Ready}}$ input on Pin 28. With 202-type Data Sets it can be used for Secondary Receive.

Bit 7
This bit is set to a logic 1 whenever there is a change in state of the $\overline{\text{Data Set Ready}}$ or $\overline{\text{Carrier Detector}}$ inputs while Data Terminal Ready (CR10) is a logic 1 or the $\overline{\text{Ring Indicator}}$ is turned ON, with DTR a logic 0. This bit is cleared when the Status Register is read onto the DAL bus.

Flow Chart Transmitter Operations

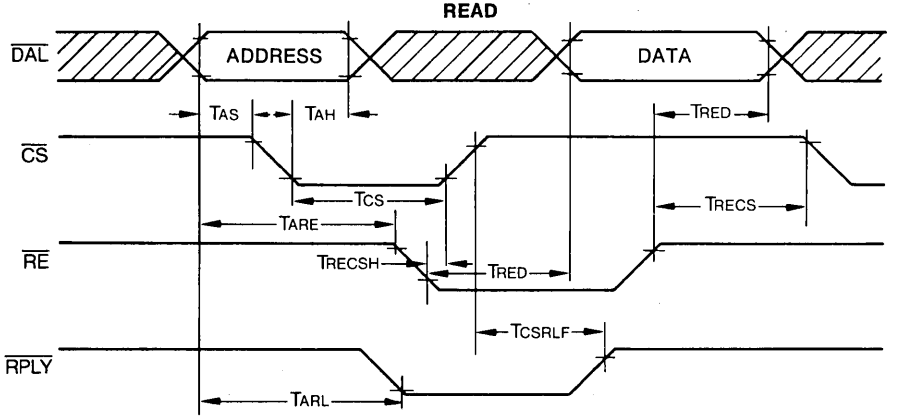


Flow Chart Receiver Operations

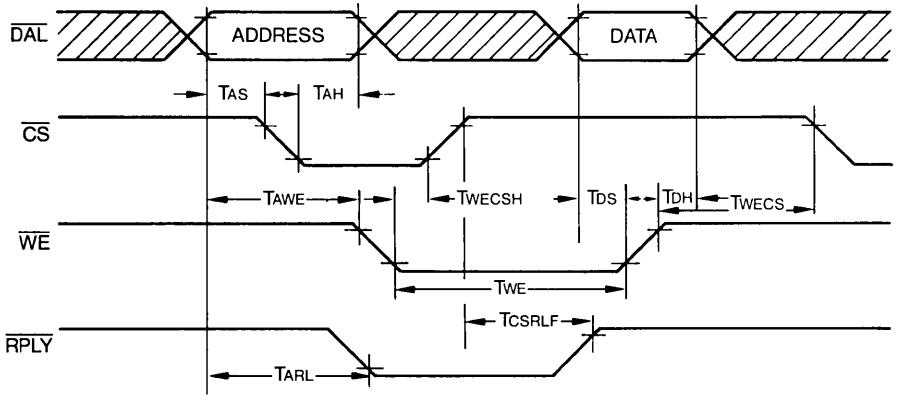


RECEIVER SECTION

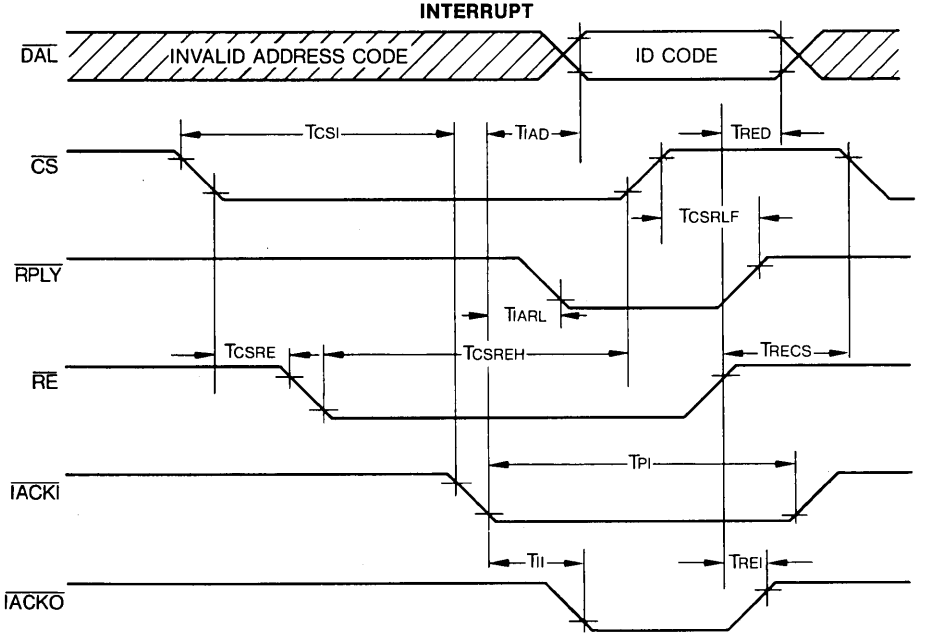
READ



WRITE



INTERRUPT



MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +18.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = +12V ±5%, V_{BB} = −5V ±5%, V_{SS} = 0V, unless otherwise noted)

Parameter		Min	Typ.	Max.	Unit	Comments
D.C. Characteristics						
INPUT VOLTAGE LEVELS						
Low Level, V_{IL}				0.8	V	
High Level, V_{IH}		2.4			V	
OUTPUT VOLTAGE LEVELS						
Low Level, V_{OL}			0.4		V	I_{OL} = 1.6ma
High Level, V_{OH}		2.4				I_{OH} = 100 μa
INPUT LEAKAGE						
Data Bus			5.0	10.0	μa	0≤V_{IN}≤5 v
All others			5.0	10.0	μa	V_{IN} = +12v
POWER SUPPLY CURRENT						
I_{CC}				80.0	ma	
I_{DD}				10.0	ma	
I_{BB}				1.0	ma	
A.C. Characteristics						T_A = 25°C
CLOCK-RCP, TCP						
frequency			1.0		MHz	
DAL Bus						
T_{AS}	Address Set-Up Time	0			ns	
T_{AH}	Address Hold Time	150			ns	
T_{ARL}	Address to $\overline{RPLY}$ Delay			400	ns	
T_{CS}	$\overline{CS}$ Width	250			ns	
T_{CSRLF}	$\overline{CS}$ to Reply OFF Relay	0		250	ns	R_L = 2.7 KΩ
Read						
T_{ARE}	Address and $\overline{RE}$ Spacing	250			ns	
T_{RECSH}	$\overline{RE}$ and $\overline{CS}$ Overlap	20			ns	
T_{RECS}	$\overline{RE}$ to $\overline{CS}$ Spacing	250			ns	
T_{RED}	$\overline{RE}$ to Data Out Delay			180	ns	C_L = 20 pf
Write						
T_{AWE}	Address to $\overline{WE}$ Spacing	250			ns	
T_{WECSH}	$\overline{WE}$ and $\overline{CS}$ Overlap	20			ns	
T_{WE}	$\overline{WE}$ Width	200		1000	ns	
T_{DS}	Data Set-Up Time	150			ns	
T_{DH}	Data Hold Time	100			ns	
T_{WECS}	$\overline{WE}$ to $\overline{CS}$ Spacing	250			ns	
Interrupt						
T_{CSI}	$\overline{CS}$ to $\overline{IACKI}$ Delay	0			ns	
T_{CSRE}	$\overline{CS}$ to $\overline{RE}$ Delay	250			ns	
T_{CSREH}	$\overline{CS}$ and $\overline{RE}$ Overlap	20			ns	
T_{RECS}	$\overline{RE}$ to $\overline{CS}$ Spacing	250			ns	
T_{PI}	$\overline{IACKI}$ Pulse Width	200			ns	
T_{IAD}	$\overline{IACKI}$ to Valid ID Code Delay			250	ns	See Note 1.
T_{RED}	$\overline{RE}$ OFF to $\overline{DAL}$ Open Delay			180	ns	
T_{IARL}	$\overline{IACKI}$ to $\overline{RPLY}$ Delay			250	ns	See Note 1.
T_{CSRLF}	$\overline{CS}$ to $\overline{RPLY}$ OFF Delay	0		250	ns	R_L = 2.7 KΩ
T_{II}	$\overline{IACKI}$ to $\overline{IACKO}$ Delay			200	ns	
T_{REI}	$\overline{RE}$ OFF to $\overline{IACKO}$ OFF Delay			250	ns	

Note 1: If $\overline{RE}$ goes low after $\overline{IACKI}$ goes low, the delay will be from the falling edge of $\overline{RE}$.

Multiple ASTRO System in Daisy-Chain Configuration