STANDARD MICROSYSTEMS CORPORATION

COM2601

Universal Synchronous Receiver/Transmitter USRT

SECTION III

FEATURES

- ☐ STR, BSC—Bi-sync and interleaved bi-sync modes of operation
- ☐ Fully Programmable—data word length, parity mode, receiver sync character, transmitter sync character
- ☐ Full or Half Duplex Operation—can receive and transmit simultaneously at different baud rates
- ☐ Fully Double Buffered—eliminates need for precise external timing
- ☐ Directly TTL Compatible—no interface components required
- ☐ Tri-State Data Outputs—bus structure oriented
- ☐ IBM Compatible—internally generated SCR and SCT signals
- ☐ High Speed Operation—250K baud, 200ns strobes
- ☐ Low Power—300mW
- ☐ Input Protected—eliminates handling problems
- ☐ Dip Package—easy board insertion

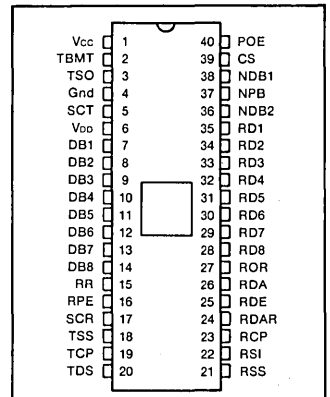
APPLICATIONS

- ☐ Bi-Sync Communications
- ☐ Cassette I/O
- ☐ Floppy Disk I/O

GENERAL DESCRIPTION

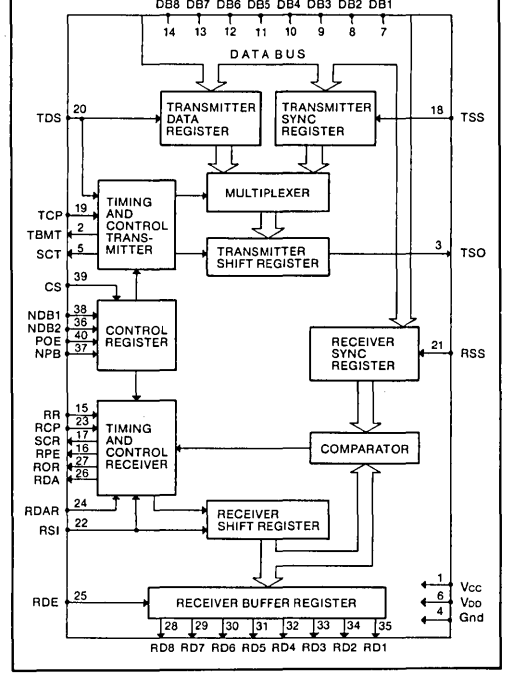
The Universal Synchronous Receiver/Transmitter is an MOS/LSI monolithic circuit that performs all the receiving and transmitting functions associated with synchronous (STR, BSC, Bi-sync, and interleaved bi-sync) data communications. This circuit is fabricated using SMC's P-channel low voltage oxide-nitride technology, allowing all inputs and outputs to be directly TTL compatible. The duplex mode, baud rate, data word length, parity mode, receiver sync character, and transmitter sync character are independently programmable through the use of external controls. The USR/T is fully double buffered and internally generates the sync character received and sync character transmitted signals. These programmable features provide the user with the ability to interface with all synchronous peripherals.

PIN CONFIGURATION



PACKAGE: 40-Pin D.I.P.

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	FUNCTION
1	V_{CC}	Power Supply	+5 volt Supply
2	TBMT	Transmitter Buffer Empty	This output is at a high-level when the transmitter data buffer register may be loaded with new data.
3	TSO	Transmitter Serial Output	This output serially provides the entire transmitted character. This character is extracted from the transmitter data buffer register provided that a TDS pulse occurs during the presently transmitted character. If TDS is not pulsed, the next transmitted character will be extracted from the transmitter sync register.
4	GND	Ground	Ground
5	SCT	Sync Character Transmitted	This output is set high when the character loaded into the transmitter shift register is extracted from the transmitter sync register, indicating that the TDS was not pulsed during the previously transmitted character. This output is reset low when the character to be transmitted is extracted from the transmitter data buffer register. This can only occur if TDS is pulsed.
6	V_{DD}	Power Supply	−12 volt Supply
7-14	DB1-DB8	Data Bus Inputs	This 8 bit bus inputs information into the receiver sync register under control of the RSS strobe, into the transmitter sync register under control of the TSS strobe, and into the transmitter data buffer register under control of the TDS strobe. The strobes operate independently of each other. Unused bus inputs may be in either logic state. The LSB should always be placed on DB1.
15	RR	Receiver Reset	This input should be pulsed to a high-level after power turn-on. This resets the RDA, SCR, ROR, and RPE outputs to a low-level. The transition of the RR input from a high-level to a low-level sets the receiver into the search mode (bit phase). In the search mode the serially received data bit stream is examined on a bit by bit basis until a sync character is found. A sync character is found, by definition, when the contents of the receiver sync register and the receiver shift register are identical. When this occurs the SCR output is set high. This character is then loaded into the receiver buffer register and the receiver is set into the character mode. In this mode each character received is loaded into the receiver buffer register.
16	RPE	Receiver Parity Error	This output is a high-level if the received character parity bit does not agree with the selected parity.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	FUNCTION
17	SCR	Sync Character Received	This output is set high each time the character loaded into the receiver buffer register is identical to the character in the receiver sync register. This output is reset low the next time the receiver buffer register is loaded with a character which is not a sync character.
18	TSS	Transmitter Sync Strobe	A high-level input strobe loads the character on the DB1-DB8 lines into the transmitter sync register.
19	TCP	Transmitter Clock	The positive going edge of this clock shifts data out of the transmitter shift register, at a baud rate equal to the TCP clock frequency.
20	TDS	Transmitter Data Buffer Strobe	A high-level input strobe loads the character on the DB1-DB8 lines into the transmitter data buffer register.
21	RSS	Receiver Sync Strobe	A high-level input strobe loads the character on the DB1-DB8 lines into the receiver sync register.
22	RSI	Receiver Serial Input	This input accepts the serial bit input stream.
23	RCP	Receiver Clock	The negative-going edge of this clock shifts data into the receiver shift register, at a baud rate equal to the RCP clock frequency.
24	RDAR	Receiver Data Available Reset	A high-level input resets the RDA output to a low-level.
25	RDE	Received Data Enable	A high-level input enables the outputs (RD8-RD1) of the receiver buffer register
26	RDA	Receiver Data Available	This output is at a high-level when an entire character has been received and transferred into the receiver buffer register.
27	ROR	Receiver Over-Run	This output is at a high-level if the previously received character is not read (RDA not reset) before the present character is transferred into the receiver buffer register.
28-35	RD8-RD1	Receiver Data Output	These are the 8 tri-state data outputs enabled by RDE. Unused data output lines, as selected by NDB1 and NDB2, have a low level output, and received characters are right justified, i.e. the LSB always appears on the RD1 output.
36, 38	NDB2, NDB1	Number of Data Bits	These 2 inputs are internally decoded to select either 5, 6, 7, or 8 data bits/character as per the following truth table: NDB2 NDB1 data bits/character L L 5 L H 6 H L 7 H H 8

DESCRIPTION OF PIN FUNCTIONS

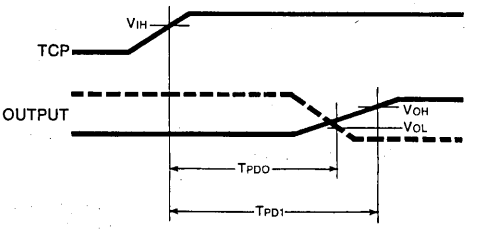
PIN NO.	SYMBOL	NAME	FUNCTION
37	NPB	No Parity Bit	A high-level input eliminates the parity bit from being transmitted. In addition, it is necessary that the received character contain no parity bit. Also, the RPE output is forced to a low-level. See pin 40, POE.
39	CS	Control Strobe	A high-level input enters the control bits (NDB1, NDB2, POE, and NPB) into the control bits register. This line may be strobed or hard wired to a high-level.
40	POE	Odd/Even Parity Select	The logic level on this input, in conjunction with the NPB input, determines the parity mode for both the reciever and transmitter, as per the following table:

NPB	POE	MODE
L	L	odd parity
L	H	even parity
H	X	no parity

X = don't care

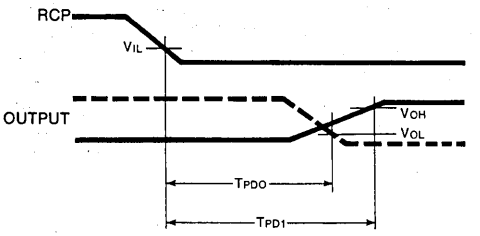
ADDITIONAL TIMING INFORMATION
(Typical Propagation Delays)

Transmitter

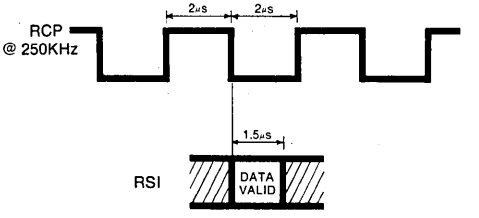


OUTPUT	TPDO	TPD1	UNITS
TBMT	NA	2.0	μs
SCT	1.0	1.5	μs
TSO	1.0	1.0	μs

Receiver



OUTPUT	TPDO	TPD1	UNITS
RDA	NA	1.0	μs
ROR	2.0	2.5	μs
RPE	2.0	2.5	μs
SCR	2.0	2.5	μs
RD1-RD8	2.5	2.5	μs



MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, V_{CC} ..... +0.3V
Negative Voltage on any Pin, V_{CC} ..... −25 V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS (T_A = 0° C to 70° C, V_{CC} = +5V ±5%, V_{DD} = −12V ±5%, unless otherwise noted)

Parameter	Min	Typ	Max	Unit	Conditions
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}	V_{DD}		0.8	V	
High-level, V_{IH}	V_{CC}-1.5		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}		0.2	0.4	V	I_{OL} = 1.6mA
High-level, V_{OH}	2.4	4.0		V	I_{OH} = −100μA
INPUT CURRENT					
Low-level, I_{IL}			1.6	mA	see note 1
OUTPUT CURRENT					
Leakage, I_{LO}			−1	μA	RDE = V_{IL}, O ≤ V_{OUT} ≤ +5V
Short circuit, I_{OS}**			10	mA	V_{OUT} = 0V
INPUT CAPACITANCE					
All inputs, C_{IN}		5	10	pf	V_{IN} = V_{CC}, f = 1MHz
OUTPUT CAPACITANCE					
All outputs, C_{OUT}		10	20	pf	R_{DE} = V_{IL}, f = 1MHz
POWER SUPPLY CURRENT					
I_{CC}			28	mA	All outputs = V_{OH}
I_{DD}			28	mA	
A.C. CHARACTERISTICS					T_A = +25° C
CLOCK FREQUENCY	DC		250	KHz	RCP, TCP
PULSE WIDTH					
Clock	1			μs	RCP, TCP
Receiver reset	1			μs	RR
Control strobe	200			ns	CS
Transmitter data strobe	200			ns	TDS
Transmitter sync strobe	200			ns	TSS
Receiver sync strobe	200			ns	RSS
Receiver data available reset	200			ns	RDAR
INPUT SET-UP TIME					
Data bits	>0			ns	DB1-DB8
Control bits	>0			ns	NPB, NDB2, NDB1, POE
INPUT HOLD TIME					
Data bits	>0			ns	DB1-DB8
Control bits	>0			ns	NPB, NDB2, NDB1, POE
STROBE TO OUTPUT DELAY					Load = 20pf +1 TTL input
Receive data enable		180	250	ns	RDE: T_{PD1}, T_{PD0}
OUTPUT DISABLE DELAY		100	250	ns	RDE

**Not more than one output should be shorted at a time.

NOTES:
1. Under steady state condition no current flows for TTL or MOS interfacing. A switching current of 1.6 mA maximum flows during a transition of the input.
2. The three-state output has 3 states:
   1) low impedance to V_{CC}
   2) low impedance to GND
   3) high impedance OFF ≅ 10M ohms
   The OFF state is controlled by the RDE input.

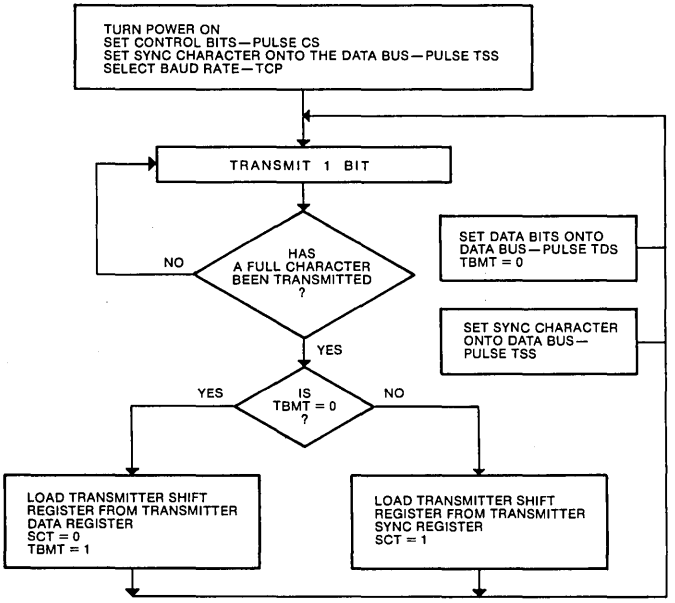
DESCRIPTION OF OPERATION—RECEIVER/TRANSMITTER

The input clock frequency for the receiver is set at the desired receiver baud rate and the desired receiver sync character (synchronous idle character) is loaded into the receiver sync register. When the Receiver Reset input transitions from a high-level to a low-level the receiver is set into the search mode (bit phase). In the search mode the serially received data bit stream is examined on a bit by bit basis until a sync character is found. A sync character is found, by definition, when the contents of the receiver sync register and the receiver shift register are identical. When this occurs the Sync Character Received output is set high. This character is then loaded into the receiver buffer register and the receiver is set into the character mode. In this mode each character received is loaded into the receiver buffer register. The receiver provides flags for Receiver Data Available, Receiver Over Run, Receiver Parity Error, and Sync Character Received. Full double buffering eliminates the need for precise external timing by allowing one full character time for received data to be read out.

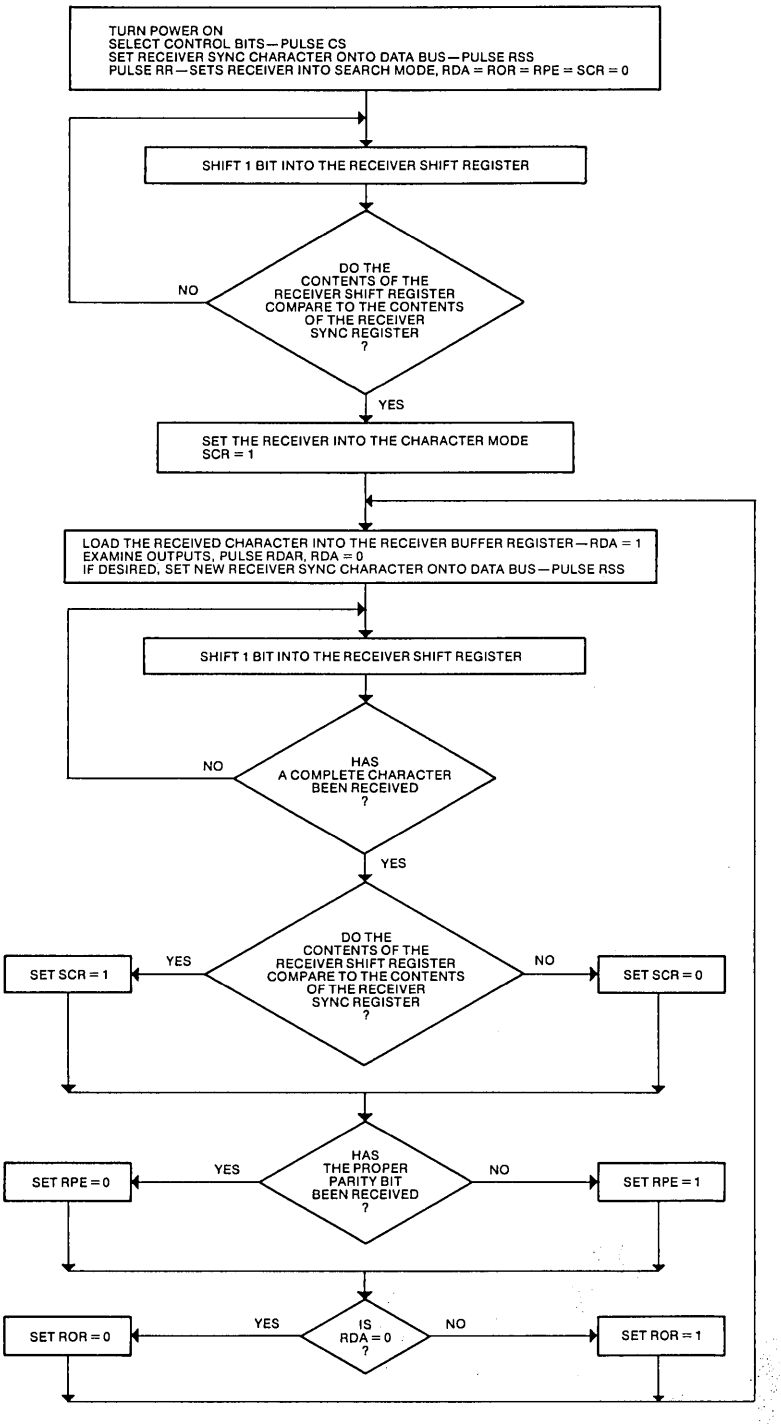
The input clock frequency for the transmitter is set at the desired baud rate and the desired transmitter sync character is loaded into the transmitter sync register. Internal logic decides if the character to be transmitted out of the transmitter shift register is extracted from the transmitter data register or the transmitter sync register. The next character transmitted is extracted from the transmitter data register provided that a Transmitter Data Strobe pulse occurs during the presently transmitted character. If the Transmitter Data Strobe is not pulsed, the next transmitted character is extracted from the transmitter sync register and the Sync Character Transmitted output is set to a high level. Full double buffering eliminates the need for precise external timing by allowing one full character time to load the next character to be transmitted.

There may be 5, 6, 7, or 8 data bits and odd/even or no parity bit. All inputs and outputs are directly TTL compatible. Tri-state data output levels are provided for the bus structure oriented signals. Input strobe widths of 200ns, output propagation delays of 250ns, and receiver/transmitter rates of 250K baud are achieved.

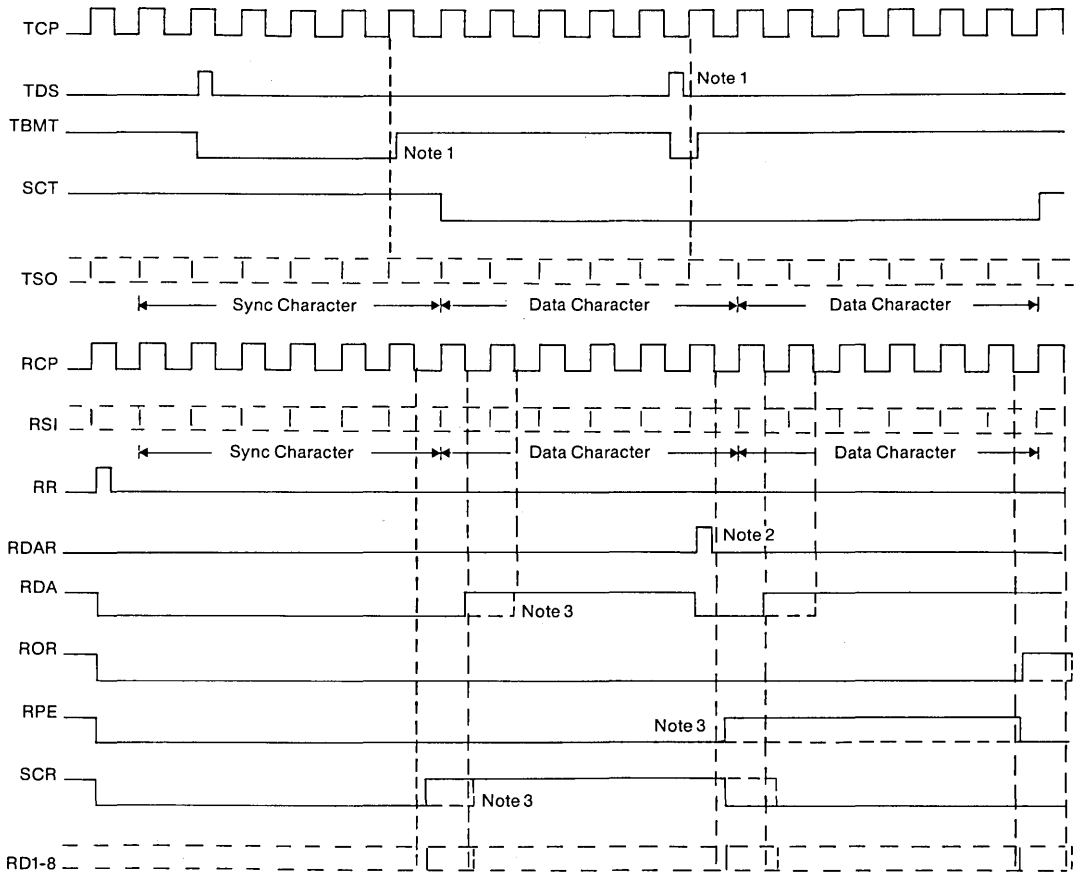
FLOW CHART—TRANSMITTER



FLOW CHART—RECEIVER



USRT TIMING DIAGRAM



NOTE 1
The transmitter shift register is loaded with the next character at the positive clock transition corresponding to the leading edge of the last bit of the current character on the TSO output. TBMT is set high approximately two microseconds after this clock transition. If it is desired that the next character be extracted from the transmitter data register the leading edge of the TDS should occur at least one microsecond prior to this clock transition.

NOTE 2
In order to avoid an ROR indication the leading edge of the RDAR pulse should occur at least one microsecond prior to the negative clock transition corresponding to the center of the first bit after the last data bit on the RSI input.

NOTE 3
The ROR, RPE, SCR and RD1-RD8 outputs are set to their correct levels approximately two microseconds after the negative clock transition corresponding to the center of the first bit after the last data bit on the RSI input. The RDA output is set high at the next negative clock transition.

The solid waveforms correspond to a control register setting of 5 data bits and a parity bit. The dashed waveforms are for a setting of 6 data bits and no parity bit.