STANDARD MICROSYSTEMS CORPORATION

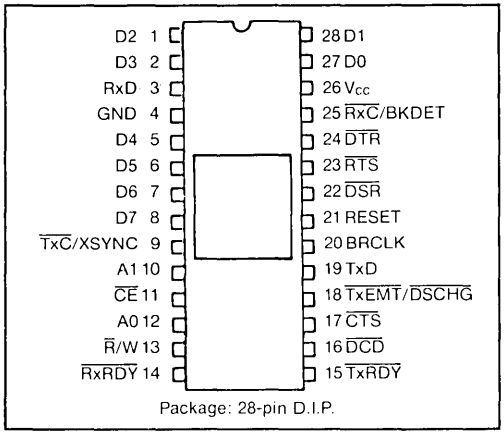
COM 2661-1
COM 2661-2
COM 2661-3
μPC FAMILY

Enhanced Programmable Communication Interface EPCI

FEATURES

- ☐ Synchronous and Asynchronous Full Duplex or Half Duplex Operations
- ☐ Re-programmable ROM on-chip baud rate generator
- ☐ Synchronous Mode Capabilities
  - —Selectable 5 to 8-Bit Characters
  - —Selectable 1 or 2 SYNC Characters
  - —Internal or External Character Synchronization
  - —Transparent or Non-Transparent Mode
  - —Transparent mode DLE stuffing (Tx) and detection (Rx)
  - —Automatic SYNC or DLE-SYNC Insertion
  - —SYNC, DLE and DLE-SYNC stripping
  - —Odd, Even, or No Parity
  - —Local or remote maintenance loop back mode
- ☐ Asynchronous Mode Capabilities
  - —Selectable 5 to 8-Bit Characters plus parity
  - —3 Selectable Clock Rates (1X, 16X, 64X the Baud Rate)
  - —Line Break Detection and Generation
  - —1, 1½, or 2-Stop Bit Detection and Generation
  - —False Start Bit Detection
  - —Odd, Even, or No Parity
  - —Parity, Overrun, and framing error detect
  - —Local or remote maintenance loop back mode
  - —Automatic serial echo mode (echoplex)
- ☐ Baud Rates
  - —DC to 1.0M Baud (Synchronous)
  - —DC to 1.0M Baud (1X, Asynchronous)
  - —DC to 62.5K Baud (16X, Asynchronous)
  - —DC to 15.625K Baud (64X, Asynchronous)

PIN CONFIGURATION



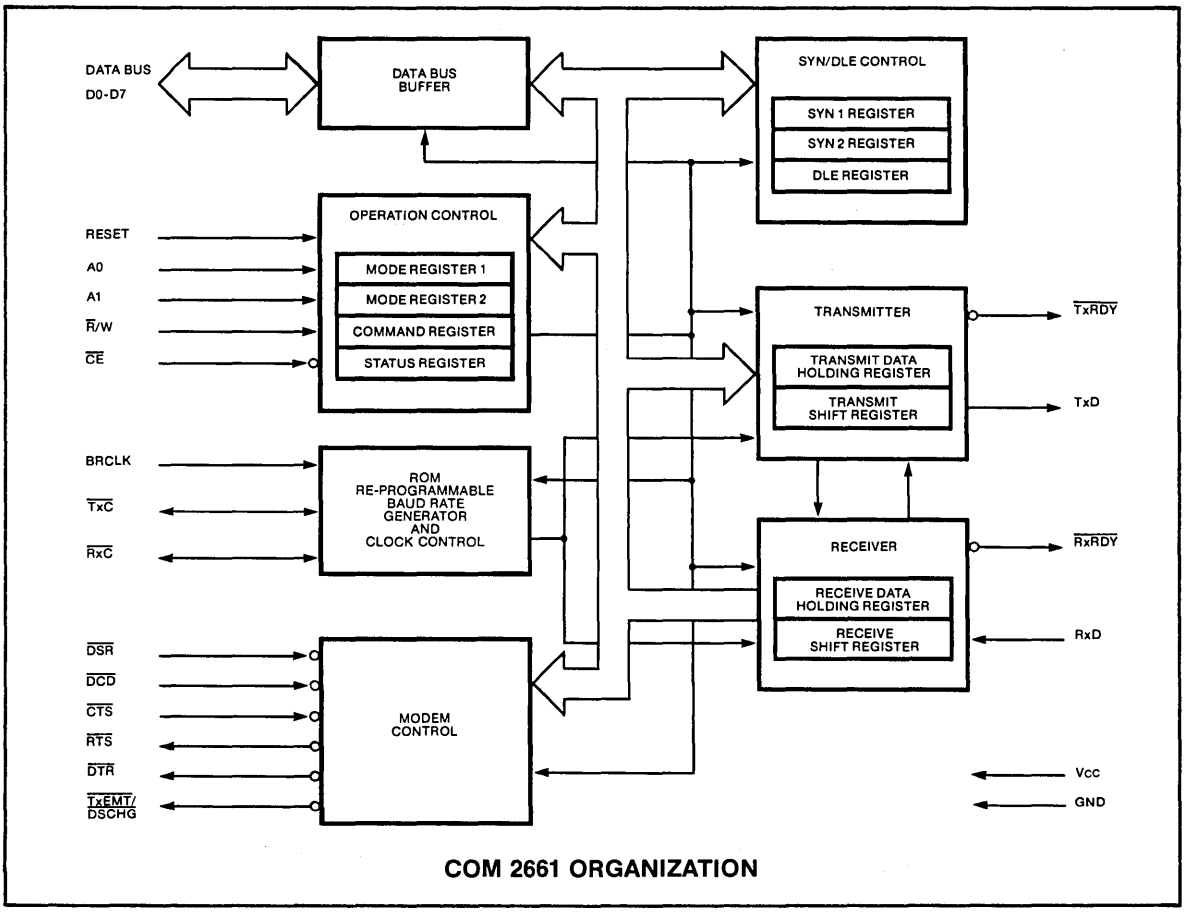
Package: 28-pin D.I.P.

- ☐ Double Buffering of Data
- ☐ RxC and TxC pins are short circuit protected
- ☐ Internal or External Baud Rate Clock
- ☐ 3 baud rate sets (2661-1, -2, -3)
- ☐ 16 internal rates for each version
- ☐ Single +5 volt Power Supply
- ☐ TTL Compatible
- ☐ No System Clock Required
- ☐ Compatible with EPCI 2661

GENERAL DESCRIPTION

The COM 2661 is an MOS/LSI device fabricated using SMC's patented COPLAMOS® technology. It is an enhanced pin and register compatible version of the COM 2651 that meets the majority of asynchronous and synchronous data communication requirements, by interfacing parallel digital systems to asynchronous and synchronous data communication channels while requiring a minimum of processor overhead. The COM2661 contains a baud rate generator which can be programmed to either accept an external clock or to generate internal transmit or receive clocks. Sixteen different baud rates can be selected under program control when operating in the internal clock mode. Each version of the COM 2661 (-1, -2, -3) has a different set of baud rates. Custom baud rates can be ROM reprogrammed to accommodate different baud rates and different starting frequencies.

The COM 2661 is a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) designed for microcomputer system data communications. The USART is used as a peripheral and is programmed by the processor to communicate in commonly used asynchronous and synchronous serial data transmission techniques including IBM Bi-Sync. The USART receives serial data streams and converts them into parallel data characters for the processor. While receiving serial data, the USART will also accept data characters from the processor in parallel format, convert them to serial format and transmit. The USART will signal the processor when it has completely received or transmitted a character and requires service. Complete USART status including data format errors and control signals is available to the processor at any time.



COM 2661 ORGANIZATION

The COM 2661 is organized into 6 major sections. Communication between each section is achieved via an internal data and control bus. The data bus buffer allows a processor access to all internal registers on the COM 2661. The differences between the COM 2661 and COM 2651 are outlined in table 1.

Operation Control

This functional block stores configuration and operation commands from the processor and generates appropriate signals to various internal sections to control the overall device operation. It contains read and write circuits to permit communications with a processor via the data bus and contains Mode Registers 1 and 2, the Command Register, and the Status Register. Details of register addressing and protocol are presented in the COM 2661 programming section of this specification.

Timing

The COM 2661 contains a Baud Rate Generator (BRG) which is programmable to accept external transmit or receive clocks or to divide an external clock to perform data communications. The unit can generate 16 commonly used baud rates, any one of which can be selected for full duplex operation. Tables 2a, b, and c illustrate all available baud rates.

Receiver

The Receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and stores the "assembled" character in the receive data holding register until read by the processor.

Transmitter

The Transmitter accepts parallel data from the processor, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin.

Modem Control

The modem control provides three output signals and accepts three input signals used for "handshaking" and status indication between the COM 2661 and a modem.

SYN/DLE Control

This section contains control circuitry and three 8-bit registers storing the SYN1, SYN2, and DLE characters provided by the processor. These registers are used in the synchronous mode of operation to provide the characters required for synchronization, idle fill and data transparency.

Interface Signals

The COM 2661 interface signals can be grouped into two types: the processor-related signals (shown in Table 3) which interface the COM 2661 to the processor, and the device-related signals (shown in Table 4), which are used to interface to the communications equipment.

TABLE 3—PROCESSOR RELATED SIGNALS

PIN NO.	NAME	SYMBOL	FUNCTION
1,2,5,6, 7,8,27,28	Data	D7-DØ	Bidirectional; 8 bit, three state data bus used to transfer commands, data and status between the COM 2661 and a processor. DØ is the least significant bit; D7 is the most significant bit.
10, 12	Address	A1, AØ	Input; Address lines used to select COM 2661 registers.
11	Chip Enable	$\overline{CE}$	Input; when this signal is low, the operation specified by the $\overline{R}$/W, A1 and AØ will be performed. When this input is high, D7-Ø are in the high impedance state.
13	Read/Write	$\overline{R}$/W	Input; Processor read/write direction control. This signal defines the direction of the data bus D7-0 when the COM 2661 is selected. D7-Ø drives out (read) when this signal is low and accepts data input when this signal is high. The input only has meaning when the $\overline{CE}$ input is active.
14	Receiver Ready	$\overline{RxRDY}$	Output; This signal is the complement of Status Register bit 1 (SR1). When low, it indicates that the Receive Data Holding Register (RHR) has a character ready for input to the processor. It goes high when the RHR is read by the processor, and also when the receiver is disabled. It is an open drain output which can be used as an interrupt to the processor.
15	Transmitter Ready	$\overline{TxRDY}$	Output; This signal is the complement of Status Register bit 0 (SR0). When low, it indicates that the Transmit Data Holding Register (THR) is ready to accept a data character from the processor. It goes high when the data character is loaded. This output is valid only when the transmitter is enabled. It is an open drain output which can be used as an interrupt to the processor.
18	Transmitter empty/data set change	$\overline{TxEMT}$/ $\overline{DSCHG}$	Output; This signal is the complement of Status Register bit 2 (SR2). When low, it indicates that the transmitter has completed serialization of the last character loaded by the processor, or that a change of state of the $\overline{DSR}$ or $\overline{DCD}$ inputs has occurred. This output goes high when the Status Register is read by the processor, if the TxEMT condition does not exist. Otherwise, the THR must be loaded by the processor for this line to go high. It is an open drain output which can be used as an interrupt to the processor.
21	Reset	Reset	Input; A high on this input performs a master reset on the COM 2661. This signal asynchronously terminates any device activity and clears the Mode, Command and Status registers. The device assumes the idle state and remains there until initialized with the appropriate control words.
26	Supply Voltage	V_{CC}	+5 volts supply.
4	Ground	GND	Ground.

TABLE 4—DEVICE RELATED SIGNALS

PIN NO.	NAME	SYMBOL	FUNCTION
3	Receive Date	RxD	Input; Serial data to the receiver. "Mark" is high "space" is low.
9	Transmitter Clock/External Sync	$\overline{TxC}$/ XSYNC	Input or Output; If the external transmitter clock is programmed, this input controls the rate at which the character is transmitted. Its frequency is 1X, 16X or 64X, the Baud rate as programmed by Mode Register 1. The transmitted data changes on the falling edge of the clock. If the internal transmitter clock is programmed, this pin can be a 1X/16X clock output or an external jam synchronization input.
16	Data Carrier Detect	$\overline{DCD}$	Input; This signal must be low in order for the receiver to function. The complement appears in the Status Register bit 6 (SR6). $\overline{DCD}$ causes a low output on $\overline{TxEMT/DSCHG}$ when its state changes if CR2 or CR0=1. If $\overline{DCD}$ goes high while receiving, the RxC is internally inhibited.
17	Clear to Send	$\overline{CTS}$	Input; This signal must be low in order for the transmitter to function. If it goes high during transmission, the character in the Transmit Shift Register will be transmitted before termination.
19	Transmit Data	TxD	Output; Serial data from the transmitter. "Mark" is high, "Space" is low. This signal is held in the "Mark" condition when the transmitter is disabled.
20	Baud Rate Clock	BRCLK	Input; Clock input to the internal baud rate generator (See Tables 2a, b and c); not required if the external receiver and transmitter clocks are used.
22	Data Set Ready	$\overline{DSR}$	Input; This general purpose signal can be used for Data Set Ready or Ring Indicator condition. Its complement appears as Status Register bit 7 (SR7). $\overline{DSR}$ causes a low output on $\overline{TxEMT/DSCHG}$ when its state changes if CR2 or CR0=1.
23	Request to Send	$\overline{RTS}$	Output; This general purpose signal is the complement of the Command Register bit 5 (CR5). It is normally used to indicate Request to Send. If the Transmit Shift Register is not empty when CR5 is reset (1 to 0), then $\overline{RTS}$ will go high on TxC time after the last serial bit is transmitted.
24	Data Terminal Ready	$\overline{DTR}$	Output; This general purpose signal is the complement of the Command Register bit 1 (CR1). It is normally used to indicate Data Terminal Ready.
25	Receive Clock/ Break Detect	$\overline{RxC}$/ BKDET	Input or Output; If the external receiver clock is programmed, this input controls the rate at which the character is to be received. Its frequency is 1X, 16X, or 64X the Baud rate, as programmed by Mode Register 1. Data are sampled on the rising edge of the clock. If internal receiver clock is programmed, this pin can be a 1X/16X clock or a break detect output.

Table 1 COM 2661 vs. COM 2651

FEATURE	EPCI	PCI
1. MR2 Bit 6, 7	Control pin 9, 25	Not used
2. DLE detect-SR3	SR3 = 0 for DLE-DLE, DLE-SYNC1	SR3 = 1 for DLE-DLE, DLE-SYNC1
3. Reset of SR3, DLE detect	Second character after DLE; or receiver disable, or CR4 = 1	Receiver disable, or CR4 = 1
4. Send DLE-CR3	One time command	Reset via CR3 on next TxRDY
5. DLE stuffing in transparent mode	Automatic DLE stuffing when DLE is loaded except if CR3 = 1	None
6. SYNC1 stripping in double sync non-transparent mode	All SYNC1	First SYNC1 of pair
7. Baud rate versions	Three	One
8. Terminate ASYNC transmission (drop RTS)	Reset CR5 in response to TxRDY changing from 0 to 1	Reset CR0 when TxEMT goes from 1 to 0. Then reset CR5 when TxEMT goes from 0 to 1
9. Break detect	Pin 25[1]	FE and null character
10. Stop bit searched	One	Two
11. External jam sync	Pin 9[2]	No
12. Data bus timing	Improved over 2651	—
13. Data bus drivers	Sink 2.2mA Source 400μA	Sink 1.6mA Source 100μA

NOTES
1. Internal BRG used for RxC.
2. Internal BRG used for TxC.

Table 2a BAUD RATE GENERATOR CHARACTERISTICS 2661-1 (BRCLK = 4.9152MHz)

MR23-20	BAUD RATE	ACTUAL FREQUENCY 16X CLOCK	PERCENT ERROR	DIVISOR
0000	50	0.8kHz	—	6144
0001	75	1.2	—	4096
0010	110	1.7598	−0.01	2793
0011	134.5	2.152	—	2284
0100	150	2.4	—	2048
0101	200	3.2	—	1536
0110	300	4.8	—	1024
0111	600	9.6	—	512
1000	1050	16.8329	0.196	292
1001	1200	19.2	—	256
1010	1800	28.7438	−0.19	171
1011	2000	31.9168	−0.26	154
1100	2400	38.4	—	128
1101	4800	76.8	—	64
1110	9600	153.6	—	32
1111	19200	307.2	—	16

Table 2b BAUD RATE GENERATOR CHARACTERISTICS 2661-2 (BRCLK = 4.9152MHz)

MR23-20	BAUD RATE	ACTUAL FREQUENCY 16X CLOCK	PERCENT ERROR	DIVISOR
0000	45.5	0.7279kHz	0.005	6752
0001	50	0.8	—	6144
0010	75	1.2	—	4096
0011	110	1.7598	−0.01	2793
0100	134.5	2.152	—	2284
0101	150	2.4	—	2048
0110	300	4.8	—	1024
0111	600	9.6	—	512
1000	1200	19.2	—	256
1001	1800	28.7438	−0.19	171
1010	2000	31.9168	−0.26	154
1011	2400	38.4	—	128
1100	4800	76.8	—	64
1101	9600	153.6	—	32
1110	19200	307.2	—	16
1111	38400	614.4	—	8

Table 2c BAUD RATE CHARACTERISTICS 2661-3 (BRCLK = 5.0688MHz)

MR23-20	BAUD RATE	ACTUAL FREQUENCY 16X CLOCK	PERCENT ERROR	DIVISOR
0000	50	0.8kHz	—	6336
0001	75	1.2	—	4224
0010	110	1.76	—	2880
0011	134.5	2.1523	0.016	2355
0100	150	2.4	—	2112
0101	300	4.8	—	1056
0110	600	9.6	—	528
0111	1200	19.2	—	264
1000	1800	28.8	—	176
1001	2000	32.081	0.253	158
1010	2400	38.4	—	132
1011	3600	57.6	—	88
1100	4800	76.8	—	66
1101	7200	115.2	—	44
1110	9600	153.6	—	33
1111	19200	316.8	3.125	16

NOTE:
16X clock is used in asynchronous mode. In synchronous mode, clock multiplier is 1X and BRG can be used only for TxC.

COM 2661 OPERATION

The functional operation of the COM 2661 is programmed by a set of control words supplied by the processor. These control words specify items such as synchronous or asynchronous mode, baud rate, number of bits per character, etc. The programming procedure is described in the COM 2661 Programming section of this data sheet.

After programming, the COM 2661 is ready to perform the desired communications functions. The receiver performs serial to parallel conversion of data received from a modem or equivalent device. The transmitter converts parallel data received from the processor to a serial bit stream. These actions are accomplished within the framework specified by the control words.

Receiver

The COM 2661 is conditioned to receive data when the $\overline{DCD}$ input is low and the RxEN bit in the command register is true. In the asynchronous mode, the receiver looks for a high to low (mark to space) transition of the start bit on the RxD input line. If a transition is detected, the state of the RxD line is sampled again after a delay of one-half of a bit time. If RxD is now high, the search for a valid start bit is begun again. If RxD is still low, a valid start bit is assumed and the receiver continues to sample the input line at one bit time intervals until the proper number of data bits, the parity bit, and one stop bit have been assembled. The data is then transferred to the Receive Data Holding Register, the RxRDY bit in the status register is set, and the $\overline{RxRDY}$ output is asserted. If the character length is less than 8 bits, the high order unused bits in the Holding Register are set to zero. The Parity Error, Framing Error, and Overrun Error status bits are strobed into the status register on the positive going edge of $\overline{RxC}$ corresponding to the received character boundary. If the stop bit is present, the receiver will immediately begin its search for the next start bit. If the stop bit is absent (framing error), the receiver will interpret a space as a start bit if it persists into the next bit time interval. If a break condition is detected (RxD is low for the entire character as well as the stop bit), only one character consisting of all zeros (with the Framing error status bit set) will be transferred to the Holding Register. The RxD input must return to a high condition before a search for the next start bit begins.

Pin 25 can be programmed to be a break detect output by appropriate setting of MR27-MR24. If so, a detected break will cause that pin to go high. When RxD returns to mark for one RxC time, pin 25 will go low. Refer to the break detection timing diagram.

When the COM 2661 is initialized into the synchronous mode, the receiver first enters the hunt mode on a 0 to 1 transition of RxEN (CR2). In this mode, as data is shifted into the Receiver Shift Register a bit at a time, the contents of the register are compared to the contents of the SYN1 register. If the two are not equal, the next bit is shifted in and the comparison is repeated. When the two registers match, the hunt mode is terminated and character assembly begins. If the single SYN operation is programmed, the SYN DETECT status bit is set. If double SYN operation is programmed, the first character assembled after SYN1 must be SYN2 in order for the SYN DETECT bit to be set. Otherwise, the COM 2661 returns to the hunt mode. (Note that the sequence SYN1-SYN1-

SYN2 will not achieve synchronization). When synchronization has been achieved, the COM 2661 continues to assemble characters and transfers them to the Holding Register. The RxRDY status bit is set and the RxRDY output is asserted each time a character is assembled and transferred to the Holding Register. The Overrun error (OE) and Parity error (PE) status bits are set as appropriate. Further receipt of the proper SYN sequence sets the SYN DETECT status bit. If the SYN stripping mode is commanded, SYN characters are not transferred to the Holding Register. Note that the SYN characters used to establish initial synchronization are not transferred to the Holding Register in any case.

External jam synchronization can be achieved via pin 9 by appropriate setting of MR27-MR24. When pin 9 is an XSYNC input, the internal SYN1, SYN1-SYN2, and DLE-SYN1 detection is disabled. Each positive going signal on XSYNC will cause the receiver to establish synchronization on the rising edge of the next RxC pulse. Character assembly will start with the RxD input at this edge. XSYNC may be lowered on the next rising edge of RxC. This external synchronization will cause the SYN DETECT status bit to be set until the status register is read. Refer to XSYNC timing diagram.

Transmitter

The COM 2661 is conditioned to transmit data when the CTS input is low and the TxEN command register bit is set. The COM 2661 indicates to the processor that it can accept a character for transmission by setting the TxRDY status bit and asserting the TxRDY output. When the processor writes a character into the Transmit Data Holding Register, the TxRDY status bit is reset and the TxRDY output is returned to a high (false) state. Data is transferred from the Holding Register to the Transmit Shift Register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again. Thus, one full character time of buffering is provided.

In the asynchronous mode, the transmitter automatically sends a start bit followed by the programmed number of data bits, the least significant bit being sent first. It then appends an optional odd or even parity bit and the programmed number of stop bits. If, following transmission of the data bits, a new character is not available in the Transmit Holding Register, the TxD output remains in the marking (high) condition and the TxEMT/DSCHG output and its corresponding status bit are asserted. Transmission resumes when the processor loads a new character into the Holding Register. The transmitter can be forced to output a continuous low (BREAK) condition by setting the Send Break command bit high.

In the synchronous mode, when the COM 2661 is initially conditioned to transmit, the TxD output remains high and the TxRDY condition is asserted until the first character to be transmitted (usually a SYN character) is loaded by the processor. Subsequent to this, a continuous stream of characters is transmitted. No extra bits (other than parity, if commanded) are generated by the COM 2661 unless the processor fails to send a new character to the COM 2661 by the time the transmitter has completed sending the previous character. Since synchronous communication does not allow gaps between characters, the COM 2661 asserts TxEMT and automatically "fills" the gap by transmitting SYN1s, SYN1-SYN2 doublets, or DLE-SYN1 doublets, depending on the state of MR16 and MR17. Normal transmission of the message resumes when a new character is available in the Transmit Data Holding Register. If the SEND DLE bit in the command register is true, the DLE character is automatically transmitted prior to transmission of the message character in the transmit holding register.

COM 2661 PROGRAMMING

Prior to initiating data communications, the COM 2661 operational mode must be programmed by performing write operations to the mode and command registers. In addition, if synchronous operation is programmed, the appropriate SYN/DLE registers must be loaded. The COM 2661 can be reconfigured at any time during program execution. A flow chart of the initialization process appears in Figure 1.

The internal registers of the COM 2661 are accessed by applying specific signals to the CE, R/W, A1 and A0 inputs. The conditions necessary to address each register are shown in Table 5.

The SYN1, SYN2, and DLE registers are accessed by performing write operations with the conditions A1=0, A0=1, and R/W=1. The first operation loads the SYN1 register. The next loads the SYN2 register, and the third loads the DLE register. Reading or loading the mode registers is done in a similar manner. The first write (or read) operation addresses Mode Register 1, and a subsequent operation addresses Mode Register 2. If more

COM 2661 INITIALIZATION FLOW CHART

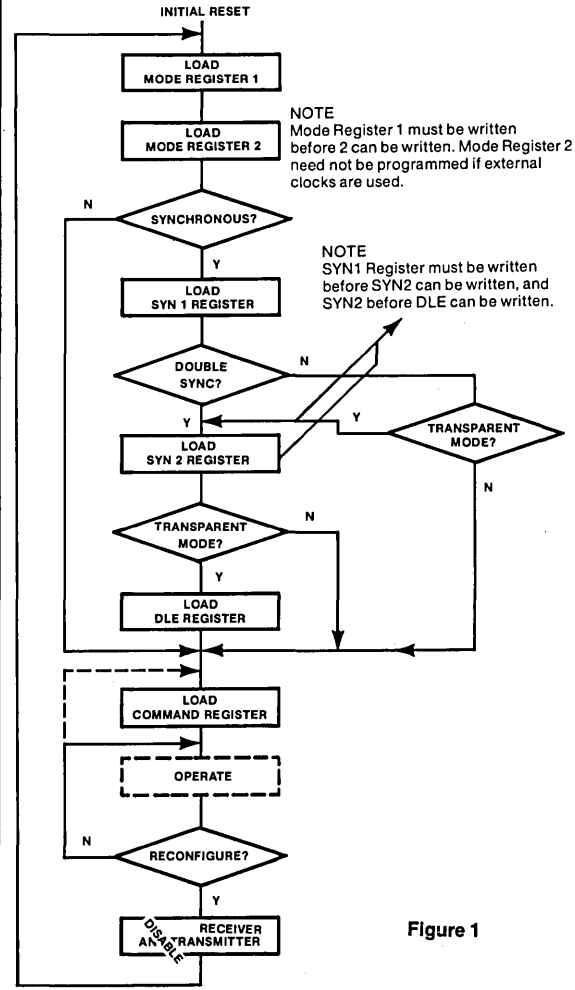


Figure 1

than the required number of accesses are made, the internal sequencer recycles to point at the first register. The pointers are reset to SYN1 Register and Mode Register 1 by a RESET input or by performing a "Read Command Register" operation, but are unaffected by any other read or write operation.

The COM 2661 register formats are summarized in Tables 6, 7, 8 and 9. Mode Registers 1 and 2 define the general operational characteristics of the COM 2661, while the Command Register controls the operation within this basic framework. The COM 2661 indicates its status in the Status Register. These registers are cleared when a RESET input is applied.

$\overline{CE}$	A1	A0	$\overline{R}$/W	FUNCTION
1	X	X	X	Tri-state data bus
0	0	0	0	Read receive holding register
0	0	0	1	Write transmit holding register
0	0	1	0	Read status register
0	0	1	1	Write SYN1/SYN2/DLE registers
0	1	0	0	Read mode registers 1 and 2
0	1	0	1	Write mode registers 1 and 2
0	1	1	0	Read command register
0	1	1	1	Write command register

NOTE
See AC Characteristics section for timing requirements.

Table 5—COM 2661 REGISTER ADDRESSING

MODE REGISTER 1 (MR1)

Table 6 illustrates Mode Register 1. Bits MR11 and MR10 select the communication format and Baud rate multiplier. 00 specifies synchronous mode and 1X multiplier. 1X, 16X, and 64X multipliers are programmable for asynchronous format. However, the multiplier in asynchronous format applies only if the external clock input option is selected by MR24 or MR25.

MR13 and MR12 select a character length of 5, 6, 7, or 8 bits. The character length does not include the parity bit, if programmed, and does not include the start and stop bits in asynchronous mode.

MR14 controls parity generation. If enabled, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR15 selects odd or even parity when parity is enabled by MR14.

In asynchronous mode, MR17 and MR16 select character framing of 1, 1.5, or 2 stop bits (if 1X baud rate is programmed, 1.5, stop bits defaults to 1 stop bits on transmit). In synchronous mode, MR17 controls the number of SYN characters used to establish synchronization and for character fill when the transmitter is idle. SYN1 alone is used if MR17=1, and SYN1-SYN2 is used when MR17=0. If the transparent mode is specified by MR16, DLE-SYN1 is used for character fill and SYN Detect, but the normal synchronization sequence is used. When transmitting, a DLE character in the transmit holding register will cause a second DLE character to be transmitted. This DLE stuffing eliminates the software DLE compare and stuff on each transparent mode data character. If the send DLE command (CR3) is active when a DLE is loaded into THR, only one additional DLE will be transmitted. Also DLE stripping and DLE Detect (with MR14=0) are enabled.

MR17	MR16	MR15	MR14	MR13	MR12	MR11	MR10
Sync/Async		Parity Type	Parity Control	Character Length		Mode and Baud Rate Factor	
ASYNCH: STOP BIT LENGTH 00=INVALID 01=1 STOP BIT 10=1½ STOP BITS 11=2 STOP BITS		0=ODD 1=EVEN	0=DISABLED 1=ENABLED	00=5 BITS 01=6 BITS 10=7 BITS 11=8 BITS		00=SYNCHRONOUS 1X RATE 01=ASYNCHRONOUS 1X RATE 10=ASYNCHRONOUS 16X RATE 11=ASYNCHRONOUS 64X RATE	
SYNCH: NUMBER OF SYN CHAR 0=DOUBLE SYN 1=SINGLE SYN	SYNCH: TRANSPARENCY CONTROL 0=NORMAL 1=TRANSPARENT						

NOTE Baud rate factor in asynchronous applies only if external clock is selected. Factor is 16X if internal clock is selected. Mode must be selected (MR11, MR10) in any case.

TABLE 6—MODE REGISTER 1 (MR1)

MODE REGISTER 2 (MR2)

Table 7 illustrates mode register 2 (MR23, MR22, MR21 and MR20 control the frequency of the internal baud rate generator (BRG). Sixteen rates are selectable for each COM 2661 version (-1, -2, -3). Version 1 and 2 specify a 4.9152 MHz TTL input at BRCLK (pin 20); version 3 specifies a 5.0688 MHz input which is identical to the COM 2651. MR23-20 are don't cares if external clocks are selected (MR25-24=0). The individual rates are given in table 2a, b and c.

MR24-MR27 select the receive and transmit clock source (either the BRG or an external input) and the function at pins 9 and 25. Refer to table 7.

MR-27-MR24											MR23-MR20
	TxC	RxC	Pin 9	Pin 25		TxC	RxC	Pin 9	Pin 25	Mode	Baud Rate Selection
0000	E	E	TxC	RxC	1000	E	E	XSYNC[1]	RxC/TxC	sync	See baud rates in table 2
0001	E	I	TxC	1X	1001	E	I	TxC	BKDET	async	
0010	I	E	1X	RxC	1010	I	E	XSYNC[1]	RxC	sync	
0011	I	I	1X	1X	1011	I	I	1X	BKDET	async	
0100	E	E	TxC	RxC	1100	E	E	XSYNC[1]	RxC/TxC	sync	
0101	E	I	TxC	16X	1101	E	I	TxC	BKDET	async	
0110	I	E	16X	RxC	1110	I	E	XSYNC[1]	RxC	sync	
0111	I	I	16X	16X	1111	I	I	16X	BKDET	async	

NOTES
1. When pin 9 is programmed as XSYNC input, SYN1, SYN1-SYN2, and DLE-SYN1 detection is disabled.

E=External clock I=Internal clock (BRG)
1X and 16X are clock outputs

TABLE 7—MODE REGISTER 2 (MR2)

COMMAND REGISTER (CR)

Table 8 illustrates the Command Register. Bits CR0 (TxEN) and CR2 (RxEN) enable or disable the transmitter and receiver respectively. A 0 to 1 transition of CR2 forces start bit search (async mode) or hunt mode (sync mode) on the second $\overline{RxC}$ rising edge. Disabling the receiver causes $\overline{RxRDY}$ to go high (inactive). If the transmitter is disabled, it will complete the transmission of the character in the Transmit Shift Register (if any) prior to terminating operation. The TxD output will then remain in the marking state (high while the $\overline{TxRDY}$ and $\overline{TxEMT}$ will go high (inactive). If the receiver is disabled, it will terminate operation immediately. Any character being assembled will be neglected. Bits CR1 (DTR) and CR5 (RTS) control the $\overline{DTR}$ and $\overline{RTS}$ outputs. Data at the outputs are the logical complement of the register data.

In asynchronous mode, setting CR3 will force and hold the TxD output low (spacing condition) at the end of the current transmitted character. Normal operation resumes when CR3 is cleared. The TxD line will go high for at least one bit time before beginning transmission of the next character in the Transmit Data Holding Register. In synchronous mode, setting CR3 causes the transmission of the DLE register contents prior to sending the character in the Transmit Data Holding Register. Since this is a one time command, CR3 does not have to be reset by software. CR3 should be set when entering and exiting transparent mode and for all DLE—non-DLE character sequences.

Setting CR4 causes the error flags in the Status Register (SR3, SR4, and SR5) to be cleared. This is a one time command. There is no internal latch for this bit. When CR5 (RTS) is set, the $\overline{RTS}$ pin is forced low and the transmit serial logic is enabled. A 1 to 0 transition of CR5 will cause $\overline{RTS}$ to go high (inactive) one TxC time after the last serial bit has been transmitted (if the transmit shift register was not empty).

The COM 2661 can operate in one of four sub-modes within each major mode (synchronous or asynchronous). The operational sub-mode is determined by CR7 and CR6. CR7-CR6=00 is the normal mode, with the transmitter and receiver operating independently in accordance with the Mode and Status Register instructions.

In asynchronous mode, CR7-CR6=01 places the COM 2661 in the Automatic Echo mode. Clocked, regenerated received data are automatically directed to the TxD line while normal receiver operation continues. The receiver must be enabled (CR2=1), but the transmitter need not be enabled. Processor to receiver communications continue normally, but the processor to transmitter link is disabled. Only the first character of a break condition is echoed. The TxD output will go high until the next valid start is detected. The following conditions are true while in Automatic Echo mode:

1. Data assembled by the receiver are automatically placed in the Transmit Holding Register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receive clock.
3. $\overline{TxRDY}$ output=1.
4. The $\overline{TxEMT/DSCHG}$ pin will reflect only the data set change condition.
5. The TxEN command (CR0) is ignored.

In synchronous mode, CR7-CR6=01 places the COM 2661 in the Automatic SYN/DLE Stripping mode. The exact action taken depends on the setting of bits MR17 and MR16:

1. In the non-transparent, single SYN mode (MR17-MR16=10), characters in the data stream matching SYN1 are not transferred to the Receive Data Holding Register (RHR).
2. In the non-transparent, double SYN mode (MR17-MR16=00), characters in the data stream matching SYN1, or SYN2 if immediately preceded by SYN1, are not transferred to the RHR.
3. In transparent mode (MR16=1), characters in the data stream matching DLE, or SYN1 if immediately preceded by DLE, are not transferred to the RHR. However, only the first DLE of a DLE-DLE pair is stripped.

Note that Automatic Stripping mode does not affect the setting of the DLE Detect and SYN Detect status bits (SR3 and SR5).

Two diagnostic sub-modes can also be configured. In Local Loop Back mode (CR7-CR6=10), the following loops are connected internally:

1. The transmitter output is connected to the receiver input.
2. $\overline{DTR}$ is connected to $\overline{DCD}$ and $\overline{RTS}$ is connected to $\overline{CTS}$.
3. The receiver is clocked by the transmit clock.
4. The $\overline{DTR}$, $\overline{RTS}$ and $\overline{TxD}$ outputs are held high.
5. The $\overline{CTS}$, $\overline{DCD}$, $\overline{DSR}$ and RxD inputs are ignored.

Additional requirements to operate in the Local Loop Back mode are that CR0 (TxEN), CR1 (DTR), and CR5 (RTS) must be set to 1. CR2 (RxEN) is ignored by the COM 2661.

The second diagnostic mode is the Remote Loop Back mode (CR7-CR6=11). In this mode:

1. Data assembled by the receiver is automatically placed in the Transmit Holding Register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receive clock.
3. No data are sent to the local processor, but the error status conditions (PE, OE, FE) are set.
4. The $\overline{RxRDY}$, $\overline{TxRDY}$, and $\overline{TxEMT/DSCHG}$ outputs are held high.
5. CR1 (TxEN) is ignored.
6. All other signals operate normally.

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
Operating Mode		Request to Send	Reset Error	Sync/Async	Receive Control (RxEN)	Data Terminal Ready	Transmit Control (TxEN)
00=NORMAL OPERATION 01=ASYNCH: AUTOMATIC ECHO MODE SYNCH: SYN AND/OR DLE STRIPPING MODE 10=LOCAL LOOP BACK 11=REMOTE LOOP BACK		0 FORCE $\overline{RTS}$ OUTPUT HIGH ONE CLOCK TIME AFTER TxSR SERIALIZATION 1 FORCE $\overline{RTS}$ OUTPUT LOW	0=NORMAL 1=RESET ERROR FLAG IN STATUS (FE, OE, PE/DLE DETECT)	**ASYNCH: FORCE BREAK** 0=NORMAL 1=FORCE BREAK **SYNCH: SEND DLE** 0=NORMAL 1=SEND DLE	0=DISABLE 1=ENABLE	0=FORCE $\overline{DTR}$ OUTPUT HIGH 1=FORCE $\overline{DTR}$ OUTPUT LOW	0=DISABLE 1=ENABLE

TABLE 8—COMMAND REGISTER (CR)

STATUS REGISTER (SR)

The data contained in the Status Register (as shown in Table 9) indicate receiver and transmitter conditions and modem/data set status.

SR0 is the Transmitter Ready (TxRDY) status bit. It, and its corresponding output, are valid only when the transmitter is enabled. If equal to 0, it indicates that the Transmit Data Holding Register has been loaded by the processor and the data has not been transferred to the Transmit Shift Register. If set equal to 1, it indicates that the Holding Register is ready to accept data from the processor. This bit is initially set when the Transmitter is enabled by CR0, unless a character has previously been loaded into the Holding Register. It is not set when the Automatic Echo or Remote Loop Back modes are programmed. When this bit is set, the $\overline{\text{TxRDY}}$ output pin is low. In the Automatic Echo and Remote Loop Back modes, the output is held high.

SR1, the Receiver Ready (RxRDY) status bit, indicates the condition of the Receive Data Holding Register. If set,it indicates that a character has been loaded into the Holding Register from the Receive Shift Register and is ready to be read by the processor. If equal to zero, there is no new character in the Holding Register. This bit is cleared when the processor reads the Receive Data Holding Register or when the receiver is disabled by CR2. When set, the $\overline{\text{RxRDY}}$ output is low.

The TxEMT/DSCHG bit, SR2, when set, indicates either a change of state of the $\overline{\text{DSR}}$ or $\overline{\text{DCD}}$ inputs (when CR2 or CR0=1) or that the Transmit Shift Register has completed transmission of a character and no new character has been loaded into the Transmit Data Holding Register. Note that in synchronous mode this bit will be set even though the appropriate "fill" character is transmitted. TxEMT will not go active until at least one character has been transmitted. It is cleared by loading the Transmit Data Holding Register. The DSCHG condition is enabled when TxEN=1 or RxEN=1. It is cleared when the status register is read by the processor. If the status register is read twice and SR2=1 while SR6 and SR7 remain unchanged, then a TxEMT condition exists. When SR2 is set, the $\overline{\text{TxEMT/DSCHG}}$ output is low.

SR3, when set, indicates a received parity error when parity is enabled by MR14. In synchronous transparent mode (MR16=1), with parity disabled, it indicates that a character matching the DLE Register has been received, and the present character is neither SYN1 nor DLE. This bit is cleared when the next character following the above sequence is loaded into the Receive Data Holding Register, when the receiver is disabled, or by a reset error command, CR4.

The Overrun Error status bit, SR4, indicates that the previous character loaded into the Receive Holding Register was not read by the processor at the time a new received character was transferred into it. This bit is cleared when the receiver is disabled and by the Reset Error command, CR4.

In asynchronous mode, bit SR5 signifies that the received character was not framed by a stop bit, i.e., only the first stop bit is checked. If the RHR contains all 0's when SR5=1, a break condition is present. In synchronous non-transparent mode (MR16=0), it indicates receipt of the SYN1 character in single SYN mode or the SYN1-SYN2 pair in double SYN mode. In synchronous transparent mode (MR16=1), this bit is set upon detection of the initial synchronizing characters (SYN1 or SYN1-SYN2) and, after synchronization has been achieved, when a DLE-SYN1 pair is received. The bit is reset when the receiver is disabled, when the Reset Error command is given in asynchronous mode, or when the Status Register is read by the processor in the synchronous mode.

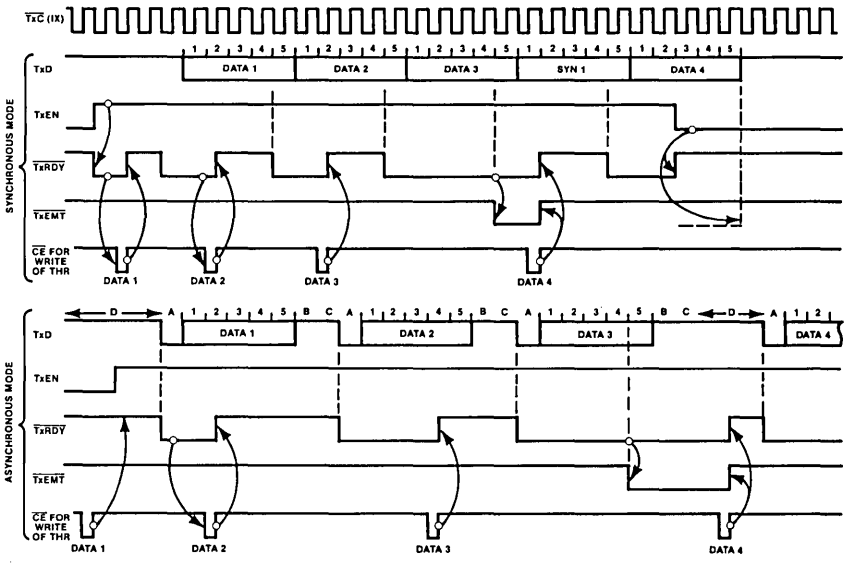
SR6 and SR7 reflect the conditions of the $\overline{\text{DCD}}$ and $\overline{\text{DSR}}$ inputs respectively. A low input sets the corresponding status bit and a high input clears it.

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
Data Set Ready	**Data Carrier Detect**	**FE/SYN Detect**	**Overrun**	**PE/DLE Detect**	**TxEMT/DSCHG**	**RxRDY**	**TxRDY**
0=$\overline{\text{DSR}}$ INPUT IS HIGH 1=$\overline{\text{DSR}}$ INPUT IS LOW	0=$\overline{\text{DCD}}$ INPUT IS HIGH 1=$\overline{\text{DCD}}$ INPUT IS LOW	**ASYNCH:** 0=NORMAL 1=FRAMING ERROR **SYNCH:** 0=NORMAL 1=SYN CHAR DETECTED	0=NORMAL 1=OVERRUN ERROR	**ASYNCH:** 0=NORMAL 1=PARITY ERROR **SYNCH:** 0=NORMAL 1=PARITY ERROR OR DLE CHAR RECEIVED	0=NORMAL 1=CHANGE IN $\overline{\text{DSR}}$ OR $\overline{\text{DCD}}$, OR TRANSMIT SHIFT REGISTER IS EMPTY	0=RECEIVE HOLDING REG EMPTY 1=RECEIVE HOLDING REG HAS DATA	0=TRANSMIT HOLDING REG BUSY 1=TRANSMIT HOLDING REG EMPTY

TABLE 9—STATUS REGISTER (SR)

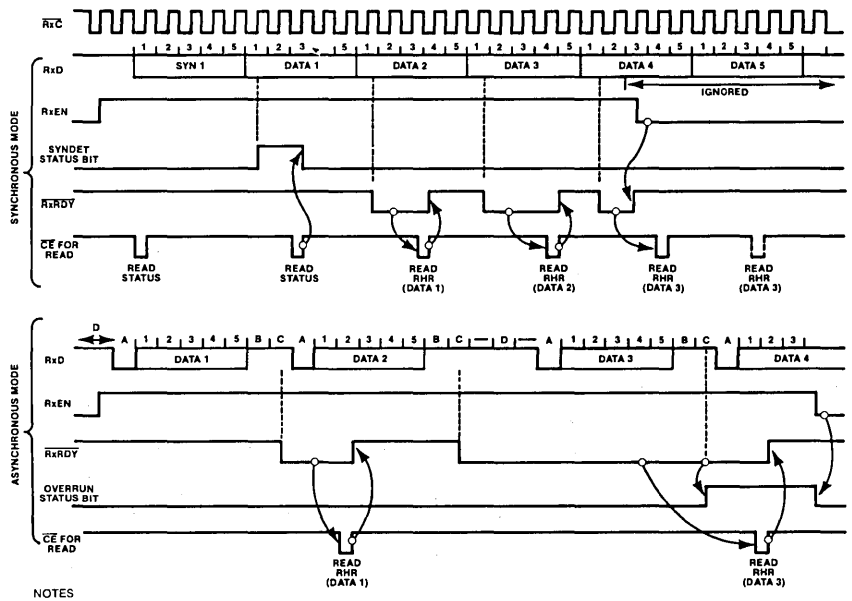
TIMING DIAGRAMS

TxRDY, TxEMT (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])



NOTES
A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition
TxEMT goes low at the beginning of the last data bit, or, if parity is enabled, at the beginning of the parity bit.

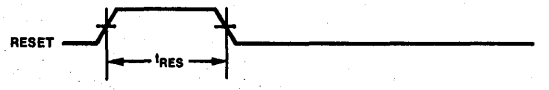
RxRDY (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])



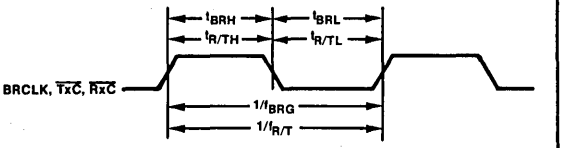
NOTES
A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition

TIMING DIAGRAMS (Cont'd)

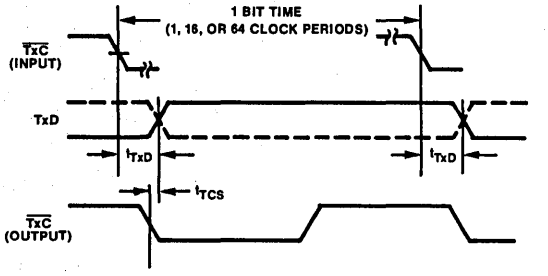
RESET



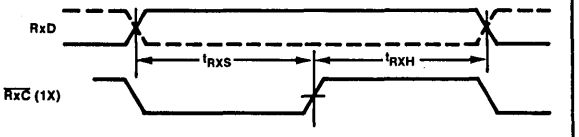
CLOCK



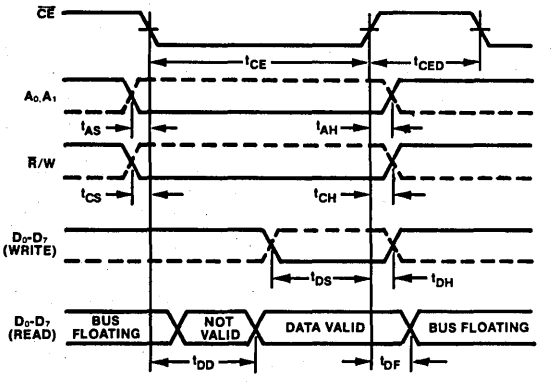
TRANSMIT



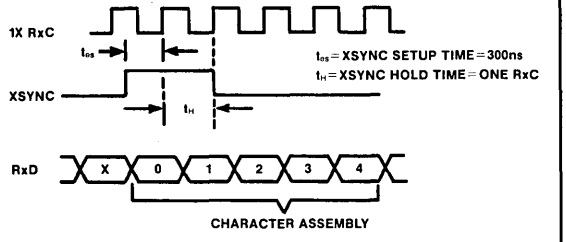
RECEIVE



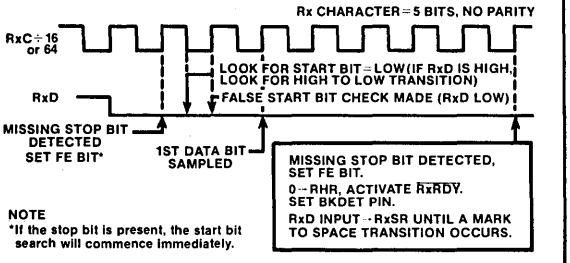
READ AND WRITE



EXTERNAL SYNCHRONIZATION WITH XSYNC



BREAK DETECTION TIMING



NOTE
*If the stop bit is present, the start bit search will commence immediately.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +18.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it it important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. For example, the bench power supply programmed to deliver +12 volts may have large voltage transients when the AC power is switched on and off. If this possibility exists it is suggested that a clamp circuit be used.

DC ELECTRICAL CHARACTERISTICS T_A=0°C to +70°C, V_{CC}=5.0V±5%

	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
	Input voltage					
V_{IL}	Low			0.8	V	
V_{IH}	High	2.0				
	Output voltage					
V_{OL}	Low			0.4	V	I_{OL}=2.2mA
V_{OH}	High	2.4				I_{OH}=−400μA
I_{IL}	Input leakage current			10	μA	V_{IN}=0 to 5.5V
	Output leakage current					
I_{LH}	Data bus high			10	μA	V_O=4.0V
I_{LL}	Data bus low			10	μA	V_O=0.45V
I_{CC}	Power supply current			150	mA	
	Capacitance					
C_{IN}	Input			20	pF	fc=1MHz
C_{OUT}	Output			20	pF	Unmeasured pins tied
$C_{I/O}$	Input/Output			20	pF	to ground

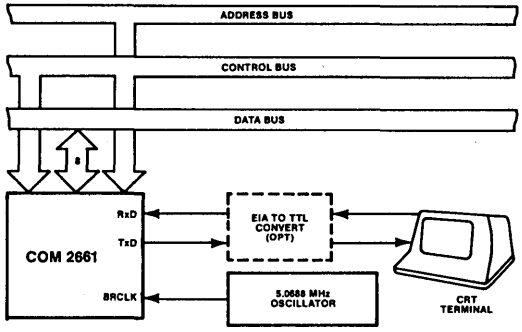
AC ELECTRICAL CHARACTERISTICS T_A=0°C to +70°C, V_{CC}=5.0V±5%

	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
	Pulse width					
t_{RES}	Reset	1000			ns	
t_{CE}	Chip enable	250			ns	
	Setup and hold time					
t_{AS}	Address setup	10			ns	
t_{AH}	Address hold	10			ns	
t_{CS}	R/W control setup	10			ns	
t_{CH}	R/W control hold	10			ns	
t_{DS}	Data setup for write	150			ns	
t_{DH}	Data hold for write	0			ns	
t_{RXS}	Rx data setup	300			ns	
t_{RXH}	Rx data hold	350			ns	
t_{DD}	Data delay time for read			200	ns	C_L=150pF
t_{DF}	Data bus floating time for read			100	ns	C_L=150pF
t_{CED}	$\overline{CE}$ to $\overline{CE}$ delay	600			ns	
	Input clock frequency					
f_{BRG}	Baud rate generator (2661-1, -2)	1.0	4.9152	4.9202	MHz	
f_{BRG}	Baud rate generator (2661-3)	1.0	5.0688	5.0738	MHz	
f_{RT}[1]	$\overline{TxC}$ or $\overline{RxC}$	dc		1.0	MHz	
	Clock width					
t_{BRH}	Baud rate high (2661-1, -2)	75			ns	f_{BRG}=4.915MHz; measured at V_{IH}
t_{BRH}	Baud rate high (2661-3)	70			ns	f_{BRG}=5.0688MHz; measured at V_{IH}
t_{BRL}	Baud rate low (2661-1, -2)	75			ns	f_{BRG}=4.915MHz; measured at V_{IL}
t_{BRL}	Baud rate low (2661-3)	70			ns	f_{BRG}=5.0688MHz; measured at V_{IL}
t_{RTH1}	$\overline{TxC}$ or $\overline{RxC}$ high	480			ns	
t_{RTL}	$\overline{TxC}$ or $\overline{RxC}$ low	480			ns	
t_{TXD}	TxD delay from falling edge of $\overline{TxC}$			650	ns	C_L=150pF
t_{TCS}	Skew between TxD changing and falling edge of $\overline{TxC}$ output		0		ns	C_L=150pF

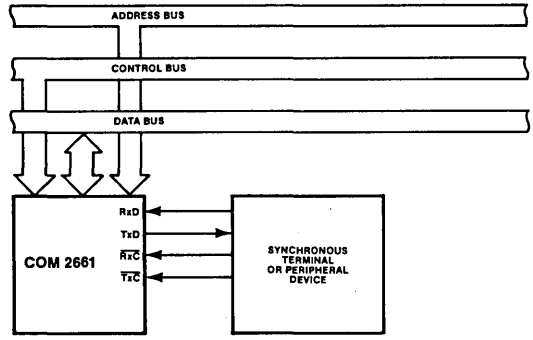
NOTE:
1. f_{RT} and t_{RTL} shown all modes except Local Loopback. For Local Loopback mode f_{RT}=0.7MHz and t_{RTL}=700ns min.

TYPICAL APPLICATIONS

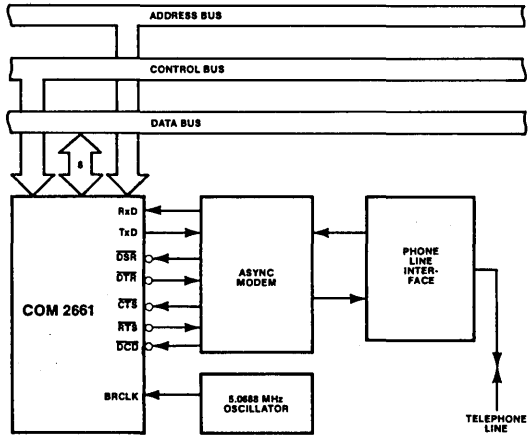
ASYNCHRONOUS INTERFACE TO CRT TERMINAL



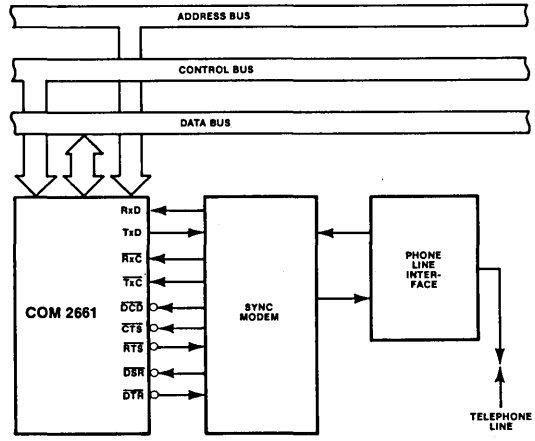
SYNCHRONOUS INTERFACE TO TERMINAL OR PERIPHERAL DEVICE



ASYNCHRONOUS INTERFACE TO TELEPHONE LINES



SYNCHRONOUS INTERFACE TO TELEPHONE LINES



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