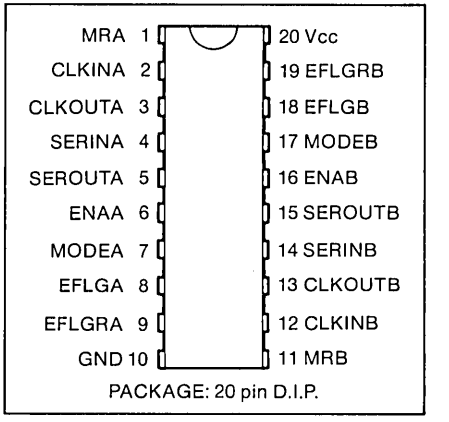
Dual 32 Bit CRC SDLC Generator/Checker CRC-32

FEATURES

- ☐ SDLC 32 bit CRC
- ☐ COM 5025 USYNRT Companion
- ☐ Data Rate—2MHz typical
- ☐ All Inputs and Outputs are TTL Compatible
- ☐ Single +5 Volt Supply
- ☐ COPLAMOS® N-Channel MOS Technology

PIN CONFIGURATION



PACKAGE: 20 pin D.I.P.

GENERAL DESCRIPTION

SMC's COM 8004 is a dual 32-bit CRC Generator/ Checker for use with SDLC protocols. It is a companion device to SMC's COM 5025 USYNRT. It operates at bit rates from DC to 2.0 MHz from a single +5v supply and is housed in a 20 lead x 0.3 inch DIP. All inputs and outputs are TTL compatible with full noise immunity.

The COM 8004 is comprised of two independent halves, and each half may be operated in the check or generate mode. The polynominal used in computations is:
$X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$.

The CRC register is initialized to all ones and the result is inverted before being appended to the message. The expected remainder is:
$X^{31} + X^{30} + X^{26} + X^{25} + X^{24} + X^{18} + X^{15} + X^{14} + X^{12} + X^{11} + X^{10} + X^8 + X^6 + X^5 + X^4 + X^3 + X + 1$.

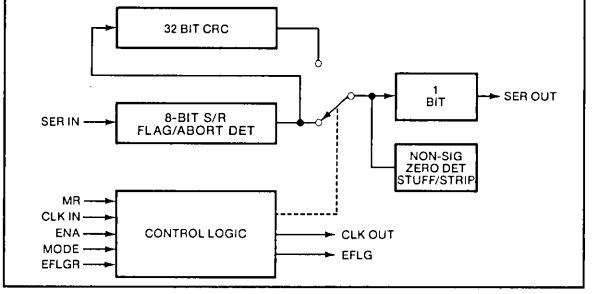
Each half has a nine-bit serial data shift register. Data moves on the positive edge of the clock, and all clocked inputs are designed for zero-hold-time (e.g. 7474). A "clock out" pin provides gated clocks to the accompanying USYNRT (COM 5025).

In the generate mode, computation is initiated upon detection of a flag character in the serial bit stream. CRC computation proceeds upon the serial data until a second flag is detected. CLK OUT to the SDLC transmitter is then halted, and the 32-bit CRC is passed out; CLK OUT is then resumed, and the flag character is passed out. Nonsignificant zeros are automatically stripped and stuffed, and shared flags are supported. If the data between flags is less than two full bytes, the CRC is discarded and the serial data stream remains unaltered.

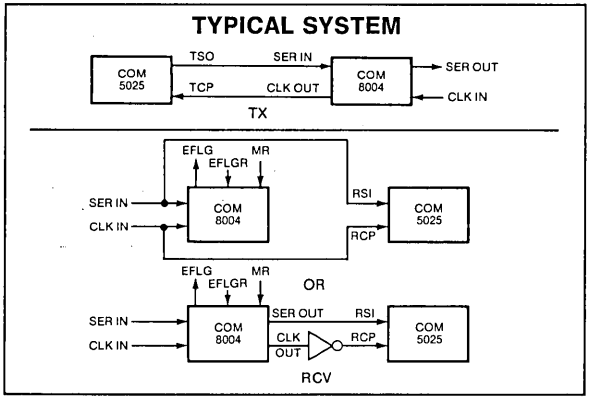
In the check mode, computation is similarly initiated upon detection of a flag. Detection of a second flag causes the conditional setting of the error flag. A separate reset pin is provided for the error flag. No error is flagged on messages of less than two full bytes between flags. Detection of an abort character (7 consecutive ones) in either mode causes computation to be reset and a search for an opening flag resumed.

BLOCK DIAGRAM

FOR ONE-HALF OF THE COM 8004



TYPICAL SYSTEM



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1	MASTER RESET-A	MRA	MRA presets the CRC calculation in Section A of the COM 8004 to all ones and forces the "pipeline" (8 shift register bits and the output flip-flop) to a logic "1" (Mark). The COM 8004 will only exit the reset state when MRA has been released and all 8 bits of a FLAG (01111110) have been received.
2	CLOCK INPUT-A	CLKINA	Baud Rate Clock for Section A.
3	CLOCK OUTPUT-A	CKLOUTA	Clock output from Section A. This is used to provide the clock for the USYNRT. CLKOUTA will normally track CLKINA. In the generate mode, when the last flag bit has been shifted into the shift register of the COM 8004, CLKOUTA will be held high until the CRC check character has been sent out. After the last bit of the CRC character is transmitted, CLKOUTA will resume tracking CLKINA.
4	SERIAL INPUT-A	SERINA	Serial input to the COM 8004 Section A. For transmission, SERINA is connected to the transmitter serial output of the USYNRT. For receiving, SERINA is connected to the received data output of the modem.
5	SERIAL OUTPUT-A	SEROUTA	Serial output from Section A of the COM 8004. For transmission, SEROUTA is connected to the transmit data input of the modem. For receiving, SEROUTA may be connected to the serial data input of the USYNRT.
6	ENABLE-A	ENAA	When ENAA is low, section A of the COM 8004 will pass data from SERINA to SEROUTA after a nine bit delay without alteration and without checking or generating CRC. If ENAA is high, CRC generation or checking will be enabled. ENAA is gated into the COM 8004 by the rising edge of CLKINA.
7	MODE SELECT-A	MODEA	MODEA determines whether Section A of the COM 8004 is in the receive (CRC check) Mode or transmit (CRC generate) Mode. Logic "1" selects CRC check. Logic "0" selects CRC generate.
8	ERROR FLAG-A	EFLGA	EFLGA will go high if, when in the CRC check mode, section A of the COM 8004 has detected an error. EFLGA can only be reset by a MASTER RESET (MRA) or by ERROR FLAG RESET (EFLGRA).
9	ERROR FLAG RESET-A	EFLGRA	A logic "1" on EFLGRA will reset EFLGA. If EFLGRA is kept at a logic "1," it will inhibit the setting of EFLGA.
10	GROUND	GND	Ground.
11	MASTER RESET-B	MRB	Master reset for Section B. See MRA for description.
12	CLOCK IN-B	CLKINB	Clock input for Section B. See CLKINA for description.
13	CLOCK OUT-B	CLKOUTB	Clock output for Section B. See CLKOUTA for description.
14	SERIAL INPUT-B	SERINB	Serial input for Section B. See SERINA for description.
15	SERIAL OUTPUT-B	SEROUTB	Serial output for Section B. See SEROUTA for description.
16	ENABLE-B	ENAB	CRC enable for Section B. See ENAA for description.
17	MODE SELECT-B	MODEB	Mode select for Section B. See MODEA for description.
18	ERROR FLAG-B	EFLGB	Error Flag for Section B. See EFLGA for description.
19	ERROR FLAG RESET-B	EFLGRB	Error flag reset for Section B. See EFLGRA for description.
20	POWER SUPPLY	V_{CC}	+5 volt power supply input.

OPERATION

The COM 8004 has 3 modes of operation, as selected by the ENABLE and MODE SELECT inputs. They are:

ENABLE	MODE SELECT	
0	0	CRC Disabled. Data is shifted from SERIN to SEROUT with no computation performed. Serial delay is 9 bit times.
0	1	Same as above.
1	0	CRC generation mode.
1	1	CRC check mode.

In the CRC generation and check modes, calculations begin upon receipt of the first data character after an opening FLAG. "Stuffed zeroes" are stripped for the purpose of the CRC calculation. CRC calculation will continue until either a MASTER RESET occurs, ENABLE is brought to logic zero, an ABORT character is received, or a closing FLAG is received.

CRC Generation

Upon detection of a closing FLAG character, CLKOUT is left high (stopping USYNRT activity), and the CRC accumulation is shifted out by CLKIN. CLKOUT then resumes clocking, and the FLAG (which has been stored in the shift register) is shifted out. The CRC check data is inverted before this data is transmitted. Zero-stuffing is performed on the inverted CRC check data.

During the time CKLOUT is forced high and CRC check data is being shifted out, data on SERIN will be ignored.

If an ABORT character is received, CRC calculation will cease after the last "1" bit of the ABORT character is shifted into the shift register. Data will pass through the COM 8004 without effect until a FLAG is received.

CRC Check (Reception)

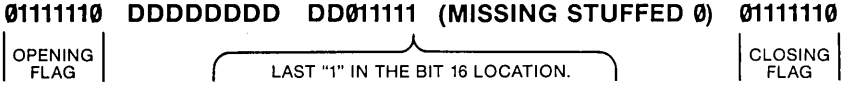
When the last bit of a closing flag enters the shift register, ERRCHK will go high on the following positive CLKIN transition if a CRC error is detected.

SECTION III

Operation Notes

Note 1: The minimum message size is sixteen significant bits following an opening flag. A stuffed zero is not considered a significant bit. If the message is less than 16 bits, the data will pass through the COM 8004 without being affected.

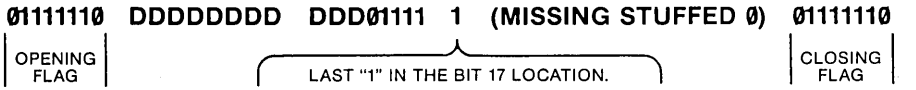
If the sixteenth received bit is the fifth consecutive one, but is not followed by a stuffed zero before a FLAG, the COM 8004 will detect the FLAG but the minimum message will not have occurred. CRC calculation will begin anew after this FLAG is detected.



Note 2: If the seventeenth bit of a message followed by a FLAG is the fifth consecutive one, but the stuffed zero is missing, the following will occur:

A) CRC Generate Mode: The last "one" bit, bit 17, will not be calculated into the CRC, but will appear at the serial output. The first bit of the CRC character will be forced to a zero, therefore looking like a stuffed zero.

B) CRC Check Mode: The last "one" bit, bit 17, will not be calculated into the CRC.



Note 3: If a stuffed zero is missing in the middle or end of a message, the reaction will depend on the next bit. If it is a one, a FLAG or ABORT may be detected. If an ABORT is detected, the message and the CRC checking is aborted. If a FLAG is detected, a CRC error will be detected.

If the missing zero is followed by a zero, the CRC computation will continue, but the zero bit will be stripped, causing a CRC error.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... -55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground .....-0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5 Volts ±5%, unless otherwise noted)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
DC CHARACTERISTICS						
Input Voltage Levels						
Low Level	V_{IL}			0.8	V	
High Level	V_{IH}	2.0			V	
Output Voltage Levels						
Low Level	V_{OL}			0.4	V	I_{OL} = 1.6 mA
High Level	V_{OH}	2.4			V	I_{OH} = -100 μA
Input Capacitance	C_{IN}		10	25	pf	
Power Supply Current	I_{CC}			100	mA	
AC CHARACTERISTICS						T_A = 25°C
Clock Frequency	f_{IN}			2	MHz	
Clock Pulse Width—High	t_{CLKH}	350			ns	Figure 1
Input Set-Up Time	t_{DC}	100			ns	Figure 1
Input Hold Time	t_{CD}	0			ns	Figure 1
Master Reset Pulse Width	t_{PW}	250			ns	Figure 2
Reset Delay	t_{MR}			250	ns	Figure 2
Error Flag Delay	t_{FD}			300	ns	Figure 3
Error Flag Reset Delay	t_{FR}			100	ns	Figure 4
ERRST Pulse Width	t_{EW}	100			ns	Figure 4
Clock Propagation Delay	t_{PD}			150	ns	Figure 5
SEROUT Propagation Delay	t_{SD}			150	ns	Figure 5

Figure 1

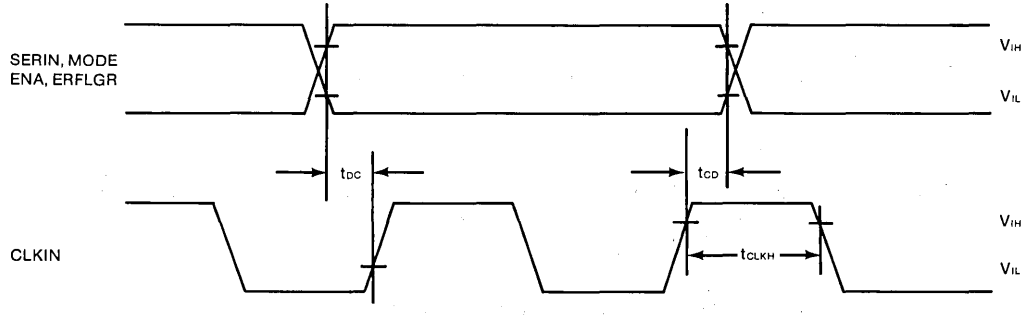


Figure 2

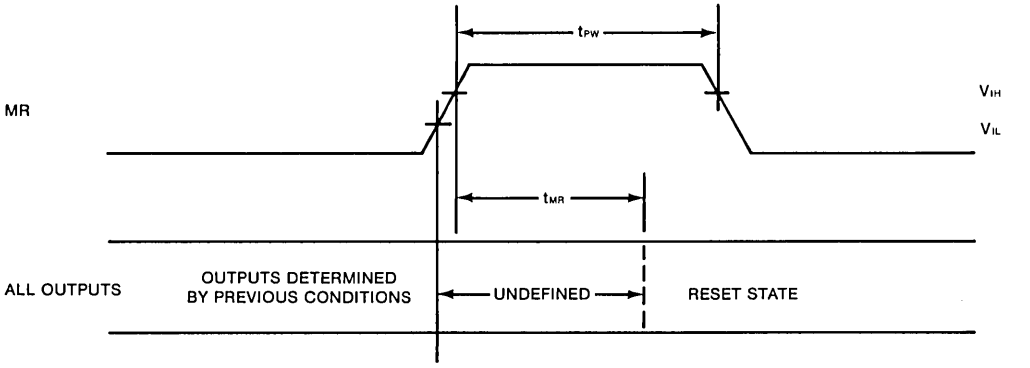


Figure 3

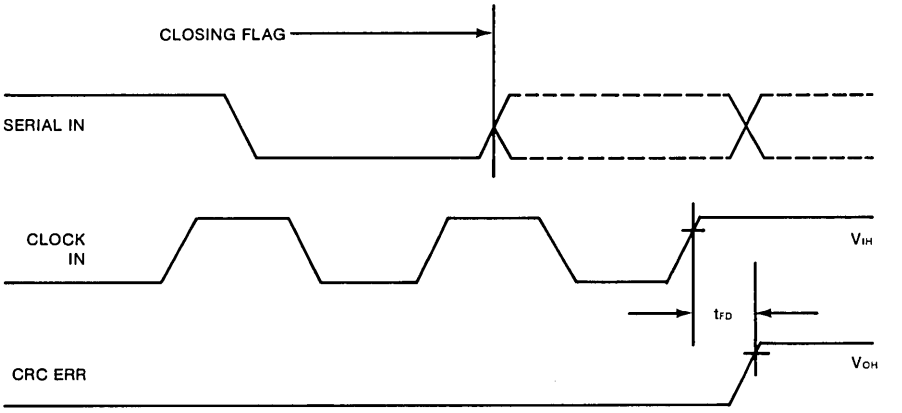


Figure 4

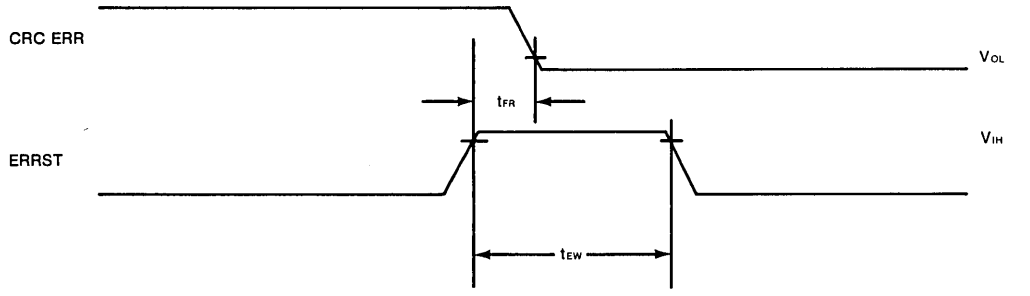


Figure 5