STANDARD MICROSYSTEMS CORPORATION
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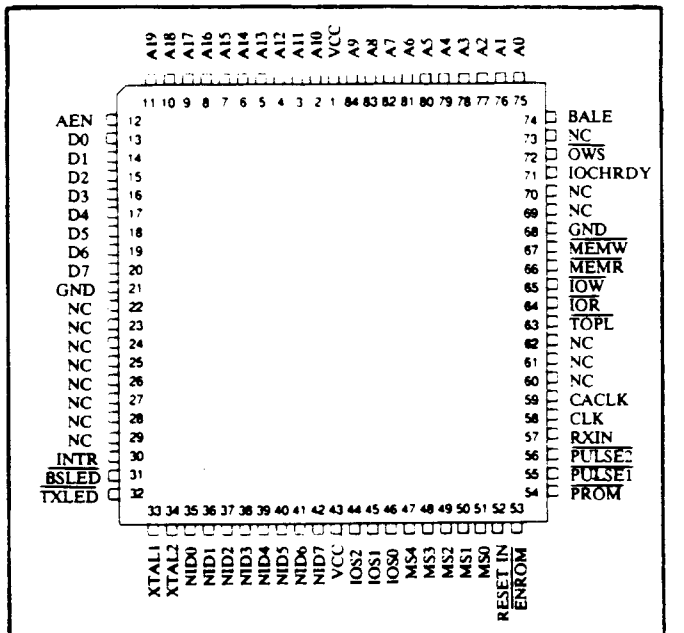
COM90C165
PRELIMINARY

ARCNET® Controller/Transceiver with XT® Interface and On-Chip RAM

FEATURES

- ARCNET LAN Controller/Transceiver/Support Logic/Dual-Port RAM
- Integrates SMC COM90C65 with 8-Bit Data Bus, Dual-Port RAM, and Enhanced Diagnostics Circuitry
- Includes IBM® PC XT® Bus Interface Circuitry
- Supports 8-Bit Data Busses
- Full 2K x 8 On-Chip Dual-Port Buffer RAM
- No Additional Wait State Arbitration
- SMC COM90C26 Software Compatible
- Command Chaining Enhances Performance
- Supports Memory Mapped and Sequential I/O Mapped Access to the Internal RAM Buffer
- Compatible with the SMC HYC9058/68/88 (COAX and Twisted Pair Drivers)
- Token Passing Protocol with Self Reconfiguration Detection
- Variable Data Length Packets
- 16 Bits CRC Check/Generation
- Includes Address Decoding Circuitry for On-Chip RAM, PROM and I/O
- Supports up to 255 Nodes
- Contains Software Accessable Node ID Register
- Compatible with Various Topologies (Star, Tree, Bus,...)
- On-Board Crystal Oscillator and Reset Circuitry
- Low Power CMOS, Single +5V Supply

PIN CONFIGURATION



PACKAGE: 84-Pin PLCC
Ordering Information: COM90C165 LJP

GENERAL DESCRIPTION

The SMC COM90C165 is a special purpose communications controller for interconnecting processors and intelligent peripherals using the ARCNET Local Area Network. The SMC COM90C165 is unique in that it integrates the core ARCNET logic found in Standard Microsystems' original COM90C26 and COM90C32 with an on-chip 2K x 8 RAM as well as the 8-bit data bus interface for the IBM PC. Because of the inclusion of the RAM buffer in the SMC COM90C165, a complete ARCNET node can be implemented with only one additional IC and a media driver circuit.

The ARCNET core remains functionally untouched, eliminating validation and compatibility concerns. The enhancements exist in the integration and the performance of the device. Maximum integration has been achieved by including the 2K x 8 RAM buffer on the chip, providing the immediate benefits of a lower device pin count and less board components. The performance is enhanced in four ways: An 8-bit data bus for operation with the IBM PC, A zero wait state arbitration mechanism, due partly to the integration of the RAM buffer on-chip, The ability of the device to do consecutive transmissions and receptions via the Command Chaining operation, and Improved diagnostics, allowing the user to control the system more efficiently. There is no need to connect the IOCHRDY line because the device handles no additional wait state transfers for IBM PC's.

Aside from the implementation of a higher-speed data bus interface, the remaining bus interface logic is identical to that found in the SMC COM90C65, which contains all the support logic circuitry.

The ARCNET Local Area Network is a token passing network which operates at a 2.5 Mbps data rate. A token passing protocol provides predictable response times because each network event occurs within a known time interval. Throughput is reliably predetermined based upon the number of nodes and their expected traffic.

The SMC COM90C165 establishes the network configuration and automatically reconfigures the token passing order as new nodes are added or deleted from the network.

The SMC COM90C165 performs address recognition, CRC checking and generation, packet acknowledgement, and other network management functions. The SMC COM90C165 interfaces directly to the IBM PC or compatibles. The internal 2K x 8 RAM buffer is used to hold up to four data packets with a maximum length of 508 bytes each.

Rev. 3 March 9, 1990

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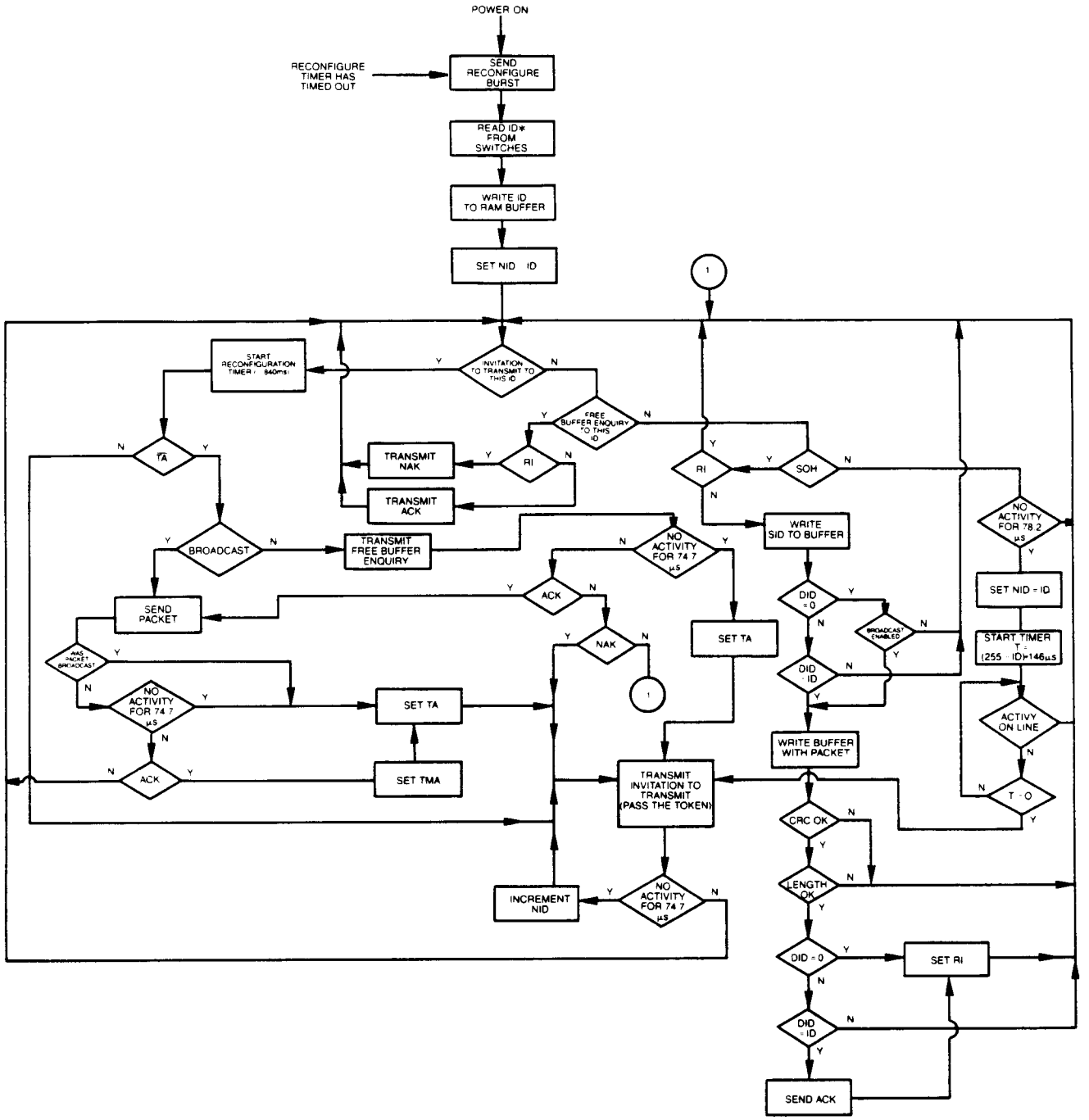
DESCRIPTION OF PIN FUNCTIONS

PLCC PIN NO.	NAME	SYMBOL	DESCRIPTION
PROCESSOR INTERFACE			
75-84, 2-11	Address 0-19	A0-A19	Input. These signals are connected to the address lines of the host processor and are used to access memory and I/O locations of the COM90C165, as well as to access the external ROM through the COM90C165.
13-20	Data 0-7	D0-D7	Input/Output. These signals are used by the host to transmit data to and from the internal registers and buffer memory of the COM90C165 and are connected to internal 50KΩ pull-up resistors.
63	Transceiver Direction Control	TOPL	Output. This active low signal controls the data bus transceiver. When this signal is high, data gets sent from the PC to the COM90C165. When this signal is low, data gets sent from the COM90C165 to the PC, or from the PROM to the PC if the PROM signal is also low.
71	I/O Channel Ready	IOCHRDY	Output. This signal, when low, is optionally used by the COM90C165 to extend host cycles. This is an open-drain signal. An external pull-up resistor is typically provided by the system.
12	Address Enable	AEN	Input. This signal, when low, acts as a qualifier for I/O Address Selection. When the signal is high, I/O decoding is disabled.
74	Address Latch Enable	BALE	Input. The falling edge of this signal is used by the COM90C165 to latch the A0-A19 lines via an internal transparent latch. This signal is connected to an internal 50KΩ pull-up resistor.
64	I/O Read	IOR	Input. This active low signal is issued by the host microprocessor to indicate an I/O Read operation. A low level on this pin when the COM90C165 is accessed enables data from the internal registers of the COM90C165 onto the Data Bus to be read by the host.
65	I/O Write	IOW	Input. This active low signal is issued by the host microprocessor to indicate an I/O Write operation. A low pulse on this pin when the COM90C165 is accessed enables data from the Data Bus into the internal registers of the COM90C165.
66	Memory Read	MEMR	Input. This active low signal is issued by the host microprocessor to indicate a Memory Read operation. A low level on this pin when the COM90C165 is accessed enables data from the internal RAM of the COM90C165 or the PROM onto the data bus to be read by the host.
67	Memory Write	MEMW	Input. This active low signal is issued by the host microprocessor to indicate a Memory Write operation. A low pulse on this pin when the COM90C165 is accessed enables data from the data bus into the internal RAM of the COM90C165.
52	Reset In	RESETIN	Input. This active high signal is the power on reset signal from the host. It is used to activate the internal reset circuitry within the COM90C165.
53	ROM Enable	ENROM	Input. This active low signal enables the decoding of the external PROM. This signal also affects the timing of IOCHRDY. This signal is connected to an internal 50KΩ pull-up resistor.
54	ROM Select	PROM	Output. This active low signal is issued by the COM90C165 to enable the external 8-bit wide PROM or the external register of the COM90C165.
30	Interrupt Request	INTR	Output. This active high signal is generated by the COM90C165 when an enabled interrupt condition occurs. INTR returns to its inactive state when the interrupt status condition or the corresponding interrupt mask bit is reset.
72	Zero Wait State	0WS	Output. This active low signal is used to force zero wait state access cycles on the IBM PC Bus. This is an open-drain signal. An external pull-up resistor is typically provided by the system.

DESCRIPTION OF PIN FUNCTIONS (CONTINUED)

PLCC PIN NO.	NAME	SYMBOL	DESCRIPTION
TRANSMISSION MEDIA INTERFACE			
56, 55	$\overline{\text{Pulse 2}}$, $\overline{\text{Pulse 1}}$	$\overline{\text{PULSE2}}$, $\overline{\text{PULSE1}}$	Output. These active low signals carry the transmit data information, encoded in pulse format, from the COM90C165 to the LAN Driver.
57	Receive In	RXIN	Input. This signal carries the receive data information from the LAN Driver to the COM90C165.
MISCELLANEOUS			
51-47	Memory Base Address Select	MS0-MS4	Input. These signals are generated by external switches. They are used by the memory decoder to select a block of memory. These signals are connected to 50KΩ internal pull-up resistors.
46-44	I/O Base Address Select	IOS0-IOS2	Input. These signals are generated by external switches. They are used by the I/O decoder to select a block of 16 I/O locations. These signals are connected to 50KΩ internal pull-up resistors.
35-42	Node ID Select	NID0-NID7	Input. These signals are generated by external switches. The Node ID code represents the node identification of this particular COM90C165. These signals are connected to 50KΩ internal pull-up resistors.
32	$\overline{\text{Transmit Activity LED}}$	TXLED	Output. This active low signal is used for direct connection to an LED through a resistor to V_{CC} to indicate transmit activity. This signal has 12mA sink capability.
31	$\overline{\text{Board Select Activity LED}}$	BSLED	Output. This active low signal is used for direct connection to an LED through a resistor to V_{CC} to indicate board activity. This signal has 12mA sink capability.
33, 34	Crystal Oscillator	XTAL1, XTAL2	An external 20 MHz crystal should be connected to these pins. If an external 20MHz TTL clock is used instead, it must be connected to XTAL1 with a 390Ω pull-up resistor, and XTAL2 should be left floating.
59	CA Clock	CACLK	Output. This is the start/stop CA clock and should be left floating for typical operation.
58	Clock	CLK	Output. This is a general purpose 5 MHz clock and should be left floating for typical operation.
1, 43	Power Supply	V_{CC}	+5 Volt Power Supply pin.
21, 68	Ground	GND	Ground pins.
22-29, 60-62, 69-70, 73	No Connect	NC	Make no connection to these pins.



*The ID set by the external switches is continually sampled during COM90C165 operation.

- ID refers to the identification number of the ID assigned to this node.
- NID refers to the next identification number that receives the token after this ID passes it.
- SID refers to the source identification.
- DID refers to the destination identification.
- SOH refers to the start of header character; preceeds all data packets.

FIGURE 1 - COM90C165 OPERATION

PROTOCOL DESCRIPTION

LINE PROTOCOL

The ARCNET line protocol can be described as isochronous because each byte is preceded by a start interval and ended with a stop interval. Unlike asynchronous protocols, there is a constant amount of time separating each data byte. Each byte takes up exactly 11 clock intervals with a single clock interval being 400 nS in duration. As a result, one byte is transmitted every 4.4 μS and the time to transmit a message can be precisely determined. The line idles in a spacing (logic "0") condition. A logic "0" is defined as no line activity and a logic "1" is defined as a pulse of 200 nS duration. A transmission starts with an ALERT BURST consisting of 6 unit intervals of mark (logic "1"). Eight bit data characters are then sent with each character preceded by 2 unit intervals of mark and one unit interval of space. Five types of transmission can be performed as described below:

Invitations To Transmit

An Invitation To Transmit is used to pass the token from one node to another and is sent by the following sequence:

- An ALERT BURST
- An EOT (End Of Transmission--ASCII code 04 HEX)
- Two (repeated) DID (Destination IDentification) characters

ALERT BURST	EOT	DID	DID

Free Buffer Enquiries

A Free Buffer Enquiry is used to ask another node if it is able to accept a packet of data and is sent by the following sequence:

- An ALERT BURST
- An ENQ (ENQuiry--ASCII code 85 HEX)
- Two (repeated) DID (Destination IDentification) characters

ALERT BURST	ENQ	DID	DID

Data Packets

A Data Packet consists of the actual data being sent to another node and is sent by the following sequence:

- An ALERT BURST
- An SOH (Start Of Header--ASCII code 01 HEX)
- An SID (Source IDentification) character
- Two (repeated) DID (Destination IDentification) characters
- A single COUNT character which is the 2's complement of the number of data bytes to follow if a short packet is being sent or 00 HEX followed by a COUNT character which is the 2's complement of the number of data bytes to follow if a long packet is being sent
- N data bytes where COUNT = 256-N (or 512-N for a long packet)
- Two CRC (Cyclic Redundancy Check) characters. The CRC polynomial used is $X^{16} + X^{15} + X^2 + 1$.

ALERT BURST	SOH	SID	DID	DID	COUNT	data	data	CRC	CRC

Acknowledgements

An Acknowledgement is used to acknowledge reception of a packet or as an affirmative response to FREE BUFFER ENQUIRIES and is sent by the following sequence:

- An ALERT BURST
- An ACK (ACKnowledgement--ASCII code 86 HEX) character

ALERT BURST	ACK

Negative Acknowledgements

A Negative Acknowledgement is used as a negative response to FREE BUFFER ENQUIRIES and is sent by the following sequence:

- An ALERT BURST
- A NAK (Negative AcKnowlegement--ASCII code 15 HEX) character

ALERT BURST	NAK

NETWORK PROTOCOL

Communication on the network is based on a token passing protocol. Establishment of the network configuration and management of the network protocol are handled entirely by the COM90C165's internal microcoded sequencer. A processer or intelligent peripheral transmits data by simply loading a data packet and its destination ID into the RAM buffer, and issuing a command to enable the transmitter. When the COM90C165 next receives the token, it verifies that the receiving node is ready by first transmitting a FREE BUFFER ENQUIRY message. If the receiving node transmits an ACKnowledge message, the data packet is transmitted followed by a 16 bit CRC. If the receiving node cannot accept the packet (typically its receiver is inhibited), it transmits a Negative AcKnowledge message and the transmitter passes the token. Once it has been established that the receiving node can accept the packet and transmission is complete, the receiving node will verify the packet. If the packet is received successfully, the receiving node transmits an ACKnowledge message (or nothing if it is received unsuccessfully) allowing the transmitter to set the appropriate status bits to indicate successful or unsuccessful delivery of the packet. An interrupt mask permits the COM90C165 to generate an interrupt to the processor when selected status bits become true. Figure 1 is a flow chart illustrating the internal operation of the COM90C165.

NETWORK RECONFIGURATION

A significant advantage of the COM90C165 is its ability to

adapt to changes on the network. Whenever a new node is activated or deactivated, a NETWORK RECONFIGURATION is performed. When a new COM90C165 is turned on (creating a new active node on the network), or if the COM90C165 has not received an INVITATION TO TRANSMIT for 840 mS, or if a software reset occurs, the device causes a NETWORK RECONFIGURATION by sending a RECONFIGURE BURST consisting of eight marks and one space repeated 765 times. The purpose of this burst is to terminate all activity on the network. Since this burst is longer than any other type of transmission, the burst will interfere with the next INVITATION TO TRANSMIT, destroy the token and keep any other node from assuming control of the line.

When any COM90C165 senses an idle line for greater than 78.2 μS, which will only occur when the token is lost, each COM90C165 starts an internal timeout equal 146 μS times the quantity 255 minus its own ID. It also sets the internally stored NID (next ID representing the next possible ID node) equal to its own ID. If the timeout expires with no line activity, the COM90C165 starts sending INVITATION TO TRANSMIT with the Destination ID (DID) equal to the currently stored NID. Within a given network, only one COM90C165 will timeout (the one with the highest ID number). After sending the INVITATION TO TRANSMIT, the COM90C165 waits for activity on the line. If there is no activity for 74.7 μS, the COM90C165 increments the NID value and transmits another INVITATION TO TRANSMIT using the NID equal to the DID. If activity appears before the 74.7 μS timeout expires, the COM90C165 releases control of the line. During NETWORK RECONFIGURATION, INVITATIONS TO TRANSMIT will be sent to all 256 possible ID's. Each COM90C165 on the network will finally have saved a NID value equal to the ID of the COM90C165 that it released control to. At this point, control is passed directly from one node to the next with no wasted INVITATIONS TO TRANSMIT being sent to ID's not on the network, until the next NETWORK RECONFIGURATION occurs. When a node is powered off, the previous node will attempt to pass it the token by issuing an INVITATION TO TRANSMIT. Since this node will not respond, the previous node will timeout and transmit another INVITATION TO TRANSMIT to an incremented ID and eventually a response will be received.

The time required to do a NETWORK RECONFIGURATION depends on the number of nodes in the network, the propogation delay between nodes, and the highest ID number on the network, but will be in the range of 24 to 61 mS.

BROADCAST MESSAGES

Broadcasting gives a particular node the ability to transmit a data packet to all nodes on the network simultaneously. ID zero is reserved for this feature and no node on the network can be assigned ID zero. To broadcast a message, the transmitting node's processor simply loads the RAM buffer with the data packet and sets the DID equal to zero. Figure 9 illustrates the position of each byte in the packet with the DID residing at address 01 HEX of the current page selected in the TRANSMIT command. Each individual node has the ability to ignore broadcast messages by setting the most significant bit of the ENABLE RECEIVE TO PAGE nn command (see Table 6) to a logic "0".

EXTENDED TIMEOUT FUNCTION

There are three timeouts associated with the COM90C165 operation.

Response Time

The Response Time is equal to the round trip propagation delay between the two furthest nodes on the network plus the maximum turn around time (the time it takes a particular COM90C165 to start sending a message in response to a received message) which is approximately 12 μS. The round trip propagation delay is a function of the transmission media and network topology. For a typical system using RG62 coax in a baseband system, a one way cable propagation delay of 31 μS translates to a distance of about 4 miles. The flow chart in figure 1 uses a value of 74.7 μS (31 + 31 + 12 + margin) to determine if any node will respond.

Idle Time

The Idle Time is associated with a NETWORK RECONFIGURATION. Figure 1 illustrates that during a NETWORK RECONFIGURATION one node will continually transmit INVITATIONS TO TRANSMIT until it encounters an active node. Every other node on the network must distinguish between this operation and an entirely idle line. During NETWORK RECONFIGURATION, activity will appear on the line every 78 μS. This 78 μS is equal to the Response Time of 74.7 μS plus the time it takes the COM90C165 to retransmit another message (usally another INVITATION TO TRANSMIT). The actual timeout is set to 78.2 μS to allow for margin.

Reconfiguration Time

If any node does not receive the token within the Reconfiguration Time, the node will initiate a NETWORK RECONFIGURATION.

The ET2 and ET1 bits (bits 3 and 4 of the Configuration Register) allow the network to operate over longer distances than the 4 miles stated earlier. The logic levels on these bits control the maximum distances over which the COM90C165 can operate by controlling the three timeout values described above. See the description of the ET1 and ET2 bits, found in Table 7 for the table containing the combinations of these bits. It should be noted that for proper network operation, all COM90C165's connected to the same network must have the same Response Time, Idle Time, and Reconfiguration Time.

SYSTEM DESCRIPTION

The System Block Diagram shown in Figure 2 illustrates a typical implementation of an ARCNET node using the COM90C165. The only external components required to complete an ARCNET node design are one bus transceiver and the LAN Driver, making the COM90C165 the most highly integrated 8-bit ARCNET solution. The COM90C165 provides for simple interfacing to both sides of the ARCNET system, namely, the microprocessor and the transmission media.

MICROPROCESSOR INTERFACE

The left half of Figure 2 illustrates a typical COM90C165 interface to the PC. The interface consists of a 20-bit address bus, an 8-bit data bus and a control bus. All accesses to the internal RAM, the optional PROM and the internal registers are controlled by the COM90C165.

The microprocessor's address lines are directly connected to the COM90C165. The address decoding circuitry of the COM90C165 monitors the address bus to determine valid accesses to the device.

Figure 2 shows an octal bus transceiver utilized as the interface between the microprocessor's data lines and the COM90C165. The transceiver is only necessary when interfacing to a high current drive data bus such as the IBM PC data bus, and may otherwise be omitted. The COM90C165 provides the $\overline{\text{TOPL}}$ signal which controls the direction of the external transceiver. The $\overline{\text{TOPL}}$ signal is also activated during PROM Read Cycles.

The microprocessor's control bus is directly connected to the COM90C165 and is used in access cycle communication between the device and the microprocessor. All accesses support zero wait state arbitration in most machines. The Control Bus has been optimized to support the intricacies of the IBM XT Bus and the EISA Bus.

TRANSMISSION MEDIA INTERFACE

The right half of Figure 2 illustrates the COM90C165 interface to the transmission media used to connect the node to the network. The HYC9058/68/88 may be used to drive the media. During transmission, the COM90C165 transmits a logic "1" by generating two 100 nS non-overlapping negative pulses, $\overline{\text{PULSE1}}$ and $\overline{\text{PULSE2}}$. These signals are sent to the LAN Driver, which in turn creates a 200 nS dipulse signal on the media. A logic "0" is transmitted by the absence of the two negative pulses, that is, the $\overline{\text{PULSE1}}$ and $\overline{\text{PULSE2}}$ outputs remain high, therefore there is an absence of a dipulse. During reception, the 200 nS dipulse appearing on the media is coupled through the RF transformer of the LAN Driver. A positive pulse at the RXIN pin of the COM90C165 is interpreted as a logic "1". Again, if no dipulse is present, the COM90C165 interprets a logic "0".

Typically, RXIN pulses occur at multiples of 400 nS. The COM90C165 can tolerate distortion of plus or minus 100 nS and still correctly capture the RXIN pulses.

During Reset, the transmitter portion of the COM90C165 is disabled and the $\overline{\text{PULSE1}}$ and $\overline{\text{PULSE2}}$ pins are inactive high.

The COM90C165 includes the $\overline{\text{TXLED}}$ and $\overline{\text{BSLED}}$ signals which, when tied to LED's, provide indication of transmit and board access activity. In addition, it is possible for the user to completely disable the transmitter through software. These two unique features represent two of the improvements made in the diagnostics of the device. Please see the Improved Diagnostics section of this document for further detail.

FUNCTIONAL DESCRIPTION

MICROSEQUENCER

The COM90C165 contains an internal microsequencer which performs all of the control operations necessary to carry out the ARCNET protocol. It consists of a clock generator, a 544 x 8 ROM, a program counter, two instruction registers, an instruction decoder, a no-op generator, jump logic, and reconfiguration logic.

The COM90C165 derives a 5 MHz and a 2.5 MHz clock from the external crystal. These clocks provide the rate at which the instructions are executed within the COM90C165. The 5 MHz clock is the rate at which the program counter operates, while the 2.5 MHz clock is the rate at which the instructions are executed. The microprogram is stored in the ROM and the instructions are fetched and then placed into the instruction registers. One register holds the op code, while the other holds the immediate data. Once the instruction is fetched, it is decoded by th internal instruction decoder, at which point the COM90C165 proceeds to execute the instruction. When a no-op instruction is encountered, the microsequencer enters a timed loop, in which case the program counter is temporarily stopped until the loop is complete. When a jump instruction is encountered, the program counter is loaded with the jump address from the ROM. The COM90C165 contains an internal reconfiguration timer which interrupts the microsequencer if it has timed out. At this point the program counter is cleared, afterwhich the MYRECON bit of the Diagnostic Status Register is set.

ADDRESS DECODING

The COM90C165 includes address decoding circuitry that compares the value of the Address Bus to the address range selected by the Memory Select (MS0-MS4) and I/O Select (IOS0-IOS2) pins in order to determine processor accesses to the on-board PROM, the on-chip RAM, and I/O locations. By placing switches on the MS0-MS4 and the IOS0-IOS2 pins, the user configures the Memory Map and I/O Map according to the possible address ranges shown in Tables 1 and 2.

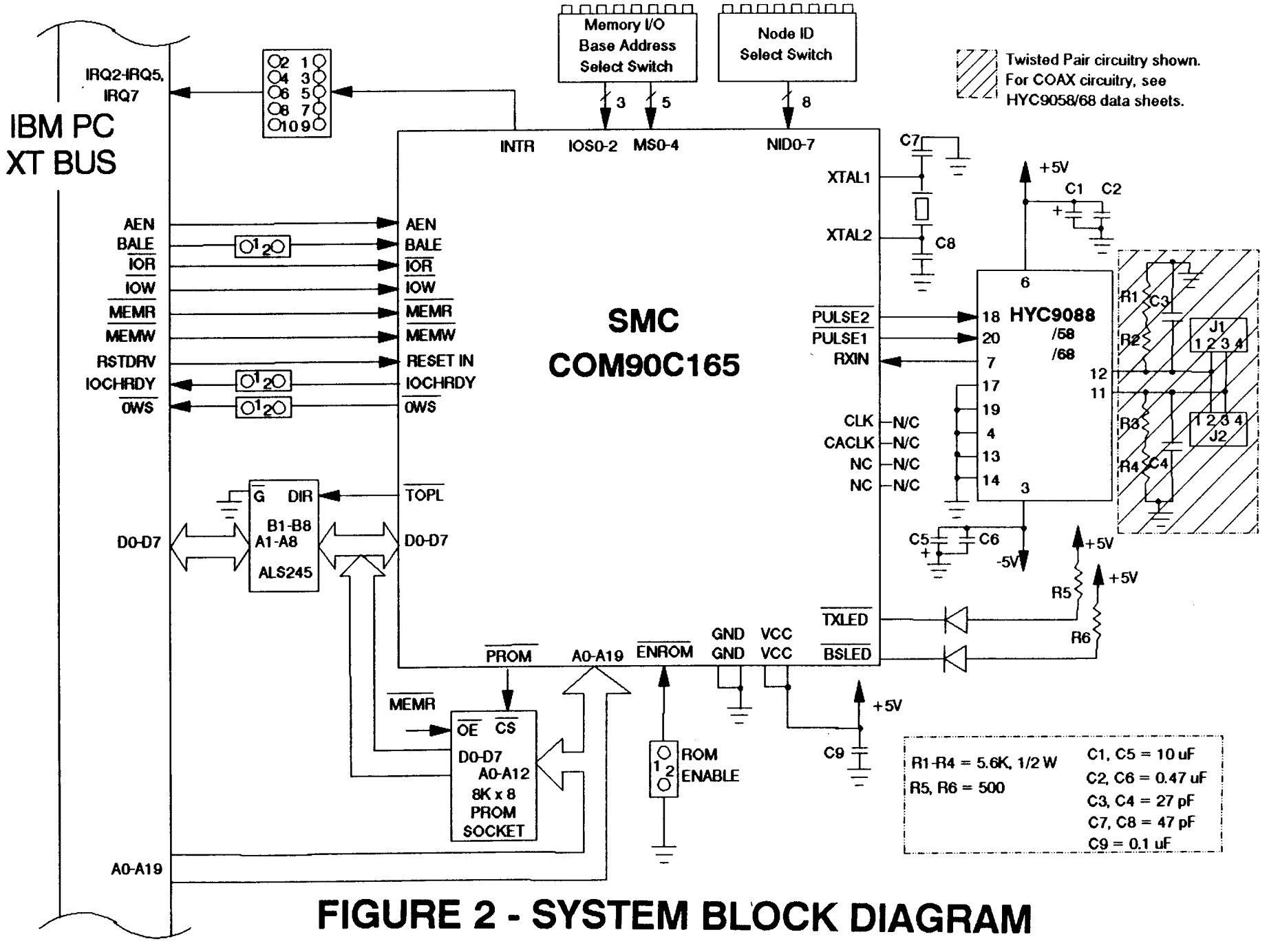


FIGURE 2 - SYSTEM BLOCK DIAGRAM

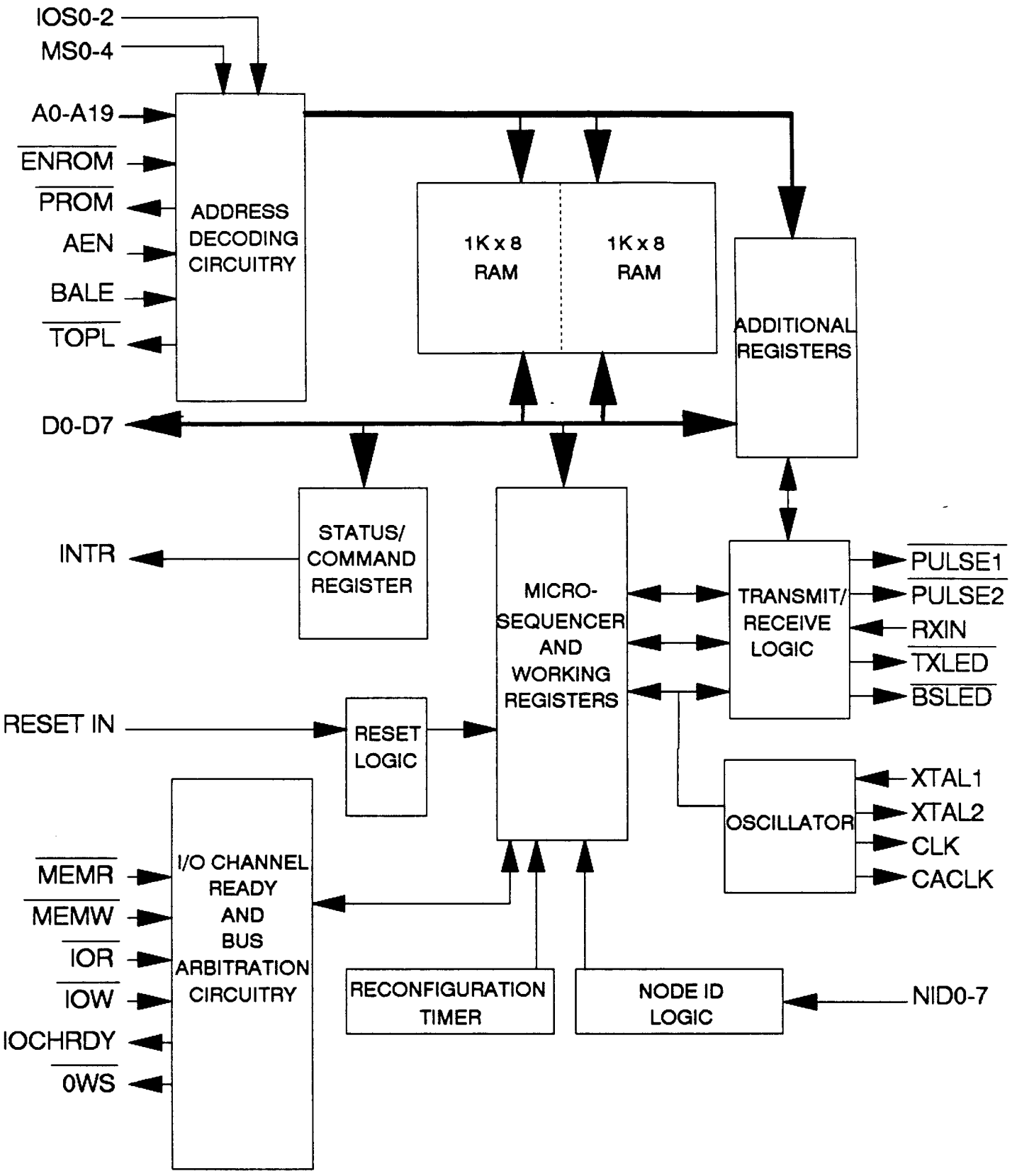


FIGURE 3 - INTERNAL BLOCK DIAGRAM

MS4	MS3	MS2	MS1	MS0	DECODED BITS FOUND IN DATA REGISTER D7	D6	D5	D4	D3	D2	D1	D0	RAM Address Range	PROM Address Range
0	0	0	0	0	1	1	0	0	0	0	0	0	C:0000-C:07FF	C:2000-C 3FFF
0	0	0	0	1	1	1	0	0	0	0	0	1	C:0800-C:0FFF	C 2000-C 3FFF
0	0	0	1	0	1	1	0	0	0	0	1	0	C:1000-C:17FF	C:2000-C 3FFF
0	0	0	1	1	1	1	0	0	0	0	1	1	C:1800-C:1FFF	C:2000-C 3FFF
0	0	1	0	0	1	1	0	0	0	1	0	0	C:4000-C:47FF	C:6000-C 7FFF
0	0	1	0	1	1	1	0	0	0	1	0	1	C:4800-C:4FFF	C:6000-C 7FFF
0	0	1	1	0	1	1	0	0	0	1	1	0	C:5000-C:57FF	C:6000-C 7FFF
0	0	1	1	1	1	1	0	0	0	1	1	1	C:5800-C:5FFF	C:6000-C:7FFF
0	1	0	0	0	1	1	0	0	1	1	0	0	C:C000-C:C7FF	C:E000-C FFFF
0	1	0	0	1	1	1	0	0	1	1	0	1	C:C800-C:CFFF	C:E000-C:FFFF
0	1	0	1	0	1	1	0	0	1	1	1	0	C:D000-C:D7FF	C:E000-C FFFF
0	1	0	1	1	1	1	0	0	1	1	1	1	C:D800-C:DFFF	C:E000-C FFFF
0	1	1	0	0	1	1	0	1	0	0	0	0	D:0000-D:07FF	D:2000-D 3FFF
0	1	1	0	1	1	1	0	1	0	0	0	1	D:0800-D:0FFF	D:2000-D:3FFF
0	1	1	1	0	1	1	0	1	0	0	1	0	D:1000-D:17FF	D:2000-D:3FFF
0	1	1	1	1	1	1	0	1	0	0	1	1	D:1800-D:1FFF	D:2000-D:3FFF
1	0	0	0	0	1	1	0	1	0	1	0	0	D:4000-D:47FF	D:6000-D:7FFF
1	0	0	0	1	1	1	0	1	0	1	0	1	D:4800-D:4FFF	D:6000-D:7FFF
1	0	0	1	0	1	1	0	1	0	1	1	0	D:5000-D:57FF	D:6000-D:7FFF
1	0	0	1	1	1	1	0	1	0	1	1	1	D:5800-D:5FFF	D:6000-D:7FFF
1	0	1	0	0	1	1	0	1	1	0	0	0	D:8000-D:87FF	D:A000-D:BFFF
1	0	1	0	1	1	1	0	1	1	0	0	1	D:8800-D:8FFF	D:A000-D:BFFF
1	0	1	1	0	1	1	0	1	1	0	1	0	D:9000-D:97FF	D:A000-D:BFFF
1	0	1	1	1	1	1	0	1	1	0	1	1	D:9800-D:9FFF	D:A000-D:BFFF
1	1	0	0	0	1	1	0	1	1	1	0	0	D:C000-D:C7FF	D:E000-D:FFFF
1	1	0	0	1	1	1	0	1	1	1	0	1	D:C800-D:CFFF	D:E000-D:FFFF
1	1	0	1	0	1	1	0	1	1	1	1	0	D:D000-D:D7FF	D:E000-D:FFFF
1	1	0	1	1	1	1	0	1	1	1	1	1	D:D800-D:DFFF	D:E000-D:FFFF
1	1	1	0	0	1	1	1	0	0	0	0	0	E:0000-E:07FF	E:2000-E 3FFF
1	1	1	0	1	1	1	1	0	0	0	0	1	E:0800-E:0FFF	E:2000-E 3FFF
1	1	1	1	0	1	1	1	0	0	0	1	0	E:1000-E:17FF	E:2000-E 3FFF
1	1	1	1	1	1	1	1	0	0	0	1	1	E:1800-E:1FFF	E:2000-E:3FFF

Table 1 - User Configuration of Memory Map

IOS2	IOS1	IOS0	I/O Address Range
0	0	0	0260-026F
0	0	1	0290-029F
0	1	0	02E0-02EF
0	1	1	02F0-02FF
1	0	0	0300-030F
1	0	1	0350-035F
1	1	0	0380-038F
1	1	1	03E0-03EF

Table 2 - User Configuration of I/O Map

Memory Address Decoding
The Memory Address Decoding circuitry is used to select a block from the memory map of the processor for PROM and RAM accesses. Figure 4 illustrates how the memory selection works. The MS4-MS0 pins are decoded through a 5 to 9 Decoder to generate a 9-bit value. These 9 bits are compared to the A19-A11 lines of the Address Bus in order to select a particular 16K memory segment. Figure 7 illustrates a 16K block of memory that has been selected by the MS4-MS0 pins. The PROM occupies the upper 8K area of the selected 16K segment and is accessed when A13 = 1. The RAM occupies one of four selectable 2K areas of the selected 16K segment and is accessed when A13 = 0. A11 and A12 are used to determine which 2K segment of the lower 8K area will be used for the RAM buffer.

Figure 5 illustrates how the external PROM selection works. The MS4-MS0 pins are decoded through a 5 to 7 decoder to generate a 7-bit value. These 7 bits are compared to the A19-A13 lines of the Address Bus in order to select an 8K memory range. Figure 7 illustrates an 8K block of memory for the PROM. In I/O 16K x 8 Mode only a 16K memory range is selected for the PROM. Figure 8 illustrates a 16K block of memory for the PROM.

The $\overline{\text{ENROM}}$ pin is used to enable decoding for the on-board PROM. If $\overline{\text{ENROM}}$ is connected to a logic "1", the COM90C165 will not generate the $\overline{\text{PROM}}$ signal, the $\overline{\text{TOPL}}$ signal, or the IOCHRDY signal for accesses to the PROM. In this configuration, the COM90C165 will only occupy a 2K segment of memory.

I/O Address Decoding
This section is used to select a block of 16 I/O locations from the I/O map of the processor. Figure 6 illustrates how the I/O selection processs works. The IOS2-IOS0 pins are decoded through a 3 to 12 decoder to generate a 12-bit value. These 12 bits are compared to the A15-A4 lines of the address bus in order to determine which block of 16 I/O locations will be used by the chip. A logic "0" on the AEN signal enables the I/O decoding process. Table 3 illustrates the COM90C165 register map. Reserved locations should not be accessed.

INTERNAL REGISTERS
The COM90C165 contains internal registers which may be accessed by the microprocessor. All undefined bits are read as undefined and must be written as logic "0".

Status Register
The COM90C165 Status Register is an 8-bit read-only register which can be accessed by the microprocessor. This register is software compatible with previous SMC ARCNET devices. The Status Register contents are traditionally defined as in Table 4. The Status Register contents are defined differently during the Command Chaining operation. Please refer to the "Command Chaining" section of this document for these definitions.

Interrupt Mask Register (IMR)
The COM90C165 is capable of generating an interrupt signal when certain status bits become true. A write to the IMR specifies which status bits will be enabled to generate the interrupt. The bit positions in the IMR are in the same position as their corresponding status bits in the Status Register, and a logic "1" in a particular position enables the corresponding interrupt. While the RI, RECON, and TA status bits are capable of generating an interrupt if enabled, the TMA status bit will never cause an interrupt. The IMR takes on the following bit definition:

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RECEIVE INHIBIT	X	X	X	X	RECON TIMER	X	TRANSMITTER AVAILABLE

The four maskable status bits are ANDed with their respective mask bits, and the results are ORed to produce the processor interrupt signal INTR. This signal returns to its inactive low state when either the interrupting status bit or the corresponding bit in the IMR is reset. To clear an interrupt generated as a result of a Reconfiguration occurance, the CLEAR FLAGS command should be used. To clear an interrupt generated as a result of a completed transmission (TA) or a completed reception (RI), the corresponding mask bits should be reset.

Diagnostic Status Register
The Diagnostic Status Register contains three read-only bits which give the user the ability to troubleshoot network or node operation. The various combinations of these bits and the Transmitter Off bit of the Configuration Register represent different situations and can be used during troubleshooting. These bits are reset to logic "0" upon reading the Diagnostic Status Register or upon software or hardware reset. The register contents are as in Table 5.

Command Register
Execution of commands are initiated by performing a processor I/O write with the written data defining the commands listed in Table 6. Any combinations of written data other than those listed in Table 6 are not permitted and can result in incorrect chip and/or network operation.

Configuration Register
The Configuration Register is a read/write register which can be accessed by the microprocessor to configure the different modes of the COM90C165. All of the bits except the ET1, ET2, and WAIT bits are reset to logic "0" upon software or hardware reset. The register contents are as in Table 7.

Memory Select Register
This register contains the decoded bits of the Memory Select 0-4 switch. For further detail refer to the Memory Address Decoding section of this document, as well as Figure 4 and Table 1.

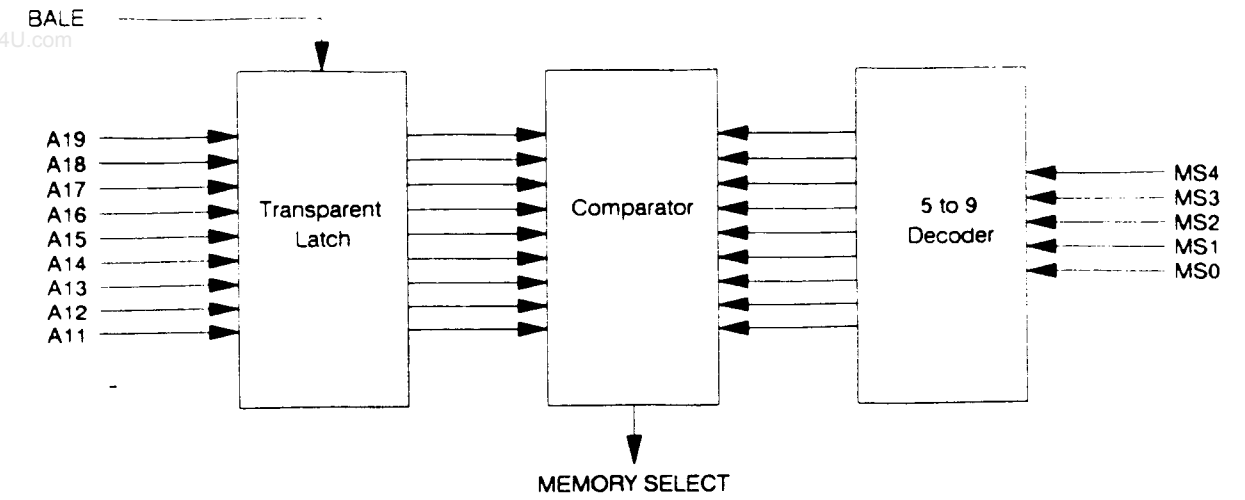
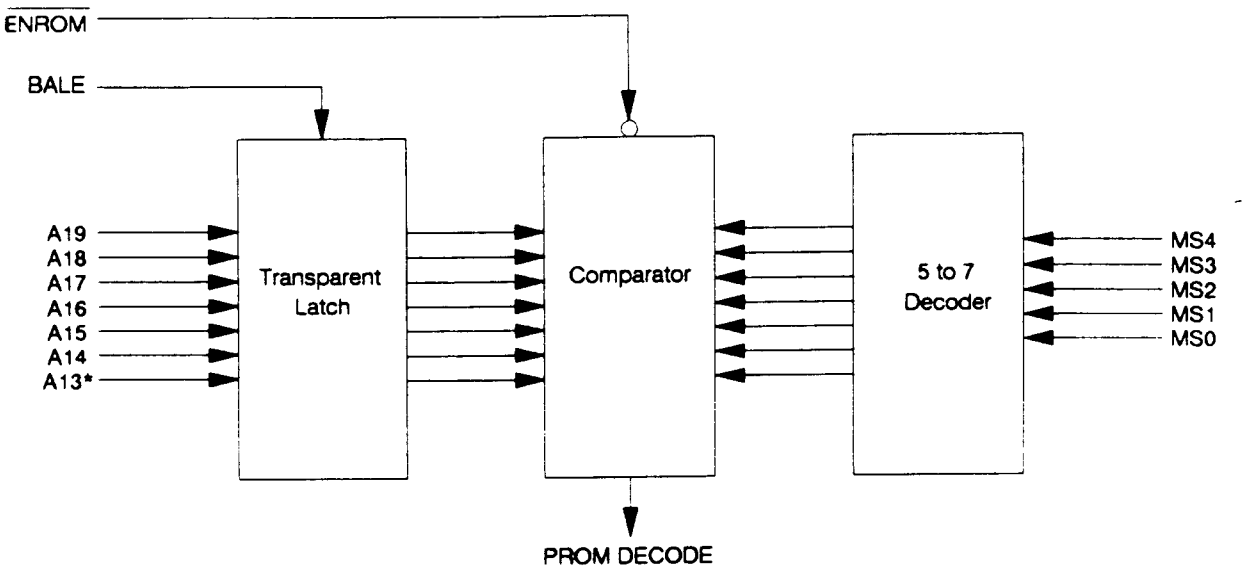


FIGURE 4 - MEMORY SELECTOR



* In I/O 16K x 8 Mode, A13 is a Don't Care

FIGURE 5 - PROM SELECTOR

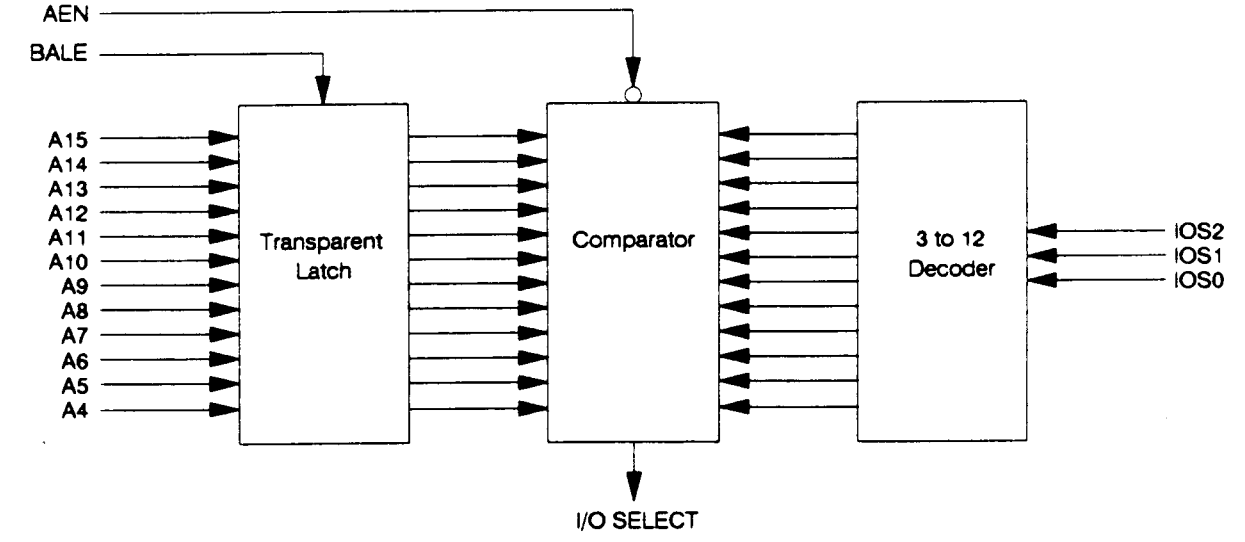
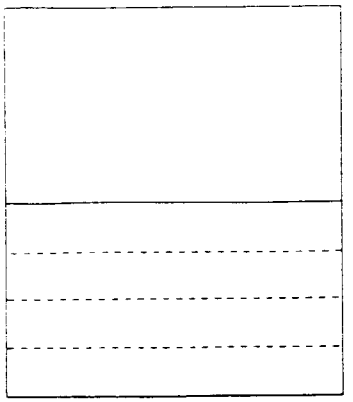


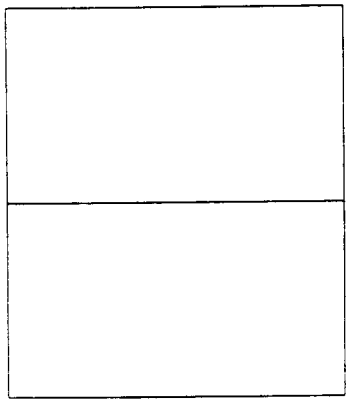
FIGURE 6 - I/O SELECTOR



A13 = 1:
8K PROM Space.

A13 = 0:
A11 and A12 select one
of these 2K RAM segments.

FIGURE 7 - 16K MEMORY SEGMENT CHOSEN BY MS0-MS4 (Memory Mapped Mode)



A13 = 1:
Upper 8K PROM Space.

A13 = 0:
Lower 8K PROM Space.

FIGURE 8 - 16K PROM SEGMENT CHOSEN BY MS0-MS4 (I/O Mapped, 16K x 8 Mode)

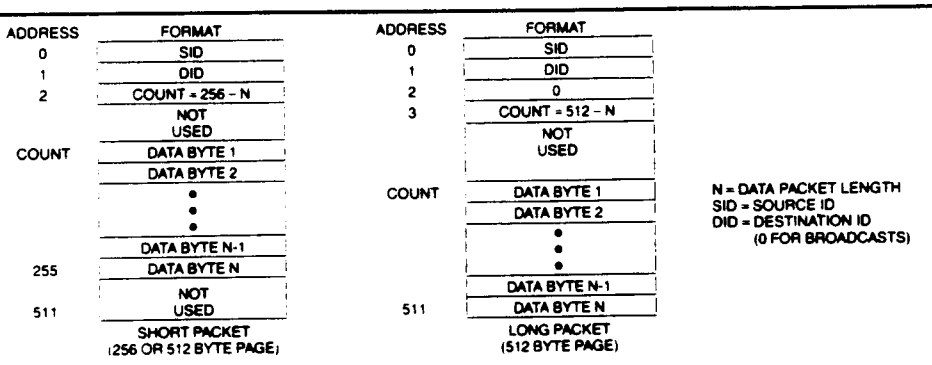


FIGURE 9 - RAM BUFFER PACKET CONFIGURATION

I/O Select Register
This register contains the decoded bits of the I/O Select 0-2 switch. For further detail refer to the I/O Address Decoding section of this document, as well as Figure 6 and Table 2.

Node ID Register
The Node ID Register contains the values of the Node ID switches. The microprocessor may read from the Node ID Register at any time for diagnostic purposes. In addition, the COM90C165 may be put into a special mode whereby the microprocessor may write to the Node ID register, thus software programming the Node ID. To enter this special mode, the Node ID switches must be set to 00H. Note that when the Node ID switches are set to 00H, the COM90C165 is put into a Disable Transmitter mode and it will not attemp to joint the network. When the device is in the Disable Transmitter mode, tokens are not passed and reconfigurations are not generated by the node. The receiver portion of the device will provide the user with useful information about the network. The device will not attempt to rejoin the network until until a valid Node ID value is placed into the Node ID Register. The I/O address of the Node ID Register is 05H. Table 3 illustrates the Node ID Register, as well as the other registers of the COM90C165.

External Register
The optional write only external register may be used for application dependent functions. A read operation at this location will provide invalid data. Whenever a write to address 07H occurs, the COM90C165 activates the $\overline{\text{PROM}}$ signal. In this case, the $\overline{\text{PROM}}$ signal is to be used as the Chip Select signal and the $\overline{\text{IOW}}$ signal should be used to write to the external register. The external PROM should use the $\overline{\text{PROM}}$ signal as Chip Select and the $\overline{\text{MEMR}}$ signal as Output Enable, as usual.

Reset Register
Any read or write access to I/O locations 08H, 09H, 0AH, or 0BH generates a software reset. These four I/O locations were preserved for software compatibility with the COM90C65 ARCNET Controller. Refer to the Reset Logic section of this document for further detail.

Data Register
This read/write 8-bit register is used in I/O Mapped Mode only. The Data Register contains the byte which is meant to be read from or written to the address location presently specified by the address pointer.

Address Pointer Low and High Registers
These read/write registers are each 8-bits wide and are used in I/O Mapped Mode only. These bits contain undefined data upon software or hardware reset. The contents of the Address Pointer Registers are defined as in Tables 8 and 9. The COM90C165 is capable of incrementing the address automatically, as explained in Table 9.

REGISTER	READ								ADD-RESS	WRITE								REGISTER
STATUS	RI	X	X	POR	TEST	RE-CON	TMA	TA	00	RI	0	0	EN-DIAG	0	RE-CON	0	TA	*INTERRUPT MASK*
DIAG. STATUS	MYRE-CON	X	RCV-ACT	TOKEN	X	X	X	X	01	D7	D6	D5	D4	D3	D2	D1	D0	*COMMAND*
CONFIG-URATION	X	CCHEN	DE-CODE	ET1	ET2	WAIT	IO-ACCESS	TXOFF	02	0	CCHEN	DE-CODE	ET1	ET2	WAIT	IO-ACCESS	TXOFF	*CONFIG-URATION*
I/O SELECT	0	0	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0	03	0	0	0	0	0	0	0	0	*RESERVED*
MEMORY SELECT	MEM 7	MEM 6	MEM 5	MEM 4	MEM 3	MEM 2	MEM 1	MEM 0	04	0	0	0	0	0	0	0	0	*RESERVED*
NODE ID	NID7	NID6	NID5	NID4	NID3	NID2	NID1	NID0	05	NID7	NID6	NID5	NID4	NID3	NID2	NID1	NID0	*NODE ID*
RESERVED	X	X	X	X	X	X	X	X	06	0	0	0	0	0	0	0	0	*RESERVED*
RESERVED	X	X	X	X	X	X	X	X	07	D7	D6	D5	D4	D3	D2	D1	D0	*EXTERNAL REGISTER*
RESET	X	X	X	X	X	X	X	X	08	X	X	X	X	X	X	X	X	*RESET*
RESET	X	X	X	X	X	X	X	X	09	X	X	X	X	X	X	X	X	*RESET*
RESET	X	X	X	X	X	X	X	X	0A	X	X	X	X	X	X	X	X	*RESET*
RESET	X	X	X	X	X	X	X	X	0B	X	X	X	X	X	X	X	X	*RESET*
DATA LOW	D7	D6	D5	D4	D3	D2	D1	D0	0C	D7	D6	D5	D4	D3	D2	D1	D0	*DATA LOW*
RESERVED	X	X	X	X	X	X	X	X	0D	0	0	0	0	0	0	0	0	*RESERVED*
ADDRESS PTR LOW	A7	A6	A5	A4	A3	A2	A1	A0	0E	A7	A6	A5	A4	A3	A2	A1	A0	*ADDRESS PTR LOW*
ADDRESS PTR HIGH	X	AUTO-INC	X	X	X	A10	A9	A8	0F	0	AUTO-INC	0	0	0	A10	A9	A8	*ADDRESS PTR HIGH*

TABLE 3 - REGISTER SUMMARY

Table 4 - Status Register

Bit	Bit Name	Symbol	Description
7	Receiver Inhibited	RI	This bit, if high, indicates that a packet has been deposited into the RAM buffer page nn as specified by the last ENABLE RECEIVE TO PAGE nn command. No messages will be received until this command is issued, and once the message has been received, the RI bit gets set, thereby inhibiting the receiver. The RI bit is cleared by issuing an ENABLE RECEIVE TO PAGE nn command. This bit, when set, will cause an interrupt if the corresponding bit of the Interrupt Mask Register is also set.
6	(not used)		This bit is undefined.
5	(not used)		This bit is undefined.
4	Power On Reset	POR	This bit, if high, indicates that the COM90C165 has been reset by either a software reset, a hardware reset, or setting the Node ID = 00H. The POR bit is cleared by the CLEAR FLAGS command.
3	Test	TEST	This bit is intended for test and diagnostic purposes. It is a logic "0" under normal operating conditions.
2	Reconfiguration	RECON	This bit, if high, indicates that the Line Idle Timer has timed out because the RXIN pin (pin 57) was idle for 78.2 μS. The RECON bit is cleared during a CLEAR FLAGS command. This bit, when set, will cause an interrupt if the corresponding bit in the Interrupt Mask Register is also set. The interrupt service routine should consist of looking at the MYRECON bit of the Diagnostic Status Register to make sure that there are not consecutive reconfigurations caused by this node.
1	Transmitter Message Acknowledged	TMA	This bit, if high, indicates that the packet transmitted as a result of an ENABLE TRANSMIT FROM PAGE nn command has been positively acknowledged. This bit should only be considered valid after the TA bit (bit 0) is set. Broadcast messages are never acknowledged. The TMA bit is cleared by issuing the ENABLE TRANSMIT FROM PAGE nn command.
0	Transmitter Available	TA	This bit, if high, indicates that the transmitter is available for transmitting. This bit is set at the conclusion of an ENABLE TRANSMIT FROM PAGE nn command or upon execution of a DISABLE TRANSMITTER command. The TA bit is cleared by issuing the ENABLE TRANSMIT FROM PAGE nn command after the node next receives the token. This bit, when set, will cause an interrupt if the corresponding bit in the Interrupt Mask Register is also set.

Table 5 - Diagnostic Status Register

Bit	Bit Name	Symbol	Description
7	My Reconfiguration	MY-RECON	This bit, if high, indicates that the reconfiguration that has just occurred was caused by this node. This bit is set when the Token Reception Timer times out. This bit is typically read after the RECON bit of the Status Register is found to be set. Refer to the Improved Diagnostics section of this document for further detail.
5	Receive Activity	RCVACT	This bit, if high, indicates that receive activity is detected on the RXIN pin of the device. This bit may be used in diagnostic troubleshooting of the network or node. Refer to the Improved Diagnostics section of this document for further detail.
4	Token Seen	TOKEN	This bit, if high, indicates that a token has been seen on the network. This bit may be used in diagnostic troubleshooting of the network or node. Refer to the Improved Diagnostics section of this document for further detail.
6, 3-0	(not used)		These bits are undefined.

Table 6 - Command Register

Written Data	Command Name	Description
0000 0000	CLEAR TRANSMIT INTERRUPT	This command is only used in the Command Chaining operation. Please refer to the Command Chaining section of this document for definition of this command.
0000 0001	DISABLE TRANSMITTER	This command will cancel any pending transmit command (transmission that has not yet started) and will set the TA (Transmitter Available) status bit to logic "1" when the COM90C165 next receives the token.
0000 0010	DISABLE RECEIVER	This command will cancel any pending receive command. If the COM90C165 is not yet receiving a packet, the RI (Receiver Inhibited) bit will be set to logic "1" the next time the token is received. If packet reception is already underway, reception will run to its normal conclusion.
000n n011	ENABLE TRANSMIT FROM PAGE nn	This command prepares the COM90C165 to begin a transmit sequence from RAM buffer page nn the next time it receives the token. When this command is loaded, the TA and TMA bits are reset to logic "0". The TA bit is set to logic "1" upon completion of the transmit sequence. The TMA bit will have been set by this time if the COM90C165 has received an acknowledgement from the destination node. This acknowledgement is strictly hardware level which is sent by the receiving node before its controlling processor is even aware of message reception. It is also possible for this acknowledgement to get lost due to line errors. This implies that the TMA bit is not a guaranteed of proper destination reception. Refer to figure 1 for details of the transmit sequence and its relation to the TA and TMA status bits.
b00n n100	ENABLE RECEIVE TO PAGE nn	This command allows the COM90C165 to receive data packets into RAM buffer page nn and resets the RI status bit to logic "0". If the value of "b" is a logic "1", the COM90C165 will also receive broadcast transmissions. A broadcast transmission is a transmission to ID zero. The RI status bit is set to logic "1" upon successful reception of a message.
0000 c101	DEFINE CONFIGUR-ATION	This command defines the maximum length of packets that may be handled by the device. If the value of "c" is a logic "1", the COM90C165 will handle long as well as short packets. If the value of "c" is a logic "0", the COM90C165 will only handle short packets (packets less than 254 bytes).
000r p110	CLEAR FLAGS	This command resets one or both flags of the COM90C165. If the value of "p" is a logic "1", the POR status flag is reset. If the value of "r" is a logic "1", the RECON status flag is reset.
0000 1000	CLEAR RECEIVE INTERRUPT	This command is only used in the Command Chaining operation. Please refer to the Command Chaining section of this document for definition of this command.

Table 7 - Configuration Register

Bit	Bit Name	Symbol	Description
7	(not used)		This bit is undefined.
6	Command Chaining Enable	CCHEN	This bit, if high, enables the Command Chaining operation of the device. Please refer to the Commain Chaining section of this document for further detail. A low level on this bit ensures software compatibility with previous SMC ARCNET devices. This bit defaults to a logic "0" upon hardware reset.
5	Decode Mode	DECODE	In I/O Mapped applications, this bit is used to choose between an 8K or 16K block of ROM. In this case, a logic "0" defines 8K, while a logic "1" defines 16K. For more detail on the use of this bit, refer to the Memory Vs. I/O Cycles section of this document. This bit defaults to a logic "0" upon hardware reset.
4, 3	Extended Timeout 1,2	ET1,ET2	These bits allow the network to operate over longer distances than the default 4 miles by controlling the Response Time, the Idle Time, and the Reconfiguration Time. For proper network operation, all nodes should be configured for the same timeout values. The bit combinations follow: ET2 / ET1 / RESPONSE TIME (uS) / IDLE TIME (uS) / RECONFIGURATION TIME (mS) 0 / 0 / 1130 / 1237 / 1680 0 / 1 / 563 / 624 / 1680 1 / 0 / 285 / 316 / 1680 1 / 1 / 78 / 86 / 840 These bits default to a logic "1" upon hardware reset.
2	Wait State	WAIT	This bit is used to select the type of cycle. A logic "1" on this bit negates the IOCHRDY signal for approximately one or two XTAL1 clocks, creating one wait state. A logic "0" selects zero wait state arbitration to the buffer RAM and generates the Zero Wait State signal. Refer to the Wait State Details section of this document for further information. This bit defaults to a logic "1" upon hardware reset.
1	I/O Access	IOACCESS	A logic "1" on this bit configures the buffer RAM for sequential I/O mapped accesses, while a logic "0" configures the buffer RAM for memory mapped accesses. This bit defaults to a logic "0" upon hardware reset.
0	Transmitter Off	TXOFF	A logic "1" on this bit disables the transmitter of the COM90C165, while the receiver remains functional. A logic "0" keeps the transmitter enabled. This bit may be used in diagnostic troubleshooting of the network or node. Refer to the Improved Diagnostics section of this document for further detail. This bit defaults to a logic "0" upon hardware reset.

Table 8 - Address Pointer Low Register

Bit	Bit Name	Symbol	Description
7-0	Address 7-0	A7-A0	These bits hold the lower 8 address bits which provide the addresses to the on-chip RAM.

Table 9 - Address Pointer High Register

Bit	Bit Name	Symbol	Description
7, 5-3	(not used)		These bits are undefined.
6	Auto Increment	AUTOINC	This bit controls whether or not the address pointer will increment automatically when the device is in I/O Mapping Mode. A logic "1" on this bit will automatically increment the pointer after each access. A logic "0" will disable this function. Please refer to the Memory Vs. I/O section of this document for further detail.
2-0	Address 10-8	A10-A8	These bits hold the upper three address bits which provide the addresses to the on-chip RAM.

INTERNAL RAM

The integration of the 2K x 8 RAM in the COM90C165 provides several advantages to the user. Firstly, a significant amount of real estate is saved due to the elimination of the external RAM, the external latch, and the multiplexed address/data bus and control functions which used to be necessary to interface to the RAM.

Secondly, the system designer is no longer dependent upon the fluctuating cost of external RAM. This and the fact that the entire solution is more integrated (reducing reliability problems, assembly time and costs, and layout complexity) adds up to significant cost reductions.

Thirdly, with the eliminated need for the RAM interfacing signals, several other innovative features now take the place of the freed-up pins without the need for increased package size and pinout. Some of the pins have been replaced with such useful features as the Zero Wait-State signal, the diagnostic pins, and the choice of Memory or I/O Mapped functionality.

Fourthly, the COM90C165 is very high speed. The ability of the device to implement zero wait state cycles is partly due to fact that the RAM is internal to the device.

The Configuration Register contains the I/O Access bit, which determines whether the RAM will be configured for sequential I/O mapped accesses or memory mapped accesses. Additionally, the Decode Mode bit allows the choice of 8K or 16K block of ROM if set for I/O mapped access.

SOFTWARE INTERFACE

The microprocessor interfaces to the COM90C165 via software by accessing the various registers. These actions were discussed in the Internal Registers section of this document. Additionally, it is necessary to understand the details of how the Internal Registers are used in the transmit and receive sequences and to know how the internal RAM buffer is properly set up. The sequence of events that tie these actions together are discussed as follows.

Transmit Sequence

During a transmit sequence, the microprocessor selects a 256 or 512 byte segment of the RAM buffer and writes into it. The appropriate buffer size is specified in the DEFINE CONFIGURATION command. When long packets are enabled, the COM90C165 interprets the packet as a long or short packet, depending on whether the content of the buffer address 2 is zero or non-zero. The format of the buffer is shown in Figure 9. Address 0 contains the Source Identifier (SID), Address 1 contains the Destination Identifier (DID), and Address 2 contains, for short packets, the value 256-N, where N represents the message length, or for long packets, the value 0, indicating that it is indeed a long packet. In the latter case, Address 3 would contain the value 512-N, where N represents the message length. The SID in Address 0 is used by the receiving node to reply to the transmitting node. The COM90C165 puts the local ID in this location, therefore it is not necessary to write into this location.

Once the buffer is written into, the microprocessor awaits a logic "1" on the TA bit, indicating that a previous transmit command has concluded and another may be issued. Each time the message is loaded and a transmit command issued, it will take a variable amount of time before the message is transmitted, depending on the traffic on the network and the location of the token at the time the transmit command was issued. Typically, the conclusion of the transmit command, which is flagged when TA becomes a logic "1", generates an interrupt. If the device is configured for the Command Chaining operation, please see the Command Chaining section of this document for further detail on the software.

Once the TA bit becomes a logic "1", the microprocessor issues the ENABLE TRANSMIT FROM PAGE nn command, which resets the TA and TMA bits to logic "0". If the message is not a BROADCAST, the COM90C165 automatically issues a FREE BUFFER ENQUIRY to the destination node in

order to send the message. At this point, one of three possibilities may occur.

The first possibility is if a free buffer is available at the destination node, in which case it responds with an ACKnowledgement. At this point, the COM90C165 fetches the data from the Transmit Buffer and performs the transmit sequence. After a successesful transmit sequence is completed, the TMA bit and the TA bit are set to logic "1".

The second possibility is if the destination node responds with a Negative AcKnowledgement. A NAK occurs when the RI bit of the destination node is a logic "1". In this case, the token is passed on from the transmitting node to the next node. The next time the transmitter receives the token, it will try to retransmit a FREE BUFFER ENQUIRY. If a NAK is again received, the token is again passed onto the next node. A software timeout on the TA bit is used to prevent this from happening endlessly. That is, if no software timeout existed, the transmitting node would keep trying to issue a Free Buffer Enquiry, even though it keeps receiving NAK's as a response. The software timeout on the TA bit is used to tell the microprocessor to disable the transmitter via the DISABLE TRANSMITTER command, which will cause the transmission to be abandoned and the TA bit to be set to a logic "1" when the node next receives the token, while the TMA bit remains at a logic "0".

The third possibility which may occur after a FREE BUFFER ENQUIRY is issued is if no response is received from the destination node. In this case, the TA bit is set to a logic "1" in preparation for the next time the token is received, while the TMA bit remains at a logic "0". The user should determine whether the node will try to retransmit the next time it receives the token.

The Disable Transmitter command may be used to cancel any pending transmit command when the COM90C165 next receives the token. Normally, in an active network, this command will set the TA status bit to a logic "1" when the token is received. If the disable transmitter command does not cause the TA bit to be set in the time it takes the token to make a round trip through the network, one of three situations exists. Either the node is disconnected from the network, or there are no other nodes on the network, or the external receive circuitry has failed. These situations can be determined either by using the Improved Diagnostics features of the COM90C165 or by using another software timeout which is greater than the worst case time for a round trip token pass which occurs when all nodes transmit a maximum length message.

Receive Sequence

A receive sequence begins with the RI status bit becoming a logic "1", which indicates that a previous reception has concluded. The microprocessor will be interrupted if the corresponding bit in the Interrupt Mask Register is set to logic "1". Otherwise, the microprocessor must periodically check the Status Register. Once the microprocessor is alerted to the fact that the previous reception has concluded, it may issue the ENABLE RECEIVE TO PAGE nn command, which resets the RI bit to logic "0" and selects a new page in the RAM buffer. Again, the appropriate buffer size is specified in the DEFINE CONFIGURATION command. Typically, the page which just received the data packet will be read by the microprocessor at this point.

Once the ENABLE RECEIVE TO PAGE nn command is issued, the microprocessor attends to other duties. There is no way of telling how long the new reception will take, since another node may transmit a packet at any time. When another node does transmit a packet to this node, if the DEFINE CONFIGURATION command has enabled the reception of long packets, the COM90C165 interprets the packet as a long or short packet, depending on whether the content of the buffer location 002 is zero or non-zero. The format of the buffer is shown in Figure 9. Address 0 contains the Source Identifier (SID), Address 1 contains the Destination Identifier (DID), and Address 2 contains, for short packets, the value 256-N, where N represents the message length, or for long packets, the value 0, indicating that it is indeed a long packet. In the latter case, Address 3 contains the value 512-N, where N represents the message length. Note that the COM90C165 deposits packets in the RAM buffer in the same format that the transmitting node aranged it, which allows for a message to be received and then retransmitted without rearranging any bytes in the RAM buffer. Once the packet is received and stored correctly in the selected buffer, the COM90C165 sets the RI bit to logic "1" to signal the microprocessor that the reception is complete.

SOFTWARE COMPATIBILITY CONSIDERATIONS

The COM90C165 guarantees compatibility with previous SMC ARCNET devices. Upon software or hardware reset, the device defaults to compatibility mode. That is, upon reset, the device defaults to 8-bit, memory mapped cycles, the device is in the non-Command Chaining mode and the non-Zero Wait State mode.

COMMAND CHAINING

The Command Chaining operation allows consecutive transmissions and receptions to occur without host intervention. Through the use of a dual two-level FIFO, commands to be transmitted and received, as well as the status bits, are pipelined.

In order for the COM90C165 to be compatible with previous SMC ARCNET devices, the device defaults to the non-chaining mode. In order to take advantage of the Command Chaining operation, the Command Chaining Mode must be enabled via a logic "1" on bit 7 of the Configuration Register.

The following is a list of Command Chaining guidelines for the software programmer to follow. Further detail can be found in the Transmit Command Chaining and Receive Command Chaining sections of this document.

- The device is designed such that the interrupt service routine latency does not affect performance. The first interrupt may be serviced prior to the generation of the second interrupt.

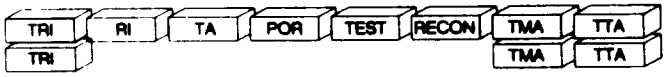
- Up to two outstanding transmissions and two outstanding receptions can be pending at any given time. The commands may be given in any order.

- Up to two outstanding transmit interrupts and two outstanding receive interrupts are stored by the device, along with their respective status bits.

- The Interrupt Mask bits act on TTA (Rising Transition on Transmitter Available) for transmit operations and TRI (Rising Transition of Receiver Inhibited) for receive operations. TTA is set upon completion of a packet transmission only. TRI is set upon completion of a packet reception only. Typically there is no need to mask the TTA and TRI bits after clearing the interrupt.

- The traditional TA and RI bits are still available to reflect the present status of the device.

In Command Chaining, the Status Register looks as follows:



Transmit Command Chaining

When the processor issues the first ENABLE TRANSMIT TO PAGE nn command, the COM90C165 responds in the usual manner by resetting the TA and TMA bits to prepare for the transmission from the specified page. The TA bit can be used to see if there is currently a transmission pending, but the TA bit is really meant to be used in the non-chaining mode only. The TTA bits provide the relevant information of the device in the Command Chaining mode.

In the Command Chaining Mode, at any time after the first command is issued, the processor can issue a second ENABLE TRANSMIT FROM PAGE nn command. The COM90C165 stores the fact that the second transmit command was issued, along with the page number.

After the first transmission is completed, the COM90C165 updates the Status Register by setting the TTA bit, which generates an interrupt. The interrupt service routine will read the Status Register. At this point, the TTA bit will be found to be a logic "1" and the TMA (Transmit Message Acknowledge) bit will tell the processor whether the transmission was successful. After reading the Status Register, the CLEAR TRANSMIT INTERRUPT command is issued, thus resetting the TTA bit and clearing the interrupt. Note that only the CLEAR TRANSMIT INTERRUPT command will clear the TTA bit and the interrupt. It is not necessary, however, to clear the bit or the interrupt right away because the status of the transmit operation is double buffered in order to retain the results of the first transmission for analysis by the processor. This information will remain in the Status Register until the CLEAR TRANSMIT INTERRUPT command is issued. Note that the interrupt will remain active until the command is issued, and the second interrupt will not occur until the first interrupt is cleared. The TMA bit is also double buffered to reflect whether the appropriate transmission was a success. The TMA bit should only be considered valid after the corresponding TTA bit has been set to a logic "1". The TMA bit never causes an interrupt.

When the token is received again, the second transmission will be automatically initiated after the first is completed by using the stored ENABLE TRANSMIT FROM PAGE nn command. The operation is as if a new ENABLE TRANSMIT FROM PAGE nn command has just been issued. After the first Transmit status bits are cleared, the Status Register will again be updated with the results of the second transmission and a second interrupt resulting from the second transmission will occur. The COM90C165 guarantees a minimum of 200nS interrupt inactive time interval before the following edge.

The Transmitter Available (TA) bit of the Interrupt Mask Register now masks only the TTA bit of the Status Register, not the TA bit as in the non-chaining mode. Since the TTA bit is only set upon transmission of a packet (not by RESET), and since the TTA bit may easily be reset by issuing a CLEAR TRANSMIT INTERRUPT command, there is no need to use the TA bit of the Interrupt Mask Register to mask interrupts generated by the TTA bit of the Status Register.

In both the Command Chaining mode and the non-chaining mode, the DISABLE TRANSMITTER command will cancel the oldest transmission. This permits cancelling a packet destined for a node not ready to receive. If both packets should be cancelled, two DISABLE TRANSMITTER commands should be issued.

Receive Command Chaining

Like the Transmit Command Chaining operation, the processor can issue two consecutive ENABLE RECEIVE FROM PAGE nn commands.

After the first packet is received into the first specified page, the TRI bit of the Status Register will be set to logic "1", causing an interrupt. Again, the interrupt need not be serviced immediately. Typically, the interrupt service routine will read the Status Register. At this point, the RI bit will be found to be a logic "1". After reading the Status Register, the CLEAR RECEIVE INTERRUPT command will be issued, thus resetting the TRI bit and clearing the interrupt. Note that only the CLEAR RECEIVE INTERRUPT command will clear the RI bit and the interrupt. It is not necessary, however, to clear the bit or the interrupt right away because the status of the receive operation is double buffered in order to retain the results of the first reception for analysis by the processor, therefore the information will remain in the Status Register until the CLEAR RECEIVE INTERRUPT command is issued. Note that the interrupt will remain active

until the CLEAR RECEIVE INTERRUPT command is issued, and the second interrupt will not occur until the first interrupt is acknowledged.

The second reception will occur as soon as a second packet is sent to the node, as long as the second ENABLE RECEIVE TO PAGE nn command was issued. The operation is as if a new ENABLE RECEIVE TO PAGE nn command has just been issued. A second interrupt will not occur until the first interrupt is acknowledged by issuing the CLEAR RECEIVE INTERRUPT command. After the first Receive status bits are cleared, the Status Register will again be updated with the results of the second reception and a second interrupt resulting from the second reception will occur. A minimum of 200nS interrupt inactive time interval before the following rising edge is guaranteed.

In the COM90C165, the Receive Inhibit (RI) bit of the Interrupt Mask Register now masks only the TRI bit of the Status Register, not the RI bit as in the non-chaining mode. Since the TRI bit is only set upon reception of a packet (not by RESET), and since the TRI bit may easily be reset by issuing a CLEAR RECEIVE INTERRUPT command, there is no need to use the RI bit of the Interrupt Mask Register to mask interrupts generated by the TRI bit of the Status Register.

In both the Command Chaining mode and the non-chaining mode, the DISABLE RECEIVER command will cancel the oldest reception, unless the reception has already begun. If both receptions should be cancelled, two DISABLE RECEIVER commands should be issued.

RESET DETAILS

Internal Reset Logic

The COM90C165 includes special reset circuitry to guarantee smooth operation during reset. Special care is taken to assure proper operation in a variety of systems and modes of operation. The design ensures that the COM90C165 will not disturb the microprocessor or the system bus until the system has reached a certain level of operation. Furthermore, in order to eliminate conflicts with other memory elements, the internal RAM of the COM90C165 is hidden from the system until a software reset is issued to the device. When the system software determines that no conflicts will arise, it then may enable the internal memory of the COM90C165 via a software reset. Because most system buses are inherently noisy, the COM90C165 contains digital filter circuitry and a Schmitt Trigger on the RESET IN signal to reject glitches in order to ensure fault-free operation.

The COM90C165 supports two reset options; software and hardware reset. An internal reset signal of pulse width equal to 102.4 μS is generated from either a hardware or a software reset. The hardware reset occurs when a high signal is asserted on the RESET IN input (pin 65). The minimum reset pulse width is 120 nS (or 2T+20 nS for crystal frequencies other than 20MHz, where T = 1/f). This pulse width is used by the internal digital filter, which filters short glitches to only allows valid resets to occur. A software reset is generated when the microprocessor accesses I/O locations 8, 9, A, or B.

Upon hardware reset, the transmitter portion of the device is disabled and the Status, Interrupt Mask, Diagnostic Status, and Configuration Registers assume the following states. The Status Register will also assume the following state following a software reset. (Note: ONLY the Status Register is affected upon software reset.)

BIT 7 (RI) =1
BIT 6 (not used) undefined
BIT 5 (not used) undefined
BIT 4 (POR) =1
BIT 3 (TEST) =0
BIT 2 (RECON) =0
BIT 1 (TMA) =0
BIT 0 (TA) =1

The Interrupt Mask Register assumes the following state:

BIT 7 (RI) =0
BIT 6 (not used) =0
BIT 5 (not used) =0
BIT 4 (ENDIAG) =0
BIT 3 (not used) =0
BIT 2 (RECON) =0
BIT 1 (not used) =0
BIT 0 (TA) =0

The Diagnostic Status Register assumes the following state:

BIT 7 (MYRECON) =0
BIT 6 (not used) =undefined
BIT 5 (RCVACT) =0
BIT 4 (TOKEN) =0
BIT 3 (not used) =undefined
BIT 2 (not used) =undefined
BIT 1 (not used) =undefined
BIT 0 (not used) =undefined

The Configuration Register assumes the following state:

BIT 7 (not used) =undefined
BIT 6 (CCHEN) =0
BIT 5 (DECODE) =0
BIT 4 (ET1) =1
BIT 3 (ET2) =1
BIT 2 (WAIT) =1
BIT 1 (IOACCESS) =0
BIT 0 (TXOFF) =0

The Data Register and Address Pointer Register both contain undefined data upon reset.

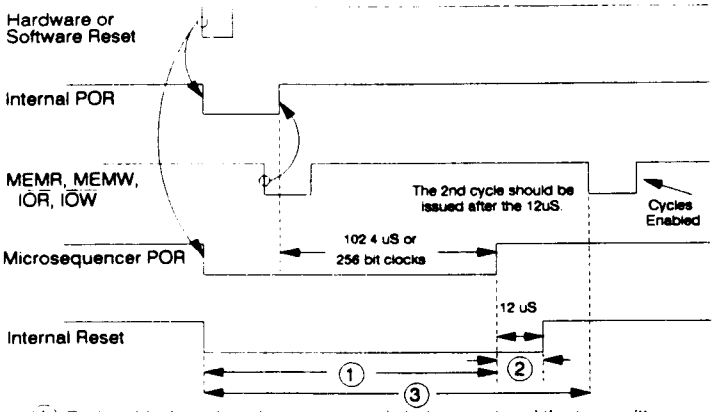
The COM90C165 will start 102.4 μS after the RESET IN signal is removed. Please note that the internal RAM buffer cannot be seen by the processor unless a software reset is issued. Therefore, following power up or hardware reset, a software reset must be issued. Note that this causes an additional delay. After this time, the COM90C165, after reading its own ID, will execute two write cycles to the RAM buffer. Address 00 HEX will be written with the data D1 HEX and address 01 HEX will be written with the ID number read from the Node ID Select Switch. The processor may then read RAM buffer address 01 to determine the ID of the COM90C165. Note that the data pattern D1 written into the RAM has been chosen arbitrarily. Only if the D1 pattern appears in the RAM buffer can proper operation be assured.

System Reset Logic

The IBM XT Bus automatically provides continuously running cycles for $\overline{MEMR}$, $\overline{MEMW}$, $\overline{IOR}$, and $\overline{IOW}$ which are utilized by the COM90C165 in its internal reset sequence.

Buses other than the IBM XT (or compatible) typically do not provide continuously running cycles. In this case, the user will need to note the following COM90C165 internal reset sequence so that the software interface will provide the proper accesses utilized by the device. Please refer to Figure 10. By satisfying the simple requirements below, the user can be assured proper operation of the COM90C165's reset sequence in a non-IBM XT environment.

A hardware or software reset begins the COM90C165's internal Power On Reset. An access cycle ($\overline{MEMR}$, $\overline{MEMW}$, $\overline{IOR}$, $\overline{IOW}$) must then occur in order to end the internal Power On Reset. At this point, an internal timeout of 102.4μS or 256 clocks occurs. After the timeout is completed, a second timeout of 12μS occurs. At the completion of the second timeout the reset sequence is complete. Any accesses thereafter will be considered valid accesses.



(1) During this time, the microsequencer is being reset and the transmitter portion of the device is disabled.
(2) During this time, the microsequencer writes D1H to address 00H, and the Node ID number to address 01H. The transmitter portion of the device is enabled.
(3) During this time, the $\overline{TOPL}$ and $\overline{PROM}$ signals are a logic "1"; the INTR signal is a logic "0"; the data bus is in the high impedance state; and the IOCHRDY signal is in normal operation.

FIGURE 10 - INTERNAL RESET SEQUENCE

READ AND WRITE CYCLES

Memory Vs. I/O Cycles

In addition to Memory Mapping, the COM90C165 performs Sequential I/O Mapped Memory accesses, thus a packet that is placed in the internal RAM buffer can be accessed by addressing only one 8-bit I/O location. The processor places the address that needs to be accessed into the Address Pointer by writing it as data to address OEH (Address Pointer Low Register). The processor then reads/writes from/to address 0CH the data found/to be placed at that address. If the Auto Increment bit is turned on, the Address Pointer will then increment the address by one until the entire packet is obtained/sent.

Although Sequential I/O Mapped RAM accesses require more steps than Memory Mapped accesses, I/O Mapped is just as efficient as Memory Mapped and does not require the large block of memory in the host addressing space that Memory Mapped does. On the other hand, Memory Mapped access is more flexible and allows the processor to analyze the data and make decisions without emptying the entire packet into system memory. Refer to Figure 11 for an illustration of the Sequential I/O Mapped Memory access operation.

The COM90C165 allows design versatility in that the board can be software configured for memory mapped or I/O mapped mode, depending on the system constraints. The following is some basic information on both Memory and I/O Modes so that the user can determine which mode is best suited for the application.

Memory Mapped Mode -

On any address bus, all address lines must at some point be latched. On the XT Bus, all of the address lines are latched on the motherboard. For other buses such as the Micro Channel® bus, the lines are not latched and thus must be latched externally by the user. The COM90C165 provides the transparent latch necessary for unlatched addresses on the Micro Channel® and other buses.

Refer to Table 10 for the Memory Mapped Decode table as a function of the $\overline{ENROM}$ pin and the DECODE MODE bit.

Table 10 - Memory Mapped Decode

$\overline{ENROM}$	DECODE MODE	RAM	ROM
0	X	2K	8K
1	0	2K	-
1	1	2K	-

The internal latches of the COM90C165 go transparent on BALE high and latch on BALE low. If all addresses being used are already latched, or valid for the entire duration of the cycle, then the BALE signal may be tied to a logic "1".

I/O Mapped Mode -

The system can also be configured as I/O mapped. In this case, the data transfers to and from the packet buffer are done by accessing an I/O location and having the internal pointer in the device sequentially address memory.

In the I/O mapped mode, addresses up to A15 are decoded to determine accesses to the device. On the XT bus the A0-A15 lines are provided as latched addresses. Therefore, the BALE signal may be tied to a logic "1". In the I/O Mode, no memory is used by the board except for the optional PROM.

A logic "0" on the $\overline{\text{ENROM}}$ pin enables ROM mapping, and in the I/O mapped mode the user can choose between an 8K or 16K block of ROM.

Refer to Table 11 for the I/O Mapped Decode table as a function of the $\overline{\text{ENROM}}$ pin and the DECODE MODE bit.

Table 11 - I/O Mapped Decode

$\overline{\text{ENROM}}$	DECODE MODE	RAM	ROM
0	0	I/O	8K
0	1	I/O	16K
1	X	I/O	-

Wait State Details

In the typical computer, the Bus Speed will be slower than the CPU speed so that the peripherals will be able to keep up with the machine. In many cases, the peripheral will need additional delays to be able to keep up, and will therefore use the IOCHRDY signal to tell the processor whether or not is is ready to continue. The use of the IOCHRDY signal effectively "slows down" the bus.

The COM90C165 is quick enough to take advantage of the maximum bus speed of most AT compatibles. This function employs the use of the $\overline{\text{0WS}}$ signal and guarantees the fastest microprocessor cycles. The use of the $\overline{\text{0WS}}$ signal effectively "speeds up" the bus.

Upon power up, the COM90C165 defaults to the non-zero wait state mode. The $\overline{\text{0WS}}$ mode can be easily configured by resetting bit 2 of the Configuration Register to a logic "0" in the initialization software.

For machines with faster buses, the COM90C165 can be configured to negate the IOCHRDY line for the minimal period of time necessary. If the IOCHRDY signal is used, it is negated for one XTAL1 clock for RAM and internal register cycles. If the optional PROM is on board, it might require a slower cycle to accommodate its access time even if the device is configured for Zero Wait State Mode. When the $\overline{\text{ENROM}}$ signal is active (logic "0"), the COM90C165 will negate the IOCHRDY signal for two XTAL1 clocks on ROM read accesses. If the optional external register is used, I/O Write cycles to it will also cause a negation of the IOCHRDY signal for two XTAL1 clocks. Note that by timing the ready circuitry from the XTAL1 clock, the IOCHRDY signal is timed in absolute time rather than relative to the bus clock.

Either the $\overline{\text{0WS}}$ signal or the IOCHRDY signal should be used (but not both), depending upon the speed of the bus. In the case where the COM90C165 spec meets the bus speed and the user does not need to "speed up" or "slow down" the bus, neither the $\overline{\text{0WS}}$ nor the IOCHRDY signal should be used. In this case, the Wait State bit of the Configuration Register should be reset to logic "0" to configure the device for Zero Wait State, but the $\overline{\text{0WS}}$ signal should not be connected to the bus. Figure 2 shows a jumper between the $\overline{\text{0WS}}$ signal and the bus to illustrate that the signal may be left unconnected. Table 12 shows the IOCHRDY and $\overline{\text{0WS}}$ signal behavior for RAM, internal register, external PROM, and external register access.

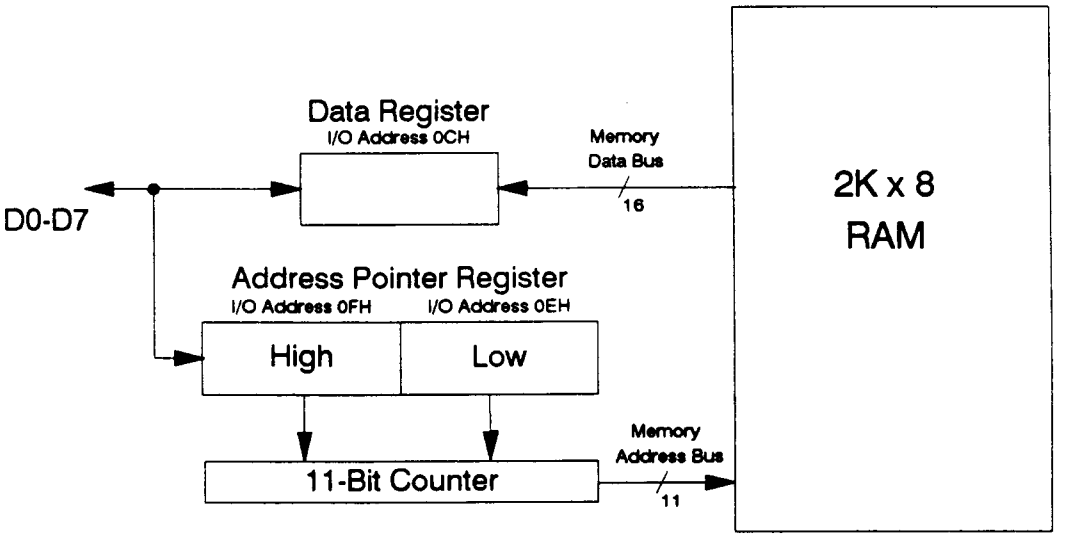


FIGURE 11 - SEQUENTIAL I/O MAPPED MEMORY ACCESS OPERATION

Please refer to the Zero Wait State and IOCHRDY Timing Diagram towards the end of this document for further details on the specifications of these two signals.

Table 12 - IOCHRDY and $\overline{0WS}$ Signal Behavior

Wait State Bit	IOCHRDY	$\overline{0WS}$
0	logic "1"	Activated on Access
1	Negated for One or Two XTAL1 Clocks	logic "1"

NODE ID LOGIC

The Node ID code generated by the external Node ID Select Switches is used to identify this particular COM90C165. The code, which is input by the COM90C165 in parallel format, is used by the COM90C165 during transmission, reception, reset, and reconfiguration.

Upon reset, the COM90C165 reads the Node ID code set up on the switches and loads them into the Node ID Register. For diagnostic purposes, the Node ID may be read by the microprocessor. The ARCNET protocol maintains that a destination Node ID of 00H will allow the source node to broadcast a message.

In addition, in order to provide the user with increased flexibility and to eliminate the cost of the Node ID switch on board, the COM90C165 provides special circuitry which allows the user to program the Node ID of any node via software. To software program the Node ID register, the Node ID switches of that node must be physically set to 00H. 00H is not recognized by the ARCNET protocol as a valid Node ID and therefore is used only to switch to this special mode. Setting the Node ID switches to all zero's puts the COM90C165 into a reset. The device will not attempt to join the network and no microcode is performed. Tokens are not passed and reconfigurations are not generated by the node. The device will not attempt to rejoin the network until a valid Node ID value is placed into the Node ID Register.

For normal operation, the Node ID switches will be set to some valid address between 01H and FFH. Writing a non-zero value to the Node ID register will allow the COM90C165 to join the network.

TRANSMIT/RECEIVE LOGIC

Figure 12 illustrates the events which occur in transmission or reception of data consisting of 1,1,0. The COM90C165, during transmission, produces two 100 nS nonoverlapping pulses on the $\overline{PULSE1}$ and $\overline{PULSE2}$ lines to indicate a logic "1", whereas a lack of pulses indicates a logic "0". The $\overline{PULSE1}$ and $\overline{PULSE2}$ signals are used to drive the HYC9058, the HYC9068 or the HYC9088, which in turn creates a 200 nS dipulse signal on the transmission media. During reception, each dipulse appearing on the transmission media is coupled through the RF transformer of the LAN Driver to produce a positive pulse on the RXIN pin. The pulse is captured by the COM90C165 and is then converted to NRZ data. Typically, RXIN pulses occur at multiples of 400 nS, plus or minus 100 nS and still correctly capture and convert the RXIN pulses to NRZ format.

IMPROVED DIAGNOSTICS

The COM90C165 allows the user to better manage the operation of the network through the use of improved diagnostics within the device.

A high level on the My Reconfiguration (MYRECON) bit indicates that the reconfiguration which has just taken place was caused by this particular node. After the Reconfiguration (RECON) bit of the Status Register interrupts the processor, the interrupt service routine will typically read the MYRECON bit of the Diagnostic Status Register. Successive occurances of a logic "1" on the MYRECON bit indicates that something is wrong with this node. At that point, the transmitter should be disabled so that the entire network is not continuously brought down while the node is being evaluated.

The Receive Activity (RCVACT) bit of the Diagnostic Status Register will be set to a logic "1" whenever a rising edge of NRZ data is detected on the RXIN pin.

The Token Seen (TOKEN) bit of the Diagnostic Status Register will be set to a logic "1" whenever any token has been seen on the network (except those tokens transmitted by this node).

The RCVACT and TOKEN bits of the Diagnostic Status Register may help the user to troubleshoot the network or the node. If unusual events are occuring on the network, the user may find it valuable to use the TXOFF bit of the Configuration Register to qualify events. Different combinations indicate different types of problems.

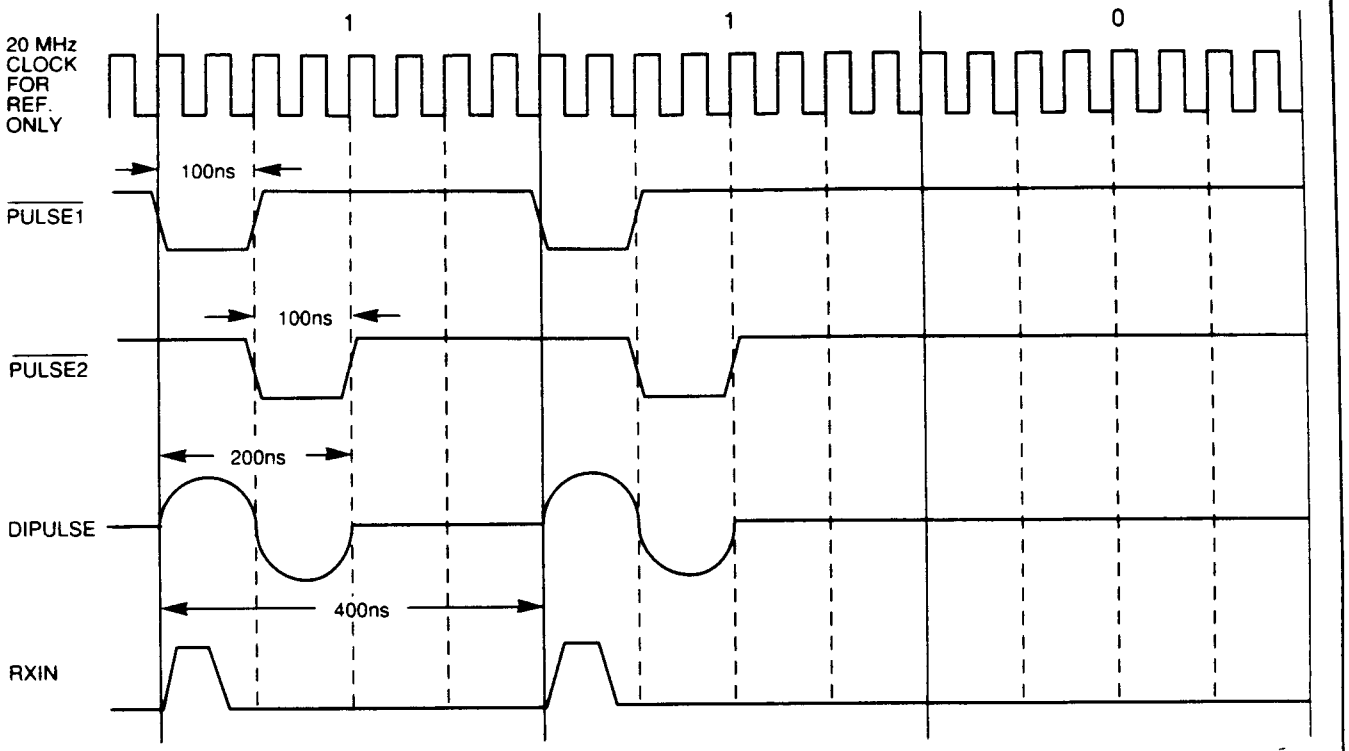


FIGURE 12 - DIPULSE GENERATION AND RECEIVE WAVEFORM FOR DATA OF 1, 1, 0

RCVACT	TOKEN	TXOFF	
Normal Results:			
1	1	1	The node is not part of the network. The network is operating properly without this node.
1	1	0	The node sees receive activity and sees the token. Transmitter is enabled. Network and node are operating properly.
Abnormal Results:			
1	0	X	The node sees receive activity, but does not see the token. Either no other nodes exist on the network, some type of data corruption exists, the media driver is not functioning properly, the topology is set up incorrectly, there is noise on the network, or a reconfiguration is occuring.
0	0	0	No receive activity and transmitter is enabled. The transmitter and/or receiver are not functioning properly.
0	0	1	No receive activity and transmitter disabled. This node is not connected to the network.

In addition to the Diagnostic Status Register bits, the COM90C165 contains two pins for direct connection to LED's. These pins are meant to immediately provide basic visual information on board and network activity with decreased dependence upon software. The COM90C165 contains an internal retriggerable digital one-shot which allows the $\overline{\text{TXLED}}$ to light for 726 uS ± 10% each time the COM90C165 transmits information. Every time the host accesses either the internal RAM, registers, or external PROM, the $\overline{\text{BSLED}}$ will light for 400 mS ± 20%. The sink capability of both the $\overline{\text{TXLED}}$ and $\overline{\text{BSLED}}$ pins is 10mA, thus allowing direct connection to the LED's to be supported by the COM90C165. The only additional components are 500Ω resistors between the LED's and V_{CC}.

OSCILLATOR

The COM90C165 incorporates on-board circuitry which, in conjunction with an external parallel resonant crystal, forms an oscillator. The oscillator frequency may vary from 8 MHz to 20MHz to allow for a variable data rate from 1.0 Mbps to 2.5 Mbps.

The COM90C165 crystal oscillator has been designed to work with a parallel resonant crystal. Only two capacitors are needed (one from each leg of the crystal to ground). The values of the capacitors are two times the load capacitance of the crystal. The COM90C165 contains an internal 1 MΩ resistor. The external crystal must have an accuracy of 0.020% or better.

OPERATIONAL DESCRIPTION

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -55°C to +150°C
Lead Temperature (soldering, 10 seconds) ..... +325°C
Positive Voltage on any pin, with respect to ground ..... V_{CC} +0.3V
Negative Voltage on any pin, with respect to ground ..... -0.3V
Maximum V_{CC} ..... +7V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

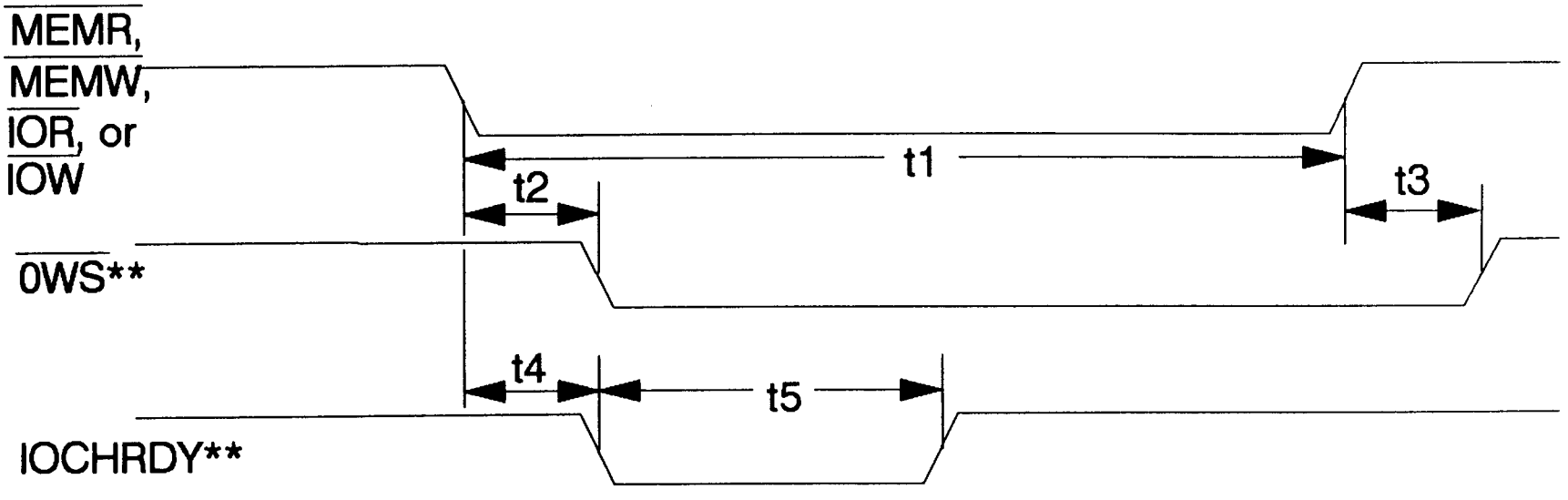
DC ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	COMMENTS
Low Input Voltage 1 (All inputs except XTAL1, RESET, AEN, IOR, IOW, MEMR, MEMW)	V_{IL1}			0.8	V	TTL Levels
High Input Voltage 1 (All inputs except XTAL1, RESET, AEN, IOR, IOW, MEMR, MEMW)	V_{IH1}	2.0			V	TTL Levels
Low Input Voltage 2 (XTAL1)	V_{IL2}			1.0	V	TTL Clock Input
High Input Volgage 2 (XTAL1)	V_{IH2}	4.0			V	
Low to High Threshold Input Voltage (RESET, AEN, IOR, IOW, MEMR, MEMW)	V_{ILH}		1.8		V	Schmitt Trigger, All Values at V_{DD} = 5V
High to Low Threshold Input Voltage (RESET, AEN, IOR, IOW, MEMR, MEMW)	V_{IHL}		1.2		V	
Low Output Voltage 1 (PULSE1, PULSE2, TOPL, PROM, CLK, CACLK)	V_{OL1}			0.4	V	I_{SINK} = 4mA
High Output Volgage 1 (PULSE1, PULSE2, TOPL, PROM, CLK, CACLK)	V_{OH1}	2.4			V	I_{SOURCE} = -12mA
Low Output Voltage 2 (D0-D7)	V_{OL2}			0.4	V	I_{SINK} = 16mA
High Output Voltage 2 (D0-D7)	V_{OH2}	2.4			V	I_{SOURCE} = -12mA
Low Output Voltage 3 (INTR)	V_{OL3}			0.8	V	I_{SINK} = 24mA
High Output Voltage 3 (INTR)	V_{OH3}	2.4			V	I_{SOURCE} = -10mA
Low Output Voltage 4 (IOCHRDY, 0WS)	V_{OL4}			0.5	V	I_{SINK} = 24mA Open Drain Drivers
Low Output Voltage 5 (TXLED, BSLED)	V_{OL5}			0.4	V	I_{SINK} = 12mA
V_{CC} Supply Current 1	I_{CC1}			20.0	mA	No output loads. All inputs at 0V or V_{CC}, at a Baud Rate of 4MHz.
Input Pull-Up Current	I_P	2.0			V	
Input Leakage Current	I_L	-10.0		+10.0	μA	V_{IN} = 0 to V_{CC}

CAPACITANCE (T_A = 25°C; f_C = 1MHz; V_{CC} = 0V)
Output and I/O pins capacitive load specified as follows:

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	COMMENTS
Input Capacitance	C_{IN}			0.5	pF	
Output Capacitance 1 (All outputs except IOCHRDY, 0WS)	C_{OUT1}			45	pF	
Output Capacitance 2 (IOCHRDY, 0WS)	C_{OUT2}			240	pF	
Output Capacitance 3 (INTR)	C_{OUT3}			120	pF	

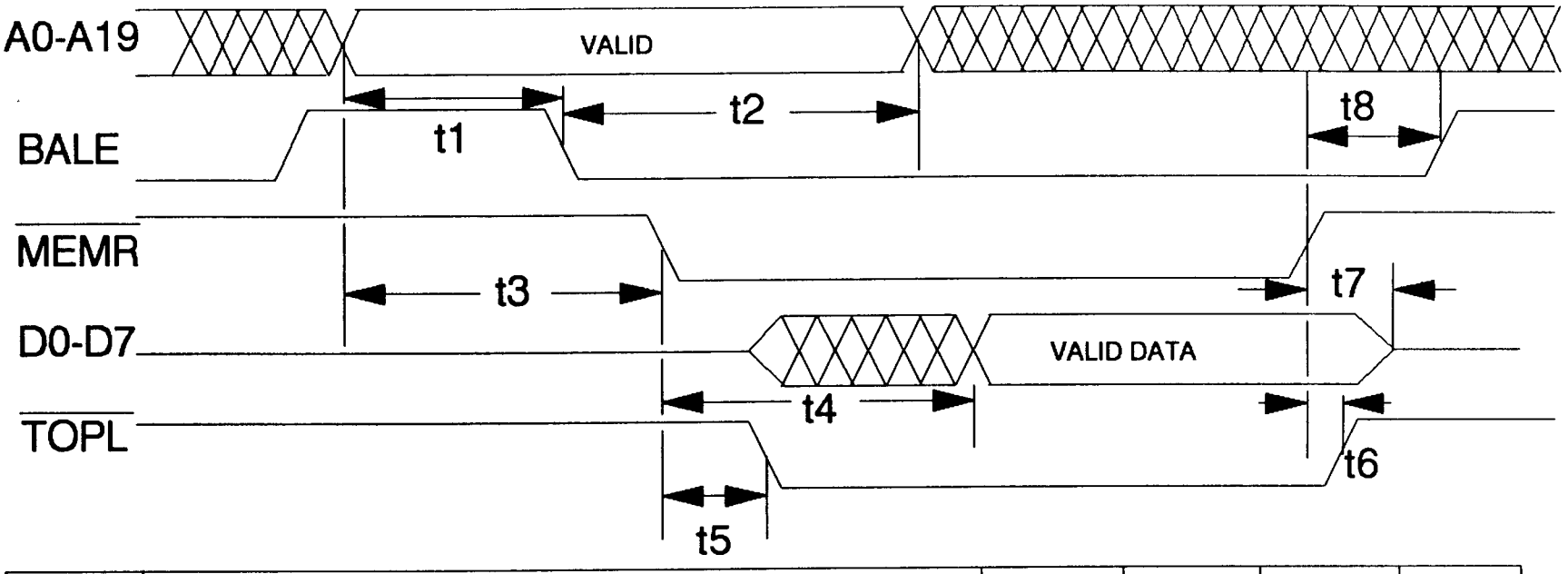
The AC parameters in Figures 13-25 are preliminary.
Enhancements will follow.



	Parameter	min	typ	max	units
t1	Control Signal Pulse Width	80		1200	nS
t2	Control Signal Low to 0WS Low	0		20	nS
t3	Control Signal High to 0WS High	0		20	nS
t4	Control Signal Low to IOCHRDY Low	0		20	nS
t5	IOCHRDY Low Pulse Width	50		115	nS

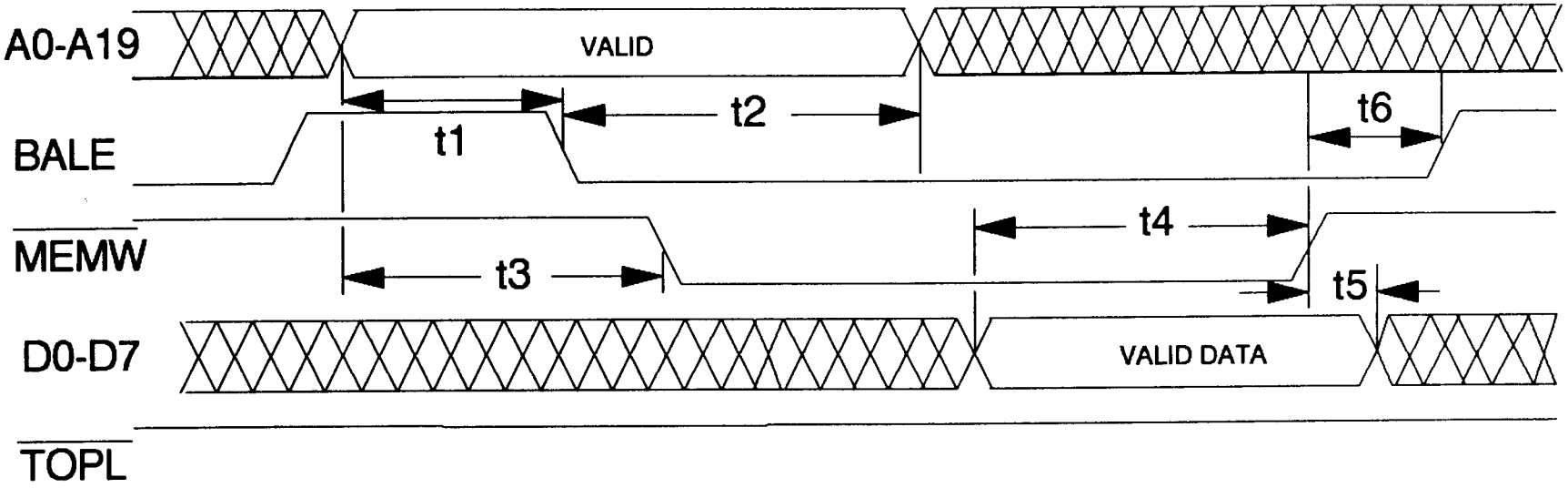
** These signals are mutually exlusive. Only one signal is active on any given board, depending on the WAIT STATE bit of the Configuration Register.

FIGURE 13 - ZERO WAIT STATE AND IOCHRDY TIMING



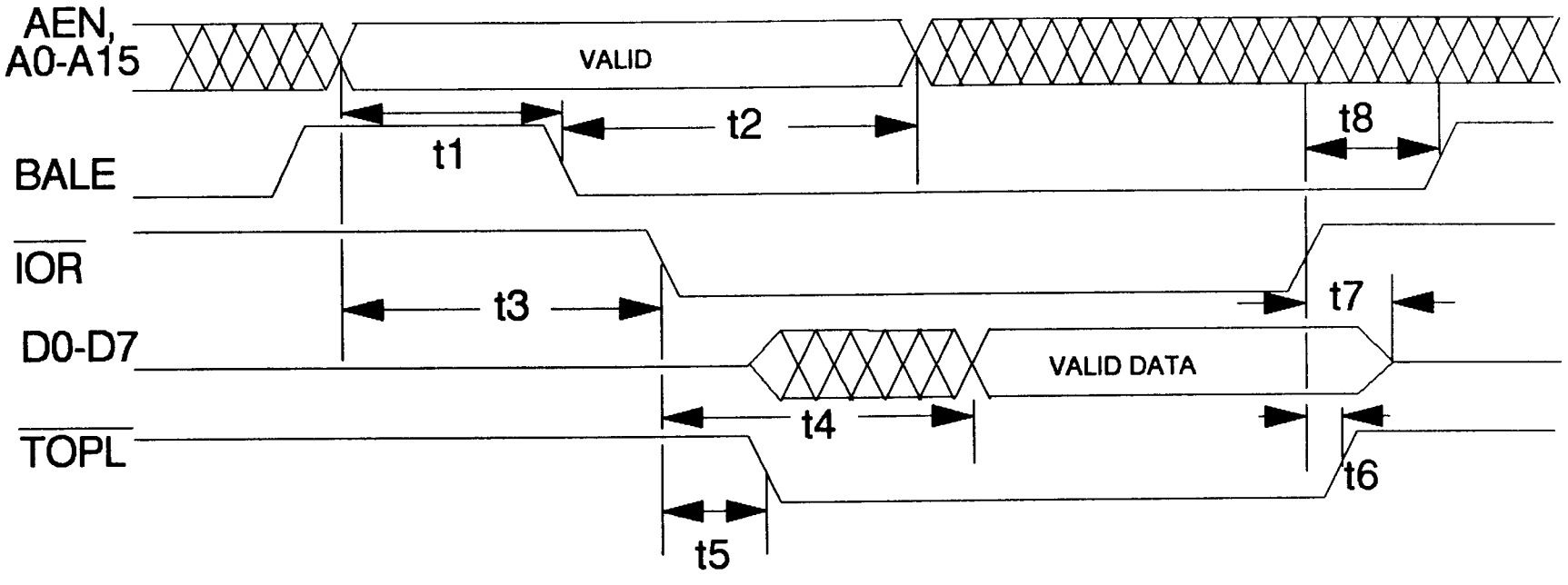
	Parameter	min	typ	max	units
t1	Address Set Up to BALE Low	20			nS
t2	Address Hold after BALE Low	20			nS
t3	Address Set Up to $\overline{\text{MEMR}}$ Low	25			nS
t4	$\overline{\text{MEMR}}$ Low to Valid Data			125	nS
t5	$\overline{\text{MEMR}}$ Low to $\overline{\text{TOPL}}$ Low	0		30	nS
t6	$\overline{\text{MEMR}}$ High to $\overline{\text{TOPL}}$ High	0		15	nS
t7	$\overline{\text{MEMR}}$ High to Data High Impedance	0		20	nS
t8	$\overline{\text{MEMR}}$ High to BALE High (Next Address)	30			nS

FIGURE 14 - READ RAM CYCLE



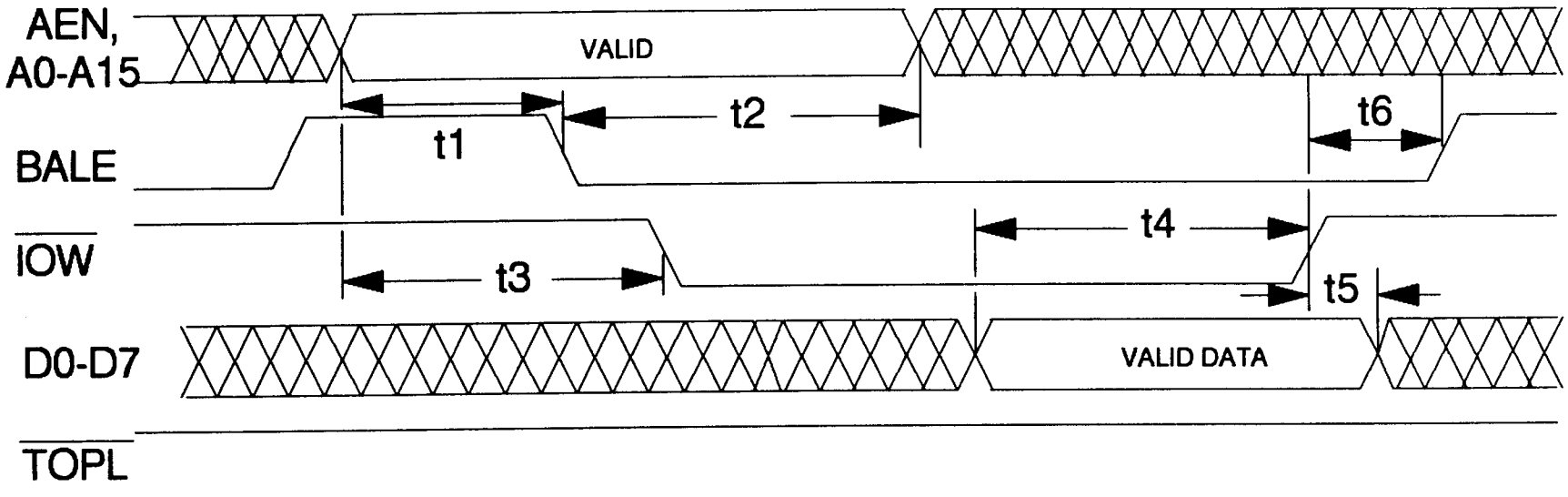
	Parameter	min	typ	max	units
t1	Address Set Up to BALE Low	20			nS
t2	Address Hold after BALE Low	20			nS
t3	Address Set Up to MEMR Low	25			nS
t4	Valid Data Set Up to MEMW High	30			nS
t5	Data Hold Time from MEMW High	9			nS
t6	MEMW High to BALE High (Next Address)	30			nS

FIGURE 15 - WRITE RAM CYCLE



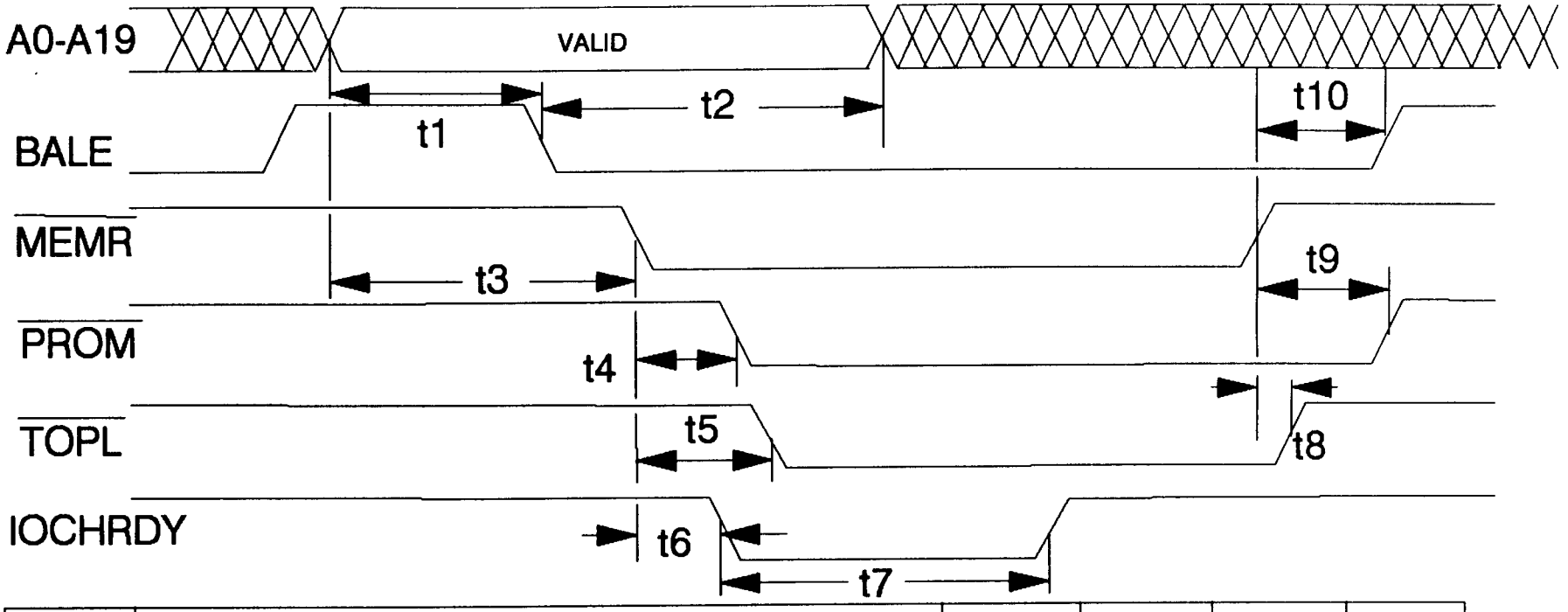
	Parameter	min	typ	max	units
t1	Address, AEN Set Up to BALE Low	20			nS
t2	Address, AEN Hold after BALE Low	20			nS
t3	Address, AEN Set Up to IOR Low	25			nS
t4	IOR Low to Valid Data			125	nS
t5	IOR Low to TOPL Low	0		30	nS
t6	IOR High to TOPL High	0		15	nS
t7	IOR High to Data High Impedance	0		20	nS
t8	IOR High to BALE High (Next Address)	30			nS

FIGURE 16 - READ I/O CYCLE



	Parameter	min	typ	max	units
t1	Address, AEN Set Up to BALE Low	20			nS
t2	Address, AEN Hold after BALE Low	20			nS
t3	Address, AEN Set Up to IOW Low	25			nS
t4	Valid Data Set Up to IOW High	30			nS
t5	Data Hold Time from IOW High	9			nS
t6	IOW High to BALE High (Next Address)	30			nS

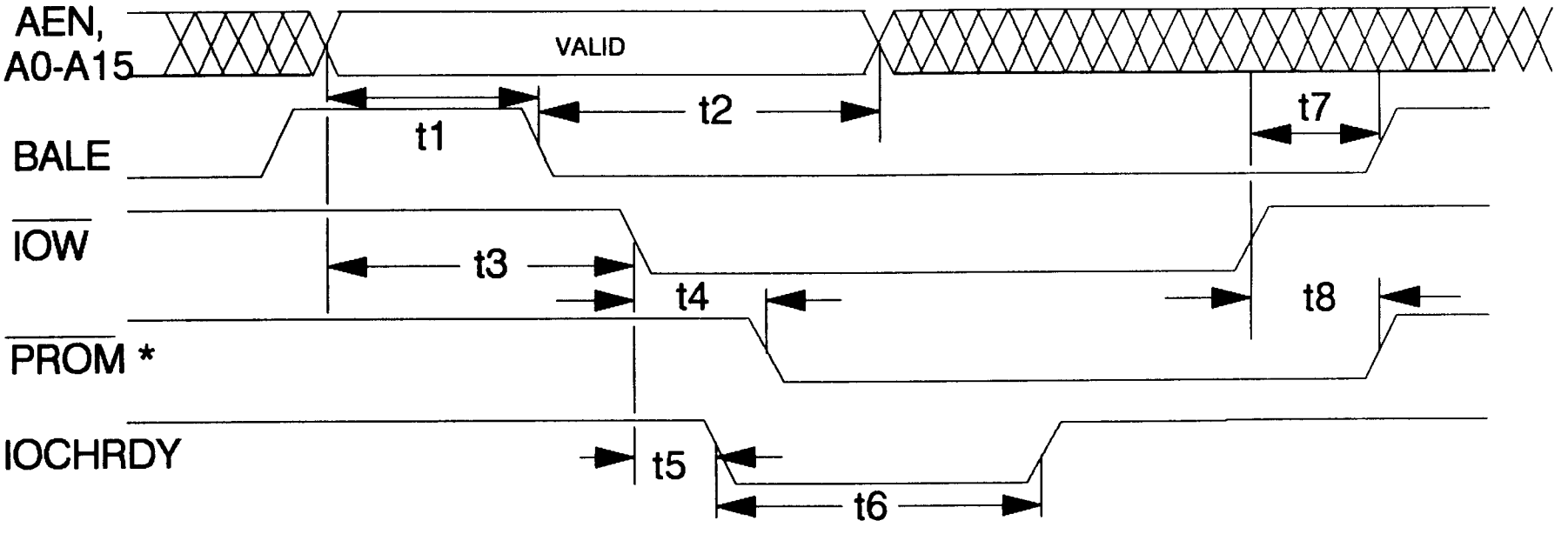
FIGURE 17 - WRITE I/O CYCLE



	Parameter	min	typ	max	units
t1	Address Set Up to BALE Low	20			nS
t2	Address Hold after BALE Low	20			nS
t3	Address Set Up to MEMR Low	50			nS
t4	MEMR Low to PROM Low	0		25	nS
t5	MEMR Low to TOPL Low	0		30	nS
t6	MEMR Low to IOCHRDY Low	0		20	nS
t7	IOCHRDY Low Pulse Width	100		165	nS
t8	MEMR High to TOPL High	0		15	nS
t9	MEMR High to PROM High	0		30	nS
t10	MEMR High to BALE High (Next Address)	30			nS

* All PROM accesses are 8-bit only, ROM should use MEMR as OE signal and PROM as CS.

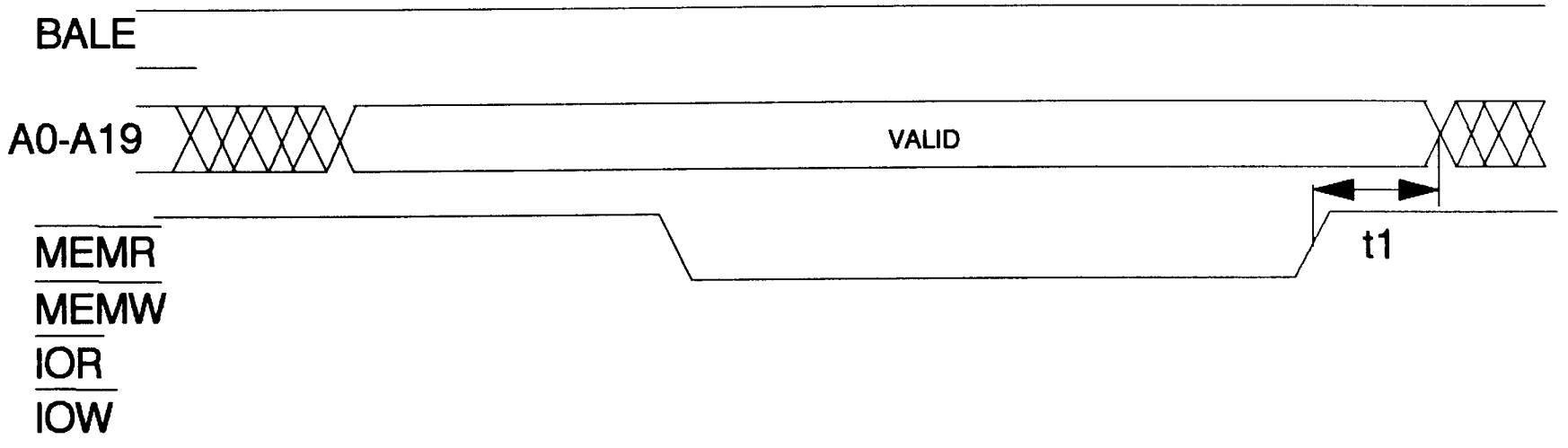
FIGURE 18 - READ PROM CYCLE



	Parameter	min	typ	max	units
t1	Address, AEN Set Up to BALE Low	20			nS
t2	Address, AEN Hold after BALE Low	20			nS
t3	Address, AEN Set Up to IOW Low	50			nS
t4	IOW Low to PROM Low	0		25	nS
t5	IOW Low to IOCHRDY Low	0		20	nS
t6	IOCHRDY Low Pulse Width	100		165	nS
t7	IOW High to BALE High (Next Address)	30			nS
t8	IOW High to PROM High	0		30	nS

* The external latch should use PROM as CS input and IOW as CLK input.

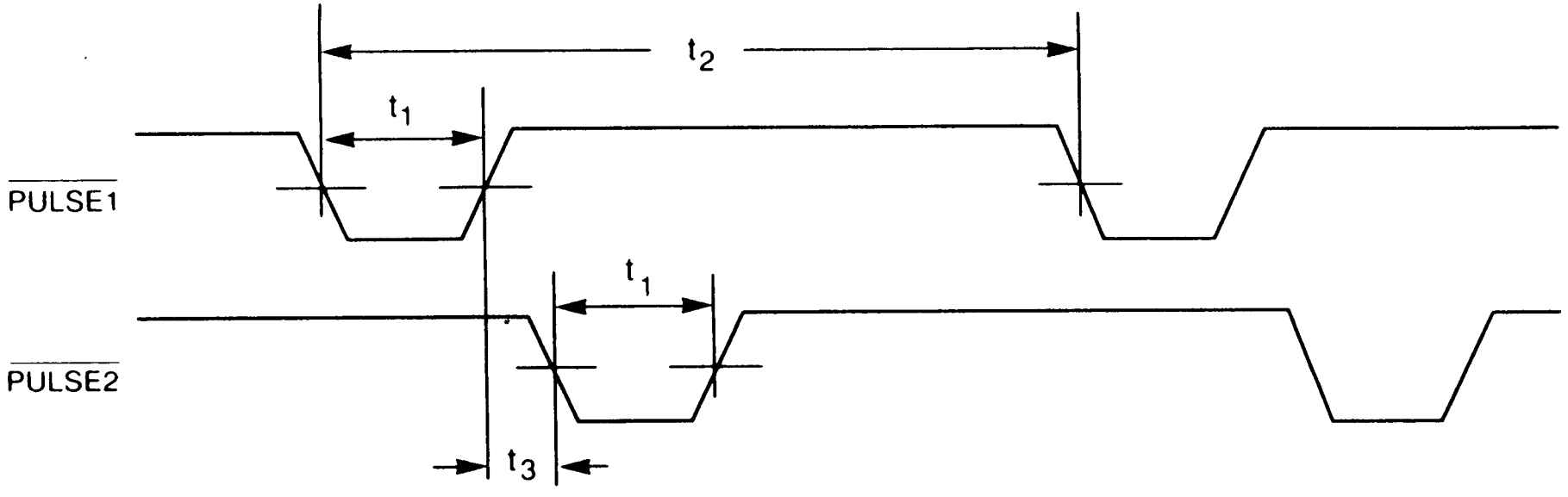
FIGURE 19 - WRITE EXTERNAL REGISTER CYCLE



	Parameter	min	typ	max	units
t1	Control Signal to Address Invalid	10			nS

In the case of Latched Addresses, when BALE is tied high, disregard t1 and t2 in Figures 11-16. Instead, use the above timing.

FIGURE 20 - LATCHED ADDRESS MODE

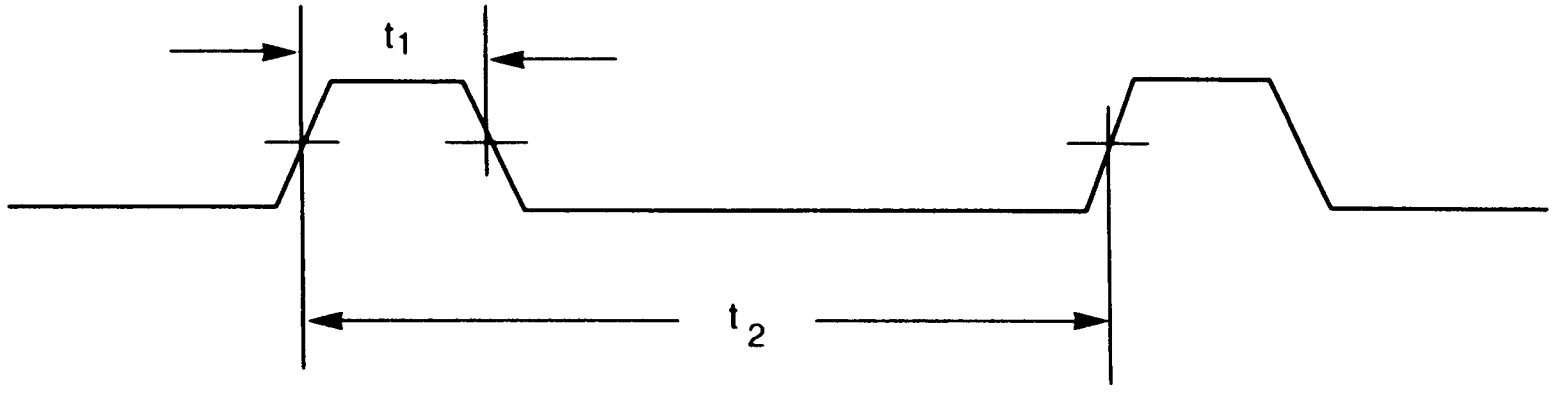


Parameter		min	typ	max	unit	
$\overline{\text{PULSE1}}$, $\overline{\text{PULSE2}}$ PULSE WIDTH	t1		100		nS	*
$\overline{\text{PULSE1}}$, $\overline{\text{PULSE2}}$ PERIOD	t2		400		nS	**
$\overline{\text{PULSE1}}$, $\overline{\text{PULSE2}}$ OVERLAP	t3	-10	0	+10	nS	

*NOTE 1: t_1 = 2 x (crystal period) for clock frequencies other than 20 MHz.

**NOTE 2: t_2 = 8 x (crystal period) for clock frequencies other than 20 MHz. This period applies to data of two consecutive one's.

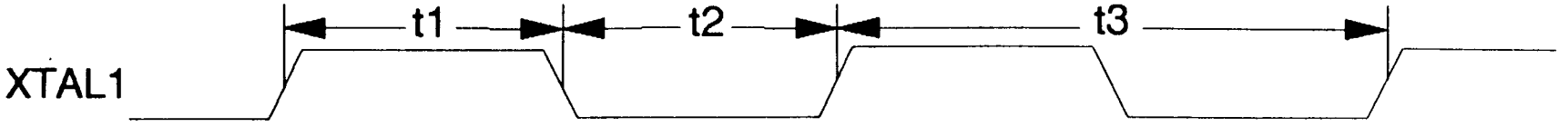
FIGURE 21 - TRANSMIT TIMING



Parameter		min	typ	max	unit	
RXIN PULSE WIDTH	t1	10			nS	
RXIN PERIOD	t2		400		nS	*

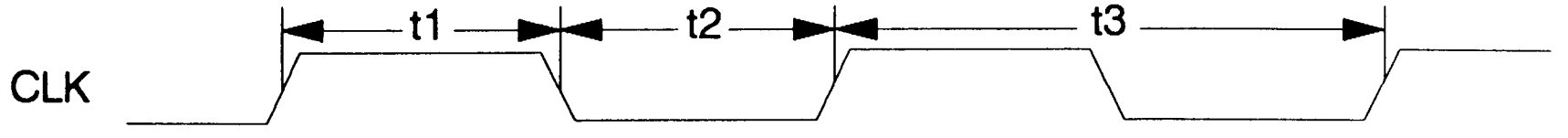
*NOTE: This period applies to data of two consecutive one's.

FIGURE 22 - RECEIVE TIMING



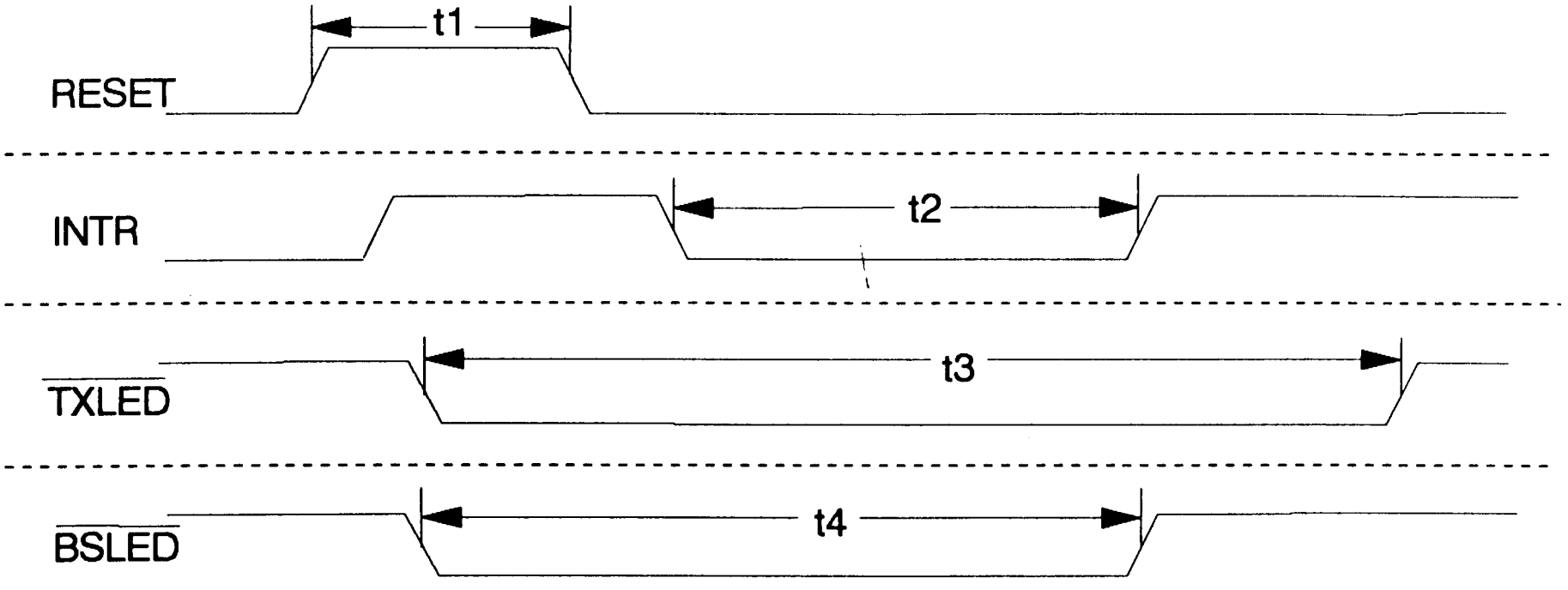
	Parameter	min	typ	max	units
t1	Input Clock High Time	20			nS
t2	Input Clock Low Time	20			nS
t3	Input Clock Period	50		125	nS
f	Input Clock Frequency	8		20	MHz

FIGURE 23 - TTL INPUT CLOCK TIMING ON XTAL1 PIN



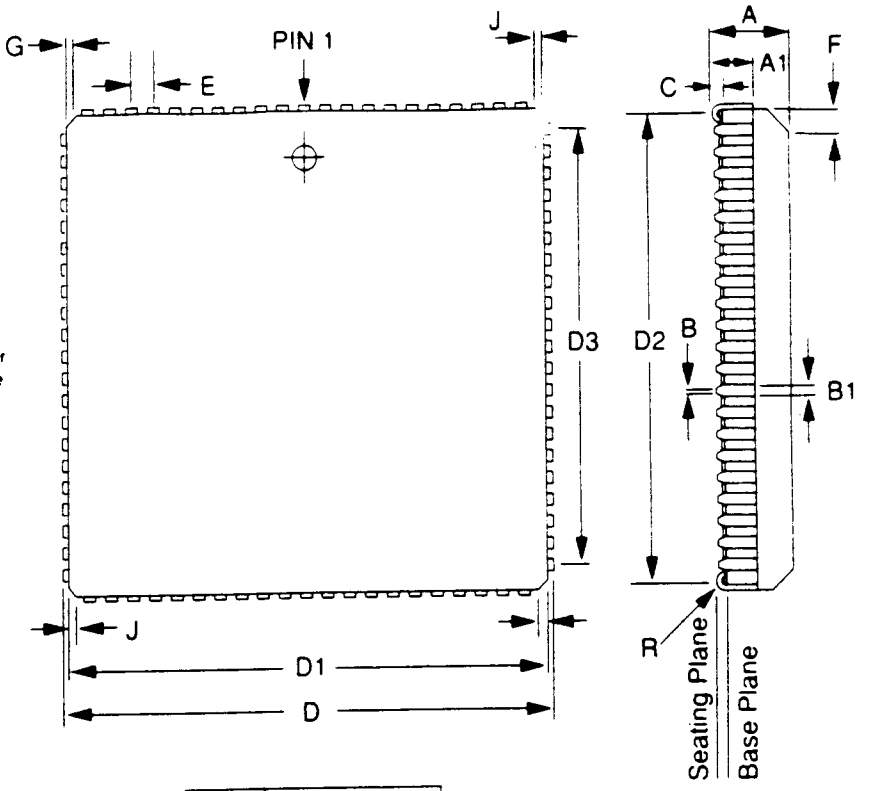
	Parameter	min	typ	max	units
t1	Output Clock High Time		100		nS
t2	Output Clock Low Time		100		nS
t3	Output Clock Period		200		nS
f	Output Clock Frequency		5		MHz

FIGURE 24 - CLK OUTPUT TIMING



	Parameter	min	typ	max	units
t1	Reset Pulse Width	120			nS
t2	INTR Low to Next INTR High	200			nS
t3	$\overline{\text{TXLED}}$ Active (Low)	650			uS
t4	$\overline{\text{BSLED}}$ Active (Low)	320			uS

FIGURE 25 - RESET, INTERRUPT, AND LED TIMING



NOTE:

1. All dimensions are in inches
2. Circle indicating pin 1 can appear on a top surface as shown on the drawing or right above it on a beveled edge.

DIM	84L
A	.165-.179
A1	.095-.109
D	1.185-1.195
D1	1.150-1.156
D2	1.090-1.130
D3	1.000
F	.050 TYP
G	.045 TYP
J	.010
E	.047-.053
R	.025-.045
B	.013-.021
B1	.027
C	.020-.045

FIGURE 26 - 84-PIN PLCC PACKAGE DIMENSIONS