PROCESS CP285

Power Transistor

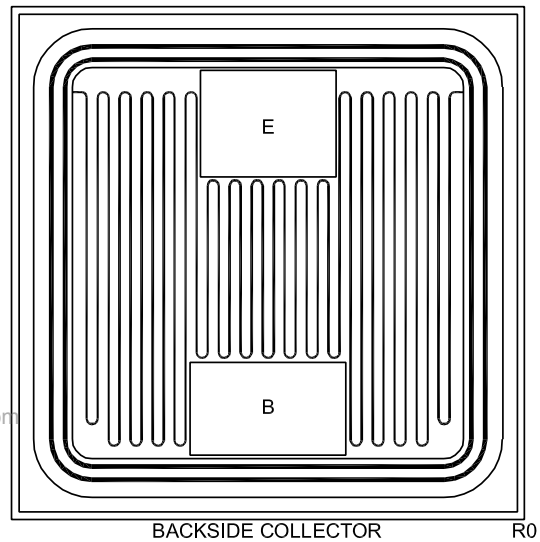
NPN - Silicon Power Transistor Chip

Central™
Semiconductor Corp.

PROCESS DETAILS

Die Size	105 x 105 MILS
Die Thickness	9.5 MILS
Base Bonding Pad Area	32 x 22 MILS
Emitter Bonding Pad Area	33 x 24 MILS
Top Side Metalization	Al - 45,000Å
Back Side Metalization	Ti/Ni/Ag - (3000Å, 10,000Å, 10,000Å)

GEOMETRY



BACKSIDE COLLECTOR R0

GROSS DIE PER 5 INCH WAFER
1,486

PRINCIPAL DEVICE TYPES
MJE13005

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R0 (20-January 2006)