

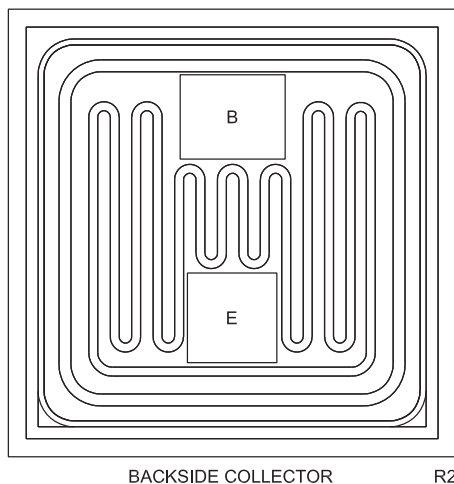
PROCESS CP310
Small Signal Transistor
NPN - High Voltage Transistor Chip



PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	26 x 26 MILS
Die Thickness	9.0 MILS
Base Bonding Pad Area	6.1 x 4.9 MILS
Emitter Bonding Pad Area	5.2 x 5.2 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 18,000Å

GEOMETRY



GROSS DIE PER 5 INCH WAFER
25,214

PRINCIPAL DEVICE TYPES

2N3439
2N3440
CMPTA42
CMPTA44
CMPT6517
CXTA44
CZTA42
CZTA44
MPSA42
MPSA44

R4 (22-March 2010)

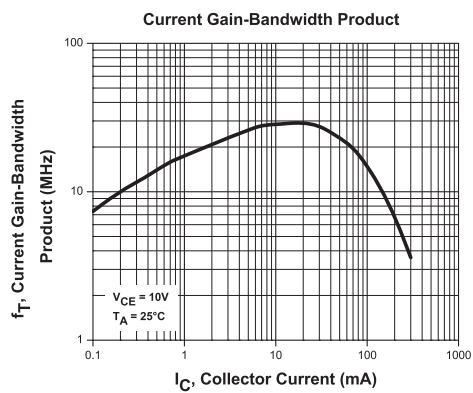
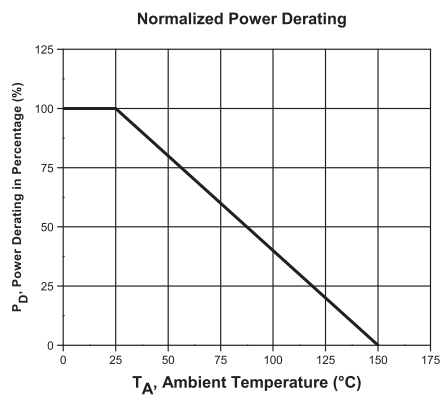
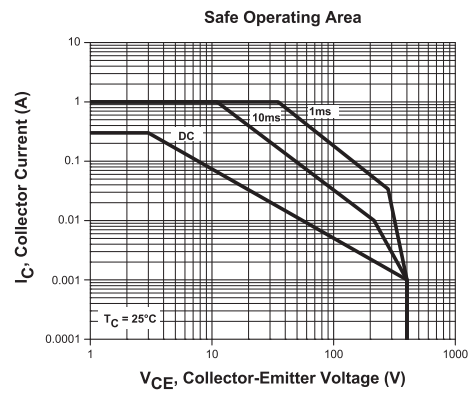
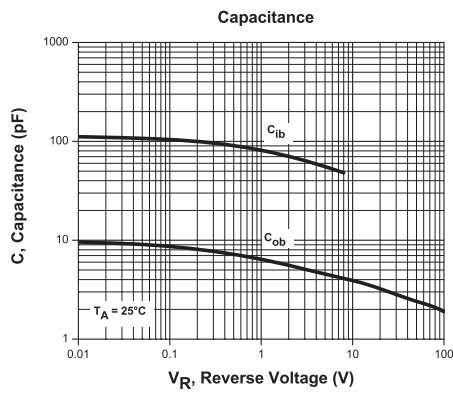
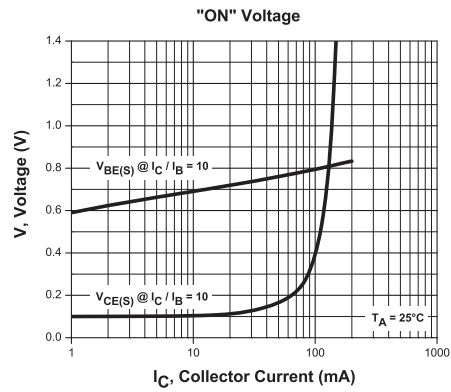
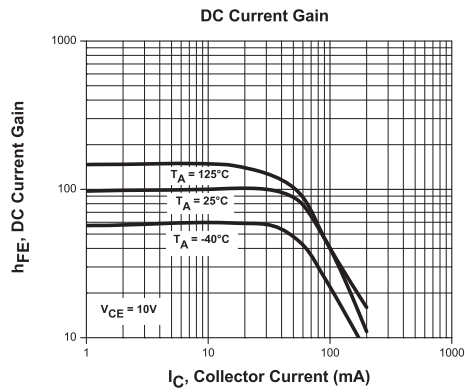
www.centrasemi.com

www.DataSheet4U.com

www.DataSheet4U.com

PROCESS CP310

Typical Electrical Characteristics



R4 (22-March 2010)

www.centalsemi.com

www.DataSheet4U.com

www.DataSheet4U.com