PROCESS CP316V

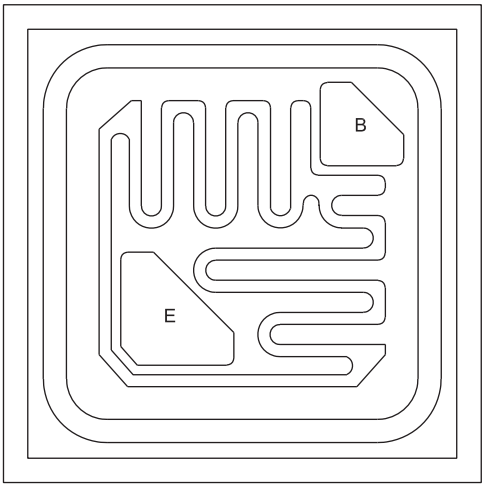
Small Signal Transistors

NPN - High Voltage Transistor Chip

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	20 x 20 MILS
Die Thickness	7.1 MILS
Base Bonding Pad Area	4.0 x 4.0 MILS
Emitter Bonding Pad Area	4.7 x 4.7 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 18,000Å

GEOMETRY



BACKSIDE COLLECTOR R0

GROSS DIE PER 5 INCH WAFER

57,735

PRINCIPAL DEVICE TYPES

CMPT5551
CXT5551
CZT5551
2N5551

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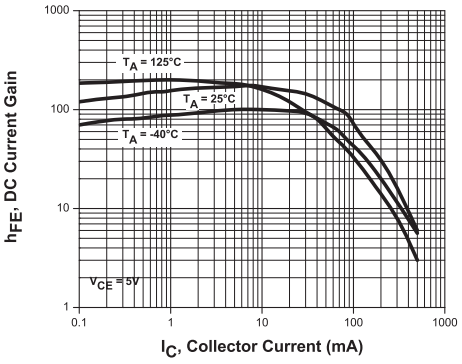
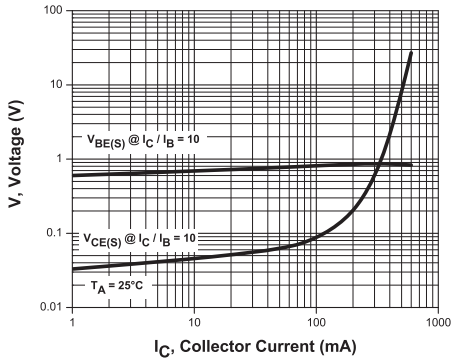
PROCESS CP316V

Typical Electrical Characteristics

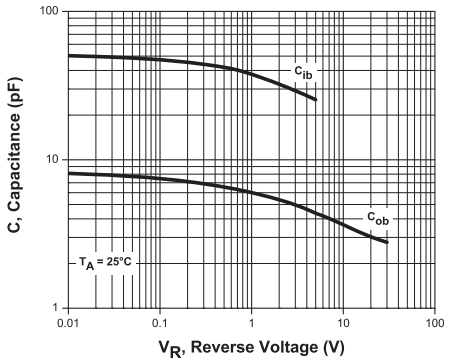
DC Current Gain



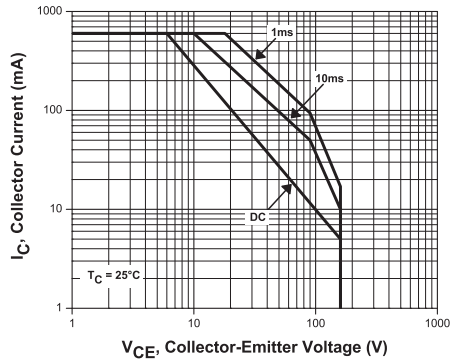
"ON" Voltage



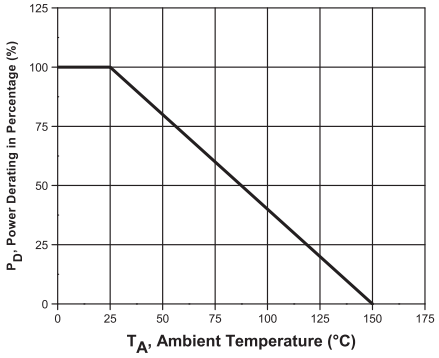
Capacitance



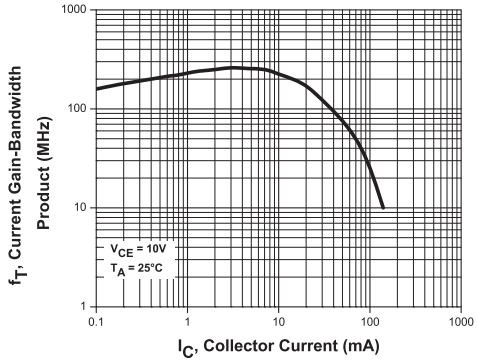
Safe Operating Area



Normalized Power Derating



Current Gain-Bandwidth Product



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