PROCESS CP317V

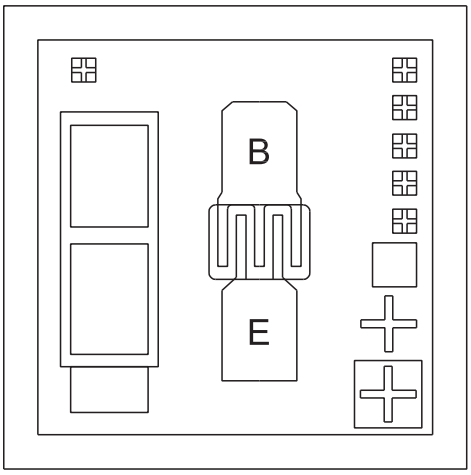
Small Signal Transistor

NPN - RF Transistor Chip

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	14.5 x 14.5 MILS
Die Thickness	7.1 MILS
Base Bonding Pad Area	2.4 x 2.2 MILS
Emitter Bonding Pad Area	2.4 x 2.2 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 18,000Å

GEOMETRY



BACKSIDE COLLECTOR R1

GROSS DIE PER 4 INCH WAFER

53,788

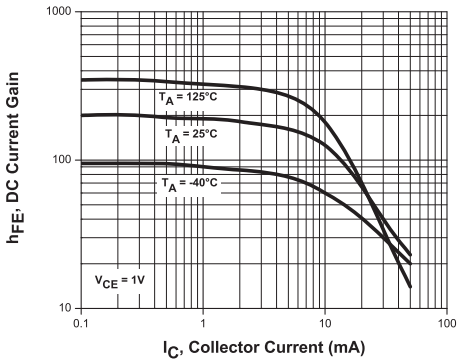
PRINCIPAL DEVICE TYPES

CMPT918
2N918
2N2857
2N5179
2N5770
BFY90
PN3563
PN3564

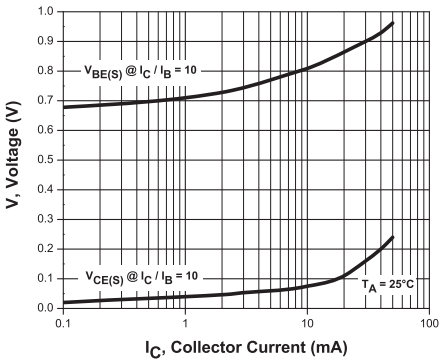
PROCESS CP317V

Typical Electrical Characteristics

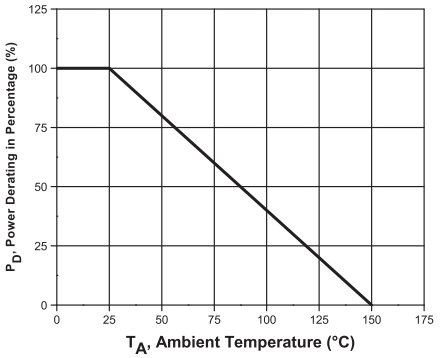
DC Current Gain



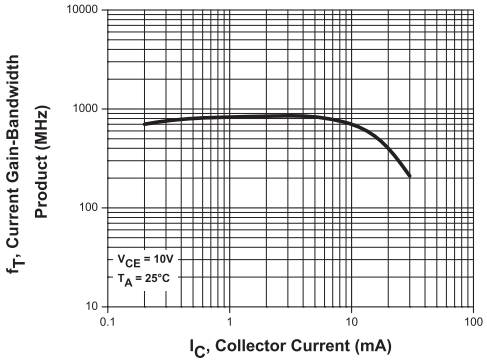
"ON" Voltage



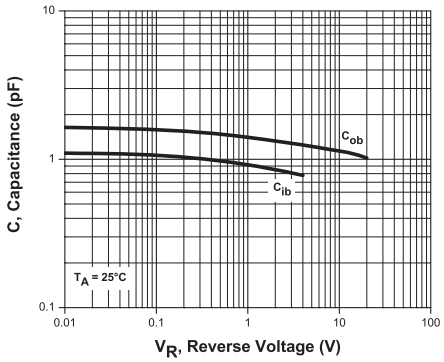
Normalized Power Derating



Current Gain-Bandwidth Product



Capacitance



R0 (30-August 2011)