

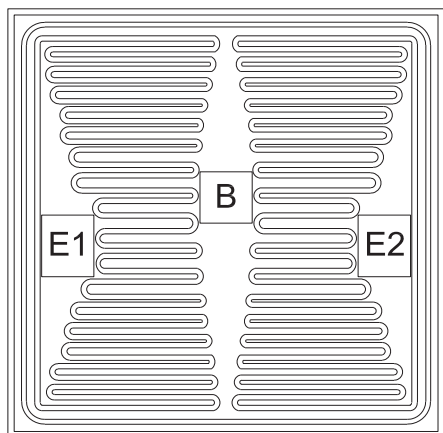
**PROCESS CP353V**  
**Small Signal Transistors**  
NPN - High Current Transistor Chip



**PROCESS DETAILS**

|                            |                                  |
|----------------------------|----------------------------------|
| Process                    | EPITAXIAL PLANAR                 |
| Die Size                   | 66 x 66 MILS                     |
| Die Thickness              | 7.1 MILS                         |
| Base Bonding Pad Area      | 7.9 x 7.9 MILS                   |
| Emitter 1 Bonding Pad Area | 7.9 x 9.5 MILS                   |
| Emitter 2 Bonding Pad Area | 7.9 x 9.5 MILS                   |
| Top Side Metalization      | Al-Si - 30,000Å                  |
| Back Side Metalization     | Ti/Ni/Ag - 2,000Å/3,000Å/20,000Å |

**GEOMETRY**



BACKSIDE: COLLECTOR R0

**GROSS DIE PER 5 INCH WAFER**

3,878

**PRINCIPAL DEVICE TYPES**

CZT853

R2 (22-March 2010)

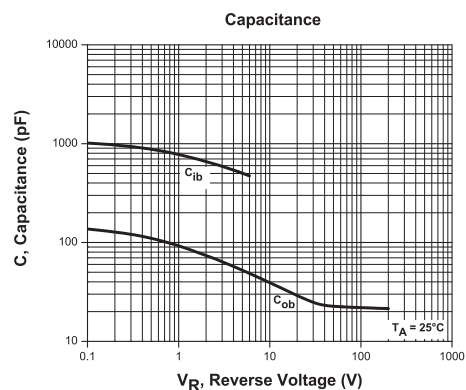
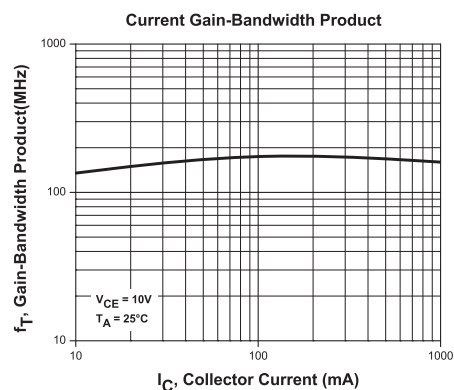
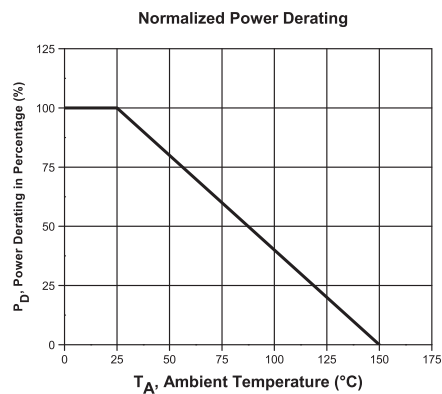
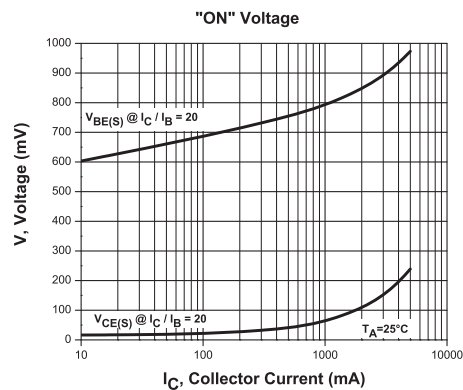
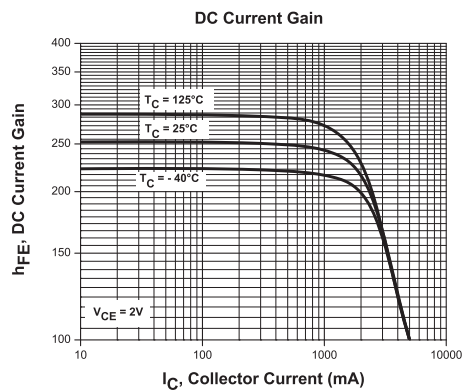
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[www.DataSheet4U.com](http://www.DataSheet4U.com)

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# PROCESS CP353V

## Typical Electrical Characteristics



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