

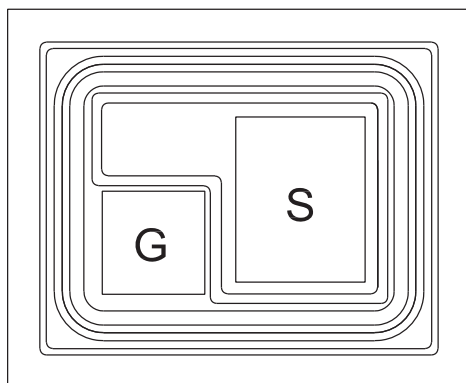
PROCESS CP764X
Small Signal MOSFET Transistor
P-Channel Enhancement-Mode Transistor Chip



PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	21.7 x 17.7 MILS
Die Thickness	5.5 MILS
Gate Bonding Pad Area	4.7 x 4.7 MILS
Source Bonding Pad Area	6.1 x 7.9 MILS
Top Side Metalization	Al-Si - 35,000Å
Back Side Metalization	Au - 12,000Å

GEOMETRY



BACKSIDE: DRAIN

R0

GROSS DIE PER 6 INCH WAFER

62,600

PRINCIPAL DEVICE TYPES

CMLDM8002A

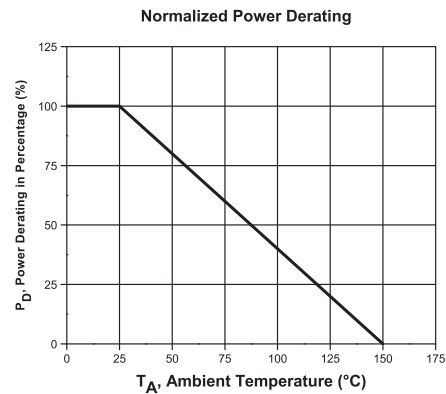
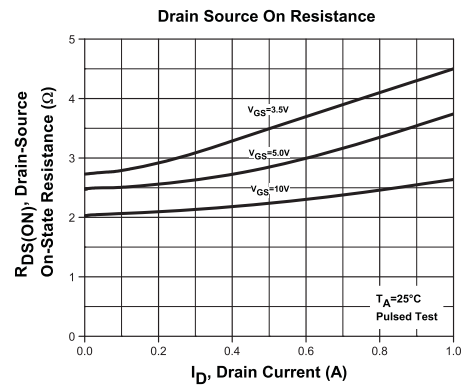
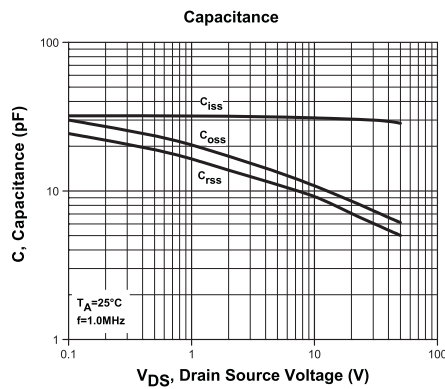
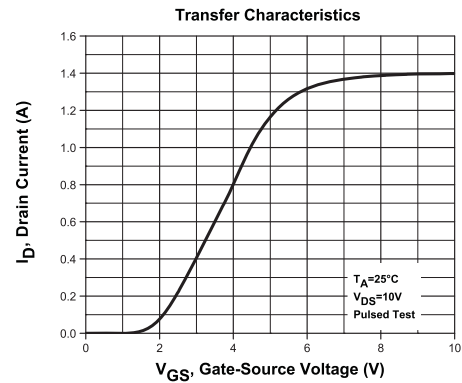
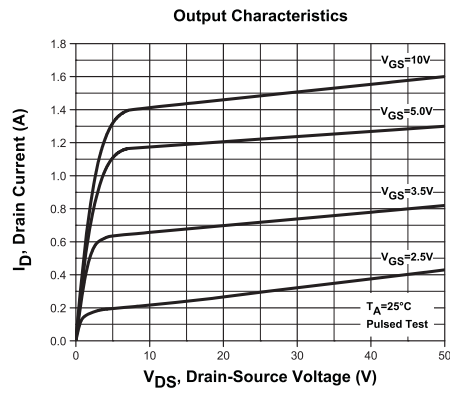
CMPDM8002A

CTLDM8002A-M621

R1 (22-March 2010)

PROCESS CP764X

Typical Electrical Characteristics



R1 (22-March 2010)