CP8108(Wideye™) Datasheet

D1 CMOS IMAGE SENSOR

Version 0.5

Document No. : CP-M-8108

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Revision History

Issue	Rev No.	Originator	Details of Change	Date
1	0.1	limks	Initial Version	2012-02-25
2	0.2	limks	Pixel array structure	2012-03-07
3	0.3	moonjj	Modified TV register description	2012-03-18
4	0.4	limks	Modified ISP1 register map	2013-03-27
5	0.5	limks	Modified maximum frame rate	2013-08-19

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1/3-Inch, CMOS D1 Image Sensor

1. Specification

DESCRIPTSION

CP8108 is a single-chip video/image camera sensor that uses a unique Wideye™ technology developed by Clairepixel to allow video capture in extremely diverse lighting conditions, hence making it suitable for auto vehicle cameras and security systems. CP8108 is set up with a 720x480 image array, outputs up to 60 frames (720x480) per second, and supports various forms of digital output format and NTSC?PAL composite output. CP8108 has various camera control functions, and can be programmed through a two-wire serial interface.

PARAMETER		TYPICAL VALUE
Optical Dimension	Optical Format	1/3 inch
	Pixel Size	6.5 um X 7.4 um
	Effective Resolution	720(H) X 480(V)
	Active Pixel Area	4.732 mm(H) X 3.611 mm(V)
Digital Output		10bit, 8bit RGB Bayer, YCbCr422, RGB565/555, CCIR656
Analog Output		CVBS(NTSC/PAL) @ 54MHz
Maximum Clock Frequency		54MHz
Maximum Frame Rate		720x480, 30fps @ 27MHz (YCbCr) 720x480, 60fps @ 54MHz (YCbCr) 720x480, 30fps @ 27MHz (Bayer) 720x480, 60fps @ 54MHz (Bayer)
Shutter Type		Electronic Rolling Shutter
Sensitivity		[T.B.D] V / lux-sec
Dynamic Range		
SNR		[T.B.D] dB
Max. Programmable Gain		analog (x72), digital (x31.5)
GADC input voltage range		0V~3V
Supply Voltage	Pixel	3.3V ± 10%
	Analog	3.3V ± 10%
	Digital	1.5V ± 10%
	I/O	3.3V ± 10%
Power Consumption	Active	[T.B.D]
	Standby	[T.B.D]
Operating Temperature		-40°C ~ 105°C
Package Type		CLCC, Wafer or Die

FEATURES

- ClairPixel's Wideye™, Wide Dynamic Range technology
- System-on-a-chip(SOC)-completely integrated camera system
- Integrated microcontroller for flexibility
- CVBS, 8-,10-bit parallel digital output
- Bayer Noise Reduction, Lens Shading Compen-sation, Defective Pixel Compensation
- Color Correction, Gamma Correction,
- Hue/Saturation, Contrast/Brightness Control
- Edge Enhancement
- Parking Guide, OSD, Privacy Zone Mask,
- Automatic features :
  Auto Exposure, Auto White Balance,
  Anti-Flicker, Black Level Calibration
- NTSC/PAL encoder with 10bit DAC
- 2 channel(Master, Slave) Two-wire serial interface
- Embedded 2 channel 8-bit General ADC for OSD & CdS

APPLICATIONS

. Automotive

. Machine Visions

. Security surveillance cameras

2. System Block Diagram

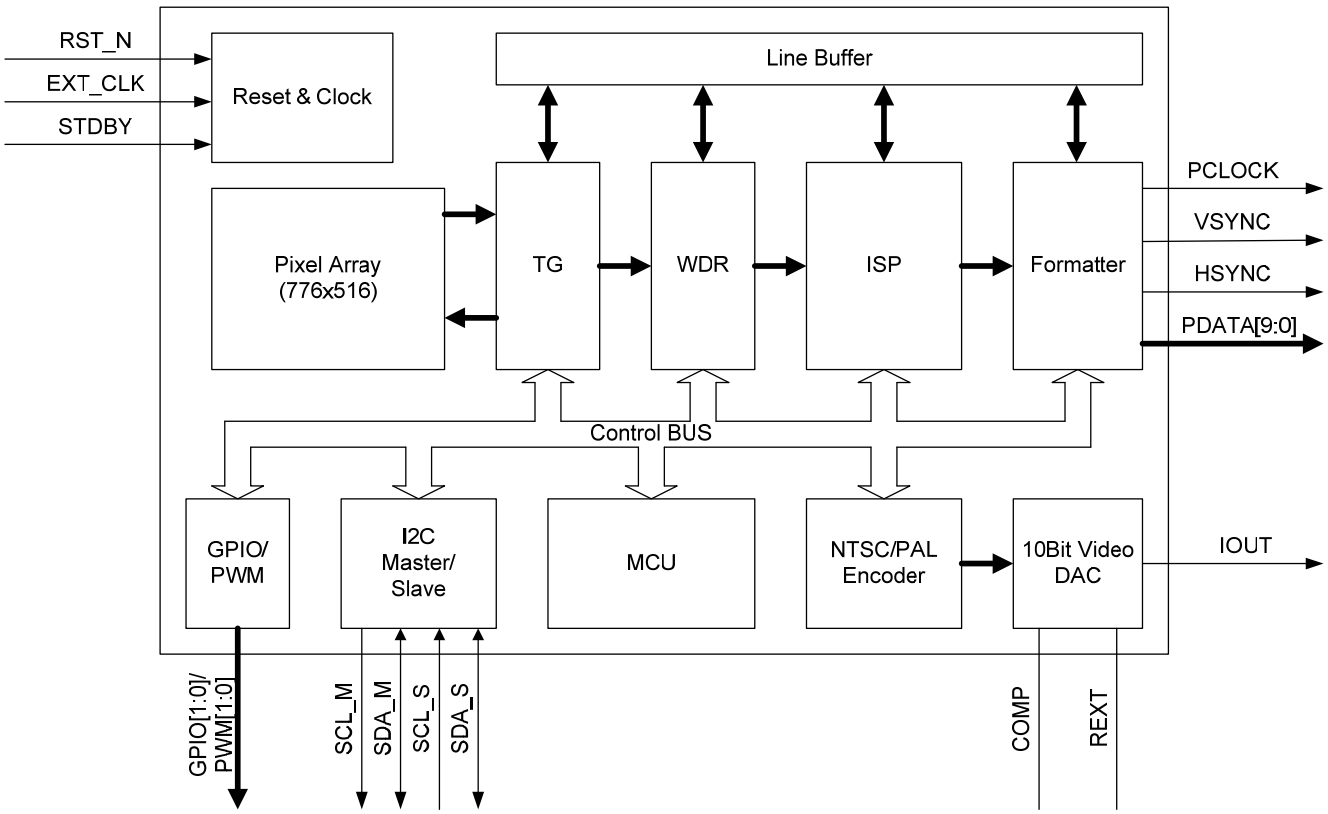


Figure 2-1 Block Diagram

CP8108 is a CMOS D1　Image Sensor in 1/3-inch optical format with 340,000 pixels.

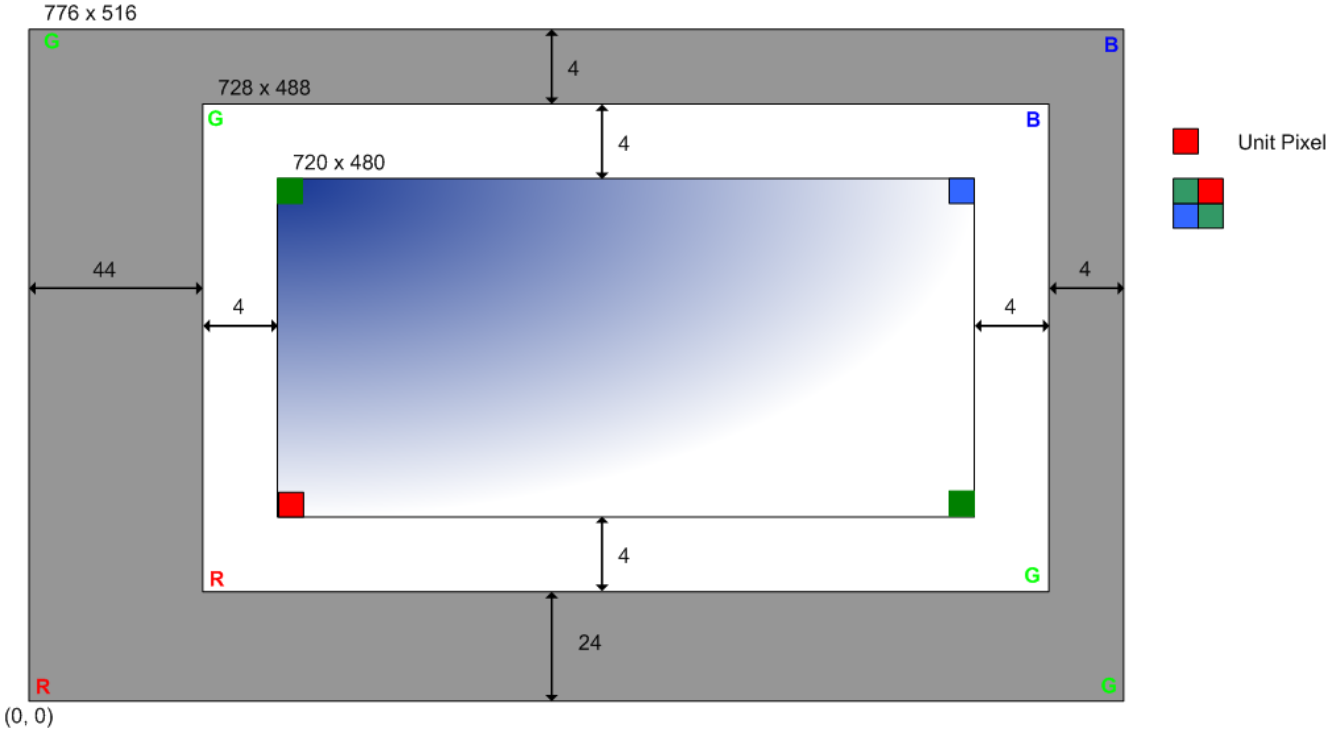
Figure 2-1 is a broad view of the block diagram of CP8108 and the 776x516 pixel array is output through TG, , ISP, Formatter to the 10-bit digital parallel port, or through NTSC/PAL Encoder, 10-bit Video DAC to analog composite port.

2 channel (master, slave) two-wire serial interface and 2 channel GPIO or PWM are provided for external interface.

8 bit MCU is built in to provide an overall chip control and flexibility.

3. Pixel Array Structure

Figure 3-1 shows the pixel array structure of CP8108.



Total number of pixels : 776 x 516
Total active pixels : 728 x 488
Total effective pixels : 720 x 480
Optical blacks : left 44, right 4, top 4, bottom 24

Figure 3-1 Pixel Array Structure

4. Pixel Data Output Timing

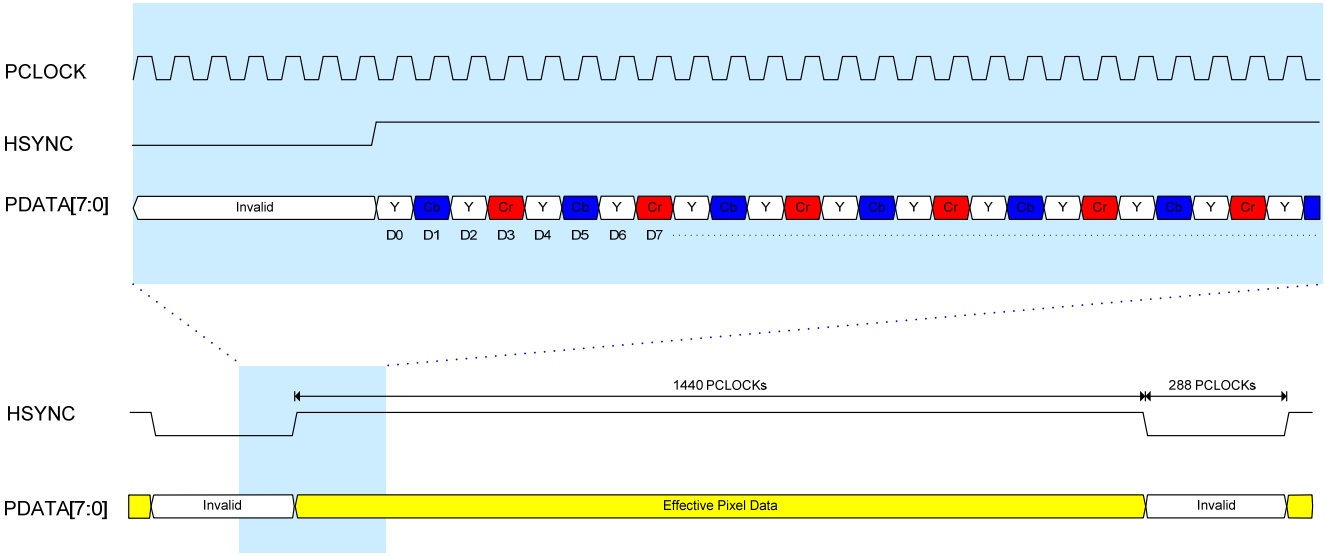


Figure 4-1 Horizontal Timing

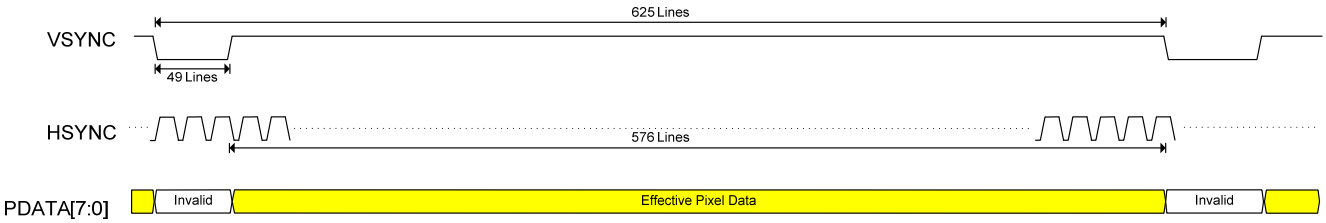


Figure 4-2 Vertical Timing

5. System Interface

5.1. System Initialization

Figure 5-1 is an outline of the reset scheme which initializes CP8108. When external reset is approved, internal reset generation is initialized, and the entire system is uninitialized together.

(Note. Reset signal needs to be maintained to 4 clock or more LOW after Ext Clock has been stabilized)

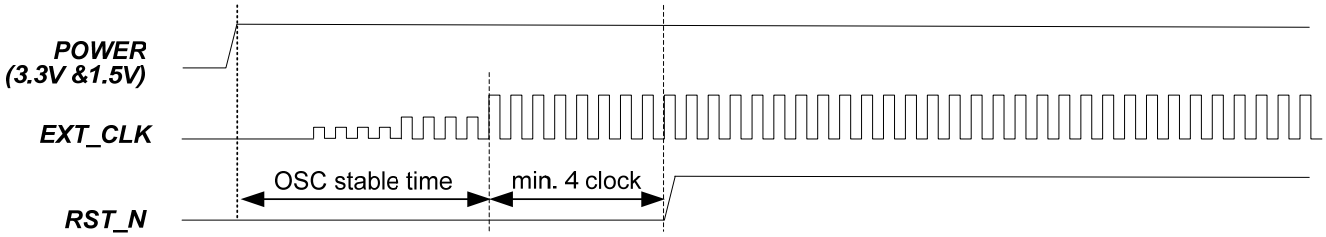


Figure 5-1 System Reset Scheme

5.2. Power-Down Mode

Power-down mode is controlled by the STDBY pin, operates as active high and enters power-down mode upon HIGH approval. Relevant pin needs to be maintained at low for normal operation mode. For accurate power down operation, at least 4 clocks of external clock needs to be approved after STDBY signal input and after 4 clock approval, external clock can be maintained at LOW for reducing power consumption.

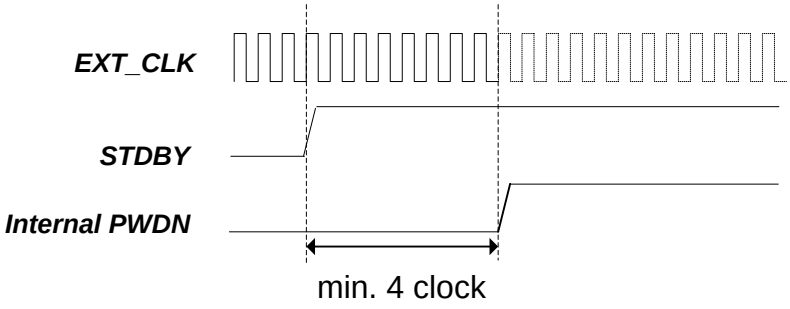


Figure 5-2 System Power Down Scheme

5.3. I2C interface

I2C Master and Slave interface each are built-in CP8108 internally. I2C device address can be modified through the MCU (system register 0x4006).

*** CP8108 I2C Slave Device Address**

Write Device Address	0x76
Read Device Address	0x77

5.3.1. I2C Condition

- **Start / Stop Condition**

Data Line is maintained at High when Bus is not in use. Start condition is defined as the time during which data line 천이 s from high to low while clock line maintains its high position. The time during when the data line 천이 s from low to high is defined as the stop condition.

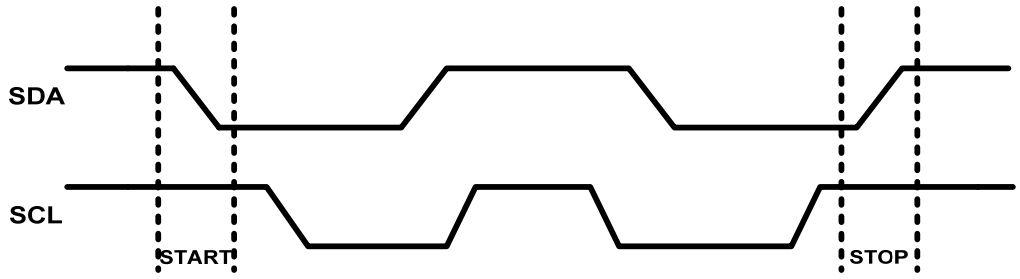


Figure 5-3 Start / Stop

- **Acknowledge**

All addresses and data are continuously transferred or received in 8-bit words to I2C slave. I2C slave sends 0 as an acknowledgement signal after each word sent. This happens in 9 clock intervals.

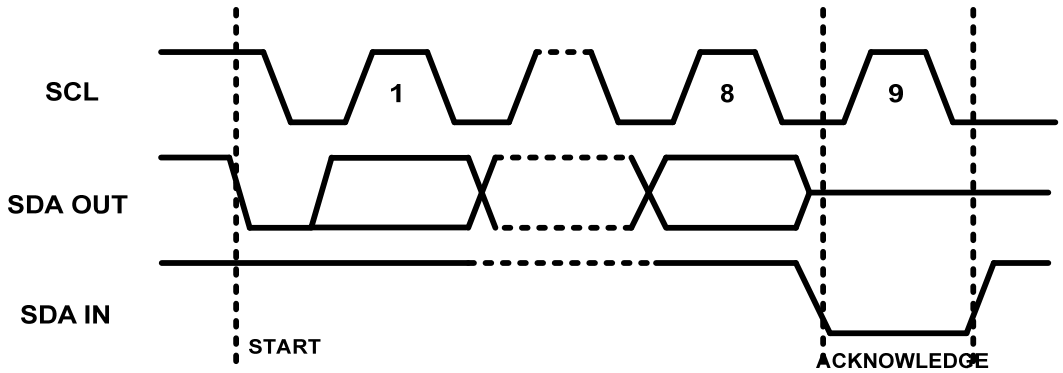


Figure 5-4 Acknowledge

5.3.2. I2C Master Operation

CP8108 operates as master through I2C interface SCL_M, SDA_M pins. It can be used as an interface to control various external devices such as AF module control.

- **Write Operation**

Write operation is composed of three parts including device address, index address and write data and the success of the communication of each part can be verified through the acknowledge bit after the transmission. I2C master can select the target device through the address of the device through which data is to be sent, and a maximum of 5byte data can be sent at once.

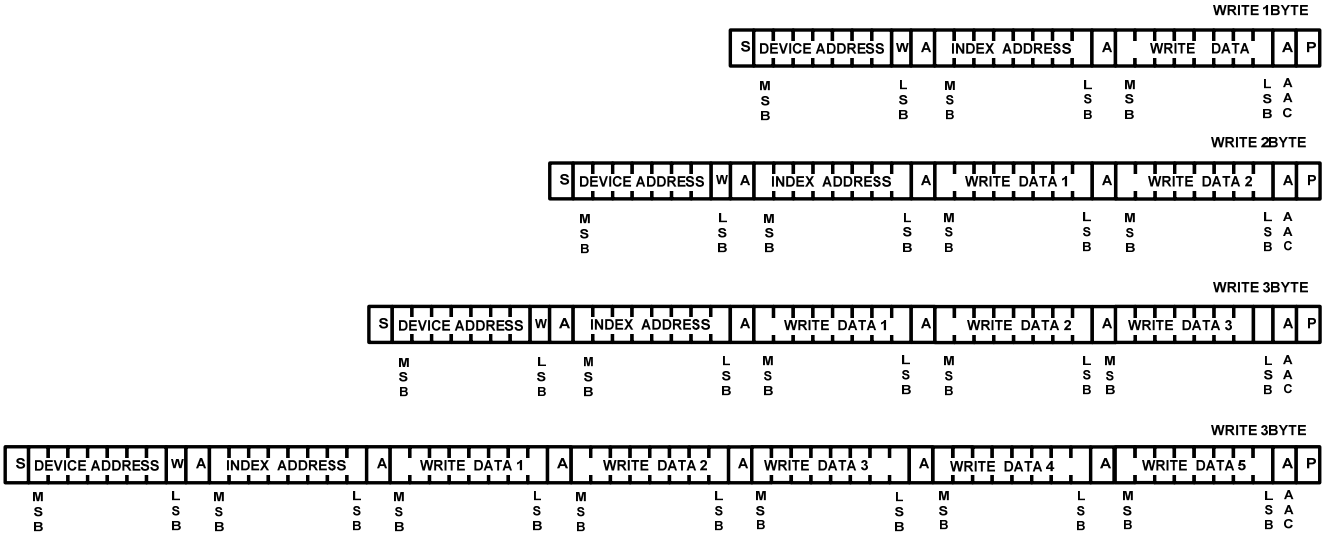


Figure 5-5 I2C Master Write Operation

- **Read Operation**

In order to access a random register to read the register value, " dummy" byte write needs to be performed. This is because internal address register automatically increases after the transmission is complete. In order to read data from a certain address register, write index address first to read the data at the relevant register.

The blue dotted line in the figure below shows that in dummy write, STOP condition may be output after the index address has been sent, or the START condition may be output without the STOP condition. The function mentioned above is carried out by internal register settings. I2C master built in CP8108 can read a maximum of 2 Bytes in series.

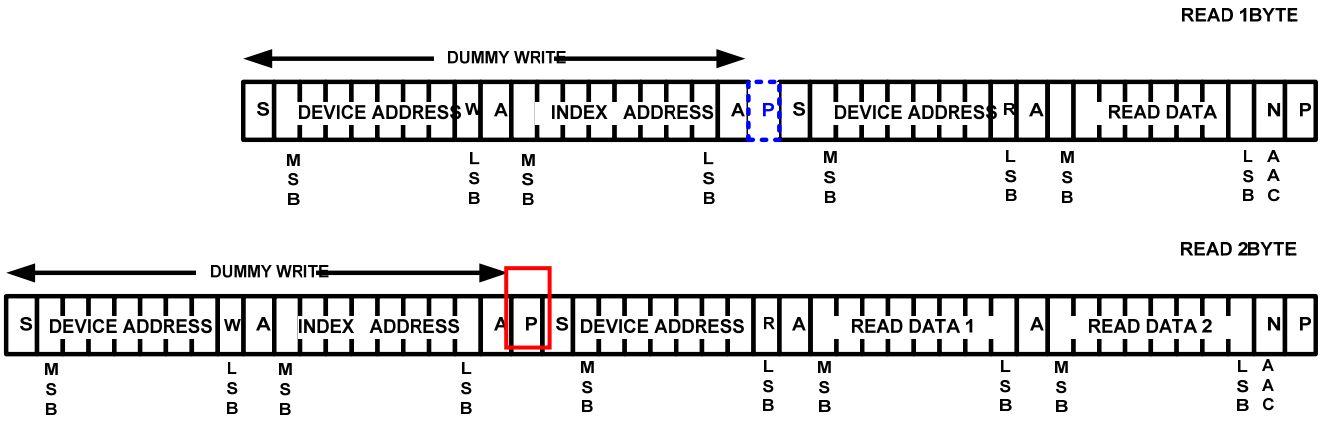


Figure 5-6 I2C Master Read Operation

5.3.3. I2C Slave Operation

CP8108 operates as slave through I2C interface SCL_S, SDA_S pin. Certain registers of CP8108 can be controlled through the I2C Slave interface. Program data can also be downloaded through the I2C Slave to the MCU Program Memory within. MCU Code Memory Data of CP8108 can be saved in byte units, and MCU is under Reset status while SRAM write takes place throug

- **Byte Write**

  Write operation is composed of three parts including Device Address, Index Address, and Write Data, and the success of the communication can be verified through Acknowledge Bit after the transmission of each parts. I2C slave only receives data when the Device Address matches its own.

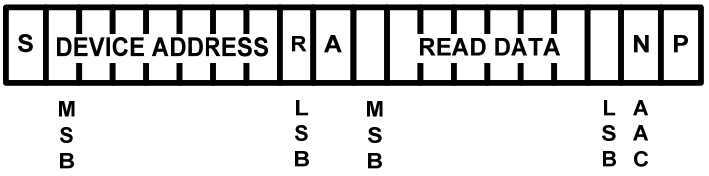
- **Random Read**

  In order to access a random register to read the register value " dummy" byte write needs to be performed. This is because internal address register automatically increases after the transmission is complete. In order to read data from a certain address register, write index address first to read the data at the relevant register.

- **Sequential Read**

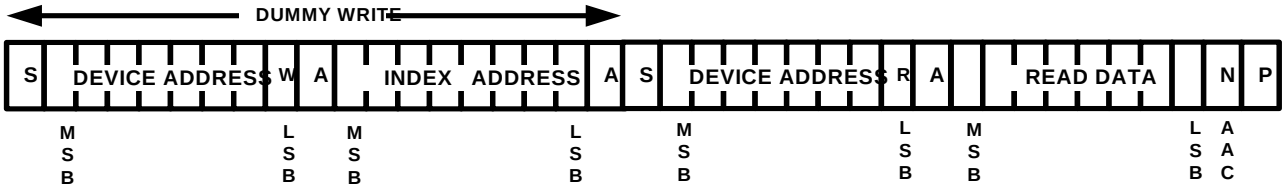
  Starts transmission together with initial Byte Read and data gets output continuously without the transmission of Device Address, Index Address to shorten communication time. I2C Master built in in CP8108 can read a maximum of 2 Bytes continuously and I2C Slave has no restrictions regarding this.

Byte Read Operation

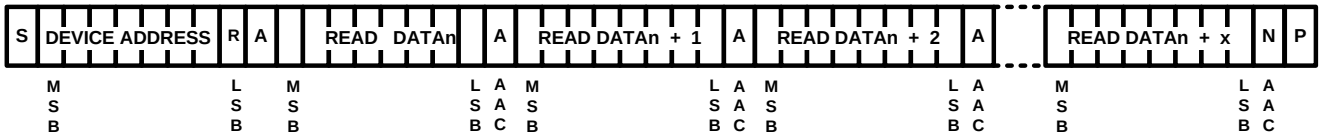


Byte Write Operation

Random Read Operation



Sequential Read Operation



S : Start Condition

P : Stop Condition

MSB : Most Significant Bit

LSB : Least Significant Bit

W : Write (1'b0)

R : Read (1'b1)

A : Acknowledge

N : No Acknowledge

AAC : Auto Address Increment

Figure 5-7 I2C Slave Read, Write Operation

5.4. GPIO, PWM Control Interface

CP8108 provides a maximum of 8 GPIOs and 4 PWMs in order to control the system control interface.

- **I/O control (system register 0x401f ~ 0x4023)**

  I/O control is used when sending output signals to external device, or when receiving input signal from external devices. A maximum of 8 ports can be used, and individual pull up/down control is possible through relevant registers.

- **PWM(Pulse Width Modulation control (system register 0x40a0 ~ 0x40c5)**

  PWM (Pulse Width Modulation) is used to control motor speed or light brightness. PWM can control the width of the pulse. These functions are analog characteristics but are possible by controlling digital pulse duty ratio and frequency divide value. In CP8103, duty ratio and frequency divide value can be controlled using 16bit control signals selected by register controls. Various PWM can be created based on main clock., and the duty cycle of each output wave can be controlled between 0%~100%.

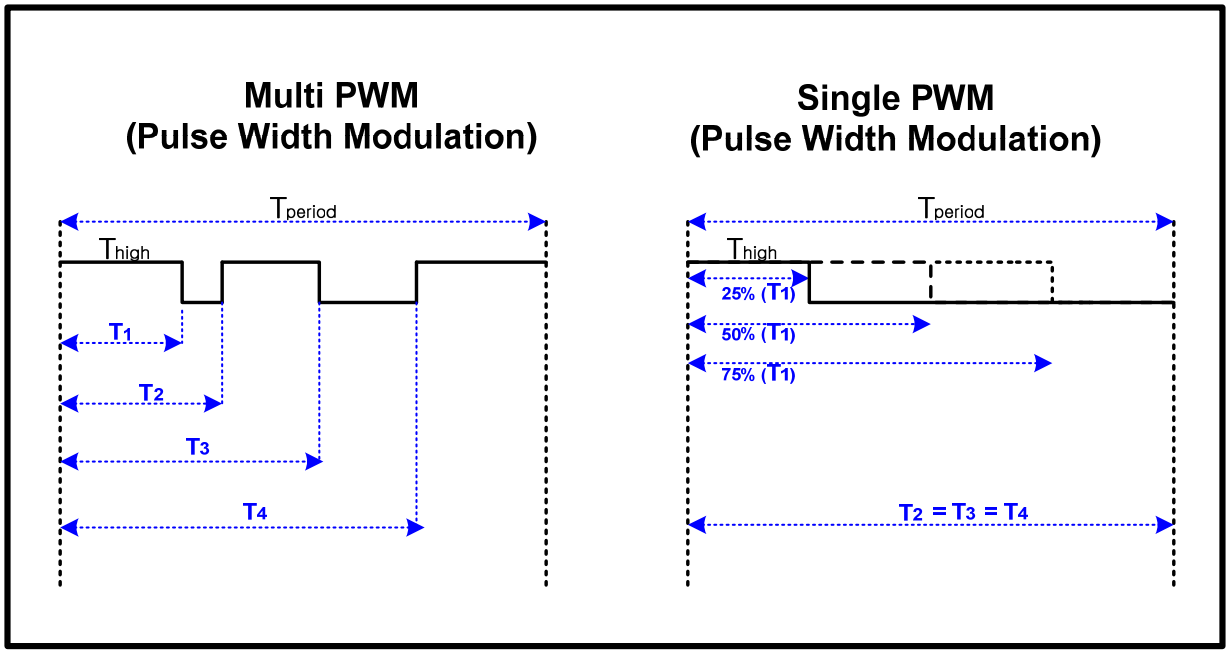


Figure 5-8 PWM Generation

5.5. PAD Control

- **GPIO1/PWM1, GPIO0/PWM0**

  GPIO1/PWM1, GPIO0/PWM0 pins can output GPIO[1:0] or PWM[1:0] using relevant register control.

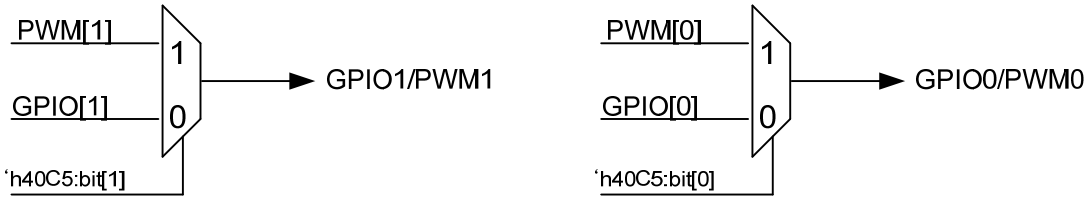


Figure 5-9 GPIO1/PWM1, GPIO0/PWM0 Control

- **PDATA Bus Control**

  PCLOCK, VSYNC, HSYNC, PDATA[9:0] pins are tri-state, pull-down control possible depending on the relevant register conditions. VSYNC, PCLOCK pins can be GPIO[3:2] or PWM[3:2] output through the register control. HSYNC, PDATA[2:0] pins can be GPIO[7:4] output through the register control.

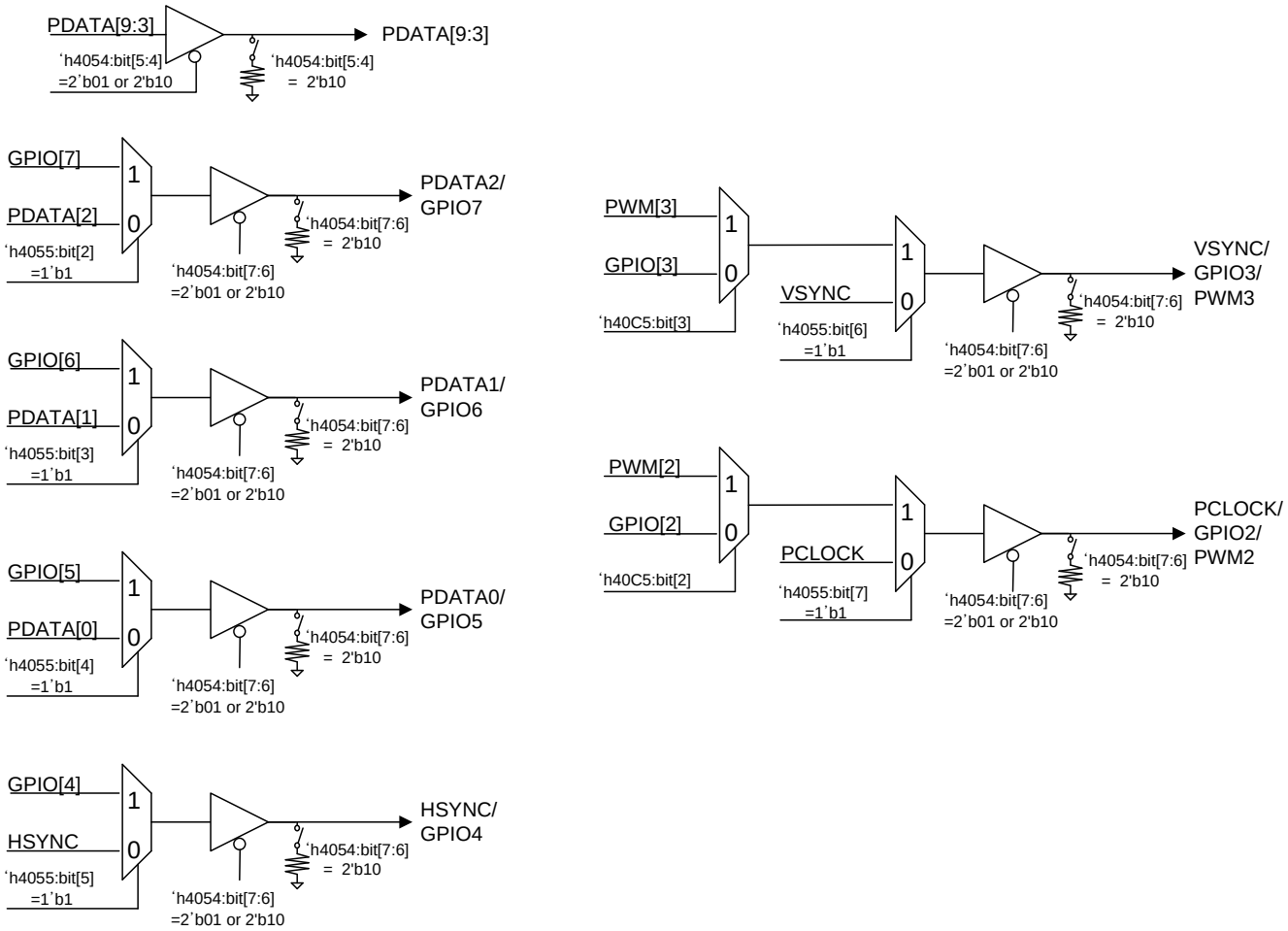


Figure 5-10 PDATA Bus Control

6. MCU interface

CP8108 has a 8bit MCU internally embedded. Memory map of the MCU block is as shown below. Code SRAM 24K byte, Data SRAM 2Kbyte are built in. CP8108 downloads the firmware using I2C master through an external EEPROM. Also, if no external EEPROM is available, the firmware can be downloaded through the system register 0x4024 ~0x4026 using I2C slave. Errors in firmware download can be checked through checksum register(0x4028 ~ 0x4029) or CRC register(0x402A ~ 0x402B). Only system register area can be accessed using I2C slave, and the other areas can be accessed using indirect mode when MCU is disabled, but the entire memory area of MCU is accessible. Interrupt Sources include VSYNC interrupt of internal Sensor and command register write interrupt.

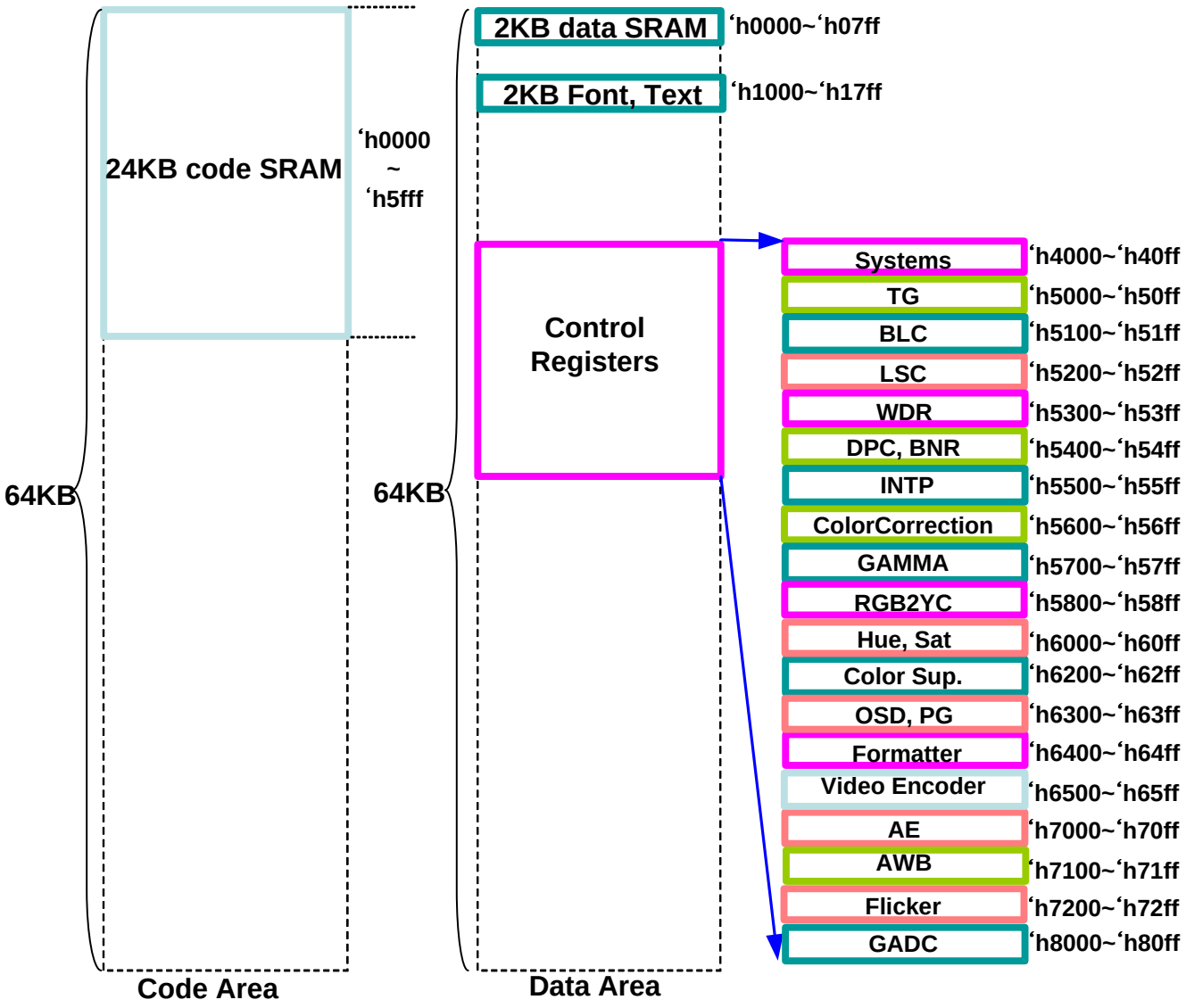


Figure 6-1 MCU Memory Map

7. EEPROM Boot Sequence

Code SRAM 24K byte and OSD Data SRAM 2Kbyte are embedded in CP8108. After initial power approval, firmware and OSD data is downloaded onto internal SRAM using I2C master through external EEPROM. Depending on the code written on certain parts of the firmware code,

- **16Kbyte Code Only**

This mode uses 16K byte to code memory and does not use the OSD data. Of 16K code and address 0x3FFC and ox3FFD area of the write 0xAA and 0x55 to operate in this mode when it is.

- **24Kbyte Code Only**

This mode uses 24K byte to code memory and does not use the OSD data. Of 24K code and address 0x3FFC and 0x3FFD area does not have the write 0xAA and 0x55, address 0x5FFC and 0x5FFD area and the write 0xAA and 0x55 if it is to operate in this mode.

- **24Kbyte Code + 2Kbyte OSD**

This mode uses 24K byte to code memory and also uses 2K byte OSD data. Of 24K code and address 0x3FFC 0x3ffD area does not have the write 0xAA and 0x55, address 0x5FFC 0x5FFD area and if it is not the write 0xAA and 0x55 to operate in this mode. Since 24Kbyte data automatically for OSD data is write into SRAM 2Kbyte.

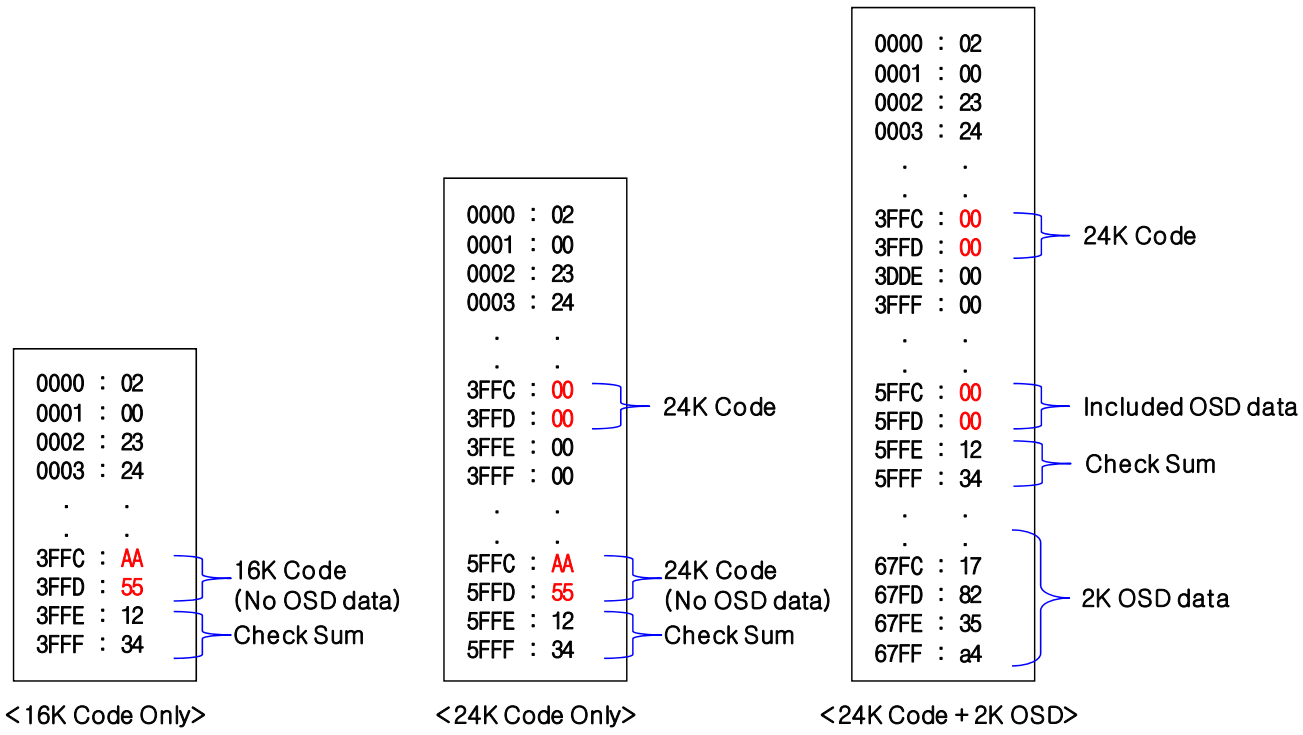


Figure 7-1 EEPROM Boot Sequence

8. TG(Timing Generator)

TG block controls the overall operation timing of the sensor and has Analog/Digital gain control, Mirror (Horizontal, Vertical) functions.

8.1. Analog/Digital Gain Control

8.1.1. Analog Gain

Analog gain can be controlled through the registers in Table 8-1.

Register Name	RW	Bits	Register Description	
			Field Name	Field Description
L_D_GAIN (Reg_0x500C)	Large Pixel Global Digital Gain control register **(Default 0x00)**			
	RW	[6:3]	**L_Cgain**	Coarse analog gain for Large pixel
	RW	[2:0]	**L_Fgain**	Fine analog gain for Large pixel
S_D_GAIN (Reg_0x500D)	Small Pixel Global Digital Gain control register **(Default 0x00)**			
	RW	[6:3]	**S_Cgain**	Coarse analog gain for Small pixel
	RW	[2:0]	**S_Fgain**	Fine analog gain for Small pixel

Table 8-1 Analog Gain Control

		Fgain[2:0]							
		000	001	010	011	100	101	110	111
Cgain[3:0]	0000	x0.63	x0.75	x0.88	x1.00	x1.13	x1.25	x1.38	x1.50
	0001	x1.25	x1.50	x1.75	x2.00	x2.25	x2.50	x2.75	x3.00
	0010	x1.88	x2.25	x2.63	x3.00	x3.38	x3.75	x4.13	x4.50
	0011	x2.50	x3.00	x3.50	x4.00	x4.50	x5.00	x5.50	x6.00
	0100	x3.13	x3.75	x4.38	x5.00	x5.63	x6.25	x6.88	x7.50
	0101	x3.75	x4.50	x5.25	x6.00	x6.75	x7.50	x8.25	x9.00
	0110	x4.41	x5.29	x6.18	x7.06	x7.94	x8.82	x9.71	x10.59
	0111	x5.00	x6.00	x7.00	x8.00	x9.00	x10.00	x11.00	x12.00
	1000	x10.00	x12.00	x14.00	x16.00	x18.00	x20.00	x22.00	x24.00
	1001	x15.00	x18.00	x21.00	x24.00	x27.00	x30.00	x33.00	x36.00
	1010	x30.00	x36.00	x42.00	x48.00	x54.00	x60.00	x66.00	x72.00

Table 8-2 Analog Gain Table

8.1.2. Digital Gain

Digital gain can be controlled through the registers in Table 8-3.

Register Name	RW	Bits	Register Description	
			Field Name	Field Description
L_D_GAIN (Reg_0x500C)	Large Pixel Global Digital Gain control register **(Default 0x00)**			

	RW	[7:0]	**L_D_GAIN**	[7:5] : Large Pixel Global Digital Gain1 control [4:0] : Large Pixel Global Digital Gain2 control Gain = 2^L_D_GAIN[7:5]*(1 + L_D_GAIN[4:0]/32)
S_D_GAIN (Reg_0x500D)	Small Pixel Global Digital Gain control register **(Default 0x00)**			
	RW	[7:0]	**S_D_GAIN**	[7:5] : Small Pixel Global Digital Gain1 control [4:0] : Small Pixel Global Digital Gain2 control Gain = 2^S_D_GAIN[7:5]*(1 + S_D_GAIN[4:0]/32)

Table 8-3 Digital Gain Control

D_GAIN[7]	D_GAIN[6]	D_GAIN[5]	Digital Gain1 Output
0	0	0	x1
0	0	1	x2
0	1	0	x4
0	1	1	x8
1	X	X	x16

Table 8-4 Digital Gain 1 Table

D_GAIN[4]	D_GAIN[3]	D_GAIN[2]	D_GAIN[1]	D_GAIN[0]	Digital Gain2 Output
0	0	0	0	0	x1.00
0	0	0	0	1	x1.03
0	0	0	1	0	x1.06
0	0	0	1	1	x1.09
0	0	1	0	0	x1.13
0	0	1	0	1	x1.16
0	0	1	1	0	x1.19
0	0	1	1	1	x1.22
0	1	0	0	0	x1.25
0	1	0	0	1	x1.28
0	1	0	1	0	x1.31
0	1	0	1	1	x1.34
0	1	1	0	0	x1.38
0	1	1	0	1	x1.41
0	1	1	1	0	x1.44
0	1	1	1	1	x1.47
1	0	0	0	0	x1.50
1	0	0	0	1	x1.53
1	0	0	1	0	x1.56
1	0	0	1	1	x1.59
1	0	1	0	0	x1.63
1	0	1	0	1	x1.66
1	0	1	1	0	x1.69
1	0	1	1	1	x1.72
1	1	0	0	0	x1.75
1	1	0	0	1	x1.78
1	1	0	1	0	x1.81
1	1	0	1	1	x1.84
1	1	1	0	0	x1.88

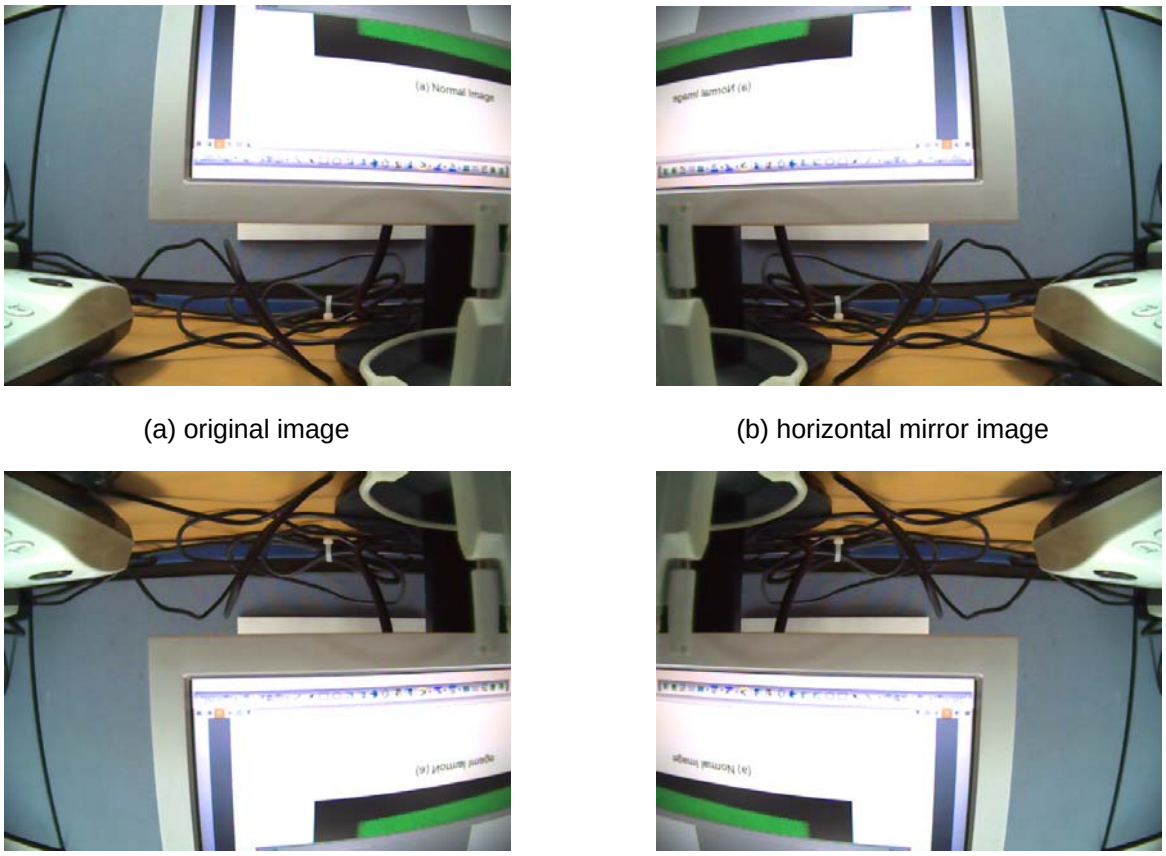
1	1	1	0	1	x1.91
1	1	1	1	0	x1.94
1	1	1	1	1	x1.97

Table 8-5 Digital Gain 2 Table

8.2. Mirror Control

CP8108 can use the horizontal/vertical mirror function through the IMG_CON(0x5014) register.

Figure 8-1 shows the image when mirror control is used.



(a) original image

(b) horizontal mirror image

(c) vertical mirror image

(b) horizontal/vertical mirror image

Figure 8-1 mirror control image

9. BLC(Black Level Compensation)

Various noises are created at the image sensor which converts light into electric signals. Among those are offset form noise from heat and noise from analog circuit which processes signals. In order to measure and remove the offset form noise, create a pixel area (optical black area) which is not affected by light due to metal blovking, and change the relevant pixel value to true ‘ 0’ . Such offset adjustment work is called BLC(Black Level Compensation).

10. ISP(Image Signal Processing)

10.1. Overview

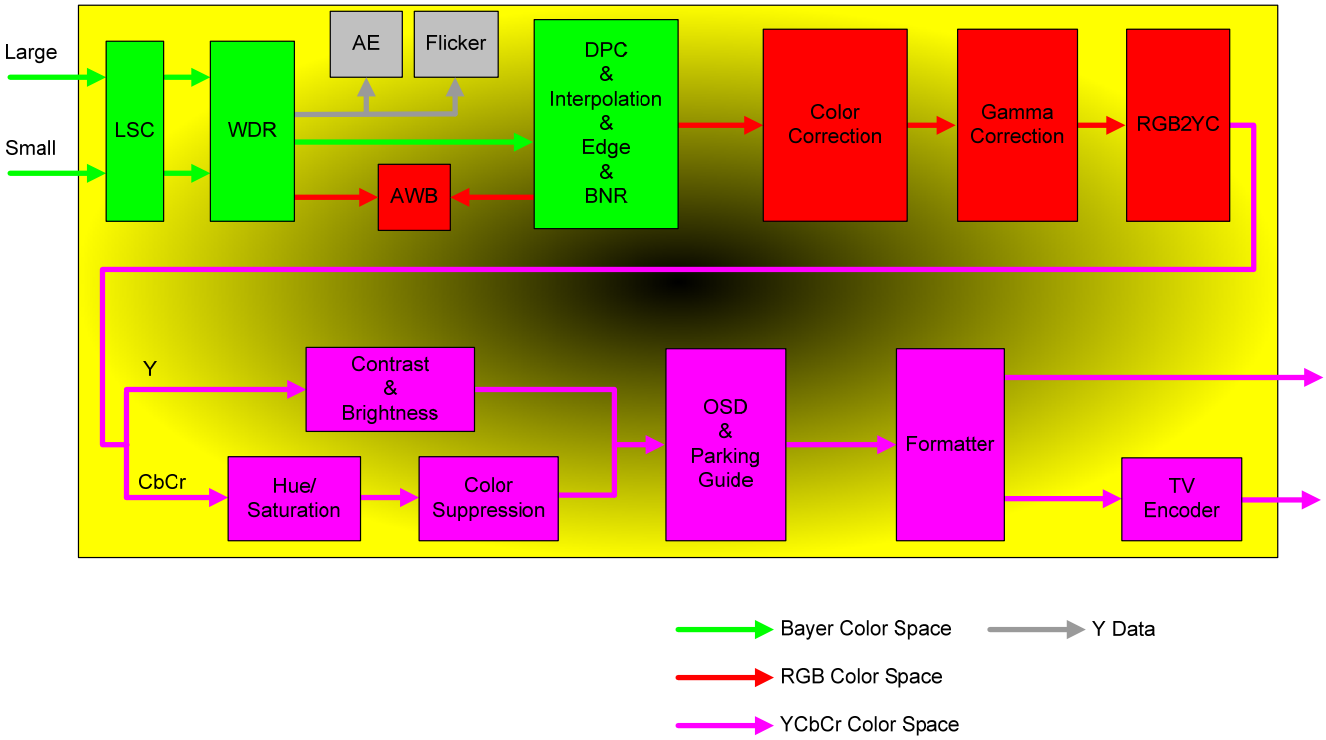


Figure 10-1 ISP Block Diagram

ISP (Image Signal Processing) carries out a function whereby the 10 bit data input from the sensor is converted into RGB and image processed to be output again. As shown in Figure 10-1 ISP Block Diagram, the input video data is processed together with Y and RGB data for Auto Exposer(AE) and Auto White Balance (AWB), through LSC and blocks. Bayer format data goes through interpolation part to be converted to R[9:0], G[9:0], B[9:0].

R, G, B data interpolated are transformed into 8 bit data after color correction and gamma correction of each R, G, and B, and transformed R, G, B data are then transformed into brightness signal YH and color difference Cb, Cr signals. Therefore the bayer format video data input from the sensor is transformed into brightness and color difference singals, and are used to enhance image quality per user request. Transformed data can be output in either of YCrCb 4:2:2, RGB565 or RGB555, Bayer formats.

10.2. LSC(Lens Shading Compensation)

As camera modules get smaller by trend, small external lens and large f number optical devices experience image distortion due to geometrical arrangement of pixel array.

Pixels of image sensor RGB Color Filter Array (CFA) center and edges are subject to light from different directions. These minute location differences cause illumination differences, and illumination differences also affect color due to light wave and micro lens curvature differences. As a result, color distortion and signal size decrease dependant on the pixel location inevitably happens, and this causes the image quality fall in the original image. Figure 10-2 white images taken with an optical instrument and lens shading image ‘ signal amplitude vs distance from the center’ is a characteristics graph.

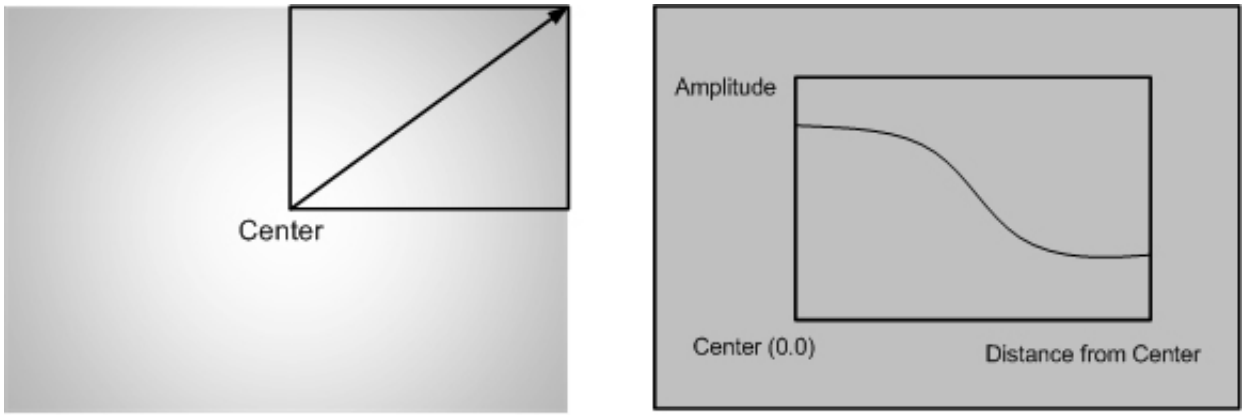


Figure 10-2 Lens Shading Image graph

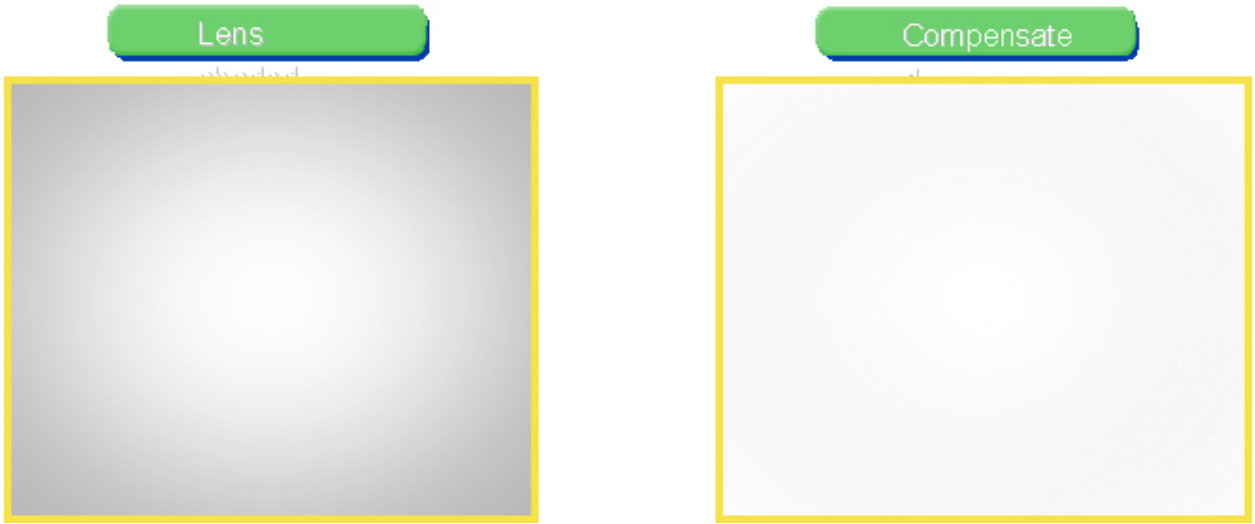


Figure 10-3 LSC Algorithm effect

10.2.1. Gain for LSC

Lens shading correction performs correction of a lens shading distortion due to gradual brightenss differences from the center to the edges. Lens shading correction gain uses the ar^2 fucntion whereby r is

a distance between the center and the relevant coordinates. Normally, the lens shading correction gain error increases from center to the edges. In CP8108, the two gains can be combined to compensate. Figure 10-4 is an illustration of such case.

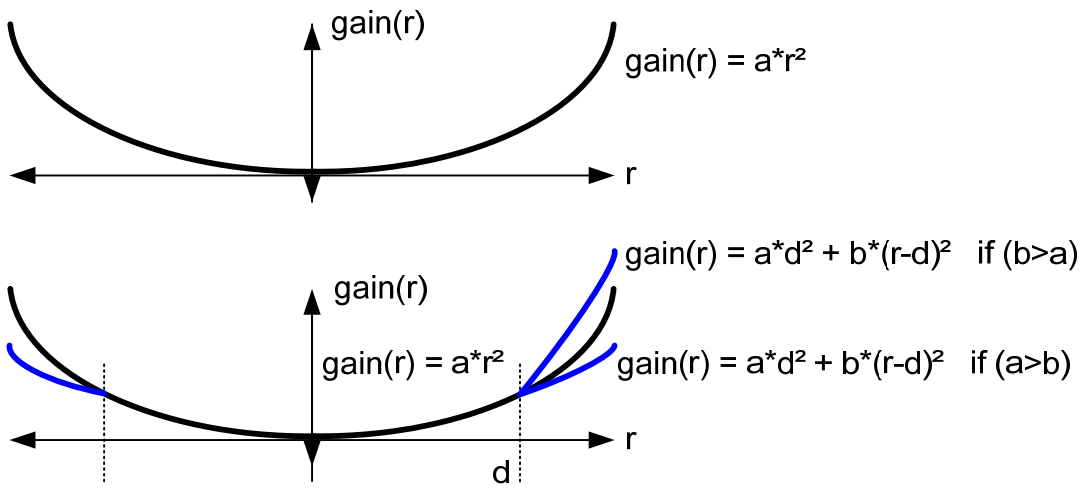


Figure 10-4 Example of Two Gain Control

Gain control for adjusting CP8108 distortion can control each of R, Gr, Gb, B of large and small pixels. (LSC register : 0x5204 ~ 0x5215)

10.2.2. LSC Centering

Compensates for the differnece bewween the center of the pixel array and the center of the lens. CP8108 provides register(0x5201~0x5203) for LSC center.

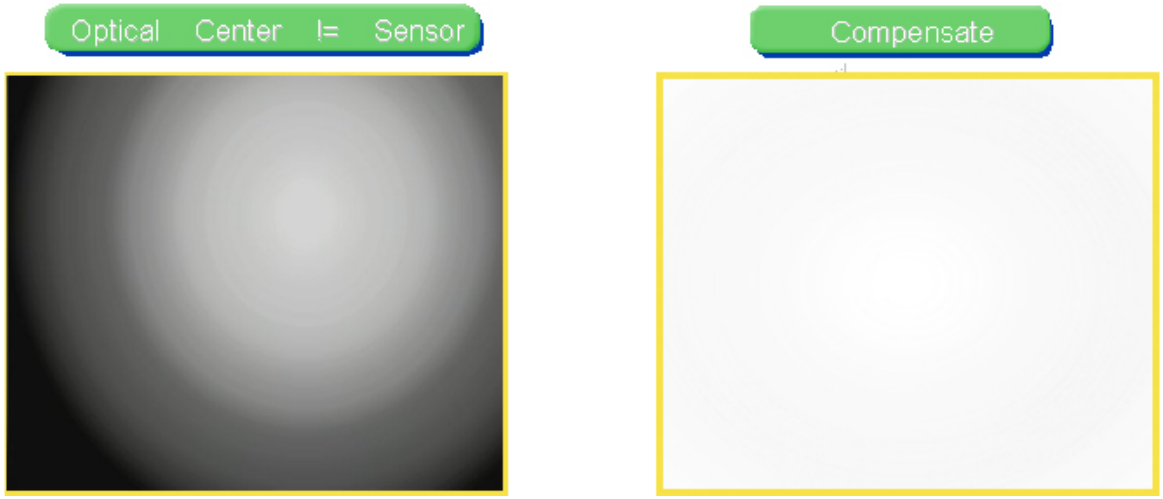


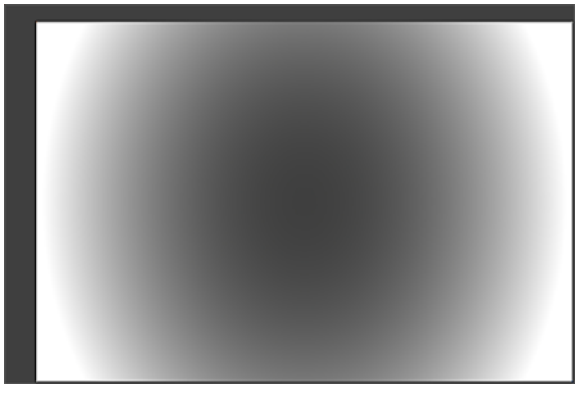
Figure 10-5 LSC Centering effect

10.2.3. LSC Centering

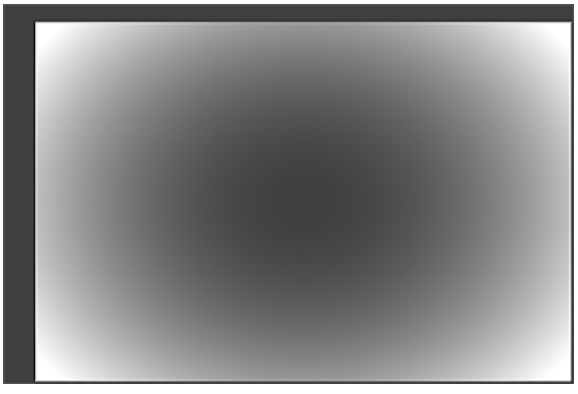
CP8014 has a width:height ratio of 1:1.1385 with height being greater. Hence when compensating for shading, 1.1385 of weight needs to be applied on the width. For design convenience, 1.125 of weight can be applied, and then up to 1.25 in 1/2 steps. Also, different weights for each of width and height can be applied.

Width Weight Ratio : LSC_CON[3:1] = 3’ d0 => 0%
= 3’ d1 => 0.390625%
= 3’ d2 => 0.78125%
= 3’ d3 => 1.5625%
= 3’ d4 => 3.125%
= 3’ d5 => 6.25%
= 3’ d6 => 12.5%
= 3’ d7 => 25.0%

Height Weight Ratio : LSC_CON[6:4] = 3’ d0 => 0%
= 3’ d1 => 0.390625%
= 3’ d2 => 0.78125%
= 3’ d3 => 1.5625%
= 3’ d4 => 3.125%
= 3’ d5 => 6.25%
= 3’ d6 => 12.5%
= 3’ d7 => 25.0%



(a) Width 25% weighting



(b) Height 25% weighting

Figure 10-6 LSC Weighting

10.3. (Wide Dynamic Range) TBD

Dynamic Range a scope of dynamics that can be expressed in one screen. The larger the dynamic range, the more likely the capture of outside/inside environments simultaneously. Figure 10-7 shows a comparison of capture with a normal sensor, and with .

CP8108 can set the light response characteristics to express 120dV dynamic range video.

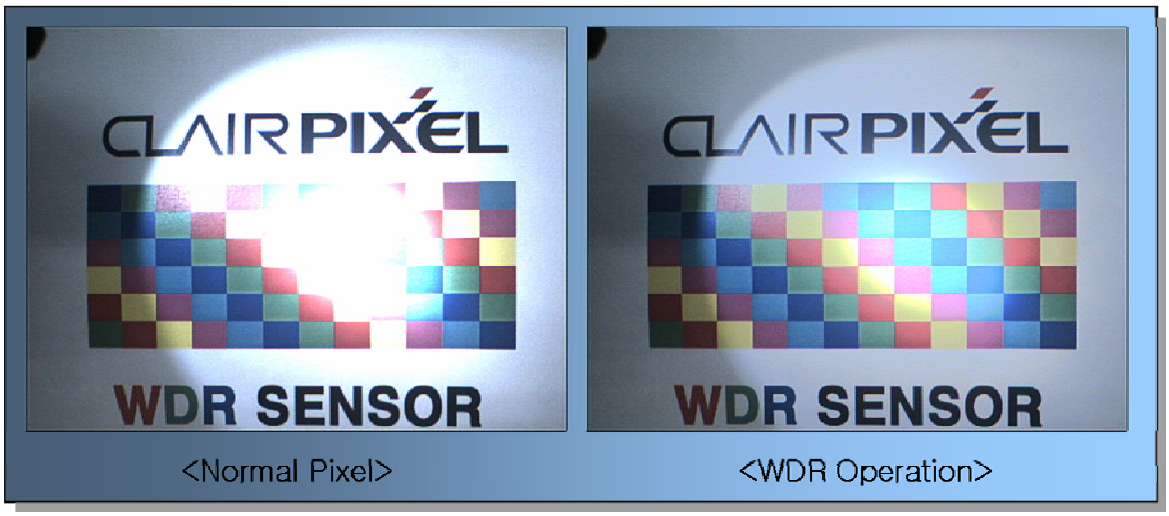


Figure 10-7 Image Comparison

10.4. ISP1

ISP1 (Image Signal Processing1) receives Bayer format 10 bit data as input, converts it to RGB and outputs after image processing. Bayer format data passes through interpolation part and is converted into R[9:0], G[9:0], B[9:0]. RGB data is converted into YCbCr data through RGB2YCbCr block, and the Hue/Saturation block controls Hue, Saturation, Contrast and Brightness.

10.4.1. Defect Pixel Compensation(DPC)

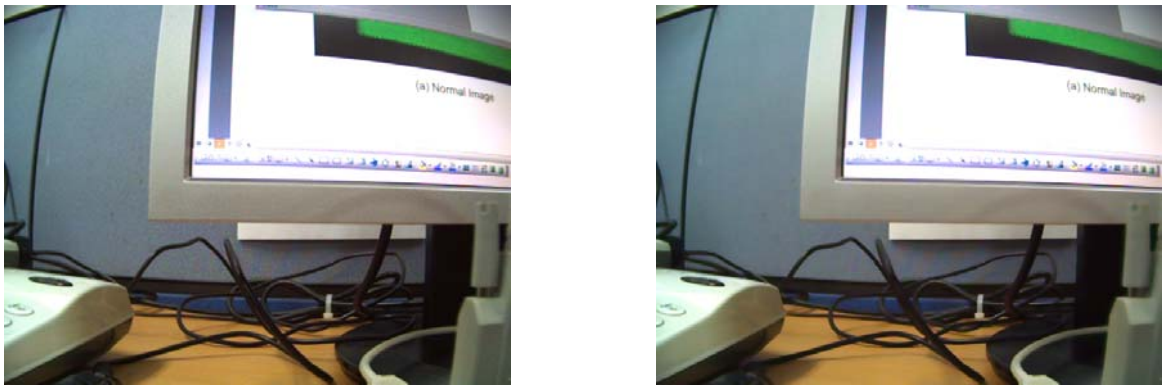
DPC finds defect pixels, and corrects it using the surrounding pixels as shown in Figure 10-8.

Figure 10-8 DPC Image

DPC used in CP8108 determines defect pixels by comparing color of pixels in a 5x5 window with the center pixel to correct it.

10.4.2. Bayer Noise Reduction(BNR)

CP8108 performs noise reduction function in order to reduce the pixel noise on Bayer image. BNR block can control the BNR strength value for each color.



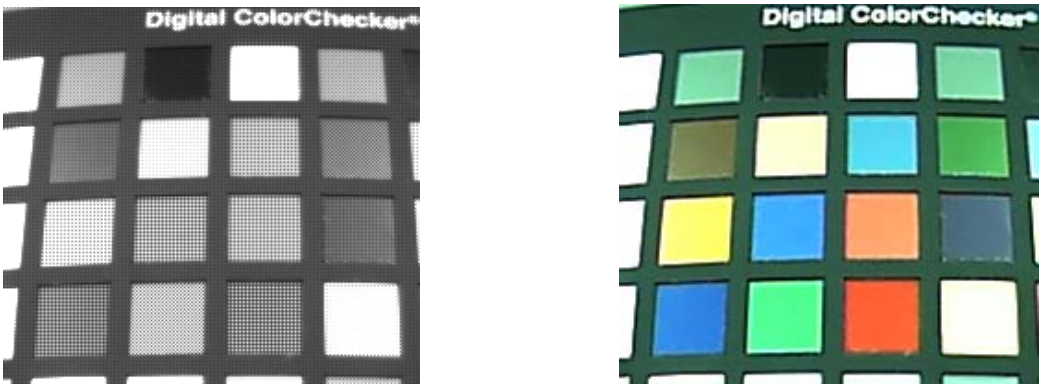
(a) Normal Image (b) Bayer Noise Reduction Image

Figure 10-9 Bayer Noise Reduction

10.4.3. Color Interpolation

Color Interpolation is a block which acquires color from surrounding pixels if a pixel only has a single

color information.



(a) Bayer Image (b) Interpolation Image

Figure 10-10 Color Interpolation Image

CP8108 Interpolation block, in addition to CP8108 Interpolation function has functions including YC noise reduction, Edge Enhancement, False Color Suppression, and RGB gain for White Balance.

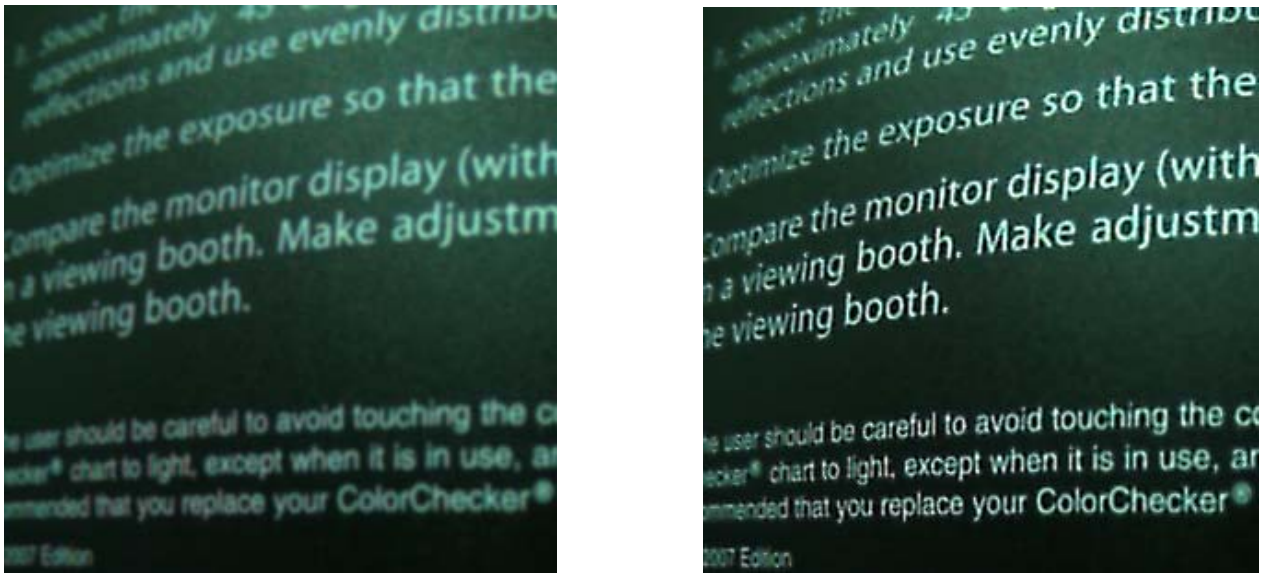
YC noise reduction classifies between the plane section and edge section of a video to blur the plane section while maintaining the edge to reduce image noise. This function can be set on Register(0x5500).

(a) YC Noise Reduction Off (b) YC Noise Reduction On

Figure 10-11 YC Noise Reduction Image

Figure 10-12 is an illustration of edge enhancement function to increase sharpness of the image. Edge Enhancement of CP8108 is controlled by Edge Threshold Leve, Corring Level, and Edge Gain. Register(0x5508~0x5509) is a register to decide the edge threshold level. If the difference between the central pixel and its surrounding pixel is less than the edge threshold level, edge gain is not applied, and for pixels where the difference is larger than the edge threshold level, edge gain is applied to increase the image sharpness. Also, coring level is set on register(0x550A~0x550B) so that edge gain is not

applied on random noise.



(a) Edge Enhancement Off (b) Edge Enhancement On(gain : x12)

Figure 10-12 Edge Enhancement Image

10.4.4. Color Correction

Color Correction controls of color balance of acquired image to suit the target color checker. When AWB is performed, the image brightness ingredients changes and color correction needs to be performed as well.

$$\begin{pmatrix} R\_out[9:0] \\ G\_out[9:0] \\ B\_out[9:0] \end{pmatrix} = \begin{pmatrix} CC\_00 & CC\_01 & CC\_02 \\ CC\_10 & CC\_11 & CC\_12 \\ CC\_20 & CC\_21 & CC\_22 \end{pmatrix} \times \begin{pmatrix} R\_in[9:0] - R\_offset[7:0] \\ G\_in[9:0] - G\_offset[7:0] \\ B\_in[9:0] - B\_offset[7:0] \end{pmatrix}$$

Figure 10-13 Color Correction Matrix

The above equation is about the color correction. As shown above, the input color signals R_in[9:0], G_in[9:0], and B_in[9:0] are adjusted to each offset values and are transformed by the color correction matrix. Each coefficient of the matrix can be set as negative value or positive value depending on the sign bit (MSB of each coefficient). In case of a negative number, it is in a form of two's complement. The coefficients which are expressed in 10bit (except sign and overflow bytes) can be divided into 256, and each coefficient value range is 04 ~ 3.996. An appropriate coefficient is found and set depending on each image system lens, IR filter, and sensor type. When configuring each coefficients, CC_00 – {CC_01 + CC_02}, CC_10 – {CC_11 + CC_12}, CC_20 – {CC_21 + CC_22} need all to be set as same values to maintain white balance.

With actual CP8108, Color Correction Matrix of each light source are saved on the firmware and applied depending on the light source.

10.4.5. Gamma Correction

CP8108 supports the following GAMMA MODES.

1) non gamma mode
2) linear gamma mode
3) non linear gamma mode (Each RGB or global)

*** Non Gamma Mode**

Only selects the low-rank 8bit out of 10bit data. If 10bit data is over 255, the output data value is 0xff.

*** Linear Gamma Mode**

Only selects the low-rank 8bit out of 10bit data.

*** Non Linear Gamma Mode**

16 registers are applied for gamma mapping in Non Linear Gamma Mode. Relevant register R, G, B are defined seperately, but when GAMMA_CONTROL[2](0x5703) is set R, B uses G register values.

Gamma control register is defined in 0x5710 ~0x574F.

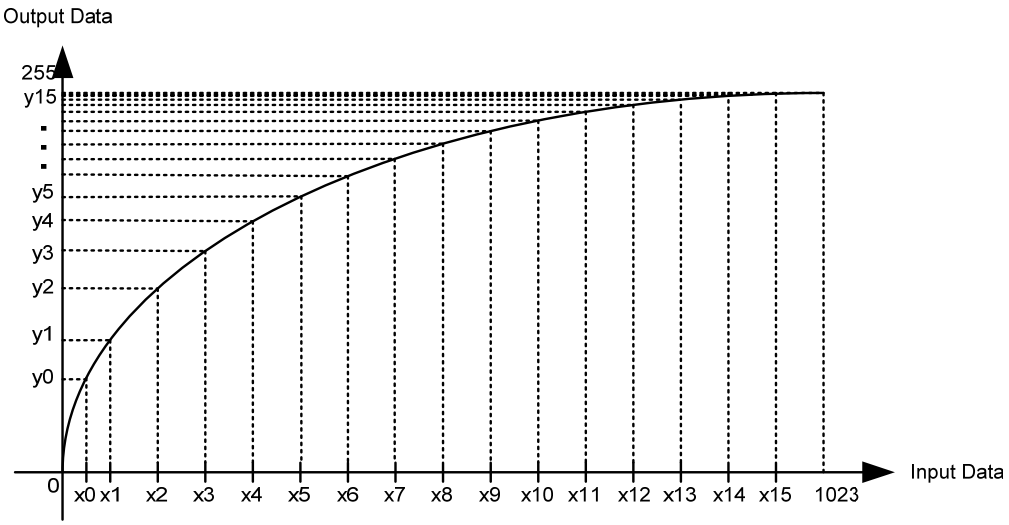


Figure 10-14 GAMMA register and GAMMA value

Figure 10-14 X0 ~ X15 look at the mapping code to each register set in the range of values and, Y0 ~ Y15 mapping of the range to be entered into a register value can be set.

Output Data = Input Data*Y0/X0	(Input Data range : 0~X0)
Output Data = Input Data*(Y1-Y0)/(X1-X0)	(Input Data range : X0~X1)
Output Data = Input Data*(Y2-Y1)/(X2-X1)	(Input Data range : X1~X2)
Output Data = Input Data*(Y3-Y2)/(X3-X2)	(Input Data range : X2~X3)

:

Output Data = Input Data*(Y15-Y14)/(X15-X14)　　(Input Data 가 X14~X15 일 때)

Output Data = Input Data*(255-Y15)/(1023-X15)　　(Input Data 가 X15~X1023 일 때)

Figure 10-15 Gain Application to Brightness Threshold

10.5. ISP2

ISP2 (Image Signal Processing2) receives output RGB format from ISP1 block as input. Input 8bit RGB data is transferred to brightness Y and color difference Cb, Cr data in RGB2YCbCr block. Data converted to YCbCr format go through image enhance functions to suit user demand including Hue, Saturation, Contrast, Edge control, and color suppression.

10.5.1. RGB to YCbCr

CP8108 RGB to YcbCr block converts R coefficient, G coefficient, B coefficient, Y offset, C offset value inputs to convert to Y, Cb, Cr values. The three below equations are normally used equations. CP8108 uses SDI equation as default setting.

Y601 = 0.299*R + 0.587*G + 0.114*B
Cb = -0.172*R – 0.339*G + 0.511*B + 128
Cr = 0.511*R – 0.428*G – 0.083*B + 128
R,G,B are in 16~235 range
Y601 is in 16~235 range (0-219, offset=16)
Cb, Cr are in 16~240 range (+/- 112, offset=16)

Figure 10-16 Basic Equations

Y601 = 0.299*R + 0.587*G + 0.114*B
Cb = -0.169*R – 0.331*G + 0.500*B + 128
Cr = 0.500*R – 0.419*G – 0.081*B + 128
R,G,B are in 0~255 range
Y601 is in 0~255 range (0-255, offset=0)
Cb, Cr are in 0~255 range (+/- 127, offset=0)

Figure 10-17 SDI Equations

Y601 = 0.257*R + 0.504*G + 0.098*B + 16
Cb = -0.148*R – 0.291*G + 0.439*B + 128
Cr = 0.439*R – 0.368*G – 0.071*B + 128
R,G,B are in 0~255 range, 8-bit values
Y601 is in 16~235 range (0-219, offset=16)
Cb, Cr are in 16~240 range (+/- 112, offset=16)

Figure 10-18 Digital Equations

10.5.2. Cb/Cr Gain

Cb/Cr gain control moves current color difference information towards Cb axis or Cr axis by applying saturation gain on color coordinates. Cb/Cr gain can be applied in 0~2x ranges.

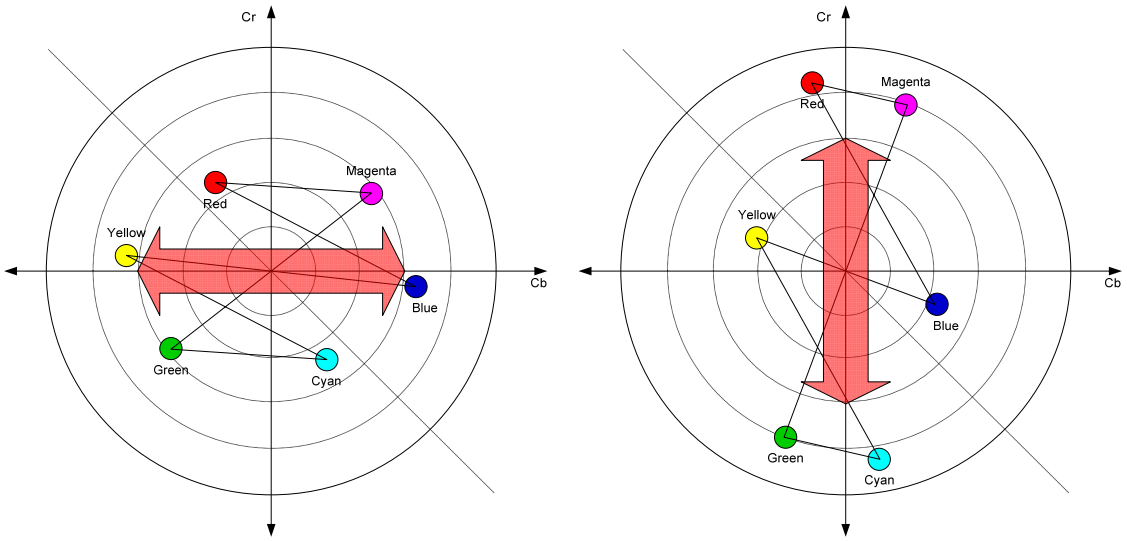


Figure 10-19 Cb/Cr gain control

10.5.3. Hue Control

Hue control is used for global or individual color information change. Hue can be changed between -45°~+45° in 1° units and uses 2's complement.

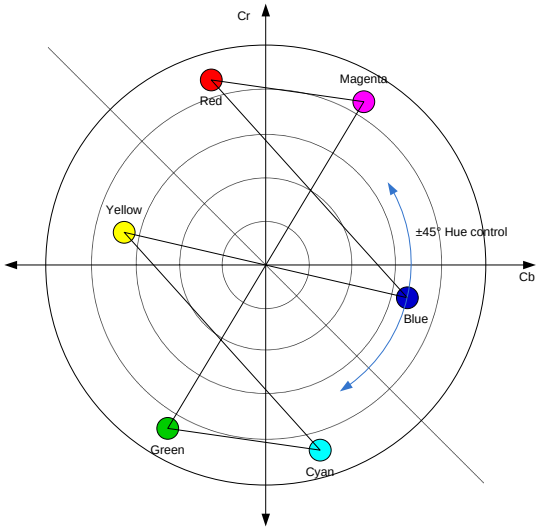


Figure 10-20 Hue control

10.5.4. Saturation Control

Saturation control is used to control the image saturation. Saturation gain can be applied in 0~2x ranges.

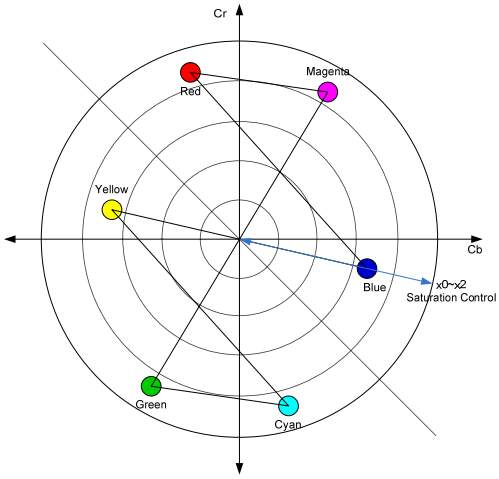


Figure 10-21 Saturation control

10.5.5. Contrast Control

Contrast control block is based on the reference point luminance, and controls the contrast by reducing the luminance of areas where luminance is lower than the reference point, and increasing the luminance of areas where luminance is above the reference point. Reference point normally used is 128, and can be changed depending on the situation. Contrast gain can be applied in 0~2x ranges.

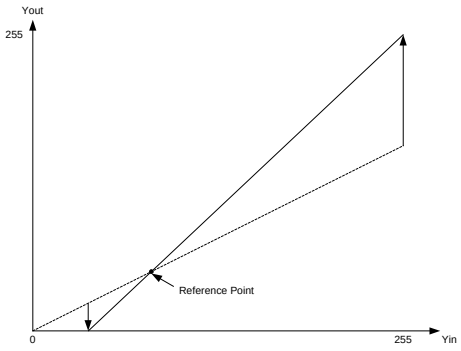
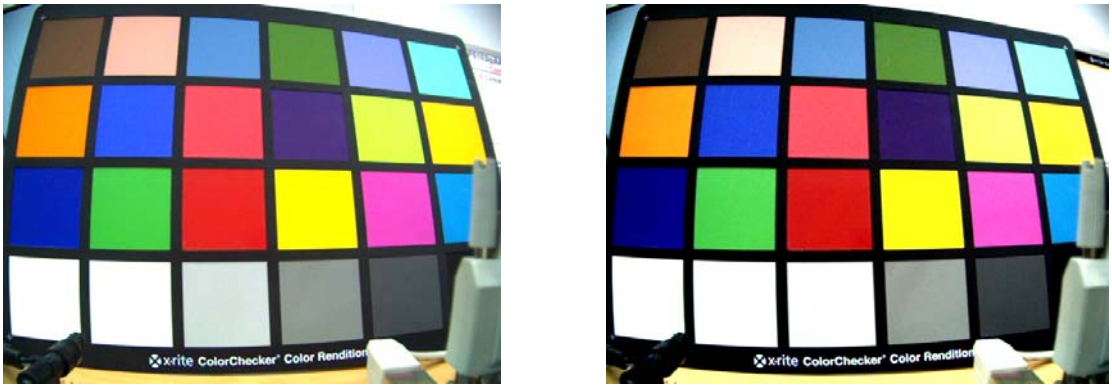


Figure 10-22 Contrast control

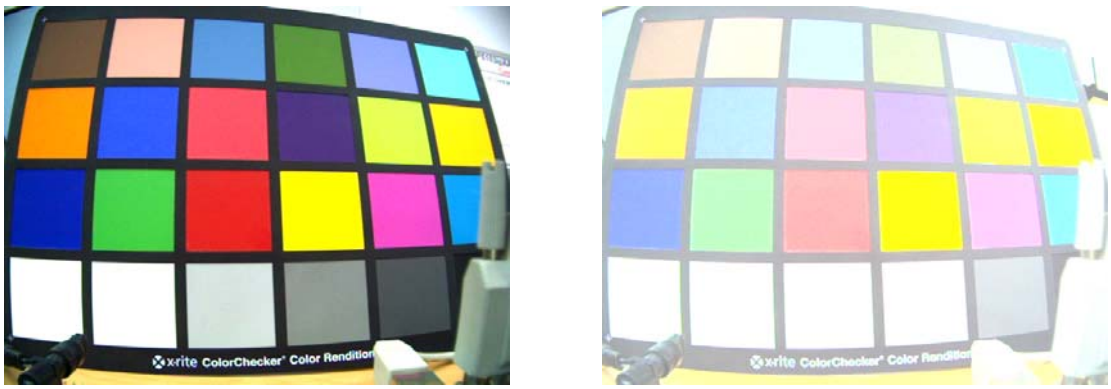


(a) Normal Image(x1.0) (b) Contrast (x1.5)

Figure 10-23 Contrast Image

10.5.6. Brightness Control

Brightness control gives offset to the image luminance to control the brightness of the image, and the size of the offset can be chosen between 0~255.



(a) Normal Image (b) Brightness=128

Figure 10-24 Brightness control

10.5.7. Color Suppression

Color Suppression function is a function to reduce the color component when luminance is too high or low or if there is unwanted color noise.

Threshold value and gain control is possible on each of Cb and Cr.

Cb => thresh hold low : ‘ h6213 thresh hold high : ‘ h6211
gain low : ‘ h6214 gain high : ‘ h6212

Cr => thresh hold low : ‘ h6218 thresh hold high : ‘ h6216
gain low : ‘ h6219 gain high : ‘ h6217

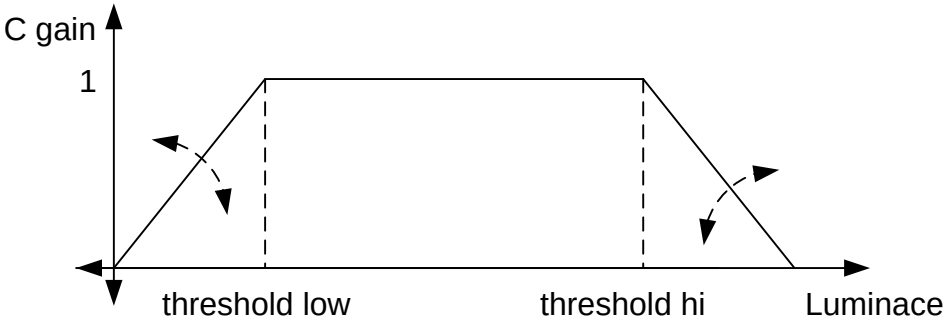


Figure 10-25 Applying Gain on Luminance Threshold

10.5.8. OSD(On Screen Display)

OSD(On Screen Display) is a function to display the information user needs directly on screen. CP8108 OSD is largely composed of three parts including text menu, parking guide, and privacy zone.

Text menu was designed for displaying text information for users to help product installation and optimization, and parking guide was designed for helping rear parking using rear-view camera, and privacy zone was designed for protecting privacy using CCTV.

10.5.8.1. Text Menu

Text menu was designed for displaying text information for users to help product installation and optimization.

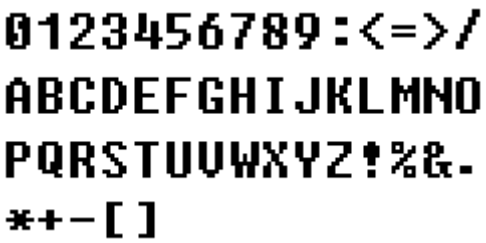


Figure 10-26 Character Font Information Example

Font information for a maximum of 51 characters can be saved simultaneously, and including the blank character provided as base a maximum of 52 font information is saved.

Figure 10-27 Text Menu Example

10.5.8.2. Parking Guide

Parking guide was designed to help rear parking using rear-view camera. The lines drawn on parking guide screen can be adjusted for their transparency, each line's width can be adjusted in pixel units, and the color information can be set with YUV. Figure 10-28 is an example of a parking guide which has been set following this method.

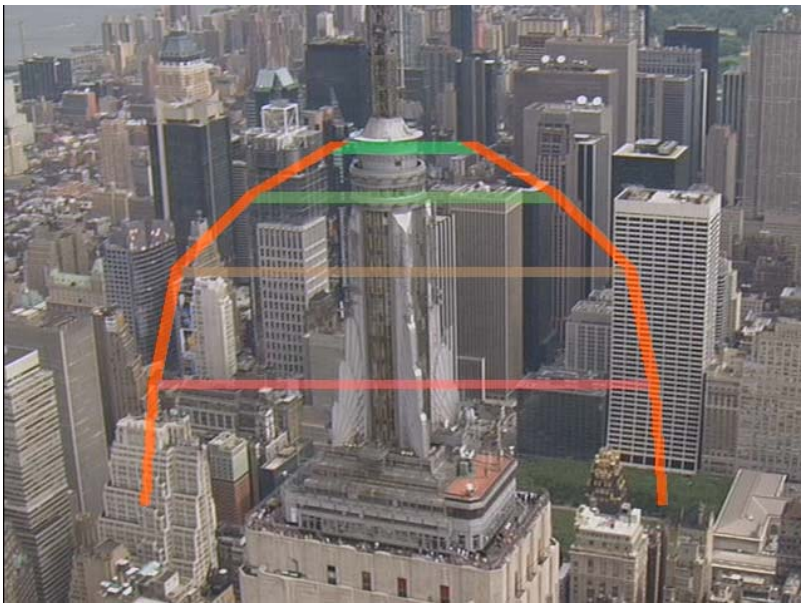


Figure 10-28 Parking Guide Example

10.5.8.3. Privacy Zone

Privacy zones were designed to protect privacy in using CCTV or others.

Rectangular masks are output instead of the sensor output at user designated locations. Up to 8 of these masks can be set, and when the different color masks overlap, the mask with the smaller internal mask number takes priority. Figure 10-29 is an example of a privacy zone set.

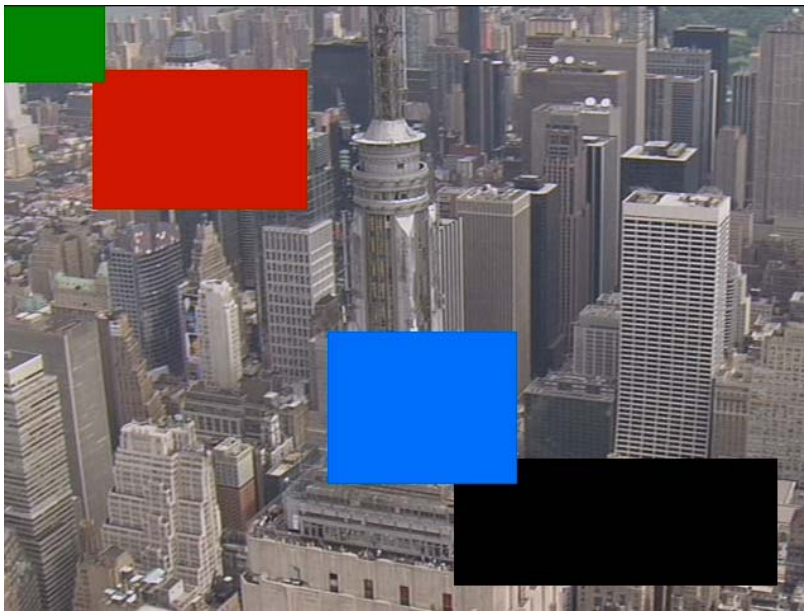


Figure 10-29 Privacy Zone Example

10.5.9. Formatter

CP8108 can output Bayer 8/10 bit, YCbCr 4:2:2 and RGB565/555 format digital data. Digital data can be output in 720x480, 640x480, 720x576 modes. In PAL mode operation, CCIR656 output is supported to suit PAL output format. In addition the polarity of Vsync/Hsync/pclock signals can be controlled and the output data sequences can be set in a preferred order. When in 8 bit output mode, the 8bit data MSB location can be changed.

10.5.9.1. Timing Diagram

- YCbCr 4:2:2 mode

YCbCr 4:2:2 format data can be output through the PDATA[9:0] port. Since the final output is 8 bit, only 8 port out of the PDATA 10bit port is used and 8 bit data location can be changed using PDATA_CON[1:0] value. Also, depending on the DATA_FMT_CON[4:3] register value, the data sequence can be changed as shown in Figure 10-30.

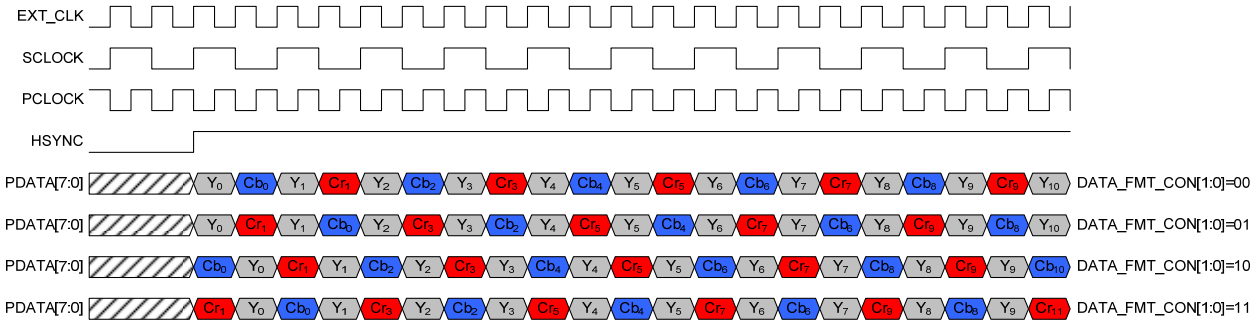
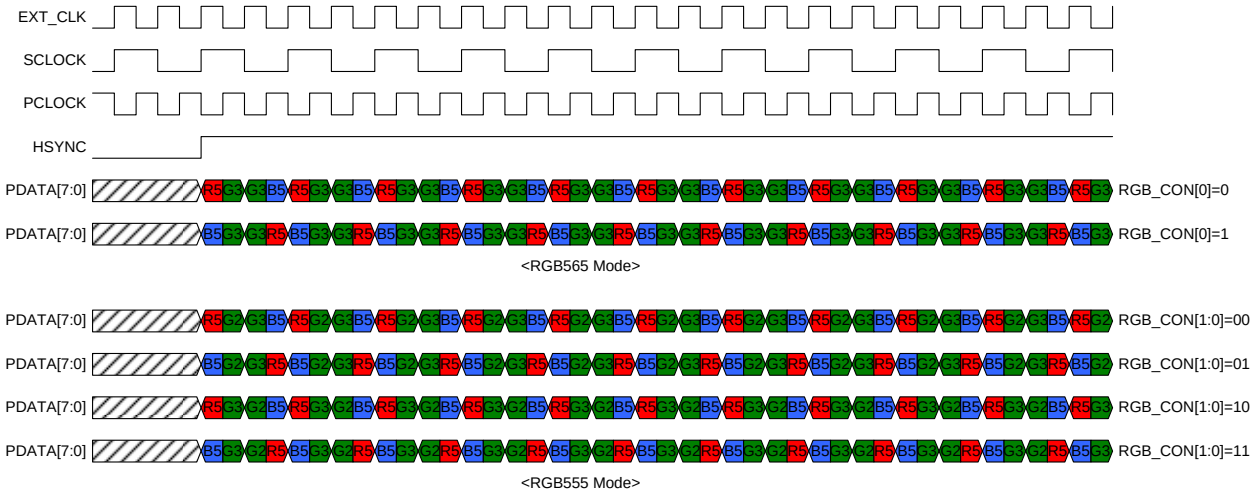


Figure 10-30 YCbCr Mode

- RGB565/555

RGB565/555 format data can be output through the PDATA[9:0] port. The final output is 8 bit in case of RGB565, and 8 or 7 bit in case of RGB555, and thus the output data location can be decided using the RGB_CON[1] value of the 10bit port PDATA. Also, depending on the RGB_CON[0] register value, the data sequence can be changed as shown below in Figure 10-31.



Mode	RGB_CON[1:0]	PDATA[7:0]
RGB555	00	0 $R_4R_3R_2R_1R_0G_4G_3$ $G_2G_1G_0B_4B_3B_2B_1B_0$
	01	0 $B_4B_3B_2B_1B_0G_4G_3$ $G_2G_1G_0R_4R_3R_2R_1R_0$
	10	$R_4R_3R_2R_1R_0G_4G_3G_2$ $G_1G_0B_4B_3B_2B_1B_0$ 0
	11	$B_4B_3B_2B_1B_0G_4G_3G_2$ $G_1G_0R_4R_3R_2R_1R_0$ 0

Figure 10-31 RGB565/555 Mode

- Bayer 8bit/10bit

Bayer 8 bit/10 bit format data can be output through the PDATA[9:0] port. Final output of Bayer 8 bit is 8 bit and so only 8 ports of 10 bit port PDATA is used and 8 bit data location can be decided using the PDATA_CON[1:0] value. Also, depending on the RGB_CON[3:2] register value, the data sequence can be changed as shown below in Figure 10-32.

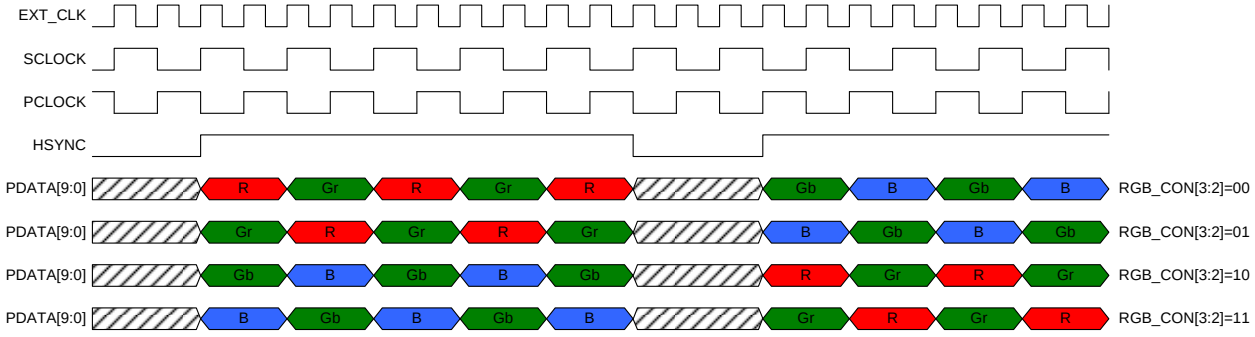


Figure 10-32 Bayer 8/10 bit Mode

10.5.9.2. Windowing

In 640x480 mode output, windowing function can be used to output the preferred section. Figure 10-33 is an example of a windowing control in 640x480 mode.

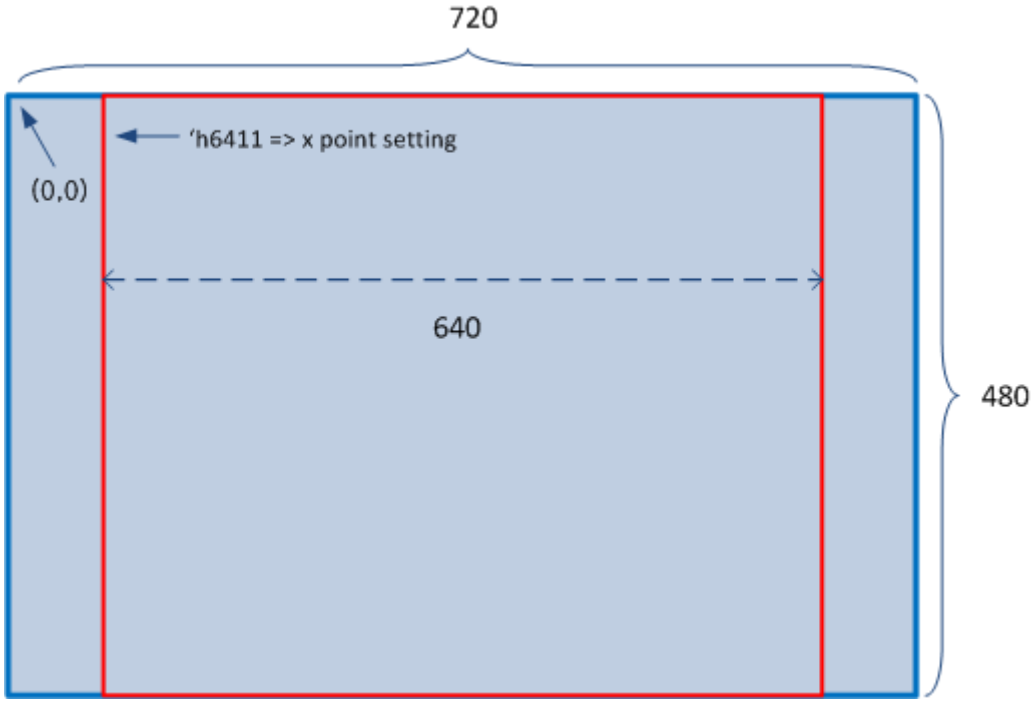


Figure 10-33 windowing control

10.5.10. Auto Control Function

CP8014 has auto control functions such as AE, Anti-Flicker, and AWB. These functions are not all processed in the ISP block, but transfers the information to the MCU that can operate the auto control algorithm. As shown in Figure 10-34, the brightness(Y) data for Anti-Flicker and RGB data for AWB are transferred to the MCU and depending on the calculation results of each algorithm, expose time, and RGB gain are performed.

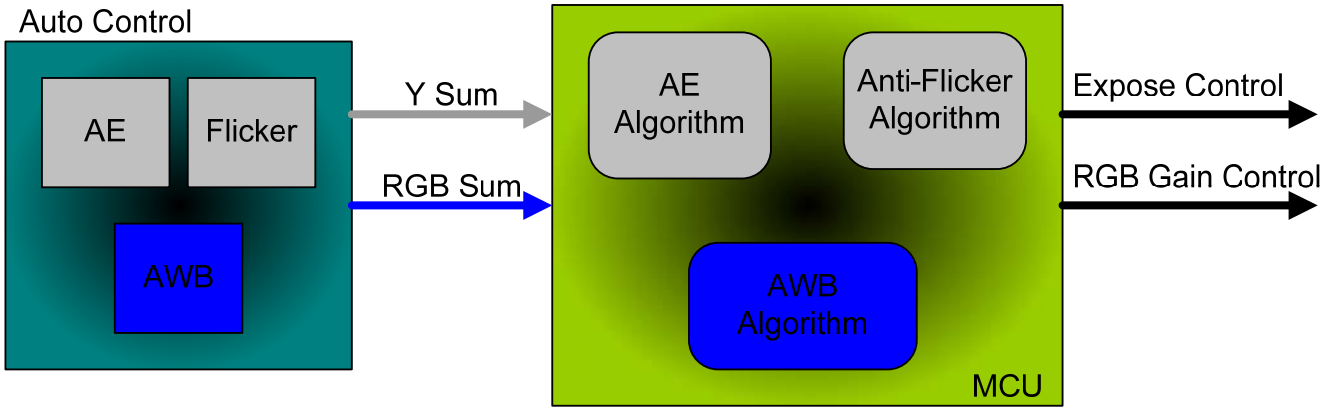


Figure 10-34 Auto Control Function

11. Register definition

11.1. System

ADDRESS (HEX)	REGISTER NAME	R/W	DEFAULT (HEX)	DESCRIPTION
0x4000	PRODUCT_ID1	R	0x81	Product ID1
0x4001	PRODUCT_ID2	R	0x04	Product ID2
0x4002	PRODUCT_ID3	R	0x30	Product ID3
0x4003	PIXEL_TYPE	R/W	0xA0	bit[7:0] : pixel type and revision number
0x4004	CLOCK_CONFIG	R/W	0x00	[7:4] : reserved [3:2] : Sensor Clock 00 : Ext Clock 01 : Ext Colck / 2 10 : Ext Colck / 3 11 : Ext Colck / 4 [1:0] : Main Clock 00 : Ext Clock 01 : Ext Colck / 2 10 : Ext Colck / 3 11 : Ext Colck / 4
0x4005	DEVICE_CONTROL	R/W	0x02	[7] : sleep [6] : power down mode selection [5] : pull down if powerdown at gpio & pbus [4] : NTSC enable [3] : ISP enable [2] : TG enable [1] : MCU reset [0] : MCU enable
0x4006	I2C_SLAVE_ID	R/W	0x77	I2C Slave Device ID Value ID = [Value[7:1], R/W Flag[0]]
0x4007	I2C_SLAVE_LAST_INDEX	R	0x00	I2C Last Index address
0x4008	I2C_SLAVE_GLITCH	W	0x08	I2C slave glitch
0x4009	I2C_MASTER_START	W	0x00	[7:1] : reserved [0] : i2c master start
0x400A	I2C_MASTER_STATUS	R	0x00	I2C Status register 0x00 : IDLE 0xAA : Transmit Success 0xBB : Transmit Fail 0xCC : I2C Line Busy
0x400B	I2C_MASTER_CONTROL	R/W	0xA0	I2C Master Control [2:0] : Transmit Byte Select 000 : 1 Byte Transfer 001 : 2 Byte Transfer 010 : 3 Byte Transfer 011 : 4 Byte Transfer 1xx : 5 Byte Transfer [3] : Dummy Write On [4] : Read Restart On [7:5] : I2C Clock Ratio Select

[7:5]	Trans	act	grap	End
3'b000	10'd100	10'd200	10'd300	10d'400
3'b001	10'd150	10'd300	10'd450	10d'600
3'b010	10'd200	10'd400	10'd600	10d'800
3'b011	10'd250	10'd500	10'd750	10d'1000

<table>
<tr><td></td><td></td><td></td><td></td><td>
<table>
<tr><td>3’b100</td><td>10’d50</td><td>10’d100</td><td>10’d150</td><td>10d’200</td></tr>
<tr><td>3’b101</td><td>10’d25</td><td>10’d50</td><td>10’d75</td><td>10d’100</td></tr>
<tr><td>3’b110</td><td>10’d12</td><td>10’d24</td><td>10’d36</td><td>10d’48</td></tr>
<tr><td>3’b111</td><td>10’d6</td><td>10’d12</td><td>10’d18</td><td>10d’24</td></tr>
</table>
</td></tr>
<tr><td>0x400C</td><td>I2C_TARGET_ADDRESS</td><td>R/W</td><td>0x00</td><td>I2C target device id</td></tr>
<tr><td>0x400D</td><td>I2C_TARGET_INDEX</td><td>R/W</td><td>0x00</td><td>I2C target Index</td></tr>
<tr><td>0x400E</td><td>I2C_TARGET_DATA1</td><td>R/W</td><td>0x00</td><td>I2C target data1</td></tr>
<tr><td>0x400F</td><td>I2C_TARGET_DATA2</td><td>R/W</td><td>0x00</td><td>I2C target data2</td></tr>
<tr><td>0x4010</td><td>I2C_TARGET_DATA3</td><td>R/W</td><td>0x00</td><td>I2C target data3</td></tr>
<tr><td>0x4011</td><td>I2C_TARGET_DATA4</td><td>R/W</td><td>0x00</td><td>I2C target data4</td></tr>
<tr><td>0x4012</td><td>I2C_TARGET_DATA5</td><td>R/W</td><td>0x00</td><td>I2C target data5</td></tr>
<tr><td>0x4013</td><td>EEPROM_CONFIG</td><td>R/W</td><td>0x00</td><td>[7:1] : reserved
[0] : eeprom disable</td></tr>
<tr><td>0x4014</td><td>I2C_TARGET_RDATA_H</td><td>R</td><td>0x00</td><td>I2C target Read data[15:8]</td></tr>
<tr><td>0x4015</td><td>I2C_TARGET_RDATA_L</td><td>R</td><td>0x00</td><td>I2C target Read data[7:0]</td></tr>
<tr><td>0x4016</td><td>LUMP_INTERVAL</td><td>R/W</td><td>0x00</td><td>
<table>
<tr><th>Interval[3:0]</th><th>Interval decision value</th></tr>
<tr><td>4’b1111</td><td>11’d50</td></tr>
<tr><td>4’b1110</td><td>11’d100</td></tr>
<tr><td>4’b1101</td><td>11’d150</td></tr>
<tr><td>4’b1100</td><td>11’d200</td></tr>
<tr><td>4’b1011</td><td>11’d250</td></tr>
<tr><td>4’b1010</td><td>11’d300</td></tr>
<tr><td>4’b1001</td><td>11’d350</td></tr>
<tr><td>4’b1000</td><td>11’d400</td></tr>
<tr><td>4’b0111</td><td>11’d450</td></tr>
<tr><td>4’b0110</td><td>11’d500</td></tr>
<tr><td>4’b0101</td><td>11’d550</td></tr>
<tr><td>4’b0100</td><td>11’d600</td></tr>
<tr><td>4’b0011</td><td>11’d700</td></tr>
<tr><td>4’b0010</td><td>11’d800</td></tr>
<tr><td>4’b0001</td><td>11’d900</td></tr>
<tr><td>4’b0000</td><td>11’d1023</td></tr>
</table>
</td></tr>
<tr><td>0x4017</td><td>HOST_COMMAND_FLAG</td><td>W</td><td>0x00</td><td>[7:0] : Host command flags
When write, it generates MCU interrupt.
When read, it clears MCU interrupt.</td></tr>
<tr><td>0x4018</td><td>HOST_COMMAND_DATA_0</td><td>W</td><td>0x00</td><td>[7:0] : Host command data 0</td></tr>
<tr><td>0x4019</td><td>HOST_COMMAND_DATA_1</td><td>W</td><td>0x00</td><td>[7:0] : Host command data 1</td></tr>
<tr><td>0x401A</td><td>HOST_COMMAND_DATA_2</td><td>W</td><td>0x00</td><td>[7:0] : Host command data 2</td></tr>
<tr><td>0x401B</td><td>COMMAND_RESULT_0</td><td>R/w</td><td>0x00</td><td>[7:0] :Command Result 0</td></tr>
<tr><td>0x401C</td><td>COMMAND_RESULT_1</td><td>R/W</td><td>0x00</td><td>[7:0] :Command Result 1</td></tr>
<tr><td>0x401D</td><td>COMMAND_RESULT_2</td><td>R/W</td><td>0x00</td><td>[7:0] :Command Result 2</td></tr>
<tr><td>0x401E</td><td>COMMAND_RESULT_3</td><td>R/W</td><td>0x00</td><td>[7:0]: Command Result 3</td></tr>
<tr><td>0x401F</td><td>GPIO_DIRECTION_CONTROL</td><td>R/W</td><td>0xFF</td><td>[7:0] : GPIO[7:0] direction control
0 :output 1 : input</td></tr>
<tr><td>0x4020</td><td>GPIO_IN_OUT_DATA</td><td>R/W</td><td>0x00</td><td>[7:4] : reserved
[3:0] : GPIO[3:0] input/output data</td></tr>
</table>

0x4021	GPIO_PULL_UD_CON	R/W	0xFF	[7:0] : GPIO[7:0] pull up/down control 0 :disable 1 : enable
0x4022	GPIO_PULL_UD_SEL	R/W	0x00	[7:0] : GPIO[7:0] pull up/down selection 0 : pull-down 1 : pull-up
0x4023	GPIO_DRIVE_STRENGTH_SEL	R/W	0x55	[7:6] : GPIO[7:6] drive strength selection 00 : 1mA 01 : 2mA 10 : 4mA 11 : 8mA [5:4] : GPIO[5:4] drive strength selection 00 : 1mA 01 : 2mA 10 : 4mA 11 : 8mA [3:2] : GPIO[3:2] drive strength selection 00 : 1mA 01 : 2mA 10 : 4mA 11 : 8mA [1:0] : GPIO[1:0] drive strength selection 00 : 1mA 01 : 2mA 10 : 4mA 11 : 8mA
0x4024	MEM_ADDR_H	R/W	0x00	[7:0] : High byte of memory address
0x4025	MEM_ADDR_L	R/W	0x00	[7:0] : Low byte of memory address
0x4026	MEM_DATA	R/W	0x00	[7:0] : memory data
0x4027	MEM_CON	R/W	0x00	[7:4] : reserved [3] : fix index address (“1” -> i2c index address is fixed) [2] : reserved [1] : code memory write enable. [0] : code or data memory selection 0 : data 1 : code
0x4028	CHECK_SUM_H	R/W	0x00	[7:0] : High byte of code data check sum
0x4029	CHECK_SUM_L	R/W	0x00	[7:0] : High byte of code data check sum
0x402A	CRC_H	R/W	0x00	[7:0] : High byte of code data CRC
0x402B	CRC_L	R/W	0x00	[7:0] : Low byte of code data CRC
0x402C	CRC_CON	R/W	0x00	[7:1] : reserved [0] : CRC control 0 : disable 1 : enable
0x4054	PDATA_CON1	R/W	0xA0	[7:6] : P_1_0 control 00 : output PDATA[1:0] 01 : floating PDATA[1:0] 10 : floating & pull-down PDATA[1:0] 11 : reserved [5:4] : P_9_2 control 00 : output PDATA[9:2] 01 : floating PDATA[9:2] 10 : floating & pull-down PDATA[9:2] 11 : reserved [3] : DAC test mode [2:0]: reserved

0x4055	PDATA_CON2	R/W	0x01	[7] : GPIO[2] to PCLOCK 0 : disable 1 : enable [6] : GPIO[3] to VSYNC 0 : disable 1 : enable [5] : GPIO[4] to HSYNC 0 : disable 1 : enable [4] : GPIO[5] to PDATA[0] 0 : disable 1 : enable [3] : GPIO[6] to PDATA[1] 0 : disable 1 : enable [2] : GPIO[7] to PDATA[2] 0 : disable 1 : enable [1:0] : PDATA drive strength selection 00 : 1mA 01 : 2mA 10 : 4mA 11 : 8mA
0x40A0	PWM_CON	R/W	0x00	[7] : PWM busy (read only) [6:5] : reserved [4] : PWM start. [3] : reserved [2] : PWM start synchronize VSYNC.falling edge. [1] : PWM loop [0] : PWM enable
0x40A1	PWM_CYC_NUM	R/W	0x00	[7:0] : PWM cycle number
0x40A2	PWM0_POINT1_H	R/W	0x00	[7:0] : High byte of PWM0 point 1
0x40A3	PWM0_POINT1_L	R/W	0x00	[7:0] : Low byte of PWM0 point 1
0x40A4	PWM0_POINT2_H	R/W	0x00	[7:0] : High byte of PWM0 point 2
0x40A5	PWM0_POINT2_L	R/W	0x00	[7:0] : Low byte of PWM0 point 2
0x40A6	PWM0_POINT3_H	R/W	0x00	[7:0] : High byte of PWM0 point 3
0x40A7	PWM0_POINT3_L	R/W	0x00	[7:0] : Low byte of PWM0 point 3
0x40A8	PWM0_POINT4_H	R/W	0x00	[7:0] : High byte of PWM0 point 4
0x40A9	PWM0_POINT4_L	R/W	0x00	[7:0] : Low byte of PWM0 point 4
0x40AA	PWM1_POINT1_H	R/W	0x00	[7:0] : High byte of PWM1 point 1
0x40AB	PWM1_POINT1_L	R/W	0x00	[7:0] : Low byte of PWM1 point 1
0x40AC	PWM1_POINT2_H	R/W	0x00	[7:0] : High byte of PWM1 point 2
0x40AD	PWM1_POINT2_L	R/W	0x00	[7:0] : Low byte of PWM1 point 2
0x40AE	PWM1_POINT3_H	R/W	0x00	[7:0] : High byte of PWM1 point 3
0x40AF	PWM1_POINT3_L	R/W	0x00	[7:0] : Low byte of PWM1 point 3
0x40B0	PWM1_POINT4_H	R/W	0x00	[7:0] : High byte of PWM1 point 4
0x40B1	PWM1_POINT4_L	R/W	0x00	[7:0] : Low byte of PWM1 point 4
0x40B2	PWM2_POINT1_H	R/W	0x00	[7:0] : High byte of PWM2 point 1
0x40B3	PWM2_POINT1_L	R/W	0x00	[7:0] : Low byte of PWM2 point 1
0x40B4	PWM2_POINT2_H	R/W	0x00	[7:0] : High byte of PWM2 point 2
0x40B5	PWM2_POINT2_L	R/W	0x00	[7:0] : Low byte of PWM2 point 2
0x40B6	PWM2_POINT3_H	R/W	0x00	[7:0] : High byte of PWM2 point 3
0x40B7	PWM2_POINT3_L	R/W	0x00	[7:0] : Low byte of PWM2 point 3
0x40B8	PWM2_POINT4_H	R/W	0x00	[7:0] : High byte of PWM2 point 4
0x40B9	PWM2_POINT4_L	R/W	0x00	[7:0] : Low byte of PWM2 point 4
0x40BA	PWM3_POINT1_H	R/W	0x00	[7:0] : High byte of PWM3 point 1
0x40BB	PWM3_POINT1_L	R/W	0x00	[7:0] : Low byte of PWM3 point 1
0x40BC	PWM3_POINT2_H	R/W	0x00	[7:0] : High byte of PWM3 point 2

0x40BD	PWM3_POINT2_L	R/W	0x00	[7:0] : Low byte of PWM3 point 2
0x40BE	PWM3_POINT3_H	R/W	0x00	[7:0] : High byte of PWM3 point 3
0x40BF	PWM3_POINT3_L	R/W	0x00	[7:0] : Low byte of PWM3 point 3
0x40C0	PWM3_POINT4_H	R/W	0x00	[7:0] : High byte of PWM3 point 4
0x40C1	PWM3_POINT4_L	R/W	0x00	[7:0] : Low byte of PWM3 point 4
0x40C2	PWM_WIDTH_H	R/W	0x00	[7:0] : High byte of PWM width
0x40C3	PWM_WIDTH_L	R/W	0x00	[7:0] : Low byte of PWM width
0x40C5	PWM2GPIO	R/W	0x00	[7] : Inverting PWM3 [6] : Inverting PWM2 [5] : Inverting PWM1 [4] : Inverting PWM0 [3] : assign PWM3 to GPIO[3] [2] : assign PWM2 to GPIO[2] [1] : assign PWM1 to GPIO[1] [0] : assign PWM0 to GPIO[0]

11.2. TG, BLC

ADDRESS (HEX)	REGISTER NAME	R/W	DEFAULT (HEX)	DESCRIPTION
TG **(VSYNC SYNCHRONIZED)**				
0x5000	L_INT_TIME_H	R/W	0x01	[7:4] : reserved [3:0] : High byte of large pixel Integration(Exposure) time
0x5001	L_INT_TIME_L	R/W	0xF8	[7:0] : Low byte of large pixel Integration(Exposure) time
0x5002	S_INT_TIME_H	R/W	0x00	[7:4] : reserved [3:0] : High byte of small pixel Integration(Exposure) time
0x5003	S_INT_TIME_L	R/W	0xFC	[7:0] : Low byte of small pixel Integration(Exposure) time
0x5004	HBLANK	R/W	0x3B	[7:0] : Horizontal blank
0x5005	HDUMMY	R/W	0x00	[7:5] : reserved [4] : High byte of horizontal blank NTSC : 0 PAL : 1 [3:0] : Horizontal dummy NTSC : 0x0 PAL : 0xF
0x5005	VBLANK_ODD	R/W	0x09	[7:0] : Odd Field Vertical blank
0x5006	VBLANK_ODD	R/W	0x06	[7:0] : Odd Field Vertical blank NTSC : 0x06 PAL : 0x02
0x5007	VBLANK_EVEN	R/W	0x06	[7:0] : Even Field Vertical blank NTSC : 0x06 PAL : 0x02
0x5008	VDUMMY_ODD	R/W	0x03	[7:0] : Odd Field Vertical dummy NTSC : 0x03 PAL : 0x02
0x5009	VDUMMY_EVEN	R/W	0x03	[7:0] : Even Field Vertical dummy NTSC : 0x03 PAL : 0x02
0x500A	L_A_GAIN	R/W	0x03	[7] : reserved [6:3] : Large Pixel coarse analog gain [2:0] : Large Pixel fine analog gain
0x500B	S_A_GAIN	R/W	0x03	[7] : reserved [6:3] : Small Pixel coarse analog gain [2:0] : Small Pixel fine analog gain
0x500C	L_D_GAIN	R/W	0x00	[7:5] : Large Pixel Global Digital Gain1 control [4:0] : Large Pixel Global Digital Gain2 control Gain = 2^L_D_GAIN[7:5]*(1 + L_D_GAIN[4:0]/32)
0x500D	S_D_GAIN	R/W	0x00	[7:5] : Small Pixel Global Digital Gain1 control [4:0] : Small Pixel Global Digital Gain2 control Gain = 2^S_D_GAIN[7:5]*(1 + S_D_GAIN[4:0]/32)
0x500E	IMG_CON	R/W	0x00	[7:2] : reserved [1] : Vertical mirror [0] : Horizontal mirror
0x5080	TP_IMG_CON	R/W	0x00	[7:6] : reserved [5] : Test Image Enable (0 : disable, 1 : enable) [4:3] : Test Image Data Select 00 : read out address 01 : large int. address 1x : small int. address [2:0] : Test Image Type 000 : diagonal 001 : horizontal 010 : vertical 011 : single color 100 : color bar 101 : gray chart 110 : gray chart for
0x5081	TP_IMG_HI	R/W	0x03	[7:6] : High byte of R color for test image [5:4] : High byte of Gr color for test image [3:2] : High byte of Gb color for test image [1:0] : High byte of B color for test image
0x5082	TP_IMG_R_LO	R/W	0x00	[7:0] : Low byte of R color value for test image

0x5083	TP_IMG_Gr_LO	R/W	0x00	[7:0] : Low byte of Gr color value for test image
0x5084	TP_IMG_Gb_LO	R/W	0x00	[7:0] : Low byte of Gb color value for test image
0x5085	TP_IMG_B_LO	R/W	0xFF	[7:0] : Low byte of B color value for test image
BLC **(VSYNC SYNCHRONIZED)**				
0x5100	BLC_MODE1	R/W	0x33	[7:6] : Reserved [5] : OB2 DPC Enable (Row BLC Area) [4] : OB1 DPC Enable (ABLC, DBLC Area) [3] : Hold Enable [2] : Digital Row BLC Enable [1] : Digital BLC Enable [0] : Analog BLC Enable
0x5101	BLC_MODE2	R/W	0x0F	[7:4] : Reserved [3]: Fixed 1x Gain Enable [2] : Gain Change Detection Enable [1] : DBLC Threshold Enable [0] : ABLC Threshold Enable
0x5102	BLC_AREA_STR	R/W	0x01	[7:5] : Reserved [4:0] : BLC area start line
0x5103	BLC_AREA_END	R/W	0x10	[7:5] : Reserved [4:0] : BLC area end line
0x5104	ABLC_TGT	R/W	0x04	[7:0] : ABLC Target
0x5105	DBLC_TGT	R/W	0x00	[7:0] : DBLC Target
0x5106	RBLC_TGT	R/W	0x00	[7:0] : RBLC Target
0x5107	ABLC_THR	R/W	0x02	[7:6] : Reserved [5:0] : ABLC RST_CDS Update Threshold
0x5108	DBLC_THR	R/W	0x02	[7:6] : Reserved [5:0] : DBLC Update Threshold
0x5109	RST_CDS_L	R/W	0x00	[7:6] : Reserved [5:0] : RST_CDS Long Setting or Monitoring
0x510A	RST_CDS_S	R/W	0x00	[7:6] : Reserved [5:0] : RST_CDS Short Setting or Monitoring
0x510B	RST1_L	R/W	0x00	[7:6] : Reserved [5:0] : RST1 Long Setting or Monitoring
0x510C	RST1_S	R/W	0x00	[7:6] : Reserved [5:0] : RST1 Short Setting or Monitoring
0x510D	RST2_L	R/W	0x00	[7:6] : Reserved [5:0] : RST2 Long Setting or Monitoring
0x510E	RST2_S	R/W	0x00	[7:6] : Reserved [5:0] : RST2 Short Setting or Monitoring

11.3. LSC,

ADDRESS (HEX)	REGISTER NAME	R/W	DEFAULT (HEX)	DESCRIPTION
LENS SHADING CONTROL (VSYNC SYNCHRONIZED)				
0x5200	LSC_CON	R/W	0x00	[7] : Reserved [6:4] : y axis weight 000 : 0% 001 : 0.391% 010 : 0.781% 011 : 1.563% 100 : 3.125% 101 : 6.250% 110 : 12.500% 111 : 25.000% [3:1] : x axis weight 000 : 0% 001 : 0.391% 010 : 0.781% 011 : 1.563% 100 : 3.125% 101 : 6.250% 110 : 12.500% 111 : 25.000% [0] : LSC enable 1'b0: Disable 1'b1: Enable
0x5201	CENTER_H	R/W	0x01	[7:3] : reserved [2] : High byte of y position [1:0] : High byte of x position
0x5202	CENTER_X_L	R/W	0x68	[7:0] : Low byte of x position
0x5203	CENTER_Y_L	R/W	0xF0	[7:0] : Low byte of y position
0x5204	D_FOR_C2_HI	R/W	0x03	[7:2] : Reserved [1:0] : Distance hi for "c2"
0x5205	D_FOR_C2	R/W	0xFF	[7:0] : Distance for "c2"
0x5206	L_C1_R	R/W	0x40	[7:0] : Long pixel R "c1"
0x5207	L_C2_R	R/W	0x00	[7:0] : Long pixel R "c2"
0x5208	L_C1_GR	R/W	0x40	[7:0] : Long pixel Gr "c1"
0x5209	L_C2_GR	R/W	0x00	[7:0] : Long pixel Gr "c2"
0x520A	L_C1_GB	R/W	0x40	[7:0] : Long pixel Gb "c1"
0x520B	L_C2_GB	R/W	0x00	[7:0] : Long pixel Gb "c2"
0x520C	L_C1_B	R/W	0x40	[7:0] : Long pixel B "c1"
0x520D	L_C2_B	R/W	0x00	[7:0] : Long pixel B "c2"
0x520E	SL_C1_R	R/W	0x40	[7:0] :Short pixel R "c1"
0x520F	S_C2_R	R/W	0x00	[7:0] : Short pixel R "c2"
0x5210	S_C1_GR	R/W	0x40	[7:0] : Short pixel Gr "c1"
0x5211	S_C2_GR	R/W	0x00	[7:0] : Short pixel Gr "c2"
0x5212	S_C1_GB	R/W	0x40	[7:0] : Short pixel Gb "c1"
0x5213	S_C2_GB	R/W	0x00	[7:0] : Short pixel Gb "c2"
0x5214	S_C1_B	R/W	0x40	[7:0] : Short pixel B "c1"
0x5215	S_C2_B	R/W	0x00	[7:0] : Short pixel B "c2"
(VSYNC SYNCHRONIZED)				

0x5300	LP_RATIO	R/W	0x10	[7:0] : LP Ratio for Input Data (integer 3bit, fraction 5bit)
0x5301	SP_RATIO	R/W	0x10	[7:0] : SP Ratio for Input Data (integer 3bit, fraction 5bit)
0x5302	_GAIN_N	R/W	0x08	[7:4] : reserved [3:0] : Negative Gain (For Shadow Area)
0x5303	_GAIN_P	R/W	0x08	[7:4] : reserved [3:0] : Positive Gain (For Highlight Area)
0x5304	_REF_X	R/W	0x80	[7:0] : X-axis Reference
0x5305	_REF_Y	R/W	0x80	[7:0] : Y-axis Reference
0x530E	PIXEL_P	R/W	0x10	[7:6] : Reserved [5] : AWB Gain Mode sel 0 : Gain = Reg/128 + 1 1 : Gain = Reg/128 + 0.5 [4] : Median Filter Enable [3] : pixel_bw_en [2] : awb p_en [1] : night_p_en [0] : pixel_p_en
0x530F	_INOUT	R/W	0x03	[7:3] : reserved < Output Selection> [2:0] : Output Group 000 : Image 100 : Gray Image
0x5311	WB_LR_GAIN	R/W	0x40	[7:0] : Long Red Pixel Gain for AWB
0x5312	WB_LGR_GAIN	R/W	0x40	[7:0] : Long Green(R) Pixel Gain for AWB
0x5313	WB_LGB_GAIN	R/W	0x40	[7:0] : Long Green(B) Pixel Gain for AWB
0x5314	WB_LB_GAIN	R/W	0x40	[7:0] : Long Blue Pixel Gain for AWB
0x5315	WB_SR_GAIN	R/W	0x40	[7:0] : Short Red Pixel Gain for AWB
0x5316	WB_SGR_GAIN	R/W	0x40	[7:0] : Short Green(R) Pixel Gain for AWB
0x5317	WB_SGB_GAIN	R/W	0x40	[7:0] : Short Green(B) Pixel Gain for AWB
0x5318	WB_SB_GAIN	R/W	0x40	[7:0] : Short Blue Pixel Gain for AWB

11.4. ISP 1

ADDRESS (HEX)	REGISTER NAME	R/W	DEFAULT (HEX)	DESCRIPTION
DPC / INTPOLATION (VSYNC SYNCHRONIZED)				
0x5400	DPC_CON	R/W	0x00	[7] : Reserved [6:5] : DPC Mode Selection 2'b00: Auto Detect Mode 2'b01: Manual Mode 2'b10: Auto + Manual Mode 2'b11: DP Position Internal Memorizing Mode [4] : Reserved [3] : DPC Diagonal Enhancement Enable 1'b0: Disable 1'b1: Enable [2:1] : Reserved [0] : DPC Enable 1'b0: Disable 1'b1: Enable
0x5401	DP_CNT	R	0x00	[7:0] : Counts of Dead Pixel
0x5402	DPC_THR_HI	R/W	0x00	[7:6] : High byte of DPC Upper Threshold1 [5:4] : High byte of DPC Lower Threshold1 [3:2] : High byte of DPC Upper Threshold2 [1:0] : High byte of DPC Lower Threshold2
0x5403	DPC_THR_UPPER1	R/W	0xFF	[7:0] : DPC Upper Threshold1
0x5404	DPC_THR_LOWER1	R/W	0xC0	[7:0] : DPC Lower Threshold1
0x5405	DPC_THR_UPPER2	R/W	0xFF	[7:0] : DPC Upper Threshold2
0x5406	DPC_THR_LOWER2	R/W	0xC0	[7:0] : DPC Lower Threshold2
0x5407	DPC_DIA_THR	R/W	0x80	[7:0] : DPC Diagonal Threshold
0x5408	DPC_OFFS	R/W	0x14	[7:0] : DPC Threshold Offset
0x5409	DPC_BKG_LV	R/W	0xFF	[7:0] : DPC Debug Mode Background Level
0x540A	DP1_ROW_H	R/W	0x03	[1:0] : High byte of 1st Dead Pixel Row Address
0x540B	DP1_ROW_L	R/W	0xFF	[7:0] : Low byte of 1st Dead Pixel Row Address
0x540C	DP1_COL_H	R/W	0x03	[1:0] : High byte of 1st Dead Pixel Column Address
0x540D	DP1_COL_L	R/W	0xFF	[7:0] : Low byte of 1st Dead Pixel Column Address
0x540E	DP2_ROW_H	R/W	0x03	[1:0] : High byte of 2nd Dead Pixel Row Address
0x540F	DP2_ROW_L	R/W	0xFF	[7:0] : Low byte of 2nd Dead Pixel Row Address
0x5410	DP2_COL_H	R/W	0x03	[1:0] : High byte of 2nd Dead Pixel Column Address
0x5411	DP2_COL_L	R/W	0xFF	[7:0] : Low byte of 2nd Dead Pixel Column Address
0x5412	DP3_ROW_H	R/W	0x03	[1:0] : High byte of 3rd Dead Pixel Row Address
0x5413	DP3_ROW_L	R/W	0xFF	[7:0] : Low byte of 3rd Dead Pixel Row Address
0x5414	DP3_COL_H	R/W	0x03	[1:0] : High byte of 3rd Dead Pixel Column Address
0x5415	DP3_COL_L	R/W	0xFF	[7:0] : Low byte of 3rd Dead Pixel Column Address
0x5416	DP4_ROW_H	R/W	0x03	[1:0] : High byte of 4th Dead Pixel Row Address
0x5417	DP4_ROW_L	R/W	0xFF	[7:0] : Low byte of 4th Dead Pixel Row Address
0x5418	DP4_COL_H	R/W	0x03	[1:0] : High byte of 4th Dead Pixel Column Address
0x5419	DP4_COL_L	R/W	0xFF	[7:0] : Low byte of 4th Dead Pixel Column Address
0x541A	DP5_ROW_H	R/W	0x03	[1:0] : High byte of 5th Dead Pixel Row Address
0x541B	DP5_ROW_L	R/W	0xFF	[7:0] : Low byte of 5th Dead Pixel Row Address
0x541C	DP5_COL_H	R/W	0x03	[1:0] : High byte of 5th Dead Pixel Column Address

0x541D	DP5_COL_L	R/W	0xFF	[7:0] : Low byte of 5th Dead Pixel Column Address
0x541E	DP6_ROW_H	R/W	0x03	[1:0] : High byte of 6th Dead Pixel Row Address
0x541F	DP6_ROW_L	R/W	0xFF	[7:0] : Low byte of 6th Dead Pixel Row Address
0x5420	DP6_COL_H	R/W	0x03	[1:0] : High byte of 6th Dead Pixel Column Address
0x5421	DP6_COL_L	R/W	0xFF	[7:0] : Low byte of 6th Dead Pixel Column Address
0x5422	DP7_ROW_H	R/W	0x03	[1:0] : High byte of 7th Dead Pixel Row Address
0x5423	DP7_ROW_L	R/W	0xFF	[7:0] : Low byte of 7th Dead Pixel Row Address
0x5424	DP7_COL_H	R/W	0x03	[1:0] : High byte of 7th Dead Pixel Column Address
0x5425	DP7_COL_L	R/W	0xFF	[7:0] : Low byte of 7th Dead Pixel Column Address
0x5426	DP8_ROW_H	R/W	0x03	[1:0] : High byte of 8th Dead Pixel Row Address
0x5427	DP8_ROW_L	R/W	0xFF	[7:0] : Low byte of 8th Dead Pixel Row Address
0x5428	DP8_COL_H	R/W	0x03	[1:0] : High byte of 8th Dead Pixel Column Address
0x5429	DP8_COL_L	R/W	0xFF	[7:0] : Low byte of 8th Dead Pixel Column Address
0x542A	DP9_ROW_H	R/W	0x03	[1:0] : High byte of 9th Dead Pixel Row Address
0x542B	DP9_ROW_L	R/W	0xFF	[7:0] : Low byte of 9th Dead Pixel Row Address
0x542C	DP9_COL_H	R/W	0x03	[1:0] : High byte of 9th Dead Pixel Column Address
0x542D	DP9_COL_L	R/W	0xFF	[7:0] : Low byte of 9th Dead Pixel Column Address
0x542E	DP10_ROW_H	R/W	0x03	[1:0] : High byte of 10th Dead Pixel Row Address
0x542F	DP10_ROW_L	R/W	0xFF	[7:0] : Low byte of 10th Dead Pixel Row Address
0x5430	DP10_COL_H	R/W	0x03	[1:0] : High byte of 10th Dead Pixel Column Address
0x5431	DP10_COL_L	R/W	0xFF	[7:0] : Low byte of 10th Dead Pixel Column Address
0x5432	DP11_ROW_H	R/W	0x03	[1:0] : High byte of 11th Dead Pixel Row Address
0x5433	DP11_ROW_L	R/W	0xFF	[7:0] : Low byte of 11th Dead Pixel Row Address
0x5434	DP11_COL_H	R/W	0x03	[1:0] : High byte of 11th Dead Pixel Column Address
0x5435	DP11_COL_L	R/W	0xFF	[7:0] : Low byte of 11th Dead Pixel Column Address
0x5436	DP12_ROW_H	R/W	0x03	[1:0] : High byte of 12th Dead Pixel Row Address
0x5437	DP12_ROW_L	R/W	0xFF	[7:0] : Low byte of 12th Dead Pixel Row Address
0x5438	DP12_COL_H	R/W	0x03	[1:0] : High byte of 12th Dead Pixel Column Address
0x5439	DP12_COL_L	R/W	0xFF	[7:0] : Low byte of 12th Dead Pixel Column Address
0x543A	DP13_ROW_H	R/W	0x03	[1:0] : High byte of 13th Dead Pixel Row Address
0x543B	DP13_ROW_L	R/W	0xFF	[7:0] : Low byte of 13th Dead Pixel Row Address
0x543C	DP13_COL_H	R/W	0x03	[1:0] : High byte of 13th Dead Pixel Column Address
0x543D	DP13_COL_L	R/W	0xFF	[7:0] : Low byte of 13th Dead Pixel Column Address
0x543E	DP14_ROW_H	R/W	0x03	[1:0] : High byte of 14th Dead Pixel Row Address
0x543F	DP14_ROW_L	R/W	0xFF	[7:0] : Low byte of 14th Dead Pixel Row Address
0x5440	DP14_COL_H	R/W	0x03	[1:0] : High byte of 14th Dead Pixel Column Address
0x5441	DP14_COL_L	R/W	0xFF	[7:0] : Low byte of 14th Dead Pixel Column Address
0x5442	DP15_ROW_H	R/W	0x03	[1:0] : High byte of 15th Dead Pixel Row Address
0x5443	DP15_ROW_L	R/W	0xFF	[7:0] : Low byte of 15th Dead Pixel Row Address
0x5444	DP15_COL_H	R/W	0x03	[1:0] : High byte of 15th Dead Pixel Column Address
0x5445	DP15_COL_L	R/W	0xFF	[7:0] : Low byte of 15th Dead Pixel Column Address
0x5446	DP16_ROW_H	R/W	0x03	[1:0] : High byte of 16th Dead Pixel Row Address
0x5447	DP16_ROW_L	R/W	0xFF	[7:0] : Low byte of 16th Dead Pixel Row Address
0x5448	DP16_COL_H	R/W	0x03	[1:0] : High byte of 16th Dead Pixel Column Address
0x5449	DP16_COL_L	R/W	0xFF	[7:0] : Low byte of 16th Dead Pixel Column Address

0x544A	DP17_ROW_H	R/W	0x03	[1:0] : High byte of 17th Dead Pixel Row Address
0x544B	DP17_ROW_L	R/W	0xFF	[7:0] : Low byte of 17th Dead Pixel Row Address
0x544C	DP17_COL_H	R/W	0x03	[1:0] : High byte of 17th Dead Pixel Column Address
0x544D	DP17_COL_L	R/W	0xFF	[7:0] : Low byte of 17th Dead Pixel Column Address
0x544E	DP18_ROW_H	R/W	0x03	[1:0] : High byte of 18th Dead Pixel Row Address
0x544F	DP18_ROW_L	R/W	0xFF	[7:0] : Low byte of 18th Dead Pixel Row Address
0x5450	DP18_COL_H	R/W	0x03	[1:0] : High byte of 18th Dead Pixel Column Address
0x5451	DP18_COL_L	R/W	0xFF	[7:0] : Low byte of 18th Dead Pixel Column Address
0x5452	DP19_ROW_H	R/W	0x03	[1:0] : High byte of 19th Dead Pixel Row Address
0x5453	DP19_ROW_L	R/W	0xFF	[7:0] : Low byte of 19th Dead Pixel Row Address
0x5454	DP19_COL_H	R/W	0x03	[1:0] : High byte of 19th Dead Pixel Column Address
0x5455	DP19_COL_L	R/W	0xFF	[7:0] : Low byte of 19th Dead Pixel Column Address
0x5456	DP20_ROW_H	R/W	0x03	[1:0] : High byte of 20th Dead Pixel Row Address
0x5457	DP20_ROW_L	R/W	0xFF	[7:0] : Low byte of 20th Dead Pixel Row Address
0x5458	DP20_COL_H	R/W	0x03	[1:0] : High byte of 20th Dead Pixel Column Address
0x5459	DP20_COL_L	R/W	0xFF	[7:0] : Low byte of 20th Dead Pixel Column Address
0x545A	DP21_ROW_H	R/W	0x03	[1:0] : High byte of 21st Dead Pixel Row Address
0x545B	DP21_ROW_L	R/W	0xFF	[7:0] : Low byte of 21st Dead Pixel Row Address
0x545C	DP21_COL_H	R/W	0x03	[1:0] : High byte of 21st Dead Pixel Column Address
0x545D	DP21_COL_L	R/W	0xFF	[7:0] : Low byte of 21st Dead Pixel Column Address
0x545E	DP22_ROW_H	R/W	0x03	[1:0] : High byte of 22nd Dead Pixel Row Address
0x545F	DP22_ROW_L	R/W	0xFF	[7:0] : Low byte of 22nd Dead Pixel Row Address
0x5460	DP22_COL_H	R/W	0x03	[1:0] : High byte of 22nd Dead Pixel Column Address
0x5461	DP22_COL_L	R/W	0xFF	[7:0] : Low byte of 22nd Dead Pixel Column Address
0x5462	DP23_ROW_H	R/W	0x03	[1:0] : High byte of 23rd Dead Pixel Row Address
0x5463	DP23_ROW_L	R/W	0xFF	[7:0] : Low byte of 23rd Dead Pixel Row Address
0x5464	DP23_COL_H	R/W	0x03	[1:0] : High byte of 23rd Dead Pixel Column Address
0x5465	DP23_COL_L	R/W	0xFF	[7:0] : Low byte of 23rd Dead Pixel Column Address
0x5466	DP24_ROW_H	R/W	0x03	[1:0] : High byte of 24th Dead Pixel Row Address
0x5467	DP24_ROW_L	R/W	0xFF	[7:0] : Low byte of 24th Dead Pixel Row Address
0x5468	DP24_COL_H	R/W	0x03	[1:0] : High byte of 24th Dead Pixel Column Address
0x5469	DP24_COL_L	R/W	0xFF	[7:0] : Low byte of 24th Dead Pixel Column Address
0x546A	DP25_ROW_H	R/W	0x03	[1:0] : High byte of 25th Dead Pixel Row Address
0x546B	DP25_ROW_L	R/W	0xFF	[7:0] : Low byte of 25th Dead Pixel Row Address
0x546C	DP25_COL_H	R/W	0x03	[1:0] : High byte of 25th Dead Pixel Column Address
0x546D	DP25_COL_L	R/W	0xFF	[7:0] : Low byte of 25th Dead Pixel Column Address
0x546E	DP26_ROW_H	R/W	0x03	[1:0] : High byte of 26th Dead Pixel Row Address
0x546F	DP26_ROW_L	R/W	0xFF	[7:0] : Low byte of 26th Dead Pixel Row Address
0x5470	DP26_COL_H	R/W	0x03	[1:0] : High byte of 26th Dead Pixel Column Address
0x5471	DP26_COL_L	R/W	0xFF	[7:0] : Low byte of 26th Dead Pixel Column Address
0x5472	DP27_ROW_H	R/W	0x03	[1:0] : High byte of 27th Dead Pixel Row Address
0x5473	DP27_ROW_L	R/W	0xFF	[7:0] : Low byte of 27th Dead Pixel Row Address
0x5474	DP27_COL_H	R/W	0x03	[1:0] : High byte of 27th Dead Pixel Column Address
0x5475	DP27_COL_L	R/W	0xFF	[7:0] : Low byte of 27th Dead Pixel Column Address
0x5476	DP28_ROW_H	R/W	0x03	[1:0] : High byte of 28th Dead Pixel Row Address

0x5477	DP28_ROW_L	R/W	0xFF	[7:0] : Low byte of 28th Dead Pixel Row Address
0x5478	DP28_COL_H	R/W	0x03	[1:0] : High byte of 28th Dead Pixel Column Address
0x5479	DP28_COL_L	R/W	0xFF	[7:0] : Low byte of 28th Dead Pixel Column Address
0x547A	DP29_ROW_H	R/W	0x03	[1:0] : High byte of 29th Dead Pixel Row Address
0x547B	DP29_ROW_L	R/W	0xFF	[7:0] : Low byte of 29th Dead Pixel Row Address
0x547C	DP29_COL_H	R/W	0x03	[1:0] : High byte of 29th Dead Pixel Column Address
0x547D	DP29_COL_L	R/W	0xFF	[7:0] : Low byte of 29th Dead Pixel Column Address
0x547E	DP30_ROW_H	R/W	0x03	[1:0] : High byte of 30th Dead Pixel Row Address
0x547F	DP30_ROW_L	R/W	0xFF	[7:0] : Low byte of 30th Dead Pixel Row Address
0x5480	DP30_COL_H	R/W	0x03	[1:0] : High byte of 30th Dead Pixel Column Address
0x5481	DP30_COL_L	R/W	0xFF	[7:0] : Low byte of 30th Dead Pixel Column Address
0x5482	DP31_ROW_H	R/W	0x03	[1:0] : High byte of 31st Dead Pixel Row Address
0x5483	DP31_ROW_L	R/W	0xFF	[7:0] : Low byte of 31st Dead Pixel Row Address
0x5484	DP31_COL_H	R/W	0x03	[1:0] : High byte of 31st Dead Pixel Column Address
0x5485	DP31_COL_L	R/W	0xFF	[7:0] : Low byte of 31st Dead Pixel Column Address
0x5486	DP32_ROW_H	R/W	0x03	[1:0] : High byte of 32nd Dead Pixel Row Address
0x5487	DP32_ROW_L	R/W	0xFF	[7:0] : Low byte of 32nd Dead Pixel Row Address
0x5488	DP32_COL_H	R/W	0x03	[1:0] : High byte of 32nd Dead Pixel Column Address
0x5489	DP32_COL_L	R/W	0xFF	[7:0] : Low byte of 32nd Dead Pixel Column Address
BAYER NOISE REDUCTION **(VSYNC SYNCHRONIZED)**				
0x548A	BNR_CON	R/W	0xC0	[7] : Pixel Position Selection 1'b0 : R/B pixel 1'b1 : G pixel [6] : Line Position Selection 1'b0 : RG line 1'b1 : GB line [5:4] : Debug mode, Test Channel Selection 3'd3 : Green 3'd2 : Blue 3'd1 : Red 3'd0 : None [3:1] : Debug mode, Luma Area Selection 3'd4 : all 3'd3 : high 3'd2 : mid 3'd1 : low 3'd0 : bypass [0] : Bayer Noise Reduction on/off 1'b0 : off 1'b1 : on
0x548B	LUMA_WIDTH	R/W	0x0	[7:3] : Reserved [2:0] : Interpolation Width within Luminance Space 3'd7 : 128 3'd6 : 64 3'd5 : 32 3'd4 : 16 3'd3 : 8 3'd2 : 4 3'd1 : 2 3'd0 : 0
0x548C	R_LUMA_L_THR_H	R/W	0x0	[7:2] : Reserved [1:0] : High byte of Low Luminance Threshold for Red

0x548D	R_LUMA_L_THR_L	R/W	0x40	[7:0] : Low byte of Low Luminance Threshold for Red
0x548E	R_LUMA_H_THR_H	R/W	0x0	[7:2] : Reserved [1:0] : High byte of High Luminance Threshold for Red
0x548F	R_LUMA_H_THR_L	R/W	0xFA	[7:0] : Low byte of High Luminance Threshold for Red
0x5490	G_LUMA_L_THR_H	R/W	0x0	[7:2] : Reserved [1:0] : High byte of Low Luminance Threshold for Green
0x5491	G_LUMA_L_THR_L	R/W	0x40	[7:0] : Low byte of Low Luminance Threshold for Green
0x5492	G_LUMA_H_THR_H	R/W	0x0	[7:2] : Reserved [1:0] : High byte of High Luminance Threshold for Green
0x5493	G_LUMA_H_THR_L	R/W	0xFA	[7:0] : Low byte of High Luminance Threshold for Green
0x5494	B_LUMA_L_THR_H	R/W	0x0	[7:2] : Reserved [1:0] : High byte of Low Luminance Threshold for Blue
0x5495	B_LUMA_L_THR_L	R/W	0x40	[7:0] : Low byte of Low Luminance Threshold for Blue
0x5496	B_LUMA_H_THR_H	R/W	0x0	[7:2] : Reserved [1:0] : High byte of High Luminance Threshold for Blue
0x5497	B_LUMA_H_THR_L	R/W	0xFA	[7:0] : Low byte of High Luminance Threshold for Blue
0x5498	R_LL_STR	R/W	0x03	[7:0] : Low Luminance Noise Reduction Filtering Strength for Red
0x5499	R_ML_STR	R/W	0x03	[7:0] : Mid Luminance Noise Reduction Filtering Strength for Red
0x549A	R_HL_STR	R/W	0x03	[7:0] : High Luminance Noise Reduction Filtering Strength for Red
0x549B	G_LL_STR	R/W	0x03	[7:0] : Low Luminance Noise Reduction Filtering Strength for Green
0x549C	G_ML_STR	R/W	0x03	[7:0] : Mid Luminance Noise Reduction Filtering Strength for Green
0x549D	G_HL_STR	R/W	0x03	[7:0] : High Luminance Noise Reduction Filtering Strength for Green
0x549E	B_LL_STR	R/W	0x03	[7:0] : Low Luminance Noise Reduction Filtering Strength for Blue
0x549F	B_ML_STR	R/W	0x03	[7:0] : Mid Luminance Noise Reduction Filtering Strength for Blue
0x54A0	B_HL_STR	R/W	0x03	[7:0] : High Luminance Noise Reduction Filtering Strength for Blue
INTERPOLATION	**(VSYNC SYNCHRONIZED)**			
0x5500	INTP_CON	R/W	0x07	[7:5] : Reserved [4] : Bypass Enable [3] : Interpolation RGB Gain Enable [2] : Crominance Noise Reduction Enable [1] : Luminance Noise Reduction Enable [0] : Adaptive False Color Suppression Eanble
0x5501	INTP_R_GAIN	R/W	0x00	[7:0] : Interpolation R Gain
0x5502	INTP_G_GAIN	R/W	0x00	[7:0] : Interpolation G Gain
0x5503	INTP_G_GAIN	R/W	0x00	[7:0] : Interpolation B Gain
0x5504	Y_NR_GAIN	R/W	0x03	[7:2] : Reserved [1:0] : Luminance Noise Reduction Rate 2'b00 : 100% reduction 2'b01 : 50% reduction 2'b10 : 25% reduction 2'b11 : 12.5% reduction
0x5505	COLOR	R/W	0x00	[7:2] : Reserved [1:0] : First Color Selection 2'b00 : R 2'b01 : Gr 2'b10 : Gb 2'b11 : B
0x5506	RGB_CLIP_H	R/W	0x03	[7:2] : Reserved [1:0] : High byte of RGB Clip Value
0x5507	RGB_CLIP_L	R/W	0xFF	[7:0] : Low byte of RGB Clip Value
0x5508	EDGE_TH_H	R/W	0x00	[7:2] : Reserved [1:0] : High byte of Edge Threshold

0x5509	EDGE_TH_L	R/W	0x80	[7:0] : Low byte of Edge Threshold
0x550A	Y_MID_COR	R/W	0x00	[7:0] : Middle Frequency Luminance Corling Value
0x550B	Y_HIGH_COR	R/W	0x00	[7:0] : High Frequency Luminance Corling Value
0x550C	Y_MID_GAIN	R/W	0x80	[7:4] : Middle Frequency Luminance Coarse Gain(Integer 4bit) [3:0] : Middle Frequency Luminance Fine Gain(Fraction 4bit)
0x550D	Y_HIGH_GAIN	R/W	0x00	[7]: Reserved [6:4]: High Frequency Luminance Coarse Gain(Integer 3bit) [3:0]: High Frequency Luminance Fine Gain(Fraction 4bit)
0x550E	GRGB_OFFSET	R/W	0x00	[7:0]: Gr/Gb Offset
0x550F	FC_MID_SCL	R/W	0x08	[7:4]: Reserved [3:0]: Middle Frequency False Color Suppression Strength(Edge) u1.0
0x5510	FC_HIGH_SCL	R/W	0x08	[7:4]: Reserved [3:0]: High Frequency False Color Suppression Strength(Moire) u1.0
COLOR CORRECTION (VSYNC SYNCHRONIZED)				
0x5600	R_OFFSET	R/W	0x00	[7:0] : offset value for R
0x5601	G_OFFSET	R/W	0x00	[7:0] : offset value for G
0x5602	B_OFFSET	R/W	0x00	[7:0] : offset value for B
0x5603	CC11_H	R/W	0x01	[7:4] : reserved [3:0] : Coefficients[11:8] of 1st row, 1st column in color correction matrix
0x5604	CC11_L	R/W	0x00	[7:0] : Coefficients[7:0] of 1st row, 1st column in color correction matrix
0x5605	CC12_H	R/W	0x00	[7:4] : reserved [3:0] : Coefficients[11:8] of 1st row, 2nd column In color correction matrix
0x5606	CC12_L	R/W	0x00	[7:0] : Coefficients[7:0]of 1st row, 2nd column In color correction matrix
0x5607	CC13_H	R/W	0x00	[7:4] : reserved [3:0] : Coefficients[11:8] of 1st row, 3rd column In color correction matrix
0x5608	CC13_L	R/W	0x00	[7:0] : Coefficients[7:0] of 1st row, 3rd column In color correction matrix
0x5609	CC21_H	R/W	0x00	[7:4] : reserved [3:0] : Coefficients[11:8] of 2nd row, 1st column In color correction matrix
0x560A	CC21_L	R/W	0x00	[7:0] : Coefficients[7:0] of 2nd row, 1st column In color correction matrix
0x560B	CC22_H	R/W	0x01	[7:4] : reserved [3:0] : Coefficients[11:8] of 2nd row, 2nd column In color correction matrix
0x560C	CC22_L	R/W	0x00	[7:0] : Coefficients[7:0] of 2nd row, 2nd column In color correction matrix
0x560D	CC23_H	R/W	0x00	[7:4] : reserved [3:0] : Coefficients[11:8] of 2nd row, 3rd column In color correction matrix
0x560E	CC23_L	R/W	0x00	[7:0] : Coefficients[7:0] of 2nd row, 3rd column In color correction matrix
0x560F	CC31_H	R/W	0x00	[7:4] : reserved [3:0] : Coefficients[11:8] of 3rd row, 1st column In color correction matrix
0x5610	CC31_L	R/W	0x00	[7:0] : Coefficients[7:0] of 3rd row, 1st column In color correction matrix

0x5611	CC32_H	R/W	0x00	[7:4] : reserved [3:0] : Coefficients[11:8] of 3rd row, 2nd column In color correction matrix
0x5612	CC32_L	R/W	0x00	[7:0] : Coefficients[7:0] of 3rd row, 2nd column In color correction matrix
0x5613	CC33_H	R/W	0x01	[7:4] : reserved [3:0] : Coefficients[11:8] of 3rd row, 3rd column in color correction matrix
0x5614	CC33_L	R/W	0x00	[7:0] : Coefficients[7:0] of 3rd row, 3rd column in color correction matrix
GAMMA (VSYNC SYNCHRONIZED)				
0x5700	R_OFFSET	R/W	0x00	[7:0] : offset value for R
0x5701	G_OFFSET	R/W	0x00	[7:0] : offset value for G
0x5702	B_OFFSET	R/W	0x00	[7:0] : offset value for B
0x5703	GAMMA_CONTROL	R/W	0x02	[7:3] : reserved [2] : gamma all enable 0 : disable 1 : enable [1] : liner gamma enable 0 : disable 1 : enable [0] : gamma enable 0 : disable 1 : enable
0x5710	GAMMA_R0	R/W	0x08	[7:0] : gamma R0
0x5711	GAMMA_R1	R/W	0x10	[7:0] : gamma R1
0x5712	GAMMA_R2	R/W	0x20	[7:0] : gamma R2
0x5713	GAMMA_R3	R/W	0x30	[7:0] : gamma R3
0x5714	GAMMA_R4	R/W	0x40	[7:0] : gamma R4
0x5715	GAMMA_R5	R/W	0x50	[7:0] : gamma R5
0x5716	GAMMA_R6	R/W	0x60	[7:0] : gamma R6
0x5717	GAMMA_R7	R/W	0x70	[7:0] : gamma R7
0x5718	GAMMA_R8	R/W	0x80	[7:0] : gamma R8
0x5719	GAMMA_R9	R/W	0x90	[7:0] : gamma R9
0x571A	GAMMA_R10	R/W	0xA0	[7:0] : gamma R10
0x571B	GAMMA_R11	R/W	0xB0	[7:0] : gamma R11
0x571C	GAMMA_R12	R/W	0xC0	[7:0] : gamma R12
0x571D	GAMMA_R13	R/W	0xD0	[7:0] : gamma R13
0x571E	GAMMA_R14	R/W	0xE0	[7:0] : gamma R14
0x571F	GAMMA_R15	R/W	0xF0	[7:0] : gamma R15
0x5720	GAMMA_G0	R/W	0x08	[7:0] : gamma G0
0x5721	GAMMA_G1	R/W	0x10	[7:0] : gamma G1
0x5722	GAMMA_G2	R/W	0x20	[7:0] : gamma G2
0x5723	GAMMA_G3	R/W	0x30	[7:0] : gamma G3
0x5724	GAMMA_G4	R/W	0x40	[7:0] : gamma G4
0x5725	GAMMA_G5	R/W	0x50	[7:0] : gamma G5
0x5726	GAMMA_G6	R/W	0x60	[7:0] : gamma G6
0x5727	GAMMA_G7	R/W	0x70	[7:0] : gamma G7
0x5728	GAMMA_G8	R/W	0x80	[7:0] : gamma G8
0x5729	GAMMA_G9	R/W	0x90	[7:0] : gamma G9
0x572A	GAMMA_G10	R/W	0xA0	[7:0] : gamma G10

0x572B	GAMMA_G11	R/W	0xB0	[7:0] : gamma G11
0x572C	GAMMA_G12	R/W	0xC0	[7:0] : gamma G12
0x572D	GAMMA_G13	R/W	0xD0	[7:0] : gamma G13
0x572E	GAMMA_G14	R/W	0xE0	[7:0] : gamma G14
0x572F	GAMMA_G15	R/W	0xF0	[7:0] : gamma G15
0x5730	GAMMA_B0	R/W	0x08	[7:0] : gamma B0
0x5731	GAMMA_B1	R/W	0x10	[7:0] : gamma B1
0x5732	GAMMA_B2	R/W	0x20	[7:0] : gamma B2
0x5733	GAMMA_B3	R/W	0x30	[7:0] : gamma B3
0x5734	GAMMA_B4	R/W	0x40	[7:0] : gamma B4
0x5735	GAMMA_B5	R/W	0x50	[7:0] : gamma B5
0x5736	GAMMA_B6	R/W	0x60	[7:0] : gamma B6
0x5737	GAMMA_B7	R/W	0x70	[7:0] : gamma B7
0x5738	GAMMA_B8	R/W	0x80	[7:0] : gamma B8
0x5739	GAMMA_B9	R/W	0x90	[7:0] : gamma B9
0x573A	GAMMA_B10	R/W	0xA0	[7:0] : gamma B10
0x573B	GAMMA_B11	R/W	0xB0	[7:0] : gamma B11
0x573C	GAMMA_B12	R/W	0xC0	[7:0] : gamma B12
0x573D	GAMMA_B13	R/W	0xD0	[7:0] : gamma B13
0x573E	GAMMA_B14	R/W	0xE0	[7:0] : gamma B14
0x573F	GAMMA_B15	R/W	0xF0	[7:0] : gamma B15
0x5740	GAMMA_X0	R/W	0x08	[7:0] : gamma X0
0x5741	GAMMA_X1	R/W	0x10	[7:0] : gamma X1
0x5742	GAMMA_X2	R/W	0x20	[7:0] : gamma X2
0x5743	GAMMA_X3	R/W	0x30	[7:0] : gamma X3
0x5744	GAMMA_X4	R/W	0x40	[7:0] : gamma X4
0x5745	GAMMA_X5	R/W	0x50	[7:0] : gamma X5
0x5746	GAMMA_X6	R/W	0x60	[7:0] : gamma X6
0x5747	GAMMA_X7	R/W	0x70	[7:0] : gamma X7
0x5748	GAMMA_X8	R/W	0x80	[7:0] : gamma X8
0x5749	GAMMA_X9	R/W	0x90	[7:0] : gamma X9
0x574A	GAMMA_XA	R/W	0xA0	[7:0] : gamma Xa
0x574B	GAMMA_XB	R/W	0xB0	[7:0] : gamma Xb
0x574C	GAMMA_XC	R/W	0xC0	[7:0] : gamma Xc
0x574D	GAMMA_XD	R/W	0xD0	[7:0] : gamma Xd
0x574E	GAMMA_XE	R/W	0xE0	[7:0] : gamma Xe
0x574F	GAMMA_XF	R/W	0xF0	[7:0] : gamma Xf
RGB TO YCBCR	**(VSYNC SYNCHRONIZED)**			
0x5800	RGB2YC_YR_COEF	R/W	0x4D	[7:0] : Red coefficient of RGB to Y conversion
0x5801	RGB2YC_YG_COEF	R/W	0x96	[7:0] : Green coefficient of RGB to Y conversion
0x5802	RGB2YC_YB_COEF	R/W	0x1D	[7:0] : Blue coefficient of RGB to Y conversion
0x5803	RGB2YC_CBR_COEF	R/W	0x2B	[7:0] : Red coefficient of RGB to Cb conversion
0x5804	RGB2YC_CBG_COEF	R/W	0x55	[7:0] : Green coefficient of RGB to Cb conversion
0x5805	RGB2YC_CBB_COEF	R/W	0x80	[7:0] : Blue coefficient of RGB to Cb conversion
0x5806	RGB2YC_CRR_COEF	R/W	0x80	[7:0] : Red coefficient of RGB to Cr conversion

0x5807	RGB2YC_CRG_COEF	R/W	0x6B	[7:0] : Green coefficient of RGB to Cr conversion
0x5808	RGB2YC_CRB_COEF	R/W	0x15	[7:0] : Blue coefficient of RGB to Cr conversion
0x5809	RGB2YC_Y_MAX	R/W	0xFF	[7:0] : Y maximum value
0x580A	RGB2YC_Y_MIN	R/W	0x00	[7:0] : Y minimum value
0x580B	RGB2YC_C_MAX	R/W	0xFF	[7:0] : C maximum value
0x580C	RGB2YC_C_MIN	R/W	0x00	[7:0] : C minimum value
0x580D	RGB2YC_Y_OFFSET	R/W	0x00	[7:0] : Offset value of RGB to Y conversion
0x580E	RGB2YC_C_OFFSET	R/W	0x80	[7:0] : Offset value of RGB to C conversion
0x580F	RGB2YC_SOLOR_EN	R/W	0x00	[7:1] : reserved [0] : Solor enable 0 : disable 1 : enable

11.5. ISP 2

ADDRESS (HEX)	REGISTER NAME	R/W	DEFAULT (HEX)	DESCRIPTION
HUE / SATURATION / CONTRAST / BRIGHTNESS (VSYNC SYNCHRONIZED)				
0x6000	HS_CON	R/W	0x00	[7:4]: Reserved [3]: Brightness enable 1'b0: Brightness disable 1'b1: Brightness enable [2]: Luminance high region contrast enable 1'b0: Luminance high region contrast disable 1'b1: Luminance high region contrast enable [1]: Contrast enable 1'b0: Contrast disable 1'b1: Contrast enable [0]: Hue/Saturation enable 1'b0: Hue/ Saturation disable 1'b1: Hue/ Saturation enable
0x6001	HS_REF	R/W	0x80	[7:0]: Reference value of Hue/saturation control
0x6002	HS_Y_REF	R/W	0x80	[7:0]: Reference value of contrast
0x6003	HS_Y_CONTRAST	R/W	0x80	[7:0]: Contrast gain. Range x0(0x00)~x1.992(0xFF)
0x6004	HS_Y_BRIGHT	R/W	0x00	[7:0]: Brightness offset
0x6005	HS_SAT_CB	R/W	0x80	[7:0]: Saturation Cb gain. Range x0(0x00)~x1.992(0xFF)
0x6006	HS_SAT_CR	R/W	0x80	[7:0]: Saturation Cr gain. Range x0(0x00)~x1.992(0xFF)
0x6007	HS_SAT_MAG	R/W	0x80	[7:0]: Saturation Magenta gain. Range x0(0x00)~x1.992(0xFF)
0x6008	HS_SAT_RED	R/W	0x80	[7:0]: Saturation Red gain. Range x0(0x00)~x1.992(0xFF)
0x6009	HS_SAT_YEL	R/W	0x80	[7:0]: Saturation Yellow gain. Range x0(0x00)~x1.992(0xFF)
0x600A	HS_SAT_GRE	R/W	0x80	[7:0]: Saturation Green gain. Range x0(0x00)~x1.992(0xFF)
0x600B	HS_SAT_CYA	R/W	0x80	[7:0]: Saturation Cyan gain. Range x0(0x00)~x1.992(0xFF)
0x600C	HS_SAT_BLU	R/W	0x80	[7:0]: Saturation Blue gain. Range x0(0x00)~x1.992(0xFF)
0x600D	HS_HUE_MAG	R/W	0x00	[7:0]: Hue control(Magenta area) Range -45° ~ +45° (2's complement)
0x600E	HS_HUE_RED	R/W	0x00	[7:0]: Hue control(Red area) Range -45° ~ +45° (2's complement)
0x600F	HS_HUE_YEL	R/W	0x00	[7:0]: Hue control(Yellow area) Range -45° ~ +45° (2's complement)
0x6010	HS_HUE_GRE	R/W	0x00	[7:0]: Hue control(Green area) Range -45° ~ +45° (2's complement)
0x6011	HS_HUE_CYA	R/W	0x00	[7:0]: Hue control(Cyan area) Range -45° ~ +45° (2's complement)
0x6012	HS_HUE_BLU	R/W	0x00	[7:0]: Hue control(Blue area) Range -45° ~ +45° (2's complement)
COLOR SUPPRESSION (VSYNC SYNCHRONIZED)				
0x6210	COLOR_SUP_CON	R/W	0x14	[5:2] : c delay [1] : crcb order [0] : color suppress enable 0 : disable 1 : enable
0x6211	Y1_H	R/W	0xDC	[7:0] : High byte of y1
0x6212	SUP1_GAIN_H	R/W	0x20	[7:0] : High byte of sup1 gain
0x6213	Y1_L	R/W	0x40	[7:0] : Low byte of y1
0x6214	SUP1_GAIN_L	R/W	0x20	[7:0] : Low byte of sup1 gain
0x6215	Y2_H	R/W	0xDC	[7:0] : High byte of y2
0x6216	SUP2_GAIN_H	R/W	0x20	[7:0] : High byte of sup2 gain
0x6217	Y2_L	R/W	0x40	[7:0] : Low byte of y2
0x6218	SUP2_GAIN_L	R/W	0x20	[7:0] : Low byte of sup2 gain

0x6219	GRAY_LVL	R/W	0x00	[7:3] : reserved [2:0] : gray level, 111 -> full gray

11.6. OSD

ADDRESS (HEX)	REGISTER NAME	R/W	DEFAULT (HEX)	DESCRIPTION
OSD (MAIN CONTROL & TEXT MENU)		**(VSYNC SYNCHRONIZED)**		
0x6300	OSD_OP_MODE0	R/W	0x00	[7:2] : reserved [1] : OSD parking guide enable [0] : OSD text menu enable
0x6301	OSD_OP_MODE1	R/W	0x00	[7] : OSD mask7 enable [6] : OSD mask6 enable [5] : OSD mask5 enable [4] : OSD mask4 enable [3] : OSD mask3 enable [2] : OSD mask2 enable [1] : OSD mask1 enable [0] : OSD mask0 enable
0x6302	TXT_FRM_CEN_X_L	R/W	0x40	[7:0] : X-coordinate of the center of the text frame (low)
0x6303	TXT_FRM_CEN_Y_L	R/W	0xF0	[7:0] : X-coordinate of the center of the text frame (low)
0x6304	TXT_FRM_CEN_HI	R/W	0x01	[7:6] : reserved [5:4] : Y-coordinate of the center of the text frame (high) [3:2] : reserved [1:0] : X-coordinate of the center of the text frame (high)
0x6305	TXT_FRM_HEIGHT_L	R/W	0x80	[7:0] : Height of the text frame (low)
0x6306	TXT_FRM_HEIGHT_H	R/W	0x01	[7:5] : reserved [1:0] : Height of the text frame (high)
0x6307	TXT_LINE_SPACE	R/W	0x48	[7:4] : Upper space between lines (Unit : pixel) [3:0] : Lower space between lines (Unit : pixel)
0x6308	COLOR_FRM_HOR_TH	R/W	0x14	[7:0] : Horizontal thickness of the outer frame (Unit : pixel)
0x6309	COLOR_FRM_VER_TH	R/W	0x18	[7:0] : Vertical thickness of the outer frame (Unit : pixel)
0x630A	TXT_FRM_DISP_MODE	R/W	0x0E	[7:6] : reserved [5:4] : Display mode of the outer area [3:2] : Display mode of the color block0 and color block1 [1:0] : Display mode of the text frame and outer frame ● Display mode 00 : 100% transparent 01 : 50% transparent 10 : 50% transparent + 50% defined color0 11 : 50% transparent + 50% defined color1
0x630B	COLOR_BLK0_CON	R/W	0x00	[7:4] : Line number of the color block0 [3:1] : reserved [0] : Color block0 enable
0x630C	COLOR_BLK0_X_S	R/W	0x00	[7:5] : reserved [4:0] : Start x-position of the color block0 (Unit : character)
0x630D	COLOR_BLK0_X_E	R/W	0x00	[7:5] : reserved [4:0] : End x-position of the color block0 (Unit : character)
0x630E	COLOR_BLK1_CON	R/W	0x00	[7:4] : Line number of the color block1 [3:1] : reserved [0] : Color block1 enable
0x630F	COLOR_BLK1_X_S	R/W	0x00	[7:5] : reserved [4:0] : Start x-position of the color block1 (Unit : character)
0x6310	COLOR_BLK1_X_E	R/W	0x00	[7:5] : reserved [4:0] : End x-position of the color block1 (Unit : character)
0x6311	FONT_COLOR_Y	R/W	0x0F	[7:4] : reserved [3:0] : Font color : Y
0x6312	FONT_COLOR_C	R/W	0x88	[7:4] : Font color : Cr [3:0] : Font color : Cb

0x6313	DEFINED_COLOR_Y	R/W	0x28	[7:4] : Defined color1 : Y [3:0] : Defined color0 : Y
0x6314	DEFINED_COLOR_C0	R/W	0x8C	[7:4] : Defined color0 : Cr [3:0] : Defined color0 : Cb
0x6315	DEFINED_COLOR_C1	R/W	0xF1	[7:4] : Defined color1 : Cr [3:0] : Defined color1 : Cb
OSD (PARKING GUIDE) **(VSYNC SYNCHRONIZED)**				
0x6320	PG_CEN_X	R/W	0x40	[7:0] : X-coordinate of the center of the parking guide (low)
0x6321	PG_LINE1_X_E	R/W	0x7C	[7:0] : X-coordinate of the end of the line1 (low)
0x6322	PG_LINE1_Y	R/W	0x6E	[7:0] : Y-coordinate of the line1 (low)
0x6323	PG_LINE2_Y	R/W	0x96	[7:0] : Y-coordinate of the line2 (low)
0x6324	PG_LINE3_Y	R/W	0xD2	[7:0] : Y-coordinate of the line3 (low)
0x6325	PG_LINE4_Y	R/W	0x2C	[7:0] : Y-coordinate of the line4 (low)
0x6326	PG_BOT_LIM_Y	R/W	0x90	[7:0] : Y-coordinate of the bottom limit of the parking guide (low)
0x6327	PG_POS0_HI	R/W	0x05	[7:6] : Y-coordinate of the line2 (high) [5:4] : Y-coordinate of the line1 (high) [3:2] : X-coordinate of the end of the line1 (high) [1:0] : X-coordinate of the center of the parking guide (high)
0x6328	PG_POS1_HI	R/W	0x14	[7:6] : reserved [5:4] : Y-coordinate of the bottom limit of the parking guide (high) [3:2] : Y-coordinate of the line4 (high) [1:0] : Y-coordinate of the line3 (high)
0x6329	PG_SLOPE1	R/W	0x35	[7:4] : dy of the slope1 [3:0] : dx of the slope1 ● Slope1 : the slope from the line1 to the line2
0x632A	PG_SLOPE2	R/W	0x11	[7:4] : dy of the slope2 [3:0] : dx of the slope2 ● Slope2 : the slope from the line2 to the line3
0x632B	PG_SLOPE3	R/W	0x51	[7:4] : dy of the slope3 [3:0] : dx of the slope3 ● Slope3 : the slope from the line3 to the line4
0x632C	PG_SLOPE4	R/W	0xF1	[7:4] : dy of the slope4 [3:0] : dx of the slope4 ● Slope4 : the slope from the line4 to the bottom limit
0x632D	PG_LINE12_COLOR_Y	R/W	0x99	[7:4] : Line2 color : Y [3:0] : Line1 color : Y
0x632E	PG_LINE1_COLOR_C	R/W	0x36	[7:4] : Line1 color : Cr [3:0] : Line1 color : Cb
0x632F	PG_LINE2_COLOR_C	R/W	0x66	[7:4] : Line2 color : Cr [3:0] : Line2 color : Cb
0x6330	PG_LINE34_COLOR_Y	R/W	0x99	[7:4] : Line4 color : Y [3:0] : Line3 color : Y
0x6331	PG_LINE3_COLOR_C	R/W	0x96	[7:4] : Line3 color : Cr [3:0] : Line3 color : Cb
0x6332	PG_LINE4_COLOR_C	R/W	0xC6	[7:4] : Line4 color : Cr [3:0] : Line4 color : Cb
0x6333	PG_LINE56_COLOR_Y	R/W	0x09	[7:4] : reserved [3:0] : Line56 color : Y
0x6334	PG_LINE56_COLOR_C	R/W	0xF2	[7:4] : Line56 color : Cr [3:0] : Line56 color : Cb
0x6335	PG_LINE1_TH	R/W	0x0A	[7:6] : reserved [5:0] : Thickness of the line1
0x6336	PG_LINE2_TH	R/W	0x09	[7:6] : reserved [5:0] : Thickness of the line2

0x6337	PG_LINE3_TH	R/W	0x08	[7:6] : reserved [5:0] : Thickness of the line3
0x6338	PG_LINE4_TH	R/W	0x07	[7:6] : reserved [5:0] : Thickness of the line4
0x6339	PG_SLOPE1_TH	R/W	0x0F	[7:6] : reserved [5:0] : Thickness of the slope1 ● Slope1 : the slope from the line1 to the line2
0x633A	PG_SLOPE2_TH	R/W	0x0C	[7:6] : reserved [5:0] : Thickness of the slope1 ● Slope2 : the slope from the line2 to the line3
0x633B	PG_SLOPE3_TH	R/W	0x0A	[7:6] : reserved [5:0] : Thickness of the slope1 ● Slope3 : the slope from the line3 to the line4
0x633C	PG_SLOPE4_TH	R/W	0x08	[7:6] : reserved [5:0] : Thickness of the slope1 ● Slope4 : the slope from the line4 to the bottom line
OSD (PRIVACY ZONE) **(VSYNC SYNCHRONIZED)**				
0x6340	MASK0_UP_LEFT_X	R/W	0x00	[7:0] : X-coordinate of the upperleft position of the mask0 (low)
0x6341	MASK0_UP_LEFT_Y	R/W	0x00	[7:0] : Y-coordinate of the upperleft position of the mask0 (low)
0x6342	MASK0_LO_RIGHT_X	R/W	0x00	[7:0] : X-coordinate of the lowerright position of the mask0 (low)
0x6343	MASK0_LO_RIGHT_Y	R/W	0x00	[7:0] : Y-coordinate of the lowerright position of the mask0 (low)
0x6344	MASK0_POS_HI	R/W	0x00	[7:6] : Y-coordinate of the lowerright position of the mask0 (high) [5:4] : X-coordinate of the lowerright position of the mask0 (high) [3:2] : Y-coordinate of the upperleft position of the mask0 (high) [1:0] : X-coordinate of the upperleft position of the mask0 (high)
0x6345	MASK1_UP_LEFT_X	R/W	0x00	[7:0] : X-coordinate of the upperleft position of the mask1 (low)
0x6346	MASK1_UP_LEFT_Y	R/W	0x00	[7:0] : Y-coordinate of the upperleft position of the mask1 (low)
0x6347	MASK1_LO_RIGHT_X	R/W	0x00	[7:0] : X-coordinate of the lowerright position of the mask1 (low)
0x6348	MASK1_LO_RIGHT_Y	R/W	0x00	[7:0] : Y-coordinate of the lowerright position of the mask1 (low)
0x6349	MASK1_POS_HI	R/W	0x00	[7:6] : Y-coordinate of the lowerright position of the mask1 (high) [5:4] : X-coordinate of the lowerright position of the mask1 (high) [3:2] : Y-coordinate of the upperleft position of the mask1 (high) [1:0] : X-coordinate of the upperleft position of the mask1 (high)
0x634A	MASK2_UP_LEFT_X	R/W	0x00	[7:0] : X-coordinate of the upperleft position of the mask2 (low)
0x634B	MASK2_UP_LEFT_Y	R/W	0x00	[7:0] : Y-coordinate of the upperleft position of the mask2 (low)
0x634C	MASK2_LO_RIGHT_X	R/W	0x00	[7:0] : X-coordinate of the lowerright position of the mask2 (low)
0x634D	MASK2_LO_RIGHT_Y	R/W	0x00	[7:0] : Y-coordinate of the lowerright position of the mask2 (low)
0x634E	MASK2_POS_HI	R/W	0x00	[7:6] : Y-coordinate of the lowerright position of the mask2 (high) [5:4] : X-coordinate of the lowerright position of the mask2 (high) [3:2] : Y-coordinate of the upperleft position of the mask2 (high) [1:0] : X-coordinate of the upperleft position of the mask2 (high)
0x634F	MASK3_UP_LEFT_X	R/W	0x00	[7:0] : X-coordinate of the upperleft position of the mask3 (low)
0x6350	MASK3_UP_LEFT_Y	R/W	0x00	[7:0] : Y-coordinate of the upperleft position of the mask3 (low)
0x6351	MASK3_LO_RIGHT_X	R/W	0x00	[7:0] : X-coordinate of the lowerright position of the mask3 (low)
0x6352	MASK3_LO_RIGHT_Y	R/W	0x00	[7:0] : Y-coordinate of the lowerright position of the mask3 (low)
0x6353	MASK3_POS_HI	R/W	0x00	[7:6] : Y-coordinate of the lowerright position of the mask3 (high) [5:4] : X-coordinate of the lowerright position of the mask3 (high) [3:2] : Y-coordinate of the upperleft position of the mask3 (high) [1:0] : X-coordinate of the upperleft position of the mask3 (high)
0x6354	MASK4_UP_LEFT_X	R/W	0x00	[7:0] : X-coordinate of the upperleft position of the mask4 (low)
0x6355	MASK4_UP_LEFT_Y	R/W	0x00	[7:0] : Y-coordinate of the upperleft position of the mask4 (low)
0x6356	MASK4_LO_RIGHT_X	R/W	0x00	[7:0] : X-coordinate of the lowerright position of the mask4 (low)

0x6357	MASK4_LO_RIGHT_Y	R/W	0x00	[7:0] : Y-coordinate of the lowerright position of the mask4 (low)
0x6358	MASK4_POS_HI	R/W	0x00	[7:6] : Y-coordinate of the lowerright position of the mask4 (high) [5:4] : X-coordinate of the lowerright position of the mask4 (high) [3:2] : Y-coordinate of the upperleft position of the mask4 (high) [1:0] : X-coordinate of the upperleft position of the mask4 (high)
0x6359	MASK5_UP_LEFT_X	R/W	0x00	[7:0] : X-coordinate of the upperleft position of the mask5 (low)
0x635A	MASK5_UP_LEFT_Y	R/W	0x00	[7:0] : Y-coordinate of the upperleft position of the mask5 (low)
0x635B	MASK5_LO_RIGHT_X	R/W	0x00	[7:0] : X-coordinate of the lowerright position of the mask5 (low)
0x635C	MASK5_LO_RIGHT_Y	R/W	0x00	[7:0] : Y-coordinate of the lowerright position of the mask5 (low)
0x635D	MASK5_POS_HI	R/W	0x00	[7:6] : Y-coordinate of the lowerright position of the mask5 (high) [5:4] : X-coordinate of the lowerright position of the mask5 (high) [3:2] : Y-coordinate of the upperleft position of the mask5 (high) [1:0] : X-coordinate of the upperleft position of the mask5 (high)
0x635E	MASK6_UP_LEFT_X	R/W	0x00	[7:0] : X-coordinate of the upperleft position of the mask6 (low)
0x635F	MASK6_UP_LEFT_Y	R/W	0x00	[7:0] : Y-coordinate of the upperleft position of the mask6 (low)
0x6360	MASK6_LO_RIGHT_X	R/W	0x00	[7:0] : X-coordinate of the lowerright position of the mask6 (low)
0x6361	MASK6_LO_RIGHT_Y	R/W	0x00	[7:0] : Y-coordinate of the lowerright position of the mask6 (low)
0x6362	MASK6_POS_HI	R/W	0x00	[7:6] : Y-coordinate of the lowerright position of the mask6 (high) [5:4] : X-coordinate of the lowerright position of the mask6 (high) [3:2] : Y-coordinate of the upperleft position of the mask6 (high) [1:0] : X-coordinate of the upperleft position of the mask6 (high)
0x6363	MASK7_UP_LEFT_X	R/W	0x00	[7:0] : X-coordinate of the upperleft position of the mask7 (low)
0x6364	MASK7_UP_LEFT_Y	R/W	0x00	[7:0] : Y-coordinate of the upperleft position of the mask7 (low)
0x6365	MASK7_LO_RIGHT_X	R/W	0x00	[7:0] : X-coordinate of the lowerright position of the mask7 (low)
0x6366	MASK7_LO_RIGHT_Y	R/W	0x00	[7:0] : Y-coordinate of the lowerright position of the mask7 (low)
0x6367	MASK7_POS_HI	R/W	0x00	[7:6] : Y-coordinate of the lowerright position of the mask7 (high) [5:4] : X-coordinate of the lowerright position of the mask7 (high) [3:2] : Y-coordinate of the upperleft position of the mask7 (high) [1:0] : X-coordinate of the upperleft position of the mask7 (high)
0x6368	MASK01_COLOR_Y	R/W	0x00	[7:4] : Mask1 color : Y [3:0] : Mask0 color : Y
0x6369	MASK0_COLOR_C	R/W	0x88	[7:4] : Mask0 color : Cr [3:0] : Mask0 color : Cb
0x636A	MASK1_COLOR_C	R/W	0x88	[7:4] : Mask1 color : Cr [3:0] : Mask1 color : Cb
0x636B	MASK23_COLOR_Y	R/W	0x00	[7:4] : Mask3 color : Y [3:0] : Mask2 color : Y
0x636C	MASK2_COLOR_C	R/W	0x88	[7:4] : Mask2 color : Cr [3:0] : Mask2 color : Cb
0x636D	MASK3_COLOR_C	R/W	0x88	[7:4] : Mask3 color : Cr [3:0] : Mask3 color : Cb
0x636E	MASK45_COLOR_Y	R/W	0x00	[7:4] : Mask5 color : Y [3:0] : Mask4 color : Y
0x636F	MASK4_COLOR_C	R/W	0x88	[7:4] : Mask4 color : Cr [3:0] : Mask4 color : Cb
0x6370	MASK5_COLOR_C	R/W	0x88	[7:4] : Mask5 color : Cr [3:0] : Mask5 color : Cb
0x6371	MASK67_COLOR_Y	R/W	0x00	[7:4] : Mask7 color : Y [3:0] : Mask6 color : Y
0x6372	MASK6_COLOR_C	R/W	0x88	[7:4] : Mask6 color : Cr [3:0] : Mask6 color : Cb
0x6373	MASK7_COLOR_C	R/W	0x88	[7:4] : Mask7 color : Cr [3:0] : Mask7 color : Cb

OSD (TEXT LINE POINTER) (VSYNC SYNCHRONIZED)				
0x63C0	TXT_LINE_PTR_L0	R/W	0x00	[7:6] : reserved [5:0] : Text line pointer located at the left-side line0
0x63C1	TXT_LINE_PTR_L1	R/W	0x00	[7:6] : reserved [5:0] : Text line pointer located at the left-side line1
0x63C2	TXT_LINE_PTR_L2	R/W	0x00	[7:6] : reserved [5:0] : Text line pointer located at the left-side line2
0x63C3	TXT_LINE_PTR_L3	R/W	0x00	[7:6] : reserved [5:0] : Text line pointer located at the left-side line3
0x63C4	TXT_LINE_PTR_L4	R/W	0x00	[7:6] : reserved [5:0] : Text line pointer located at the left-side line4
0x63C5	TXT_LINE_PTR_L5	R/W	0x00	[7:6] : reserved [5:0] : Text line pointer located at the left-side line5
0x63C6	TXT_LINE_PTR_L6	R/W	0x00	[7:6] : reserved [5:0] : Text line pointer located at the left-side line6
0x63C7	TXT_LINE_PTR_L7	R/W	0x00	[7:6] : reserved [5:0] : Text line pointer located at the left-side line7
0x63C8	TXT_LINE_PTR_L8	R/W	0x00	[7:6] : reserved [5:0] : Text line pointer located at the left-side line8
0x63C9	TXT_LINE_PTR_L9	R/W	0x00	[7:6] : reserved [5:0] : Text line pointer located at the left-side line9
0x63CA	TXT_LINE_PTR_L10	R/W	0x00	[7:6] : reserved [5:0] : Text line pointer located at the left-side line10
0x63CB	TXT_LINE_PTR_L11	R/W	0x00	[7:6] : reserved [5:0] : Text line pointer located at the left-side line11
0x63CC	TXT_LINE_PTR_L12	R/W	0x00	[7:6] : reserved [5:0] : Text line pointer located at the left-side line12
0x63CD	TXT_LINE_PTR_L13	R/W	0x00	[7:6] : reserved [5:0] : Text line pointer located at the left-side line13
0x63CE	TXT_LINE_PTR_L14	R/W	0x00	[7:6] : reserved [5:0] : Text line pointer located at the left-side line14
0x63CF	TXT_LINE_PTR_L15	R/W	0x00	[7:6] : reserved [5:0] : Text line pointer located at the left-side line15
0x63D0	TXT_LINE_PTR_R0	R/W	0x00	[7:6] : reserved [5:0] : Text line pointer located at the right-side line0
0x63D1	TXT_LINE_PTR_R1	R/W	0x00	[7:6] : reserved [5:0] : Text line pointer located at the right-side line1
0x63D2	TXT_LINE_PTR_R2	R/W	0x00	[7:6] : reserved [5:0] : Text line pointer located at the right-side line2
0x63D3	TXT_LINE_PTR_R3	R/W	0x00	[7:6] : reserved [5:0] : Text line pointer located at the right-side line3
0x63D4	TXT_LINE_PTR_R4	R/W	0x00	[7:6] : reserved [5:0] : Text line pointer located at the right-side line4
0x63D5	TXT_LINE_PTR_R5	R/W	0x00	[7:6] : reserved [5:0] : Text line pointer located at the right-side line5
0x63D6	TXT_LINE_PTR_R6	R/W	0x00	[7:6] : reserved [5:0] : Text line pointer located at the right-side line6
0x63D7	TXT_LINE_PTR_R7	R/W	0x00	[7:6] : reserved [5:0] : Text line pointer located at the right-side line7
0x63D8	TXT_LINE_PTR_R8	R/W	0x00	[7:6] : reserved [5:0] : Text line pointer located at the right-side line8
0x63D9	TXT_LINE_PTR_R9	R/W	0x00	[7:6] : reserved [5:0] : Text line pointer located at the right-side line9
0x63DA	TXT_LINE_PTR_R10	R/W	0x00	[7:6] : reserved [5:0] : Text line pointer located at the right-side line10
0x63DB	TXT_LINE_PTR_R11	R/W	0x00	[7:6] : reserved

				[5:0] : Text line pointer located at the right-side line11
0x63DC	TXT_LINE_PTR_R12	R/W	0x00	[7:6] : reserved [5:0] : Text line pointer located at the right-side line12
0x63DD	TXT_LINE_PTR_R13	R/W	0x00	[7:6] : reserved [5:0] : Text line pointer located at the right-side line13
0x63DE	TXT_LINE_PTR_R14	R/W	0x00	[7:6] : reserved [5:0] : Text line pointer located at the right-side line14
0x63DF	TXT_LINE_PTR_R15	R/W	0x00	[7:6] : reserved [5:0] : Text line pointer located at the right-side line15

11.7. FORMATTER

ADDRESS (HEX)	REGISTER NAME	R/W	DEFAULT (HEX)	DESCRIPTION
FORMATTER	**(VSYNC SYNCHRONIZED)**			
0x6400	DATA_FMAT_CON	R/W	0x00	[7:5] : reserved [4:3] : YCbCr Output Order Control 00 : YCbYCr 01 : YCrYCb 10 : CbYCrY 11 : CrYCbY [2:0] : DATA Format Selection 000 : YCbCr 4:2:2 001 : RGB565 010 : RGB555 011 : Bayer 8 bit 100 : Bayer 10 bit 101 : CCIR656
0x6401	RGB_CON	R/W	0x00	[7:4] : reserved [3:2] : Bayer Output Order Control 00 : RGr-GbB 01 : GrR-BGb 10 : GbB-RGr 11 : BGb-GrR [1] : RGB555 Bit Position Control [0] : R/B Swap Control 0 : RG-GB 1 : BG-GR
0x6402	YC2RGB_RGB_MAX	R/W	0xFF	[7:0] : RGB maximum
0x6403	YC2RGB_RGB_MIN	R/W	0x00	[7:0] : RGB minimum
0x6404	YC2RGB_Y_OFFSET	R/W	0x00	[7:0] : Y offset
0x6405	YC2RGB_C_OFFSET	R/W	0x80	[7:0] : C offset
0x6406	YC2RGB_RGB_Y_COEF_HIGH	R/W	0x01	[7:2] : reserved [1:0] : High byte of RGB Y coefficient
0x6407	YC2RGB_RGB_Y_COEF_LOW	R/W	0x00	[7:0] : Low byte of RGB Y coefficient
0x6408	YC2RGB_R_CR_COEF_HIGH	R/W	0x01	[7:2] : reserved [1:0] : High byte of R Cr coefficient
0x6409	YC2RGB_R_CR_COEF_LOW	R/W	0x67	[7:0] : Low byte of R Cr coefficient
0x640A	YC2RGB_G_CR_COEF_HIGH	R/W	0x00	[7:2] : reserved [1:0] : High byte of G Cr coefficient
0x640B	YC2RGB_G_CR_COEF_LOW	R/W	0xB7	[7:0] : Low byte of G Cr coefficient
0x640C	YC2RGB_G_CB_COEF_HIGH	R/W	0x00	[7:2] : reserved [1:0] : High byte of G Cb coefficient
0x640D	YC2RGB_G_CB_COEF_LOW	R/W	0x58	[7:0] : Low byte of G Cb coefficient
0x640E	YC2RGB_B_CB_COEF_HIGH	R/W	0x01	[7:2] : reserved [1:0] : High byte of B Cb coefficient
0x640F	YC2RGB_B_CB_COEF_LOW	R/W	0xC6	[7:0] : Low byte of B Cb coefficient
0x6410	FMAT_PDATA_CON	R/W	0x00	[7] : reserved [6] : Hsync enable for Vblank [5] : OPB output enable (0 : disable, 1 : enable) [4] : pclock polarity inversion [3] : Vsync polarity inversion [2] : Hsync polarity inversion [1:0] : Bit Position Control 00 : xxPDATA[7:0] 01 : xPDATA[7:0]x 1x : PDATA[7:0]xx
0x6411	VGA_WIN_CON	R/W	0x28	[7] : VGA mode enable (640x480) [6:0] : x position start point
0x6412	TV_DATA_CON	R/W	0x04	[7:4] : reserved

				[4] : TV Format Selection 0 : NTSC 1 : PAL [3:0] : TV Out Line Delay Control 0000 : -4 line delay 0001 : -3 line delay 0010 : -2 line delay 0011 : -1 line delay 0100 : 0 line delay 0101 : 1 line delay 0110 : 2 line delay 0111 : 3 line delay 1000 : 4 line delay
0x6413	TAG_ENABLE	R/W	0x00	[7:6] : reserved [1:0] : tag enable (pink: , green : small/large →0x5325) 00 : disable 01 : 6x6 pixel display 10 : 2 line display

11.8. TV Encoder

ADDRESS (HEX)	REGISTER NAME	R/W	DEFAULT (HEX)	DESCRIPTION
TV ENCODER	(VSYNC SYNCHRONIZED)			
0x6500	VER_STS	R	0x01	[7:3] : reserved [3:0] : VERID
0x6501	MD_CTL0	R/W	0x10	[7] : reserved [6] : Subcarrier phase reset Control 0 : Subcarrier Reset Disable 1 : Subcarrier Reset Enable (Reset to “0” at the beginning of every 4(8) field) [5] : NTSC/PAL selection 0 : NTSC 1 : PAL [4] : Pedestal setup control 0 : Pedestal SETUP Disable (NTSC-J, PAL-BDGHI, PAL-Nc, PAL60) 1 : Pedestal SETUP Enable (7.5 IRE) (NTSC-M, NTSC4.43, PAL_N, PAL-M, NTSC50) [3] : Burst Level Control 0 : BURST Level 40 IRE (NTSC-M, NTSC-J, NTSC4.43, PAL-N, PAL-M, NTSC50) 1 : BURST Level 42.86 IRE (PAL-BDGHI, PAL-N, PAL-Nc, PAL-M, PAL60) [2] : Sync Level Control 0 : Sync Level 40 IRE (NTSC-M, NTSC-J, NTSC4.43,PAL-N, PAL-M, NTSC50) 1 : Sync Level 43 IRE (PAL-BGDHI, PAL-Nc, PAL60) [1] : Vsync Width Control 0 : VSYNC 2.5 Line (NTSC-M, PAL-BDGHI, PAL-Nc, NTSC50) 1 : VSYNC 3 Line (NTSC-J, NTSC4.43, PAL-N, PAL-M, PAL60) [0] : 525/625 line format 0 : 525 line format (NTSC-M, NTSC-J, NTSC4.43, PAL-M, PAL60) 1 : 625 line format (PAL-BDGHI, PAL-N, PAL-Nc, NTSC50)
0x6502	MD_CTL1	R/W	0x00	[7:2] : reserved [1:0] : Chroma Frequency Selection 00 : 3.579545455MHz (NTSC-M, NTSC-J) 01 : 4.43361875MHz (NTSC4.43, PAL-BDGHI, PAL-N, PAL60) 10 : 3.57561189MHz (PAL-M) 11 : 3.58205625MHz (PAL-Nc)
0x6503	IF_CTL0	R/W	0x19	[7:0] : reserved
0x6504	IF_CTL1	R/W	0x0B	[7:0] : reserved
0x6505	IF_STS0	R/W	0x00	[7:0] : Low byte of Horizontal Count Number Status (Real Number -1)
0x6506	IF_STS1	R/W	0x00	[7:4] : reserved [3:0] : High byte of Horizontal Count Number Status (Real Number -1)
0x6507	IF_STS2	R/W	0x00	[7:0] : Low byte of Vertical Line Count Number per Frame (Real Number -1)
0x6508	IF_STS3	R/W	0x00	[7:5] : reserved [4:2] : Current Field Count Number [1:0] : High byte of Vertical Line Count Number per Frame (Real Number -1)
0x6509	DAC_CTL0	R/W	0x10	[7:5] : reserved [4] : Video DAC power down control

				0 : active 1 : power down [3:2] : High byte of DAC data [1:0] : Encoder output selection 00 : CVBS 01 : 0x000 10 : 0x3FF 11 : DAC data
0x650A	DAC_CTL1	R/W	0x00	[7:0] : Low byte of DAC data
0x650B	ConBr_CTL0	R/W	0x80	[7:0] : Brightness Control, 2's Compliment
0x650C	ConBr_CTL1	R/W	0x00	[7:0] : Contrast Control, Max Gain = 255/128
0x650D	SatGn_CTL0	R/W	0x80	[7:0] : Cb Gain Control, Max Gain = 255/128
0x650E	SatGn_CTL1	R/W	0x80	[7:0] : Cr Gain Control, Max Gain = 255/128
0x650F	HUE_CTL0	R/W	0x00	[7:0] : Hue Control, 1 LSB = 1.40625°
0x6510	HUE_CTL1	R/W	0x00	[7:1] : reserved [0] : Video Mute Control 0 : Normal Operation 1 : Video Mute Enable
0x6511	M_PAT_CTL	R/W	0x00	[7:2] : reserved [1] : Internal Pattern Selection 0 : 100% Color Bar 1 : 75% Color Bar [0] : Internal Pattern Control 0 : Internal Pattern Disable 1 : Internal Pattern Enable
0x6512	FLTSEL_CTL0	R/W	0x00	[7:6] : reserved [5:3] : UV Filter Control 0 : Wide Bandwidth 4 : Narrow Bandwidth [2:0] : Y Filter Control 0 : Wide Bandwidth 4 : Narrow Bandwidth
0x6513	FLTSEL_CTL1	R/W	0x03	[7:4] : reserved [3] : Sync Filter Control 0 : disable 1 : enable [2:0] : Sync Filter Selection
0x6514	DTO_OS_CTL0	R/W	0x00	[7:0] : Low byte of FSC Offset Control
0x6515	DTO_OS_CTL0	R/W	0x00	[7:0] : High byte of FSC Offset Control
0x6516	M_FSC_CTL0	R/W	0x00	Manual Chroma Frequency Control. This register s are only effective when M_FSC_CTL3[7] = '1' FSCDTO = int(Fsc / CLK * 2^32 +0.5) [7:0] : Fsc[7:0]
0x6517	M_FSC_CTL1	R/W	0x00	[7:0] : Fsc[15:8]
0x6518	M_FSC_CTL2	R/W	0x00	[7:0] : Fsc[23:16]
0x6519	M_FSC_CTL3	R/W	0x00	[7] : Chroma Subcarrier Frequency Control 0 : Automatic Chroma Subcarrier Frequency Control Mode 1 : Manual Chroma Subcarrier Frequency Control Enable [6:0] : Fsc[30:24]
0x651A	SINX_CTL	R/W	0x01	[7:0] : reserved
0x651B	MY_CTL0	R/W	0x5D	[7:0] : Low byte of Manual Y gain MY = int(VMax/(219 * VFULL) * 2^18 +0.5)
0x651C	MY_CTL1	R/W	0x02	[7:3] : reserved [2] : Manual Gain Control Enable (when YCbCr to YUV Conversion) 0 : Automatic Color Space Conversion 1 : Manual Color Space Conversion [1:0] : High byte of Manual Y gain
0x651D	MCb_CTL0	R/W	0x04	[7:0] : Low byte of Manual Cb gain MCb = int(VMax*0.492*1.772/(VFULL*224)*2^18 +0.5) *VMax = 100% White Voltage Level (NTSC-M/PALM/N=0.661, NTSC-J=0.714, PAL=0.7), *VFULL=DAC Full Scale Output Voltage
0x651E	MCb_CTL1	R/W	0x02	[7:2] : reserved [1:0] : High byte of Manual Cb gain
0x651F	MCr_CTL0	R/W	0xD8	[7:0] : Low byte of Manual Cr gain MCr = int(VMax*0.877*1.403/(VFULL*224)*2^18+0.5)

0x6520	MCr_CTL1	R/W	0x02	[7:2] : reserved [1:0] : High byte of Manual Cr gain
0x6521	MLVL_CTL	R/W	0x00	[7:3] : reserved [2] : Manual Sync Level Control 0 : Automatic Sync Level Control 1 : Manual Sync Level Control Enable [1] : Manual Burst Level Control 0 : Automatic Burst Level Control 1 : Manual Burst Level Control Enable [0] : Manual Pedestal Set-up Level Control 0 : Automatic Pedestal Set-up Level Control 1 : Manual Pedestal Set-up Level Control Enable
0x6522	MSYNC_CTL	R/W	0xE0	[7:0] : Manual Sync Level Control . This register s are only effective when MLVL_CTL[2] = ”1” M_SyncLevel = int(VSync/ VFULL * 2^10 +0.5) *VSync = Sync Voltage Level (NTSC-M/J/PALM/N=0.286, PAL=0.3) *VFULL=DAC Full Scale Output Voltage
0x6523	MBST_CTL	R/W	0x70	[7:0] : Manual Burst Level Control. This register s are only effective when MLVL_CTL[1] = ”1” NTSC : M_ Burst = int(VBurst/ VFULL * 2^9 +0.5) PAL :M_ Burst = int(VBurst/ VFULL * 2^9 * 2^-0.5 +0.5) * VBurst = Burst Voltage Level (NTSC-M/J/PALM/N=0.286, PAL=0.299) *VFULL=DAC Full Scale Output Voltage
0x6524	MSUP_CTL	R/W	0x2A	[7:0] : Manual Pedestal Set-up Level Control. This register s are only effective when MLVL_CTL[0] =”1” & SETUP=”1” M_SetUpLevel = int(7.5*0.00715/ VFULL * 2^10 +0.5) *VFULL=DAC Full Scale Output Voltage
0x6525	MHSWd_CTL0	R/W	0x40	[7:0] : Manual HSYNC Width Control. This register s are only effective when MHSWd_CTL1[0] =”1” CLK/2 * (M_HSWd+1)
0x6526	MHSWd_CTL1	R/W	0x00	[7:1] : reserved [0] : Manual HSYNC Width Control 0 : Automatic HSYNC Width Control 1 : Manual HSYNC Width Control Enable
0x6527	MBWd_CTL0	R/W	0x47	[7:0] : Manual Burst Start Control. This register s are only effective when MBWd_CTL1[0] =”1” CLK/2 * (M_ BurstSt +1)
0x6528	MBWd_CTL1	R/W	0x00	[7:1] : reserved [0] : Manual Burst Width Control 0 : Automatic Burst Width Control 1 : Manual Burst Width Control Enable
0x6529	MBWd_CTL2	R/W	0x69	[7:0] : Low byte of Manual Burst End Control This register s are only effective when MBWd_CTL1[0] =”1” CLK/2 * (M_ BurstEnd +1)
0x652A	MBWd_CTL3	R/W	0x00	[7:1] : reserved [0] : High byte of Manual Burst End Control
0x652B	MHAV_CTL0	R/W	0x79	[7:0] : Manual Horizontal Active Start Control This register s are only effective when MHAV_CTL1[0] =”1” CLK/2 * (M_ HAVSt +1)
0x652C	MHAV_CTL1	R/W	0x00	[7:2] : reserved [1] : Slave HAV & VAV Timing Control 1 : HAV & VAV Timing is controlled by Input Timing [0] : Manual Horizontal Active Start and End Control 0 : Automatic Horizontal Active Start and End Control 1 : Manual Horizontal Active Start and End Control Enable
0x652D	MHAV_CTL2	R/W	0x49	[7:0] : Low byte of Manual Horizontal Active End Control This register s are only effective when MHAV_CTL1[0] =”1” CLK/2 * (M_ HAVEnd +1)
0x653E	MHAV_CTL3	R/W	0x03	[7:3] : reserved

				[2:0] : High byte of Manual Horizontal Active End Control
0x653F	MVAV_CTL0	R/W	0x12	[7:0] : Manual Vertical Active Start Control This register s are only effective when MVAV_CTL1[0] =”1” (M_ HAVSt +1) From Vsync
0x6530	MVAV_CTL1	R/W	0x00	[7:1] : reserved [0] : Manual Vertical Active Start and End Control 0 : Automatic Vertical Active Start and End Control 1 : Manual Vertical Active Start and End Control Enable
0x6531	MVAV_CTL2	R/W	0x02	[7:0] : Low byte of Manual Vertical Active End Control This register s are only effective when MVAV_CTL1[0] =”1” (M_ VAVEnd +1) From Vsync
0x6532	MVAV_CTL3	R/W	0x01	[7:1] : reserved [0] : High byte of Manual Vertical Active End Control
0x6533	VBIE_CTL	R/W	0x00	[7:0] : reserved
0x6534	VBI_STS	R/W	0x00	[7:0] : reserved
0x6535	CCF1D_CTL0	R/W	0x00	[7:0] : reserved
0x6536	CCF1D_CTL1	R/W	0x00	[7:0] : reserved
0x6537	CCF2D_CTL0	R/W	0x00	[7:0] : reserved
0x6538	CCF2D_CTL1	R/W	0x00	[7:0] : reserved
0x6539	VBIGN_CTL	R/W	0x00	[7:0] : reserved

11.9. CCP

ADDRESS (HEX)	REGISTER NAME	R/W	DEFAULT (HEX)	DESCRIPTION
AE **(VSYNC SYNCHRONIZED)**				
0x7000	AE_WIN01_SEL	R/W	0x00	[7:4] : reserved [3] : AE window1 display enable (1:on) [2] : Luminance data out [1] : LP Luminance data out [0] : SP Luminance data out
0x7001	AE_WIN02_SEL	R/W	0x00	[7:4] : reserved [3] : AE window2 display enable (1:on) [2] : Luminance data out [1] : LP Luminance data out [0] : SP Luminance data out
0x7002	AE_WIN03_SEL	R/W	0x00	[7:4] : reserved [3] : AE window3 display enable (1:on) [2] : Luminance data out [1] : LP Luminance data out [0] : SP Luminance data out
0x7003	AE_WIN04_SEL	R/W	0x00	[7:4] : reserved [3] : AE window4 display enable (1:on) [2] : Luminance data out [1] : LP Luminance data out [0] : SP Luminance data out
0x7004	AE_WIN05_SEL	R/W	0x00	[7:4] : reserved [3] : AE window5 display enable (1:on) [2] : Luminance data out [1] : LP Luminance data out [0] : SP Luminance data out
0x7005	AE_WIN06_SEL	R/W	0x00	[7:4] : reserved [3] : AE window6 display enable (1:on) [2] : Luminance data out [1] : LP Luminance data out [0] : SP Luminance data out
0x7006	AE_WIN07_SEL	R/W	0x00	[7:4] : reserved [3] : AE window7 display enable (1:on) [2] : Luminance data out [1] : LP Luminance data out [0] : SP Luminance data out
0x7007	AE_WIN08_SEL	R/W	0x00	[7:4] : reserved [3] : AE window8 display enable (1:on) [2] : Luminance data out [1] : LP Luminance data out [0] : SP Luminance data out
0x7008	AE_WIN09_SEL	R/W	0x00	[7:4] : reserved [3] : AE window9 display enable (1:on) [2] : Luminance data out [1] : LP Luminance data out [0] : SP Luminance data out
0x7009	AE_WIN10_SEL	R/W	0x00	[7:4] : reserved [3] : AE window10 display enable (1:on) [2] : Luminance data out [1] : LP Luminance data out [0] : SP Luminance data out
0x700D	AE_SAT01_SEL	R/W	0x00	[7:4] : reserved [3] : SP saturation area selection

				0 : LP saturation area 1 : SP whole area [2] : AE window21 sat.window1 win,rgn display enable [1] : AE window21 sat.window1 data sel (0:LP&SP,1:) [0] : AE window21 sat.window1 enable
0x700E	AE_SAT02_SEL	R/W	0x00	[7:3] : reserved [2] : AE window22 sat.window2 win,rgn display enable [1] : AE window22 sat.window2 data sel (0:LP&SP,1:) [0] : AE window22 sat.window2 enable
0x700F	AE_SAT03_SEL	R/W	0x00	[7:3] : reserved [2] : AE window23 sat.window3 win,rgn display enable [1] : AE window23 sat.window3 data sel (0:LP&SP,1:) [0] : AE window23 sat.window3 enable
0x7010	AE_SAT04_SEL	R/W	0x00	[7:3] : reserved [2] : AE window24 sat.window4 win,rgn display enable [1] : AE window24 sat.window4 data sel (0:LP&SP,1:) [0] : AE window24 sat.window4 enable
0x7011	AE_SAT05_SEL	R/W	0x00	[7:3] : reserved [2] : AE window25 sat.window5 win,rgn display enable [1] : AE window25 sat.window5 data sel (0:LP&SP,1:) [0] : AE window25 sat.window5 enable
0x7020	AE_WIN01_LR	R/W	0x0F	[7:4] : Left value of AE window 1 [3:0] : Right value of AE window 1
0x7021	AE_WIN01_UD	R/W	0x0F	[7:4] : Up value of AE window 1 [3:0] : Down value of AE window 1
0x7022	AE_WIN02_LR	R/W	0x0F	[7:4] : Left value of AE window 2 [3:0] : Right value of AE window 2
0x7023	AE_WIN02_UD	R/W	0x0F	[7:4] : Up value of AE window 2 [3:0] : Down value of AE window 2
0x7024	AE_WIN03_LR	R/W	0x0F	[7:4] : Left value of AE window 3 [3:0] : Right value of AE window 3
0x7025	AE_WIN03_UD	R/W	0x0F	[7:4] : Up value of AE window 3 [3:0] : Down value of AE window 3
0x7026	AE_WIN04_LR	R/W	0x0F	[7:4] : Left value of AE window 4 [3:0] : Right value of AE window 4
0x7027	AE_WIN04_UD	R/W	0x0F	[7:4] : Up value of AE window 4 [3:0] : Down value of AE window 4
0x7028	AE_WIN05_LR	R/W	0x0F	[7:4] : Left value of AE window 5 [3:0] : Right value of AE window 5
0x7029	AE_WIN05_UD	R/W	0x0F	[7:4] : Up value of AE window 5 [3:0] : Down value of AE window 5
0x702A	AE_WIN06_LR	R/W	0x0F	[7:4] : Left value of AE window 6 [3:0] : Right value of AE window 6
0x702B	AE_WIN06_UD	R/W	0x0F	[7:4] : Up value of AE window 6 [3:0] : Down value of AE window 6
0x702C	AE_WIN07_LR	R/W	0x0F	[7:4] : Left value of AE window 7 [3:0] : Right value of AE window 7
0x702D	AE_WIN07_UD	R/W	0x0F	[7:4] : Up value of AE window 7 [3:0] : Down value of AE window 7
0x702E	AE_WIN08_LR	R/W	0x0F	[7:4] : Left value of AE window 8 [3:0] : Right value of AE window 8
0x702F	AE_WIN08_UD	R/W	0x0F	[7:4] : Up value of AE window 8 [3:0] : Down value of AE window 8
0x7030	AE_WIN09_LR	R/W	0x0F	[7:4] : Left value of AE window 9 [3:0] : Right value of AE window 9
0x7031	AE_WIN09_UD	R/W	0x0F	[7:4] : Up value of AE window 9 [3:0] : Down value of AE window 9

0x7032	AE_WIN10_LR	R/W	0x0F	[7:4] : Left value of AE window 10 [3:0] : Right value of AE window 10
0x7033	AE_WIN10_UD	R/W	0x0F	[7:4] : Up value of AE window 10 [3:0] : Down value of AE window 10
0x7038	AE_WIN21_LR	R/W	0x0F	[7:4] : Left value of Saturation Window1 [3:0] : Right value of Saturation Window1
0x7039	AE_WIN21_UD	R/W	0x0F	[7:4] : Up value of Saturation Window1 [3:0] : Down value of Saturation Window1
0x703A	AE_WIN22_LR	R/W	0x0F	[7:4] : Left value of Saturation Window2 [3:0] : Right value of Saturation Window2
0x703B	AE_WIN22_UD	R/W	0x0F	[7:4] : Up value of Saturation Window2 [3:0] : Down value of Saturation Window2
0x703C	AE_WIN23_LR	R/W	0x0F	[7:4] : Left value of Saturation Window3 [3:0] : Right value of Saturation Window3
0x703D	AE_WIN23_UD	R/W	0x0F	[7:4] : Up value of Saturation Window3 [3:0] : Down value of Saturation Window3
0x703E	AE_WIN24_LR	R/W	0x0F	[7:4] : Left value of Saturation Window4 [3:0] : Right value of Saturation Window4
0x703F	AE_WIN24_UD	R/W	0x0F	[7:4] : Up value of Saturation Window4 [3:0] : Down value of Saturation Window4
0x7040	AE_WIN25_LR	R/W	0x0F	[7:4] : Left value of Saturation Window5 [3:0] : Right value of Saturation Window5
0x7041	AE_WIN25_UD	R/W	0x0F	[7:4] : Up value of Saturation Window5 [3:0] : Down value of Saturation Window5
0x7050	AE01_SUM3	R	0x00	[7:5] : Reserved [4:0] : Summation of Y data out in AE window 1[28:24]
0x7051	AE01_SUM2	R	0x00	[7:0] : Summation of Y data out in AE window 1[23:16]
0x7052	AE01_SUM1	R	0x00	[7:0] : Summation of Y data out in AE window 1[15:8]
0x7053	AE01_SUM0	R	0x00	[7:0] : Summation of Y data out in AE window 1[7:0]
0x7054	AE02_SUM3	R	0x00	[7:5] : Reserved [4:0] : Summation of Y data out in AE window 2[28:24]
0x7055	AE02_SUM2	R	0x00	[7:0] : Summation of Y data out in AE window 2[23:16]
0x7056	AE02_SUM1	R	0x00	[7:0] : Summation of Y data out in AE window 2[15:8]
0x7057	AE02_SUM0	R	0x00	[7:0] : Summation of Y data out in AE window 2[7:0]
0x7058	AE03_SUM3	R	0x00	[7:5] : Reserved [4:0] : Summation of Y data out in AE window 3[28:24]
0x7059	AE03_SUM2	R	0x00	[7:0] : Summation of Y data out in AE window 3[23:16]
0x705A	AE03_SUM1	R	0x00	[7:0] : Summation of Y data out in AE window 3[15:8]
0x705B	AE03_SUM0	R	0x00	[7:0] : Summation of Y data out in AE window 3[7:0]
0x705C	AE04_SUM3	R	0x00	[7:5] : Reserved [4:0] : Summation of Y data out in AE window 4[28:24]
0x705D	AE04_SUM2	R	0x00	[7:0] : Summation of Y data out in AE window 4[23:16]
0x705E	AE04_SUM1	R	0x00	[7:0] : Summation of Y data out in AE window 4[15:8]
0x705F	AE04_SUM0	R	0x00	[7:0] : Summation of Y data out in AE window 4[7:0]
0x7060	AE05_SUM3	R	0x00	[7:5] : Reserved [4:0] : Summation of Y data out in AE window 5[28:24]
0x7061	AE05_SUM2	R	0x00	[7:0] : Summation of Y data out in AE window 5[23:16]
0x7062	AE05_SUM1	R	0x00	[7:0] : Summation of Y data out in AE window 5[15:8]
0x7063	AE05_SUM0	R	0x00	[7:0] : Summation of Y data out in AE window 5[7:0]
0x7064	AE06_SUM3	R	0x00	[7:5] : Reserved [4:0] : Summation of Y data out in AE window 6[28:24]
0x7065	AE06_SUM2	R	0x00	[7:0] : Summation of Y data out in AE window 6[23:16]

0x7066	AE06_SUM1	R	0x00	[7:0] : Summation of Y data out in AE window 6[15:8]
0x7067	AE06_SUM0	R	0x00	[7:0] : Summation of Y data out in AE window 6[7:0]
0x7068	AE07_SUM3	R	0x00	[7:5] : Reserved [4:0] : Summation of Y data out in AE window 7[28:24]
0x7069	AE07_SUM2	R	0x00	[7:0] : Summation of Y data out in AE window 7[23:16]
0x706A	AE07_SUM1	R	0x00	[7:0] : Summation of Y data out in AE window 7[15:8]
0x706B	AE07_SUM0	R	0x00	[7:0] : Summation of Y data out in AE window 7[7:0]
0x706C	AE08_SUM3	R	0x00	[7:5] : Reserved [4:0] : Summation of Y data out in AE window 8[28:24]
0x706D	AE08_SUM2	R	0x00	[7:0] : Summation of Y data out in AE window 8[23:16]
0x706E	AE08_SUM1	R	0x00	[7:0] : Summation of Y data out in AE window 8[15:8]
0x706F	AE08_SUM0	R	0x00	[7:0] : Summation of Y data out in AE window 8[7:0]
0x7070	AE09_SUM3	R	0x00	[7:5] : Reserved [4:0] : Summation of Y data out in AE window 9[28:24]
0x7071	AE09_SUM2	R	0x00	[7:0] : Summation of Y data out in AE window 9[23:16]
0x7072	AE09_SUM1	R	0x00	[7:0] : Summation of Y data out in AE window 9[15:8]
0x7073	AE09_SUM0	R	0x00	[7:0] : Summation of Y data out in AE window 9[7:0]
0x7074	AE10_SUM3	R	0x00	[7:5] : Reserved [4:0] : Summation of Y data out in AE window 10[28:24]
0x7075	AE10_SUM2	R	0x00	[7:0] : Summation of Y data out in AE window 10[23:16]
0x7076	AE10_SUM1	R	0x00	[7:0] : Summation of Y data out in AE window 10[15:8]
0x7077	AE10_SUM0	R	0x00	[7:0] : Summation of Y data out in AE window 10[7:0]
0x7080	AE21_SP_SAT_HTHR	R/W	0xB0	[7:0] : Small Pixel Saturation Histogram High Threshold
0x7081	AE21_SP_SAT_LTHR	R/W	0x28	[7:0] : Small Pixel Saturation Histogram Low Threshold
0x7082	AE21_SP_SAT_HCNT2	R	0x00	[7:3] : Reserved [2:0] : High part of Small Pixel saturation count[18:16]
0x7083	AE21_SP_SAT_HCNT1	R	0x00	[7:0] : High part of Small Pixel saturation count[15:8]
0x7084	AE21_SP_SAT_HCNT0	R	0x00	[7:0] : High part of Small Pixel saturation count[7:0]
0x7085	AE21_SP_SAT_MCNT2	R	0x00	[7:3] : Reserved [2:0] : Middle part of Small Pixel saturation count[18:16]
0x7086	AE21_SP_SAT_MCNT1	R	0x00	[7:0] : Middle part of Small Pixel saturation count[15:8]
0x7087	AE21_SP_SAT_MCNT0	R	0x00	[7:0] : Middle part of Small Pixel saturation count[7:0]
0x7088	AE21_SP_SAT_LCNT2	R	0x00	[7:3] : Reserved [2:0] : Low part of Small Pixel saturation count[18:16]
0x7089	AE21_SP_SAT_LCNT1	R	0x00	[7:0] : Low part of Small Pixel saturation count[15:8]
0x708A	AE21_SP_SAT_LCNT0	R	0x00	[7:0] : Low part of Small Pixel saturation count[7:0]
0x70A0	AE21_LP_SAT_THR	R/W	0xF0	[7:0] : Large Pixel saturation threshold in saturation window1
0x70A1	AE21_LP_SAT_CNT2	R	0x00	[7:0] : Count of Large Pixel Y in SAT window 1[23:16]
0x70A2	AE21_LP_SAT_CNT1	R	0x00	[7:0] : Count of Large Pixel Y in SAT window 1[15:8]
0x70A3	AE21_LP_SAT_CNT0	R	0x00	[7:0] : Count of Large Pixel Y in SAT window 1[7:0]
0x70A4	AE21_LP_SAT_SUM3	R	0x00	[7:5] : Reserved [4:0] : Sum of Large Pixel Y in SAT window 1[28:24]
0x70A5	AE21_LP_SAT_SUM2	R	0x00	[7:0] : Sum of Large Pixel Y in SAT window 1[23:16]
0x70A6	AE21_LP_SAT_SUM1	R	0x00	[7:0] : Sum of Large Pixel Y in SAT window 1[15:8]
0x70A7	AE21_LP_SAT_SUM0	R	0x00	[7:0] : Sum of Large Pixel Y in SAT window 1[7:0]
0x70A8	AE21_SP_SAT_SUM3	R	0x00	[7:5] : Reserved [4:0] : Sum of Small Pixel Y in SAT window 1[28:24]
0x70A9	AE21_SP_SAT_SUM2	R	0x00	[7:0] : Sum of Small Pixel Y in SAT window 1[23:16]

0x70AA	AE21_SP_SAT_SUM1	R	0x00	[7:0] : Sum of Small Pixel Y in SAT window 1[15:8]
0x70AB	AE21_SP_SAT_SUM0	R	0x00	[7:0] : Sum of Small Pixel Y in SAT window 1[7:0]
0x70B0	AE22_LP_SAT_THR	R/W	0x8C	[7:0] : Large Pixel saturation threshold in saturation window2
0x70B1	AE22_LP_SAT_CNT2	R	0x00	[7:0] : Count of Large Pixel Y in SAT window 2[23:16]
0x70B2	AE22_LP_SAT_CNT1	R	0x00	[7:0] : Count of Large Pixel Y in SAT window 2[15:8]
0x70B3	AE22_LP_SAT_CNT0	R	0x00	[7:0] : Count of Large Pixel Y in SAT window 2[7:0]
0x70B4	AE22_LP_SAT_SUM3	R	0x00	[7:5] : Reserved [4:0] : Sum of Large Pixel Y in SAT window 2[28:24]
0x70B5	AE22_LP_SAT_SUM2	R	0x00	[7:0] : Sum of Large Pixel Y in SAT window 2[23:16]
0x70B6	AE22_LP_SAT_SUM1	R	0x00	[7:0] : Sum of Large Pixel Y in SAT window 2[15:8]
0x70B7	AE22_LP_SAT_SUM0	R	0x00	[7:0] : Sum of Large Pixel Y in SAT window 2[7:0]
0x70B8	AE22_SP_SAT_SUM3	R	0x00	[7:5] : Reserved [4:0] : Sum of Small Pixel Y in SAT window 2[28:24]
0x70B9	AE22_SP_SAT_SUM2	R	0x00	[7:0] : Sum of Small Pixel Y in SAT window 2[23:16]
0x70BA	AE22_SP_SAT_SUM1	R	0x00	[7:0] : Sum of Small Pixel Y in SAT window 2[15:8]
0x70BB	AE22_SP_SAT_SUM0	R	0x00	[7:0] : Sum of Small Pixel Y in SAT window 2[7:0]
0x70C0	AE23_LP_SAT_THR	R/W	0x80	[7:0] : Large Pixel saturation threshold in saturation window3
0x70C1	AE23_LP_SAT_CNT2	R	0x00	[7:0] : Count of Large Pixel Y in SAT window 3[23:16]
0x70C2	AE23_LP_SAT_CNT1	R	0x00	[7:0] : Count of Large Pixel Y in SAT window 3[15:8]
0x70C3	AE23_LP_SAT_CNT0	R	0x00	[7:0] : Count of Large Pixel Y in SAT window 3[7:0]
0x70C4	AE23_LP_SAT_SUM3	R	0x00	[7:5] : Reserved [4:0] : Sum of Large Pixel Y in SAT window 3[28:24]
0x70C5	AE23_LP_SAT_SUM2	R	0x00	[7:0] : Sum of Large Pixel Y in SAT window 3[23:16]
0x70C6	AE23_LP_SAT_SUM1	R	0x00	[7:0] : Sum of Large Pixel Y in SAT window 3[15:8]
0x70C7	AE23_LP_SAT_SUM0	R	0x00	[7:0] : Sum of Large Pixel Y in SAT window 3[7:0]
0x70C8	AE23_SP_SAT_SUM3	R	0x00	[7:5] : Reserved [4:0] : Sum of Small Pixel Y in SAT window 3[28:24]
0x70C9	AE23_SP_SAT_SUM2	R	0x00	[7:0] : Sum of Small Pixel Y in SAT window 3[23:16]
0x70CA	AE23_SP_SAT_SUM1	R	0x00	[7:0] : Sum of Small Pixel Y in SAT window 3[15:8]
0x70CB	AE23_SP_SAT_SUM0	R	0x00	[7:0] : Sum of Small Pixel Y in SAT window 3[7:0]
0x70D0	AE24_LP_SAT_THR	R/W	0x28	[7:0] : Large Pixel saturation threshold in saturation window4
0x70D1	AE24_LP_SAT_CNT2	R	0x00	[7:0] : Count of Large Pixel Y in SAT window 4[23:16]
0x70D2	AE24_LP_SAT_CNT1	R	0x00	[7:0] : Count of Large Pixel Y in SAT window 4[15:8]
0x70D3	AE24_LP_SAT_CNT0	R	0x00	[7:0] : Count of Large Pixel Y in SAT window 4[7:0]
0x70D4	AE24_LP_SAT_SUM3	R	0x00	[7:5] : Reserved [4:0] : Sum of Large Pixel Y in SAT window 4[28:24]
0x70D5	AE24_LP_SAT_SUM2	R	0x00	[7:0] : Sum of Large Pixel Y in SAT window 4[23:16]
0x70D6	AE24_LP_SAT_SUM1	R	0x00	[7:0] : Sum of Large Pixel Y in SAT window 4[15:8]
0x70D7	AE24_LP_SAT_SUM0	R	0x00	[7:0] : Sum of Large Pixel Y in SAT window 4[7:0]
0x70D8	AE24_SP_SAT_SUM3	R	0x00	[7:5] : Reserved [4:0] : Sum of Small Pixel Y in SAT window 4[28:24]
0x70D9	AE24_SP_SAT_SUM2	R	0x00	[7:0] : Sum of Small Pixel Y in SAT window 4[23:16]
0x70DA	AE24_SP_SAT_SUM1	R	0x00	[7:0] : Sum of Small Pixel Y in SAT window 4[15:8]
0x70DB	AE24_SP_SAT_SUM0	R	0x00	[7:0] : Sum of Small Pixel Y in SAT window 4[7:0]
0x70E0	AE25_LP_SAT_THR	R/W	0x14	[7:0] : Large Pixel saturation threshold in saturation window5
0x70E1	AE25_LP_SAT_CNT2	R	0x00	[7:0] : Count of Large Pixel Y in SAT window 5[23:16]
0x70E2	AE25_LP_SAT_CNT1	R	0x00	[7:0] : Count of Large Pixel Y in SAT window 5[15:8]

0x70E3	AE25_LP_SAT_CNT0	R	0x00	[7:0] : Count of Large Pixel Y in SAT window 5[7:0]
0x70E4	AE25_LP_SAT_SUM3	R	0x00	[7:5] : Reserved [4:0] : Sum of Large Pixel Y in SAT window 5[28:24]
0x70E5	AE25_LP_SAT_SUM2	R	0x00	[7:0] : Sum of Large Pixel Y in SAT window 5[23:16]
0x70E6	AE25_LP_SAT_SUM1	R	0x00	[7:0] : Sum of Large Pixel Y in SAT window 5[15:8]
0x70E7	AE25_LP_SAT_SUM0	R	0x00	[7:0] : Sum of Large Pixel Y in SAT window 5[7:0]
0x70E8	AE25_SP_SAT_SUM3	R	0x00	[7:5] : Reserved [4:0] : Sum of Small Pixel Y in SAT window 5[28:24]
0x70E9	AE25_SP_SAT_SUM2	R	0x00	[7:0] : Sum of Small Pixel Y in SAT window 5[23:16]
0x70EA	AE25_SP_SAT_SUM1	R	0x00	[7:0] : Sum of Small Pixel Y in SAT window 5[15:8]
0x70EB	AE25_SP_SAT_SUM0	R	0x00	[7:0] : Sum of Small Pixel Y in SAT window 5[7:0]
0x7000	AE_WIN01_SEL	R/W	0x00	[7:4] : reserved [3] : AE window1 display enable (1:on) [2] : Luminance data out [1] : LP Luminance data out [0] : SP Luminance data out
0x7001	AE_WIN02_SEL	R/W	0x00	[7:4] : reserved [3] : AE window2 display enable (1:on) [2] : Luminance data out [1] : LP Luminance data out [0] : SP Luminance data out
0x7002	AE_WIN03_SEL	R/W	0x00	[7:4] : reserved [3] : AE window3 display enable (1:on) [2] : Luminance data out [1] : LP Luminance data out [0] : SP Luminance data out
0x7003	AE_WIN04_SEL	R/W	0x00	[7:4] : reserved [3] : AE window4 display enable (1:on) [2] : Luminance data out [1] : LP Luminance data out [0] : SP Luminance data out
0x7004	AE_WIN05_SEL	R/W	0x00	[7:4] : reserved [3] : AE window5 display enable (1:on) [2] : Luminance data out [1] : LP Luminance data out [0] : SP Luminance data out
0x7005	AE_WIN06_SEL	R/W	0x00	[7:4] : reserved [3] : AE window6 display enable (1:on) [2] : Luminance data out [1] : LP Luminance data out [0] : SP Luminance data out
0x7006	AE_WIN07_SEL	R/W	0x00	[7:4] : reserved [3] : AE window7 display enable (1:on) [2] : Luminance data out [1] : LP Luminance data out [0] : SP Luminance data out
0x7007	AE_WIN08_SEL	R/W	0x00	[7:4] : reserved [3] : AE window8 display enable (1:on) [2] : Luminance data out [1] : LP Luminance data out [0] : SP Luminance data out
0x7008	AE_WIN09_SEL	R/W	0x00	[7:4] : reserved [3] : AE window9 display enable (1:on) [2] : Luminance data out [1] : LP Luminance data out

				[0] : SP Luminance data out
0x7009	AE_WIN10_SEL	R/W	0x00	[7:4] : reserved [3] : AE window10 display enable (1:on) [2] : Luminance data out [1] : LP Luminance data out [0] : SP Luminance data out
0x700D	AE_SAT01_SEL	R/W	0x00	[7:4] : reserved [3] : SP saturation area selection 0 : LP saturation area 1 : SP whole area [2] : AE window21 sat.window1 win,rgn display enable [1] : AE window21 sat.window1 data sel (0:LP&SP,1:) [0] : AE window21 sat.window1 enable
AWB **(VSYNC SYNCHRONIZED)**				
0x7100	WB_BOUND_EN	R/W	0x00	[7] : R, G, B data selection (0 : , 1 : Interpolation) [6] : Using Long Pixel display enable(1:on) [5] : Using Short Pixel display enable(1:on) [4] : AWB window 5 display enable [3] : AWB window 4 display enable [2] : AWB window 3 display enable [1] : AWB window 2 display enable [0] : AWB window 1 display enable
0x7101	WB_WIN1_LR	R/W	0x1E	[7:4] : Left value of AWB window 1 [3:0] : Right value of AWB window 1
0x7102	WB_WIN1_UD	R/W	0x14	[7:4] : Up value of AWB window 1 [3:0] : Down value of AWB window 1
0x7103	WB_WIN2_LR	R/W	0x14	[7:4] : Left value of AWB window 2 [3:0] : Right value of AWB window 2
0x7104	WB_WIN2_UD	R/W	0x5A	[7:4] : Up value of AWB window 2 [3:0] : Down value of AWB window 2
0x7105	WB_WIN3_LR	R/W	0x5A	[7:4] : Left value of AWB window 3 [3:0] : Right value of AWB window 3
0x7106	WB_WIN3_UD	R/W	0x5A	[7:4] : Up value of AWB window 3 [3:0] : Down value of AWB window 3
0x7107	WB_WIN4_LR	R/W	0xBE	[7:4] : Left value of AWB window 4 [3:0] : Right value of AWB window 4
0x7108	WB_WIN4_UD	R/W	0x5A	[7:4] : Up value of AWB window 4 [3:0] : Down value of AWB window 4
0x7109	WB_WIN5_LR	R/W	0x1E	[7:4] : Left value of AWB window 5 [3:0] : Right value of AWB window 5
0x710A	WB_WIN5_UD	R/W	0xBE	[7:4] : Up value of AWB window 5 [3:0] : Down value of AWB window 5
0x710B	WB_LP_YUP	R/W	0xC0	[7:0] : Up Threshold of Long Pixel Y Data
0x710C	WB_LP_YDN	R/W	0x04	[7:0] : Down Threshold of Long Pixel Y Data
0x710D	WB_SP_YUP	R/W	0xC0	[7:0] : Up Threshold of Short Pixel Y Data
0x710E	WB_SP_YDN	R/W	0x04	[7:0] : Down Threshold of Short Pixel Y Data
0x710F	WB_LP_THR	R/W	0x08	[7] : Long pixel CbCr data disable [3:0] : CbCr Threshold of Long Pixel Data
0x7110	WB_SP_THR	R/W	0x08	[7] : Short pixel CbCr data disable [3:0] : CbCr Threshold of Short Pixel Data
0x7111	WB_LP_SAT_UP	R/W	0xC0	[7:0] : Up Threshold of Long Pixel RGB Data
0x7112	WB_LP_SAT_DN	R/W	0x04	[7:0] : Down Threshold of Long Pixel RGB Data
0x7113	WB_SP_SAT_UP	R/W	0xC0	[7:0] : Up Threshold of Short Pixel RGB Data
0x7114	WB_SP_SAT_DN	R/W	0x04	[7:0] : Down Threshold of Short Pixel RGB Data

0x7115	WB1_LP_RSUM3	R	0x00	[28:24] : Summation of Long Pixel Red data out in WB window 1
0x7116	WB1_LP_RSUM2	R	0x00	[23:16] : Summation of Long Pixel Red data out in WB window 1
0x7117	WB1_LP_RSUM1	R	0x00	[15:8] : Summation of Long Pixel Red data out in WB window 1
0x7118	WB1_LP_RSUM0	R	0x00	[7:0] : Summation of Long Pixel Red data out in WB window 1
0x7119	WB1_LP_GSUM3	R	0x00	[28:24] : Summation of Long Pixel Green data out in WB window 1
0x711A	WB1_LP_GSUM2	R	0x00	[23:16] : Summation of Long Pixel Green data out in WB window 1
0x711B	WB1_LP_GSUM1	R	0x00	[15:8] : Summation of Long Pixel Green data out in WB window 1
0x711C	WB1_LP_GSUM0	R	0x00	[7:0] : Summation of Long Pixel Green data out in WB window 1
0x711D	WB1_LP_BSUM3	R	0x00	[28:24] : Summation of Long Pixel Blue data out in WB window 1
0x711E	WB1_LP_BSUM2	R	0x00	[23:16] : Summation of Long Pixel Blue data out in WB window 1
0x711F	WB1_LP_BSUM1	R	0x00	[15:8] : Summation of Long Pixel Blue data out in WB window 1
0x7120	WB1_LP_BSUM0	R	0x00	[7:0] : Summation of Long Pixel Blue data out in WB window 1
0x7121	WB1_SP_RSUM3	R	0x00	[28:24] : Summation of Short Pixel Red data out in WB window 1
0x7122	WB1_SP_RSUM2	R	0x00	[23:16] : Summation of Short Pixel Red data out in WB window 1
0x7123	WB1_SP_RSUM1	R	0x00	[15:8] : Summation of Short Pixel Red data out in WB window 1
0x7124	WB1_SP_RSUM0	R	0x00	[7:0] : Summation of Short Pixel Red data out in WB window 1
0x7125	WB1_SP_GSUM3	R	0x00	[28:24] : Summation of Short Pixel Green data out in WB window 1
0x7126	WB1_SP_GSUM2	R	0x00	[23:16] : Summation of Short Pixel Green data out in WB window 1
0x7127	WB1_SP_GSUM1	R	0x00	[15:8] : Summation of Short Pixel Green data out in WB window 1
0x7128	WB1_SP_GSUM0	R	0x00	[7:0] : Summation of Short Pixel Green data out in WB window 1
0x7129	WB1_SP_BSUM3	R	0x00	[28:24] : Summation of Short Pixel Blue data out in WB window 1
0x712A	WB1_SP_BSUM2	R	0x00	[23:16] : Summation of Short Pixel Blue data out in WB window 1
0x712B	WB1_SP_BSUM1	R	0x00	[15:8] : Summation of Short Pixel Blue data out in WB window 1
0x712C	WB1_SP_BSUM0	R	0x00	[7:0] : Summation of Short Pixel Blue data out in WB window 1
0x712D	WB2_LP_RSUM3	R	0x00	[28:24] : Summation of Long Pixel Red data out in WB window 2
0x712E	WB2_LP_RSUM2	R	0x00	[23:16] : Summation of Long Pixel Red data out in WB window 2
0x712F	WB2_LP_RSUM1	R	0x00	[15:8] : Summation of Long Pixel Red data out in WB window 2
0x7130	WB2_LP_RSUM0	R	0x00	[7:0] : Summation of Long Pixel Red data out in WB window 2
0x7131	WB2_LP_GSUM3	R	0x00	[28:24] : Summation of Long Pixel Green data out in WB window 2
0x7132	WB2_LP_GSUM2	R	0x00	[23:16] : Summation of Long Pixel Green data out in WB window 2
0x7133	WB2_LP_GSUM1	R	0x00	[15:8] : Summation of Long Pixel Green data out in WB window 2
0x7134	WB2_LP_GSUM0	R	0x00	[7:0] : Summation of Long Pixel Green data out in WB window 2
0x7135	WB2_LP_BSUM3	R	0x00	[28:24] : Summation of Long Pixel Blue data out in WB window 2
0x7136	WB2_LP_BSUM2	R	0x00	[23:16] : Summation of Long Pixel Blue data out in WB window 2
0x7137	WB2_LP_BSUM1	R	0x00	[15:8] : Summation of Long Pixel Blue data out in WB window 2
0x7138	WB2_LP_BSUM0	R	0x00	[7:0] : Summation of Long Pixel Blue data out in WB window 2
0x7139	WB2_SP_RSUM3	R	0x00	[28:24] : Summation of Short Pixel Red data out in WB window 2
0x713A	WB2_SP_RSUM2	R	0x00	[23:16] : Summation of Short Pixel Red data out in WB window 2
0x713B	WB2_SP_RSUM1	R	0x00	[15:8] : Summation of Short Pixel Red data out in WB window 2
0x713C	WB2_SP_RSUM0	R	0x00	[7:0] : Summation of Short Pixel Red data out in WB window 2
0x713D	WB2_SP_GSUM3	R	0x00	[28:24] : Summation of Short Pixel Green data out in WB window 2
0x713E	WB2_SP_GSUM2	R	0x00	[23:16] : Summation of Short Pixel Green data out in WB window 2
0x713F	WB2_SP_GSUM1	R	0x00	[15:8] : Summation of Short Pixel Green data out in WB window 2
0x7140	WB2_SP_GSUM0	R	0x00	[7:0] : Summation of Short Pixel Green data out in WB window 2
0x7141	WB2_SP_BSUM3	R	0x00	[28:24] : Summation of Short Pixel Blue data out in WB window 2

0x7142	WB2_SP_BSUM2	R	0x00	[23:16] : Summation of Short Pixel Blue data out in WB window 2
0x7143	WB2_SP_BSUM1	R	0x00	[15:8] : Summation of Short Pixel Blue data out in WB window 2
0x7144	WB2_SP_BSUM0	R	0x00	[7:0] : Summation of Short Pixel Blue data out in WB window 2
0x7145	WB3_LP_RSUM3	R	0x00	[28:24] : Summation of Long Pixel Red data out in WB window 3
0x7146	WB3_LP_RSUM2	R	0x00	[23:16] : Summation of Long Pixel Red data out in WB window 3
0x7147	WB3_LP_RSUM1	R	0x00	[15:8] : Summation of Long Pixel Red data out in WB window 3
0x7148	WB3_LP_RSUM0	R	0x00	[7:0] : Summation of Long Pixel Red data out in WB window 3
0x7149	WB3_LP_GSUM3	R	0x00	[28:24] : Summation of Long Pixel Green data out in WB window 3
0x714A	WB3_LP_GSUM2	R	0x00	[23:16] : Summation of Long Pixel Green data out in WB window 3
0x714B	WB3_LP_GSUM1	R	0x00	[15:8] : Summation of Long Pixel Green data out in WB window 3
0x714C	WB3_LP_GSUM0	R	0x00	[7:0] : Summation of Long Pixel Green data out in WB window 3
0x714D	WB3_LP_BSUM3	R	0x00	[28:24] : Summation of Long Pixel Blue data out in WB window 3
0x714E	WB3_LP_BSUM2	R	0x00	[23:16] : Summation of Long Pixel Blue data out in WB window 3
0x714F	WB3_LP_BSUM1	R	0x00	[15:8] : Summation of Long Pixel Blue data out in WB window 3
0x7150	WB3_LP_BSUM0	R	0x00	[7:0] : Summation of Long Pixel Blue data out in WB window 3
0x7151	WB3_SP_RSUM3	R	0x00	[28:24] : Summation of Short Pixel Red data out in WB window 3
0x7152	WB3_SP_RSUM2	R	0x00	[23:16] : Summation of Short Pixel Red data out in WB window 3
0x7153	WB3_SP_RSUM1	R	0x00	[15:8] : Summation of Short Pixel Red data out in WB window 3
0x7154	WB3_SP_RSUM0	R	0x00	[7:0] : Summation of Short Pixel Red data out in WB window 3
0x7155	WB3_SP_GSUM3	R	0x00	[28:24] : Summation of Short Pixel Green data out in WB window 3
0x7156	WB3_SP_GSUM2	R	0x00	[23:16] : Summation of Short Pixel Green data out in WB window 3
0x7157	WB3_SP_GSUM1	R	0x00	[15:8] : Summation of Short Pixel Green data out in WB window 3
0x7158	WB3_SP_GSUM0	R	0x00	[7:0] : Summation of Short Pixel Green data out in WB window 3
0x7159	WB3_SP_BSUM3	R	0x00	[28:24] : Summation of Short Pixel Blue data out in WB window 3
0x715A	WB3_SP_BSUM2	R	0x00	[23:16] : Summation of Short Pixel Blue data out in WB window 3
0x715B	WB3_SP_BSUM1	R	0x00	[15:8] : Summation of Short Pixel Blue data out in WB window 3
0x715C	WB3_SP_BSUM0	R	0x00	[7:0] : Summation of Short Pixel Blue data out in WB window 3
0x715D	WB4_LP_RSUM3	R	0x00	[28:24] : Summation of Long Pixel Red data out in WB window 4
0x715E	WB4_LP_RSUM2	R	0x00	[23:16] : Summation of Long Pixel Red data out in WB window 4
0x715F	WB4_LP_RSUM1	R	0x00	[15:8] : Summation of Long Pixel Red data out in WB window 4
0x7160	WB4_LP_RSUM0	R	0x00	[7:0] : Summation of Long Pixel Red data out in WB window 4
0x7161	WB4_LP_GSUM3	R	0x00	[28:24] : Summation of Long Pixel Green data out in WB window 4
0x7162	WB4_LP_GSUM2	R	0x00	[23:16] : Summation of Long Pixel Green data out in WB window 4
0x7163	WB4_LP_GSUM1	R	0x00	[15:8] : Summation of Long Pixel Green data out in WB window 4
0x7164	WB4_LP_GSUM0	R	0x00	[7:0] : Summation of Long Pixel Green data out in WB window 4
0x7165	WB4_LP_BSUM3	R	0x00	[28:24] : Summation of Long Pixel Blue data out in WB window 4
0x7166	WB4_LP_BSUM2	R	0x00	[23:16] : Summation of Long Pixel Blue data out in WB window 4
0x7167	WB4_LP_BSUM1	R	0x00	[15:8] : Summation of Long Pixel Blue data out in WB window 4
0x7168	WB4_LP_BSUM0	R	0x00	[7:0] : Summation of Long Pixel Blue data out in WB window 4
0x7169	WB4_SP_RSUM3	R	0x00	[28:24] : Summation of Short Pixel Red data out in WB window 4
0x716A	WB4_SP_RSUM2	R	0x00	[23:16] : Summation of Short Pixel Red data out in WB window 4
0x716B	WB4_SP_RSUM1	R	0x00	[15:8] : Summation of Short Pixel Red data out in WB window 4
0x716C	WB4_SP_RSUM0	R	0x00	[7:0] : Summation of Short Pixel Red data out in WB window 4
0x716D	WB4_SP_GSUM3	R	0x00	[28:24] : Summation of Short Pixel Green data out in WB window 4
0x716E	WB4_SP_GSUM2	R	0x00	[23:16] : Summation of Short Pixel Green data out in WB window 4

0x716F	WB4_SP_GSUM1	R	0x00	[15:8] : Summation of Short Pixel Green data out in WB window 4
0x7170	WB4_SP_GSUM0	R	0x00	[7:0] : Summation of Short Pixel Green data out in WB window 4
0x7171	WB4_SP_BSUM3	R	0x00	[28:24] : Summation of Short Pixel Blue data out in WB window 4
0x7172	WB4_SP_BSUM2	R	0x00	[23:16] : Summation of Short Pixel Blue data out in WB window 4
0x7173	WB4_SP_BSUM1	R	0x00	[15:8] : Summation of Short Pixel Blue data out in WB window 4
0x7174	WB4_SP_BSUM0	R	0x00	[7:0] : Summation of Short Pixel Blue data out in WB window 4
0x7175	WB5_LP_RSUM3	R	0x00	[28:24] : Summation of Long Pixel Red data out in WB window 5
0x7176	WB5_LP_RSUM2	R	0x00	[23:16] : Summation of Long Pixel Red data out in WB window 5
0x7177	WB5_LP_RSUM1	R	0x00	[15:8] : Summation of Long Pixel Red data out in WB window 5
0x7178	WB5_LP_RSUM0	R	0x00	[7:0] : Summation of Long Pixel Red data out in WB window 5
0x7179	WB5_LP_GSUM3	R	0x00	[28:24] : Summation of Long Pixel Green data out in WB window 5
0x717A	WB5_LP_GSUM2	R	0x00	[23:16] : Summation of Long Pixel Green data out in WB window 5
0x717B	WB5_LP_GSUM1	R	0x00	[15:8] : Summation of Long Pixel Green data out in WB window 5
0x717C	WB5_LP_GSUM0	R	0x00	[7:0] : Summation of Long Pixel Green data out in WB window 5
0x717D	WB5_LP_BSUM3	R	0x00	[28:24] : Summation of Long Pixel Blue data out in WB window 5
0x717E	WB5_LP_BSUM2	R	0x00	[23:16] : Summation of Long Pixel Blue data out in WB window 5
0x717F	WB5_LP_BSUM1	R	0x00	[15:8] : Summation of Long Pixel Blue data out in WB window 5
0x7180	WB5_LP_BSUM0	R	0x00	[7:0] : Summation of Long Pixel Blue data out in WB window 5
0x7181	WB5_SP_RSUM3	R	0x00	[28:24] : Summation of Short Pixel Red data out in WB window 5
0x7182	WB5_SP_RSUM2	R	0x00	[23:16] : Summation of Short Pixel Red data out in WB window 5
0x7183	WB5_SP_RSUM1	R	0x00	[15:8] : Summation of Short Pixel Red data out in WB window 5
0x7184	WB5_SP_RSUM0	R	0x00	[7:0] : Summation of Short Pixel Red data out in WB window 5
0x7185	WB5_SP_GSUM3	R	0x00	[28:24] : Summation of Short Pixel Green data out in WB window 5
0x7186	WB5_SP_GSUM2	R	0x00	[23:16] : Summation of Short Pixel Green data out in WB window 5
0x7187	WB5_SP_GSUM1	R	0x00	[15:8] : Summation of Short Pixel Green data out in WB window 5
0x7188	WB5_SP_GSUM0	R	0x00	[7:0] : Summation of Short Pixel Green data out in WB window 5
0x7189	WB5_SP_BSUM3	R	0x00	[28:24] : Summation of Short Pixel Blue data out in WB window 5
0x718A	WB5_SP_BSUM2	R	0x00	[23:16] : Summation of Short Pixel Blue data out in WB window 5
0x718B	WB5_SP_BSUM1	R	0x00	[15:8] : Summation of Short Pixel Blue data out in WB window 5
0x718C	WB5_SP_BSUM0	R	0x00	[7:0] : Summation of Short Pixel Blue data out in WB window 5
0x718D	WB1_LP_YCNT2	R	0x00	[18:16] : Count of Long Pixel Y data in WB window 1
0x718E	WB1_LP_YCNT1	R	0x00	[15:8] : Count of Long Pixel Y data in WB window 1
0x718F	WB1_LP_YCNT0	R	0x00	[7:0] : Count of Long Pixel Y data in WB window 1
0x7190	WB1_SP_YCNT2	R	0x00	[18:16] : Count of Short Pixel Y data in WB window 1
0x7191	WB1_SP_YCNT1	R	0x00	[15:8] : Count of Short Pixel Y data in WB window 1
0x7192	WB1_SP_YCNT0	R	0x00	[7:0] : Count of Short Pixel Y data in WB window 1
0x7193	WB2_LP_YCNT2	R	0x00	[18:16] : Count of Long Pixel Y data in WB window 2
0x7194	WB2_LP_YCNT1	R	0x00	[15:8] : Count of Long Pixel Y data in WB window 2
0x7195	WB2_LP_YCNT0	R	0x00	[7:0] : Count of Long Pixel Y data in WB window 2
0x7196	WB2_SP_YCNT2	R	0x00	[18:16] : Count of Short Pixel Y data in WB window 2
0x7197	WB2_SP_YCNT1	R	0x00	[15:8] : Count of Short Pixel Y data in WB window 2
0x7198	WB2_SP_YCNT0	R	0x00	[7:0] : Count of Short Pixel Y data in WB window 2
0x7199	WB3_LP_YCNT2	R	0x00	[18:16] : Count of Long Pixel Y data in WB window 3
0x719A	WB3_LP_YCNT1	R	0x00	[15:8] : Count of Long Pixel Y data in WB window 3
0x719B	WB3_LP_YCNT0	R	0x00	[7:0] : Count of Long Pixel Y data in WB window 3

0x719C	WB3_SP_YCNT2	R	0x00	[18:16] : Count of Short Pixel Y data in WB window 3
0x719D	WB3_SP_YCNT1	R	0x00	[15:8] : Count of Short Pixel Y data in WB window 3
0x719E	WB3_SP_YCNT0	R	0x00	[7:0] : Count of Short Pixel Y data in WB window 3
0x719F	WB4_LP_YCNT2	R	0x00	[18:16] : Count of Long Pixel Y data in WB window 4
0x71A0	WB4_LP_YCNT1	R	0x00	[15:8] : Count of Long Pixel Y data in WB window 4
0x71A1	WB4_LP_YCNT0	R	0x00	[7:0] : Count of Long Pixel Y data in WB window 4
0x71A2	WB4_SP_YCNT2	R	0x00	[18:16] : Count of Short Pixel Y data in WB window 4
0x71A3	WB4_SP_YCNT1	R	0x00	[15:8] : Count of Short Pixel Y data in WB window 4
0x71A4	WB4_SP_YCNT0	R	0x00	[7:0] : Count of Short Pixel Y data in WB window 4
0x71A5	WB5_LP_YCNT2	R	0x00	[18:16] : Count of Long Pixel Y data in WB window 5
0x71A6	WB5_LP_YCNT1	R	0x00	[15:8] : Count of Long Pixel Y data in WB window 5
0x71A7	WB5_LP_YCNT0	R	0x00	[7:0] : Count of Long Pixel Y data in WB window 5
0x71A8	WB5_SP_YCNT2	R	0x00	[18:16] : Count of Short Pixel Y data in WB window 5
0x71A9	WB5_SP_YCNT1	R	0x00	[15:8] : Count of Short Pixel Y data in WB window 5
0x71AA	WB5_SP_YCNT0	R	0x00	[7:0] : Count of Short Pixel Y data in WB window 5
0x71AB	WB_LP_PSUM3	R	0x00	[26:24] : Summation of Long P Pixel data out;
0x71AC	WB_LP_PSUM2	R	0x00	[23:16] : Summation of Long P Pixel data out;
0x71AD	WB_LP_PSUM1	R	0x00	[15:8] : Summation of Long P Pixel data out;
0x71AE	WB_LP_PSUM0	R	0x00	[7:0] : Summation of Long P Pixel data out;
0x71AF	WB_SP_PSUM3	R	0x00	[26:24] : Summation of Short P Pixel data out;
0x71B0	WB_SP_PSUM2	R	0x00	[23:16] : Summation of Short P Pixel data out;
0x71B1	WB_SP_PSUM1	R	0x00	[15:8] : Summation of Short P Pixel data out;
0x71B2	WB_SP_PSUM0	R	0x00	[7:0] : Summation of Short P Pixel data out;
FLICK	**(VSYNC SYNCHRONIZED)**			
0x7200	FLICK_CONTROL	R/W	0x00	[7:6] : reserved [5:4] : selection Y 00 : short 01 : long 10 : [3:2] : data bit selection 00 : y_data[7:0] 01 : y_data[8:1] 10 : y_data[9:2] [1] : zone display enable [0] : line sum enable 0 : disable 1 : enable
0x7201	FLICK_HSCALE	R/W	0xA0	[7:0] : hscale
0x7202	FLICK_WIN_UP	R/W	0x10	[7:0] : x position
0x7203	FLICK_WIN_LFT	R/W	0x10	[7:0] : y position
0x7204	FLICK_LENGTH	R/W	0x00	[7:0] : window length
0x7205	FLICK_HEIGHT	R/W	0x80	[7:0] : window height
0x7206	FLICK_HIS	R/W	0x10	[7] : reserved [6] : hi_height [5:4] : hi_length [3] : reserved [2] : hi_win_y [1:0] : hi_win_x
0x7207	FLICK_SUM_DATA0	R	0x00	[7:0]: sum data0
0x7208	FLICK_SUM_DATA1	R	0x00	[7:0]: sum data1
0x7209	FLICK_SUM_DATA2	R	0x00	[7:0]: sum data2

0x720A	FLICK_SUM_DATA3	R	0x00	[7:0]: sum data3
0x720B	FLICK_SUM_DATA4	R	0x00	[7:0]: sum data4
0x720C	FLICK_SUM_DATA5	R	0x00	[7:0]: sum data5
0x720D	FLICK_SUM_DATA6	R	0x00	[7:0]: sum data6
0x720E	FLICK_SUM_DATA7	R	0x00	[7:0]: sum data7
0x720F	FLICK_SUM_DATA8	R	0x00	[7:0]: sum data8
0x7210	FLICK_SUM_DATA9	R	0x00	[7:0]: sum data9
0x7211	FLICK_SUM_DATA10	R	0x00	[7:0]: sum data10
0x7212	FLICK_SUM_DATA11	R	0x00	[7:0]: sum data11
0x7213	FLICK_SUM_DATA12	R	0x00	[7:0]: sum data12
0x7214	FLICK_SUM_DATA13	R	0x00	[7:0]: sum data13
0x7215	FLICK_SUM_DATA14	R	0x00	[7:0]: sum data14
0x7216	FLICK_SUM_DATA15	R	0x00	[7:0]: sum data15
0x7217	FLICK_SUM_DATA16	R	0x00	[7:0]: sum data16
0x7218	FLICK_SUM_DATA17	R	0x00	[7:0]: sum data17
0x7219	FLICK_SUM_DATA18	R	0x00	[7:0]: sum data18
0x721A	FLICK_SUM_DATA19	R	0x00	[7:0]: sum data19
0x721B	FLICK_SUM_DATA20	R	0x00	[7:0]: sum data20
0x721C	FLICK_SUM_DATA21	R	0x00	[7:0]: sum data21
0x721D	FLICK_SUM_DATA22	R	0x00	[7:0]: sum data22
0x721E	FLICK_SUM_DATA23	R	0x00	[7:0]: sum data23
0x721F	FLICK_SUM_DATA24	R	0x00	[7:0]: sum data24
0x7220	FLICK_SUM_DATA25	R	0x00	[7:0]: sum data25
0x7221	FLICK_SUM_DATA26	R	0x00	[7:0]: sum data26
0x7222	FLICK_SUM_DATA27	R	0x00	[7:0]: sum data27
0x7223	FLICK_SUM_DATA28	R	0x00	[7:0]: sum data28
0x7224	FLICK_SUM_DATA29	R	0x00	[7:0]: sum data29
0x7225	FLICK_SUM_DATA30	R	0x00	[7:0]: sum data30
0x7226	FLICK_SUM_DATA31	R	0x00	[7:0]: sum data31

11.10. Global ADC

ADDRESS (HEX)	REGISTER NAME	R/W	DEFAULT (HEX)	DESCRIPTION
GADC				
0x8000	GADC_CON	R/W	0x08	[7] : reserved [6] : GADC current control 2 [5] : GADC current control 1 [4] : GADC current control 0 [3] : GADC power down 0 : active 1 : power down [2] : GADC channel selection 0 : channel 0 1 : channel 1 [1] : GADC start control [0] : GADC end flag
0x8001	GADC_DATA	R	0x00	[7:0] : GADC data

12. Spectral Response Of Color Filter

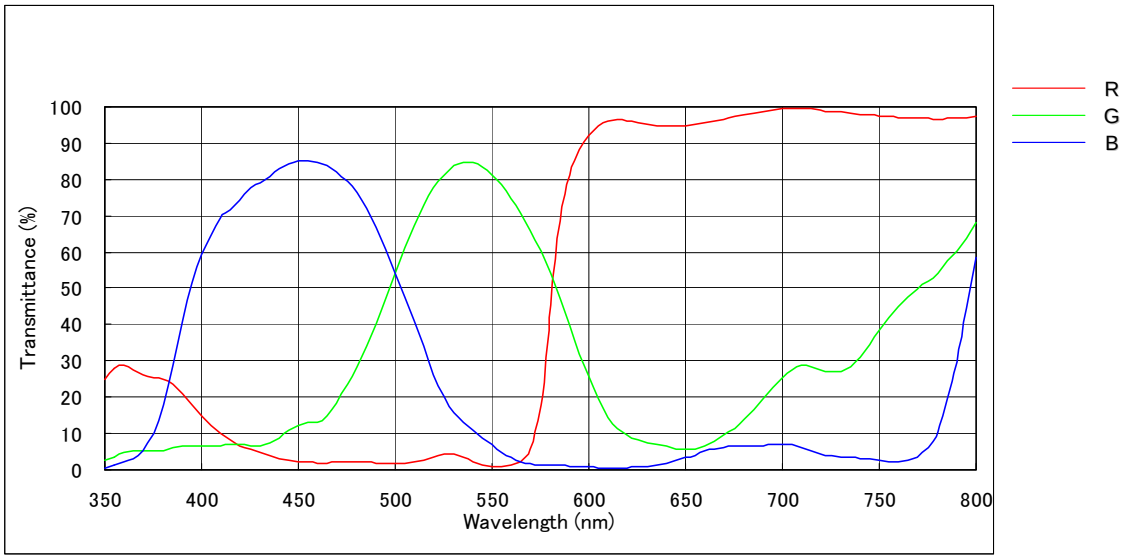


Figure 12-1 spectral response of color filter

13. Electrical Characteristics

Symbol	Parameter	Rating	Units
VDDIO	Supply Voltage for IO	4	V
VDDP	Supply Voltage for Analog	4	V
VDDD		4	V
VDDA		4	V
VDDN		4	V
VDD	Supply Voltage for Digital Core	2.4	V
T	Storage Temperature	-50 to 125	℃

Table 13-1 Absolute Maximum Ratings

Symbol	Parameter	Rating			Units
		MIN	TYP	MAX	
VDDIO	Supply Voltage for IO	2.97	3.3	3.63	V
VDDP	Supply Voltage for Analog	2.97	3.3	3.63	V
VDDD		2.97	3.3	3.63	V
VDDA		2.97	3.3	3.63	V
VDDN		2.97	3.3	3.63	V
VDD	Supply Voltage for Digital Core	1.35	1.5	1.65	V
T_A	Commercial Temperature Range	0 to 70			℃
	Industrial Temperature Range	-40 to 105			

Table 13-2 Recommended Operating Condition

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
IDDS	Quiescent Current	VDDIO = 3.3V VDD = 1.5V		[T.B.D]		mW
IDD	Dynamic IDD	VDDIO = 3.3V VDD = 1.5V EXT_CLK = 27MHz		[T.B.D]		mW

Table 13-3 Power Consumption

Items	VDDIO = 3.3V±10%			Unit
	MIN	TYP	MAX	
VIL			0.35*VDDIO	V
VIH	0.7*VDDIO			
IIH	-5		5	μA
IIL	-5		5	
VOL (PAD)			0.4	V
VOH (PAD)	VDDIO-0.4			
Schmitt trigger L to H Threshold	1.74		1.92	V
Schmitt trigger H to L Threshold	1.26		1.46	V

Table 13-4 DC Characteristics

14. Pin Information

Figure 14-1 and Figure 14-2 are pin maps when packaging CP8108 in 40 pin CLCC. Depending on the package kind, pin maps may change.

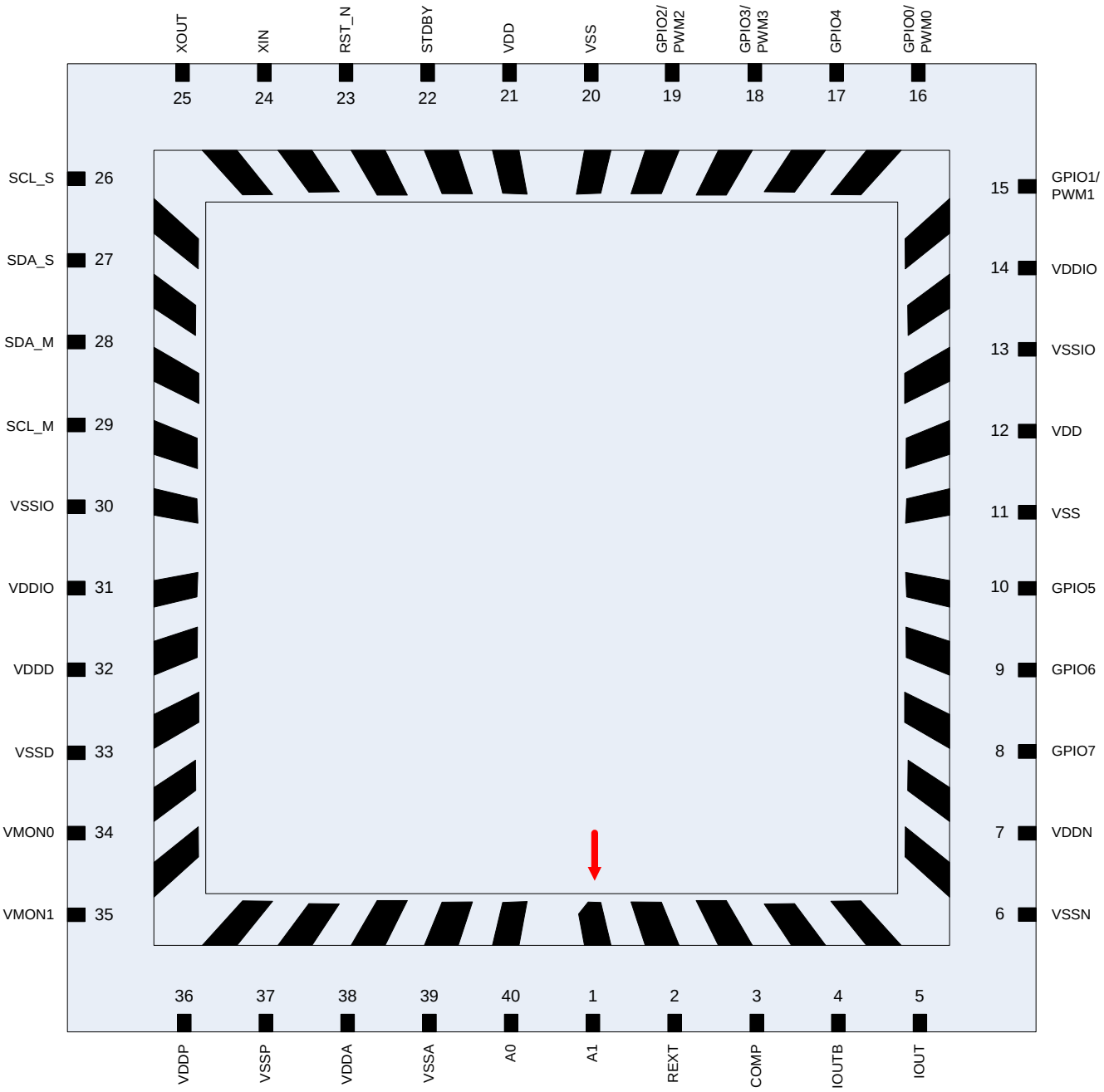


Figure 14-1 40 Pin CLCC PKG Pin Map(Analog)

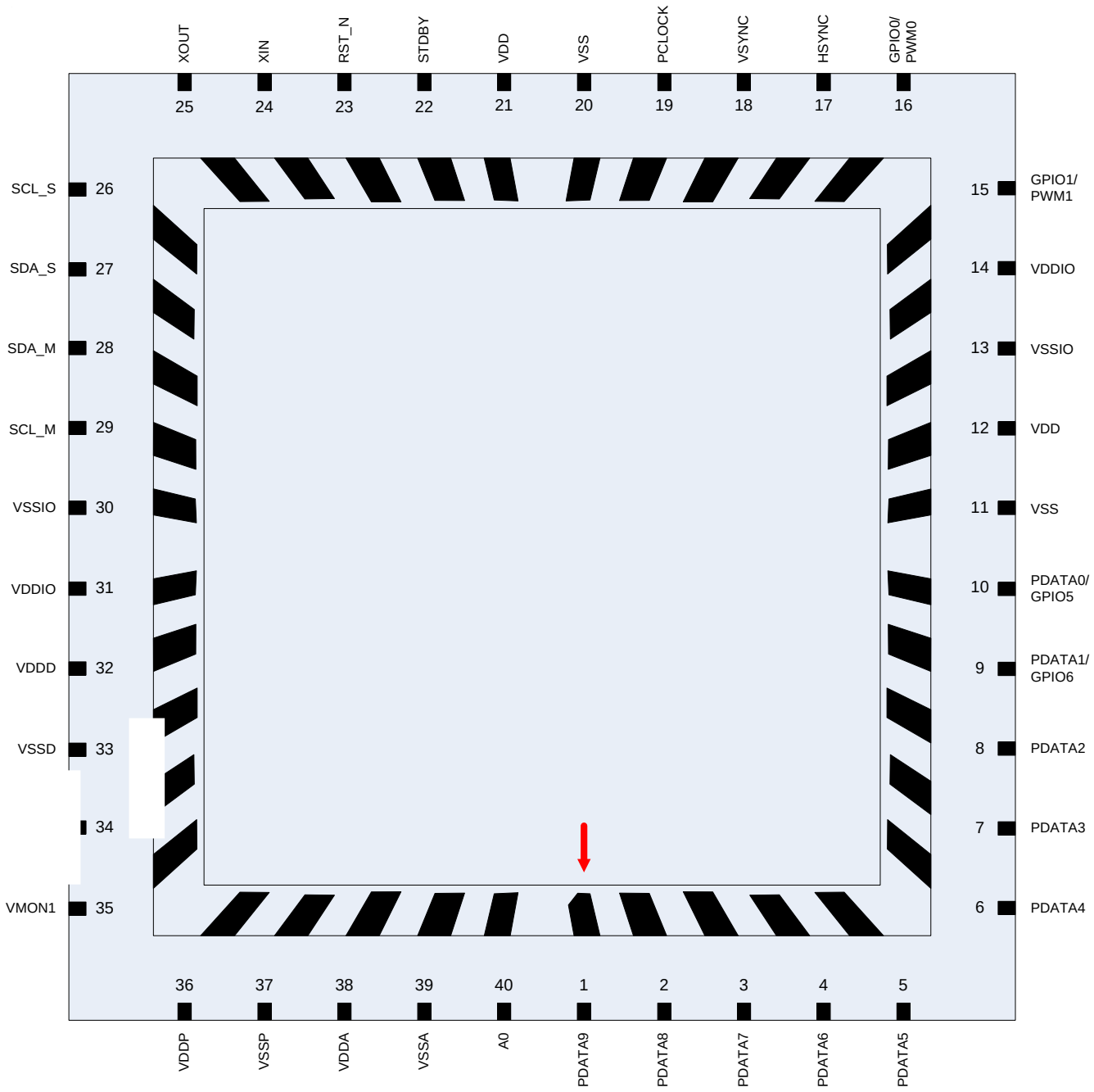


Figure 14-2 40 Pin CLCC PKG Pin Map(Digital)

Loc	PIN Num.	PIN Name	I/O	Description	Note
BOTTOM	1	A1	A	External ADC Input Channel 1	Analog PAD
	2	REXT	A	External Reference Resistor	Analog PAD
	3	COMP	A	Compensation Pin	Analog PAD
	4	IOUTB	A	10bit DAC Negative Output	Analog PAD
	5	IOUT	A	10bit DAC Positive Output	Analog PAD
RIGHT	6	VSSN	G	Analog Ground for 10bit DAC	
	7	VDDN	P	Analog Power for 10bit DAC	
	8	PDATA2/ GPIO7	O	Pixel Data[2] output port/ GPIO 7 port	Default PDATA2
	9	PDATA1/ GPIO6	O	Pixel Data[1] output port/ GPIO 6 port	Default PDATA1
	10	PDATA0/ GPIO5	O	Pixel Data[0] output port/ GPIO 5 port	Default PDATA0
	11	VSS	G	Digital ground for core	
	12	VDD	P	Digital power for core	
	13	VSSIO	G	Digital ground for IO	
	14	VDDIO	P	Digital power for IO	
	15	GPIO1/ PWM1	O	GPIO 1 port/ PWM1 port	Default GPIO 1
TOP	16	GPIO0/ PWM0	O	GPIO 0 port/ PWM0 port	Default GPIO 0
	17	HSYNC/ GPIO4	O	HSYNC output port/ GPIO4 port	Default HSYNC
	18	VSYNC/ GPIO3/ PWM3/	O	VSYNC output port/ GPIO3 port/ PWM3 port	Default VSYNC
	19	PCLOCK/ GPIO2/ PWM2	O	PCLOCK output port/ GPIO2 port/ PWM2 port	Default PCLOCK
	20	VSS	G	Digital ground for core	
	21	VDD	P	Digital power for core	
	22	STDBY	I	Standby input port	
	23	RST_N	I	Reset input port	
	24	XI	I	External Clock Input port	
	25	XO	O	External Clock Output port	
LEFT	26	SCL_S	I	Slave Serial Clock port	
	27	SDA_S	B	Slave Serial Data port	
	28	SDA_M	B	Master Serial Data port	
	29	SCL_M	O	Master Serial Clock port	
	30	VSSIO	G	Digital ground for IO	
	31	VDDIO	P	Digital power for IO	
	32	VDDD	P	Analog Power for Digital	
	33	VSSD	G	Analog Ground for Digital	
	34	–			
	35	–			
BOTT	36	VDDP	P	Analog Power for Pixel	
	37	VSSP	G	Analog Ground for Pixel	
	38	VDDA	P	Analog Power for Core	

OM	39	VSSA	G	Analog Ground for Core	
	40	A0	A	External ADC Input Channel 0	Analog PAD

Table 14-1 Pin Information(Analog)

Loc	PIN Num.	PIN Name	I/O	Description	Note
BOTTOM	1	PDATA9	O	Pixel Data[9] output port	
	2	PDATA8	O	Pixel Data[8] output port	
	3	PDATA7	O	Pixel Data[7] output port	
	4	PDATA6	O	Pixel Data[6] output port	
	5	PDATA5	O	Pixel Data[5] output port	
RIGHT	6	PDATA4	O	Pixel Data[4] output port	
	7	PDATA3	O	Pixel Data[3] output port	
	8	PDATA2/ GPIO7	O	Pixel Data[2] output port/ GPIO 7 port	Default PDATA2
	9	PDATA1/ GPIO6	O	Pixel Data[1] output port/ GPIO 6 port	Default PDATA1
	10	PDATA0/ GPIO5	O	Pixel Data[0] output port/ GPIO 5 port	Default PDATA0
	11	VSS	G	Digital ground for core	
	12	VDD	P	Digital power for core	
	13	VSSIO	G	Digital ground for IO	
	14	VDDIO	P	Digital power for IO	
	15	GPIO1/ PWM1	O	GPIO 1 port/ PWM1 port	Default GPIO 1
TOP	16	GPIO0/ PWM0	O	GPIO 0 port/ PWM0 port	Default GPIO 0
	17	HSYNC/ GPIO4	O	HSYNC output port/ GPIO4 port	Default HSYNC
	18	VSYNC/ GPIO3/ PWM3/	O	VSYNC output port/ GPIO3 port/ PWM3 port	Default VSYNC
	19	PCLOCK/ GPIO2/ PWM2	O	PCLOCK output port/ GPIO2 port/ PWM2 port	Default PCLOCK
	20	VSS	G	Digital ground for core	
	21	VDD	P	Digital power for core	
	22	STDBY	I	Standby input port	
	23	RST_N	I	Reset input port	
	24	XI	I	External Clock Input port	
	25	XO	O	External Clock Output port	
LEFT	26	SCL_S	I	Slave Serial Clock port	
	27	SDA_S	B	Slave Serial Data port	
	28	SDA_M	B	Master Serial Data port	
	29	SCL_M	O	Master Serial Clock port	
	30	VSSIO	G	Digital ground for IO	
	31	VDDIO	P	Digital power for IO	
	32	VDDD	P	Analog Power for Digital	
	33	VSSD	G	Analog Ground for Digital	

	34	–			
	35	–			
BOTTOM	36	VDDP	P	Analog Power for Pixel	
	37	VSSP	G	Analog Ground for Pixel	
	38	VDDA	P	Analog Power for Core	
	39	VSSA	G	Analog Ground for Core	
	40	A0	A	External ADC Input Channel 0	Analog PAD

Table 14-2 Pin Information(Digital)

15. Typical Circuit Configuration

Figure 15-1 and Figure 15-2 are examples of circuit diagrams when CP8108 is packaged in 40 pin CLCC. Depending on the package kind, circuit diagrams may change.

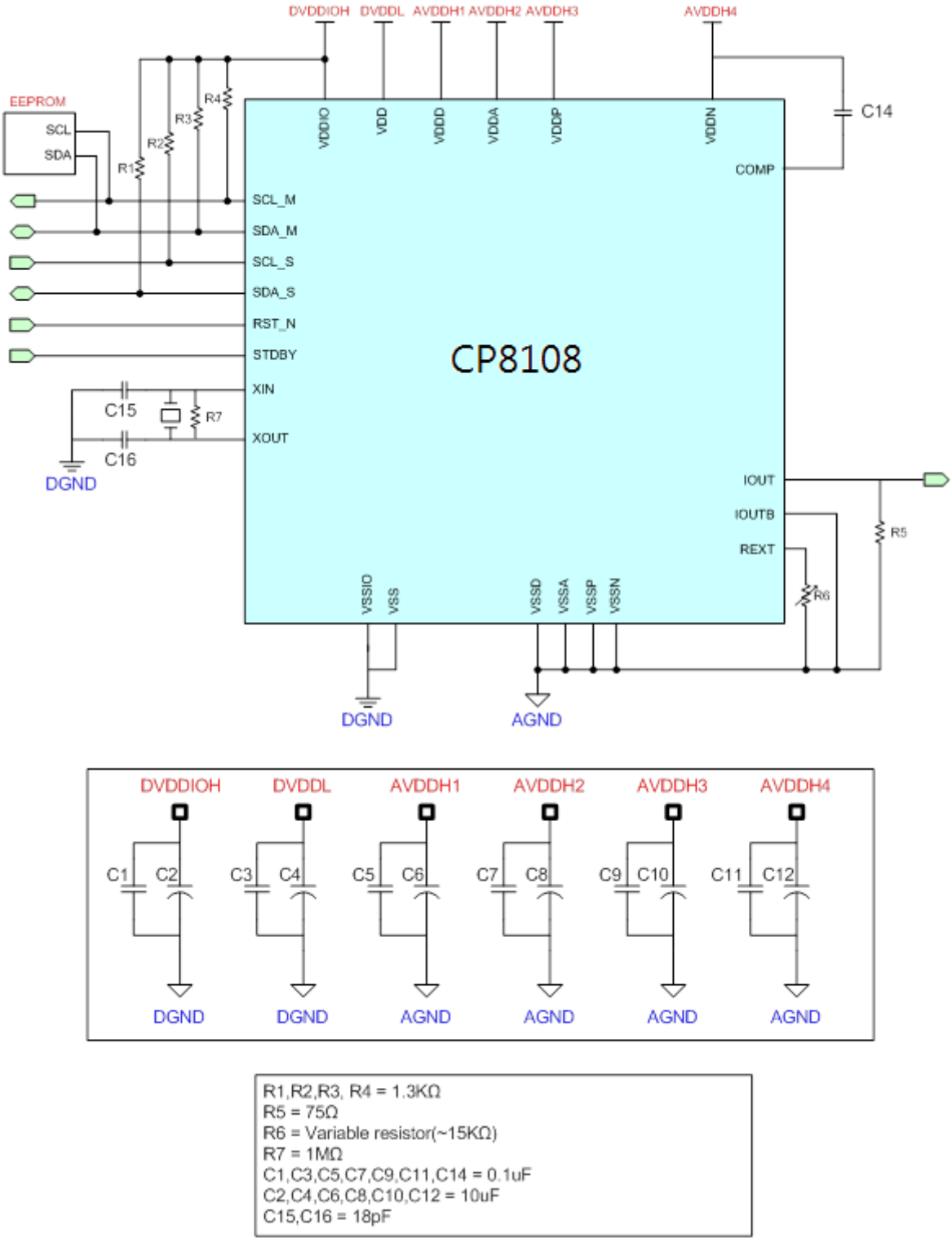


Figure 15-1 Typical Circuit Configuration(Analog)

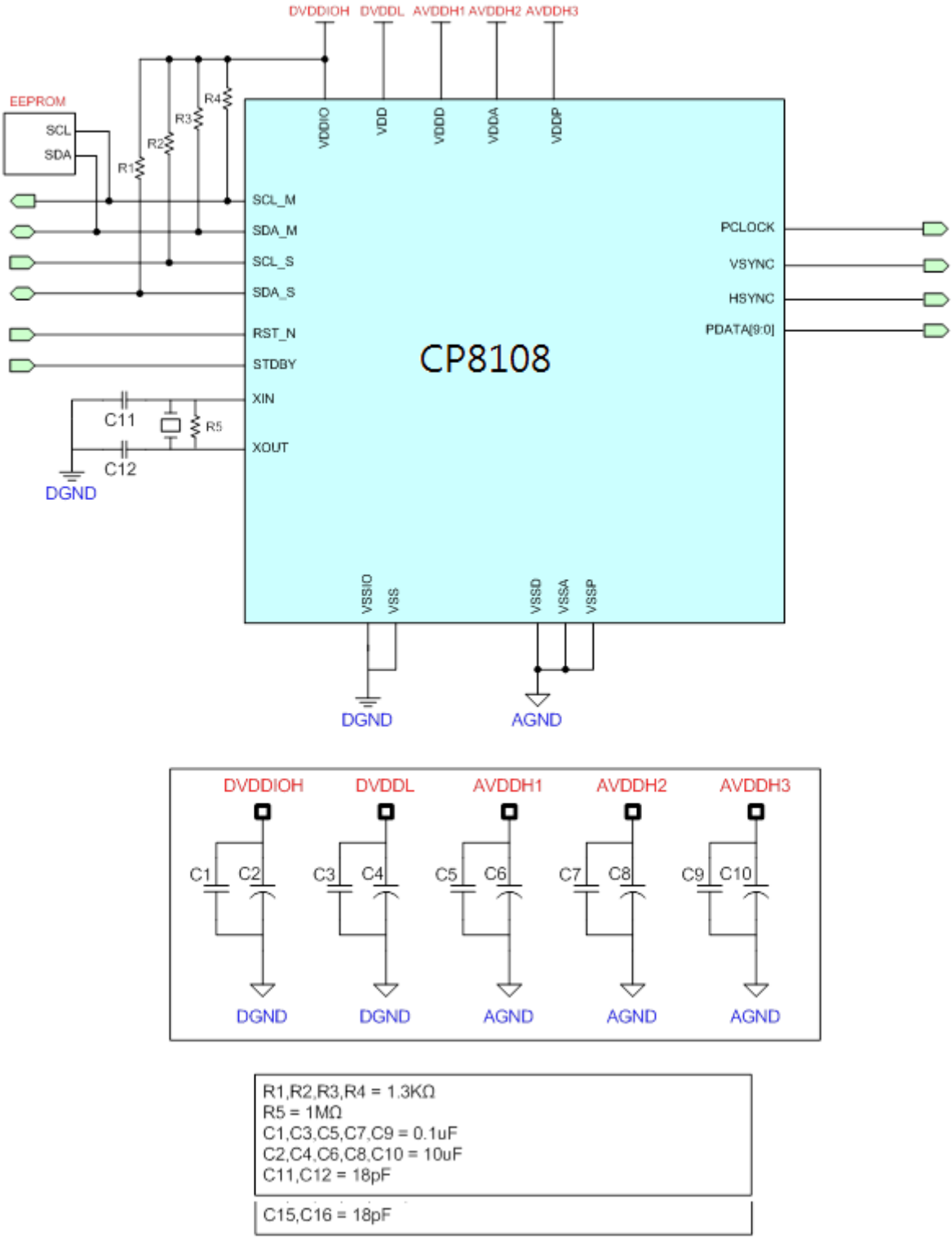
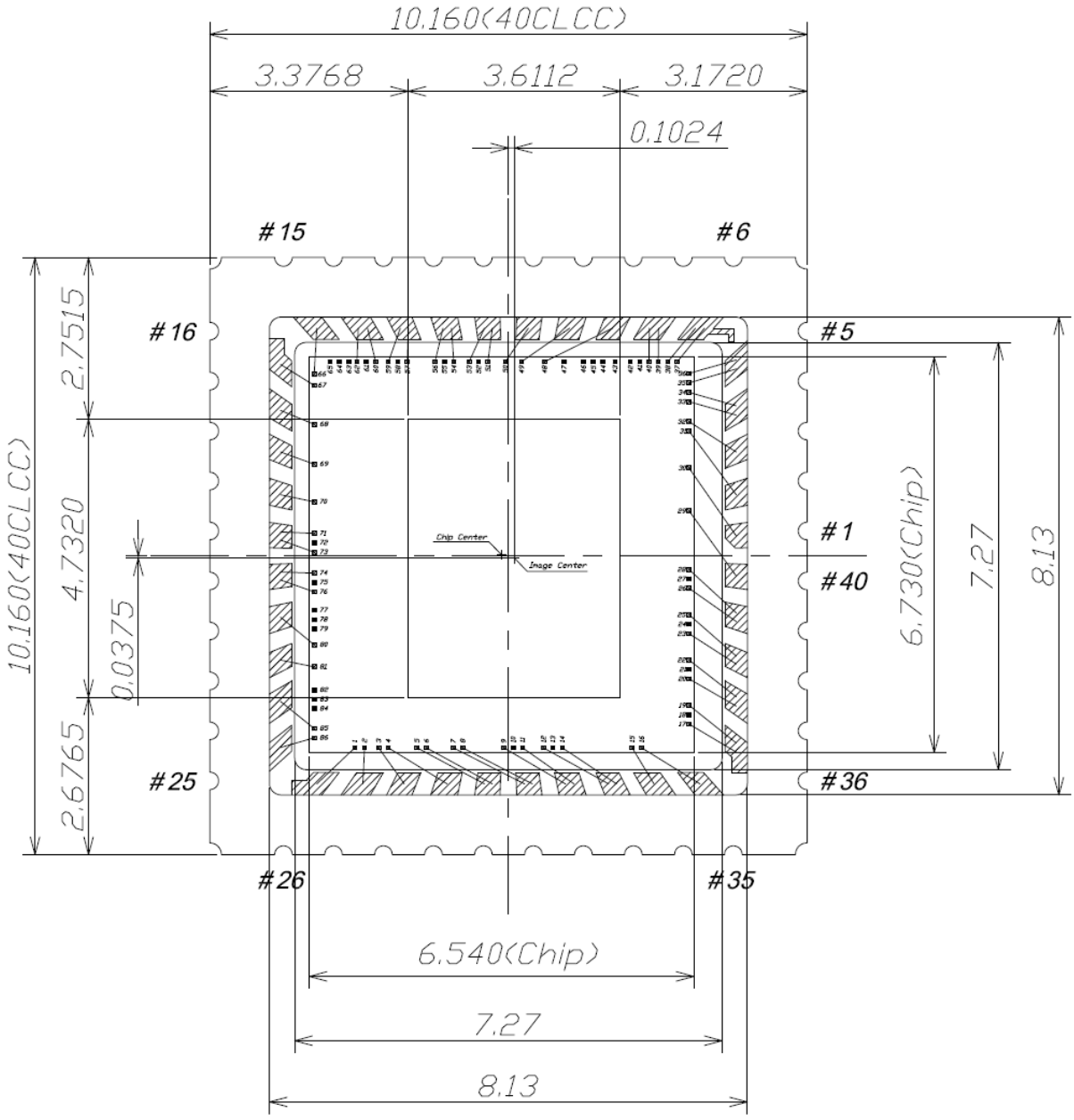


Figure 15-2 Typical Circuit Configuration(Digital)

16. PKG Dimension



PKG TYPE	40CLCC	CHIP SIZE(mm) (W/O S/L)	6.540 * 6.730
PKG SIZE(mm)	10.16 * 10.16	Image Area	3.6112 * 4.7320
PAD OPEN(mm)	0.066 X 0.066	Chip Thickness	-

Designed By	'13.01.09. K.D.KANG	Approved By	
Checked By		Confirmed By (PKG Tech. Team)	

TOP VIEW

Figure 16-1 40 Pin CLCC PKG Image Center

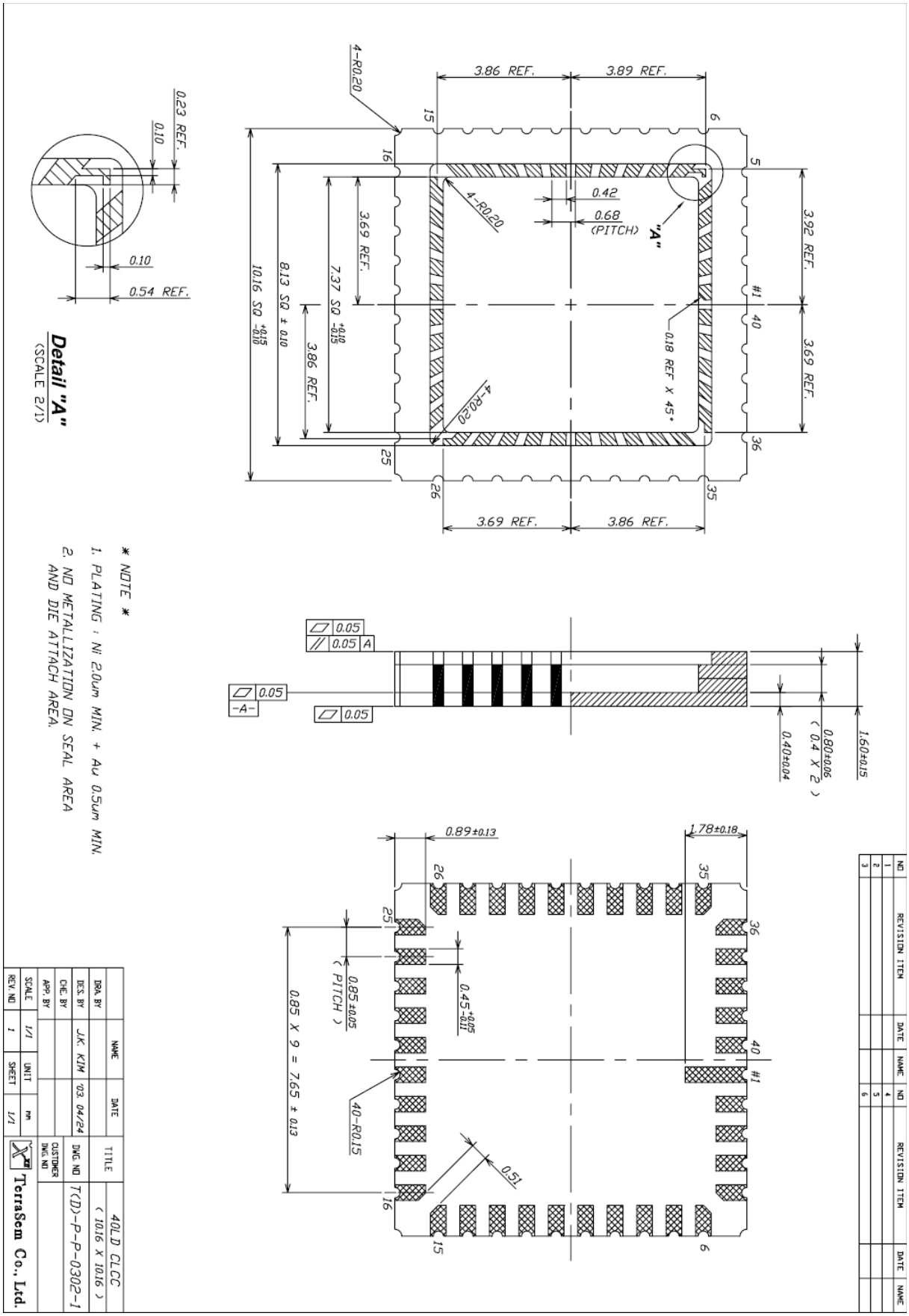


Figure 16-2 40 Pin CLCC PKG Dimension