CP8210(Wideye™)
Datasheet

1M WDR CMOS IMAGE SENSOR

Version 0.47

Document No. : CP-M-8210

ClairPixel Co., Ltd.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

How to reach us: #1206, U-Space 1-B, 670 Sampyeong-dong, Bundang-gu, Seongnam-si, Gyeonggi-do, 463-400, Rep. of Korea

82-31-628-4186

HOME PAGE: http://www.clairpixel.com

Revision History

Issue	Rev No.	Originator	Details of Change	Date
1	0.1	limks	Initial Version	2015-04-14
2	0.2	limks	Formatter Description Modified	2015-04-28
3	0.3	moonjj	Active Pixel Area Modified	2015-05-20
4	0.4	limks	Specification Description Modified	2015-05-21

Table of Contents

List of Figures

List of Tables

1/3-Inch, CMOS 1M WDR Image Sensor

1. Specification

DESCRIPSION

CP8210 is a single-chip video/image camera sensor that uses a unique WideyeTM technology developed by Clairepixel to allow video capture in extremely diverse lighting conditions, hence making it suitable for auto vehicle cameras and security systems. CP8210 is set up with a 1280x720 image array, outputs up to 60 frames (1280x720) per second, and supports various forms of digital output format. CP8210 has various camera control functions, and can be programmed through a two-wire serial interface.

PARAMETER		TYPICAL VALUE
Optical Dimension	Optical Format	1/3 inch
	Pixel Size	4.0 um X 4.0 um
	Effective Resolution	1280(H) X 720(V)
	Active Pixel Area	5.120 mm(H) X 2.880 mm(V)
Digital Output		10bit, 8bit RGB Bayer, YCbCr422, RGB565/555 SMPTE296M
Input Clock Frequency		27MHz
Maximum Frame Rate		1280x720, 60fps(Bayer)@74.25MHz 1280x720, 30fps(YCbCr)@74.25MHz
Shutter Type		Electronic Rolling Shutter
Sensitivity		3.2V / lux-sec
Dynamic Range		120 dB
SNR		39 dB
Max. Programmable Gain		analog (x64), digital (x32)
Supply Voltage	Pixel	3.3V ± 10%
	Analog	3.3V ± 10%
	Digital	1.5V ± 10%
	I/O	3.3V ± 10%
Power Consumption	Active	[T.B.D]
	Standby	[T.B.D]
Operating Temperature		-40°C ~ 85°C
Package Type		CLCC or PLCC

FEATURES

- ClairPixel's Wideye™, Wide Dynamic Range technology
- System-on-a-chip(SOC)-completely integrated camera system
- Integrated microcontroller for flexibility
- 8-,10-bit parallel digital output
- Bayer Noise Reduction, Lens Shading Compensation, Defective Pixel Compensation
- Color Correction, Gamma Correction,
- Hue/Saturation, Contrast/Brightness Control
- Edge Enhancement
- Parking Guide, OSD, Privacy Zone Mask,
- Automatic features :
  Auto Exposure, Auto White Balance,
  Anti-Flicker, Black Level Calibration
- 2 channel(Master, Slave) Two-wire serial interface

APPLICATIONS

. Automotive

. Machine Visions

. Security surveillance cameras

2. System Block Diagram

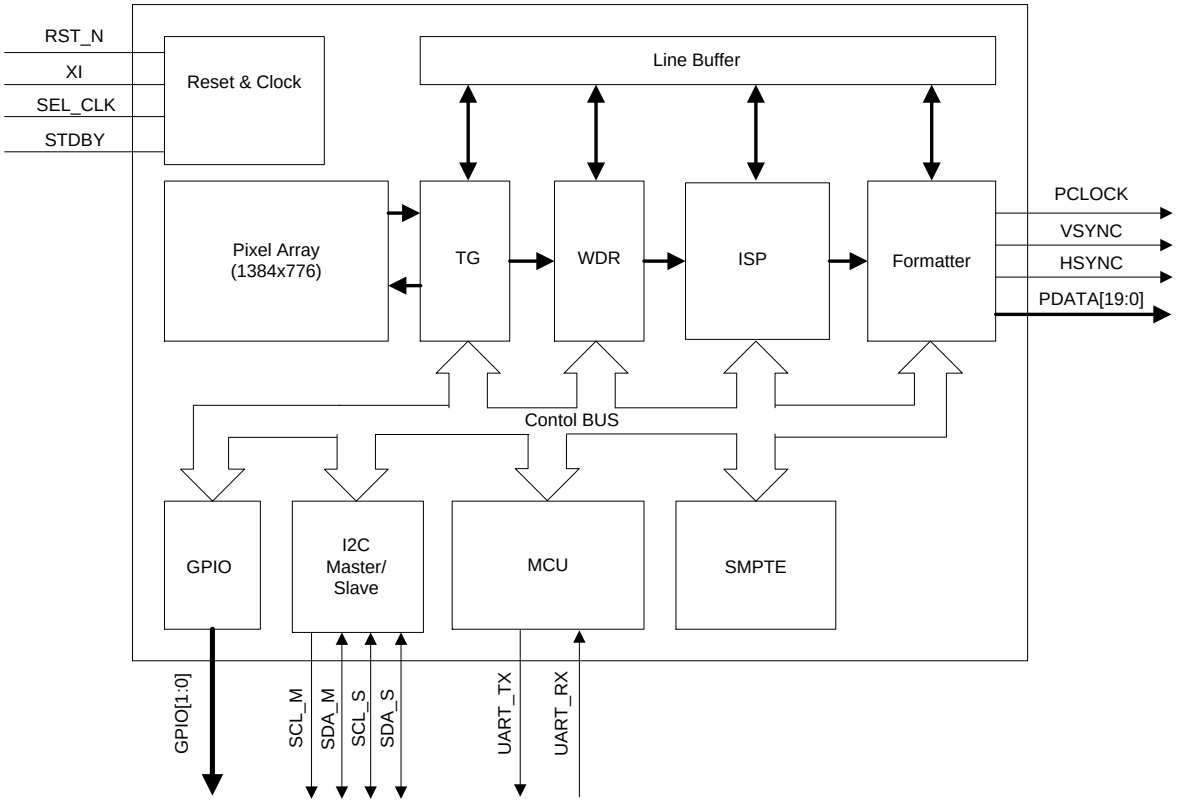


Figure 2-1 Block Diagram

CP8210 is a CMOS SXGA WDR Image Sensor in 1/3-inch optical format with 1,000,000 pixels.

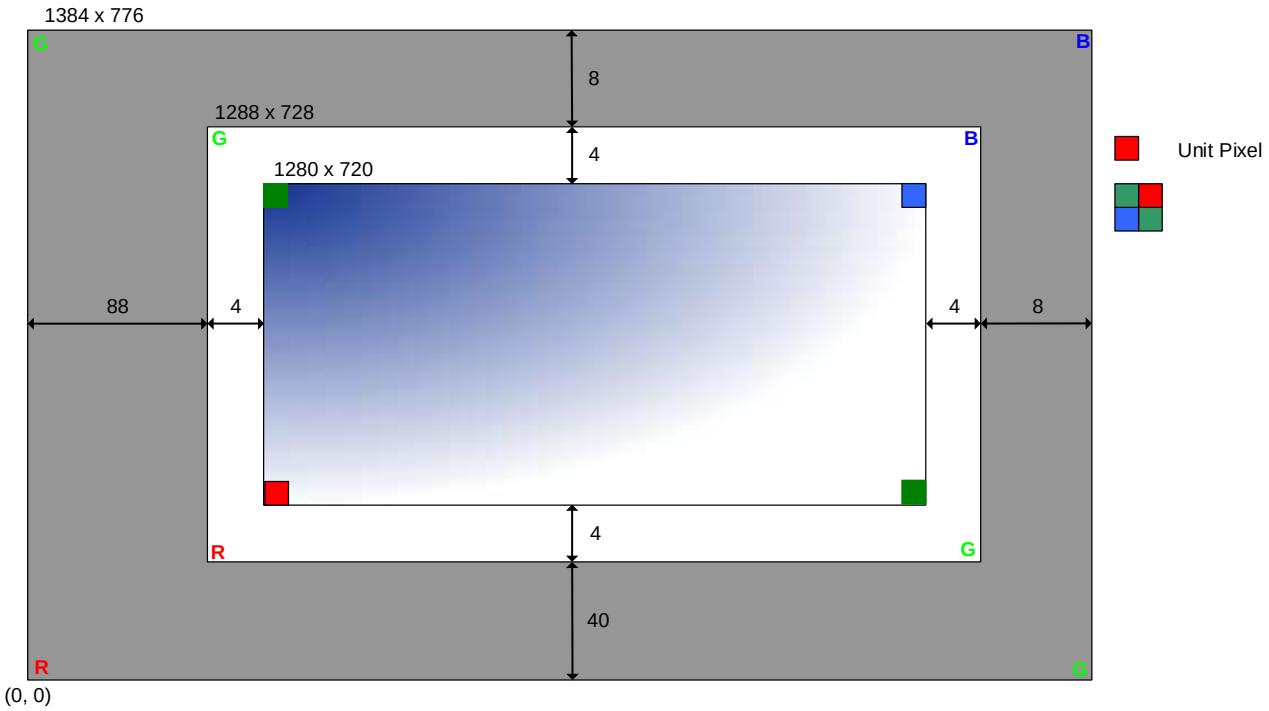
.

Figure 2-1 is a broad view of the block diagram of CP8210 and the 1384x776 pixel array is output through TG, WDR, ISP, Formatter to the 10-bit digital parallel port 2 channel (master, slave) two-wire serial interface and 8 channel GPIO, 4 channel PWM are provided for external interface.

8 bit MCU is built in to provide an overall chip control and flexibility.

3. Pixel Array Structure

Figure 3-1 shows the pixel array structure of CP8210.



Total number of pixels : 1384 x 776
Total active pixels : 1288 x 728
Total effective pixels : 1280 x 720
Optical blacks : left 88, right 8, top 8, bottom 40

Figure 3-1 Pixel Array Structure

4. Pixel Data Output Timing

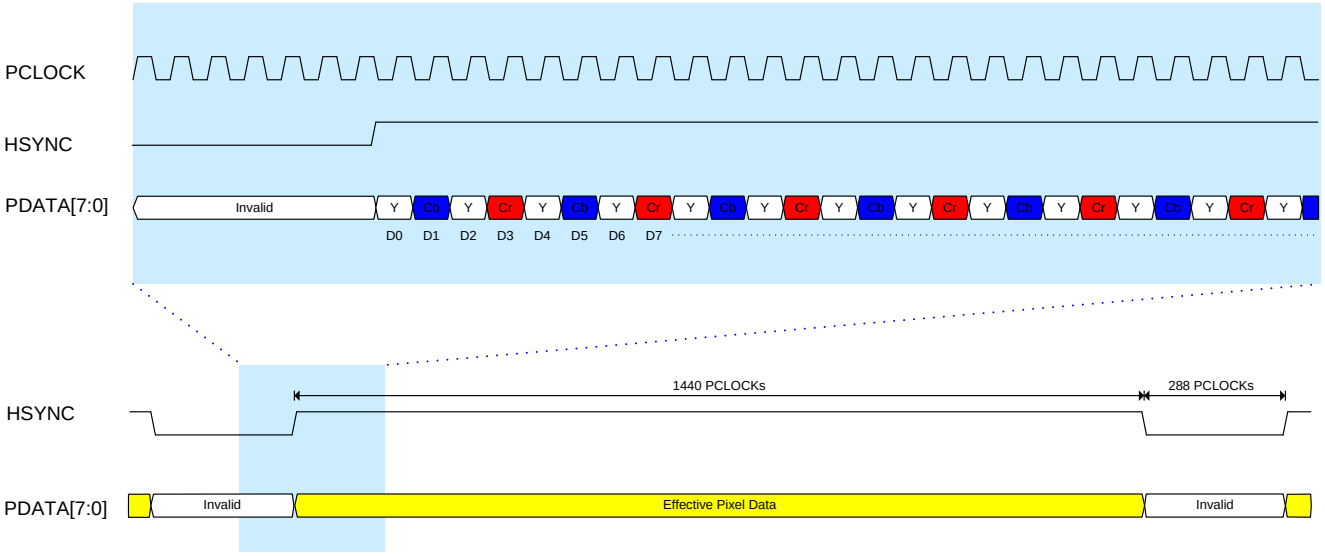


Figure 4-1 Horizontal Timing

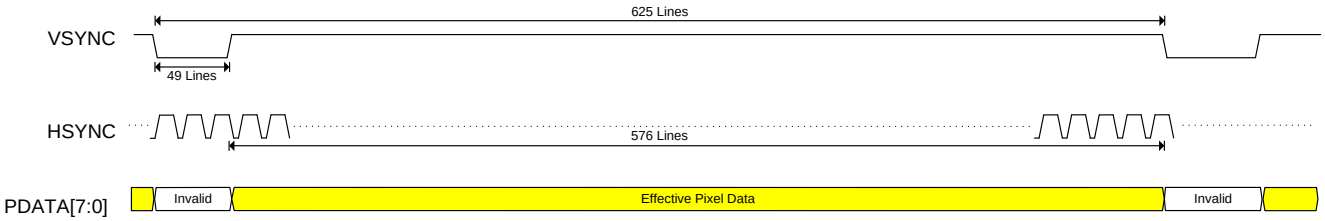


Figure 4-2 Vertical Timing

5. System Interface

5.1. System Initialization

Figure 5-1 is an outline of the reset scheme which initializes CP8210. When external reset is approved, internal reset generation is initialized, and the entire system is uninitialized together.

(Reset signal needs to be maintained to 200us more LOW after Ext Clock has been stabilized)

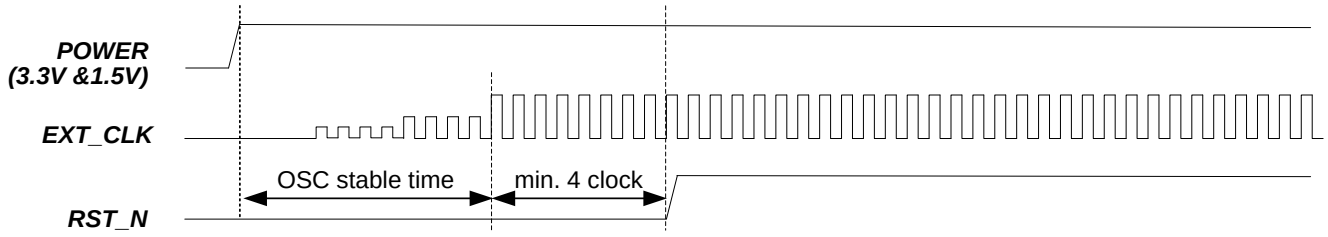


Figure 5-1 System Reset Scheme

5.2. Power-Down Mode

Power-down mode is controlled by the STDBY pin, operates as active high and enters power-down mode upon HIGH approval. Relevant pin needs to be maintained at low for Normal Operation Mode. For accurate power down operation, at least 4 clocks of external clock needs to be approved after STDBY signal input and after 4 clock approval, external clock can be maintained at LOW for reducing power consumption.

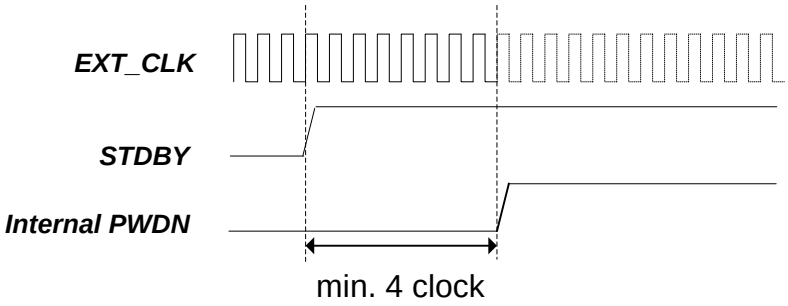


Figure 5-2 System Power Down Scheme

5.3. I2C interface

I2C Master and Slave interface each are built-in CP8210 internally. I2C device address can be modified through the MCU (system register 0x4006).

*** I2C Slave Device Address**

Write Device Address	0x76
Read Device Address	0x77

5.3.1. I2C Condition

- **Start / Stop Condition**

Data Line and Clock Line are maintained at High when Bus is not in use. Start condition is defined as the time during which Data Line transits from high to low while Clock Line maintains its high position. The time during when the data line transits from low to high is defined as the stop condition.

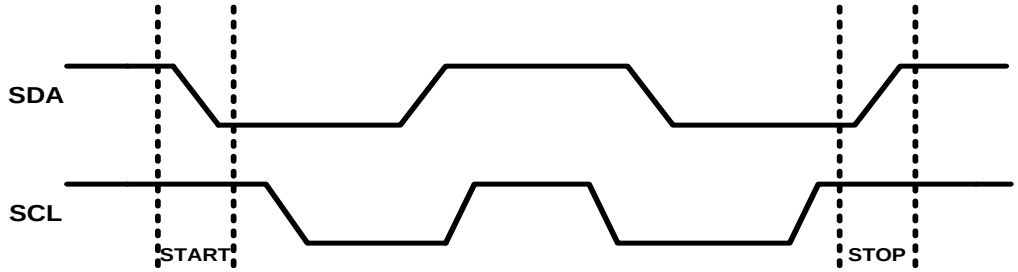


Figure 5-3 Start / Stop

- **Acknowledge**

All addresses and data are continuously transferred or received in 8-bit words to I2C slave. I2C slave sends 0 as an acknowledgement signal after each word sent. This happens in 9 clock intervals..

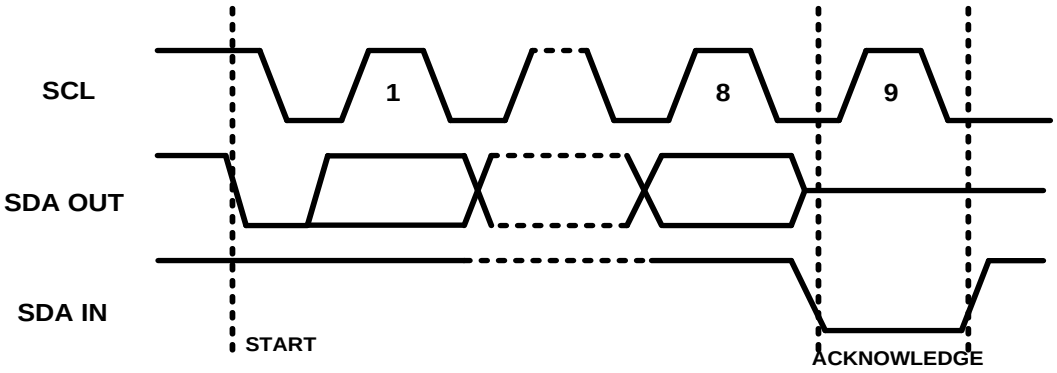


Figure 5-4 Acknowledge

5.3.2. I2C Master Operation

CP8210 operates as master through I2C interface SCL_M, SDA_M pins. It can be used as an interface to control various external devices such as AF module control.

- **Write Operation**

Write operation is composed of three parts including Device Address, Index Address and Write Data and the success of the communication of each part can be verified through the Acknowledge Bit after the transmission. I2C master can select the Target Device through the Address of the Device through which data is to be sent, and a maximum of 5byte data can be sent at once.

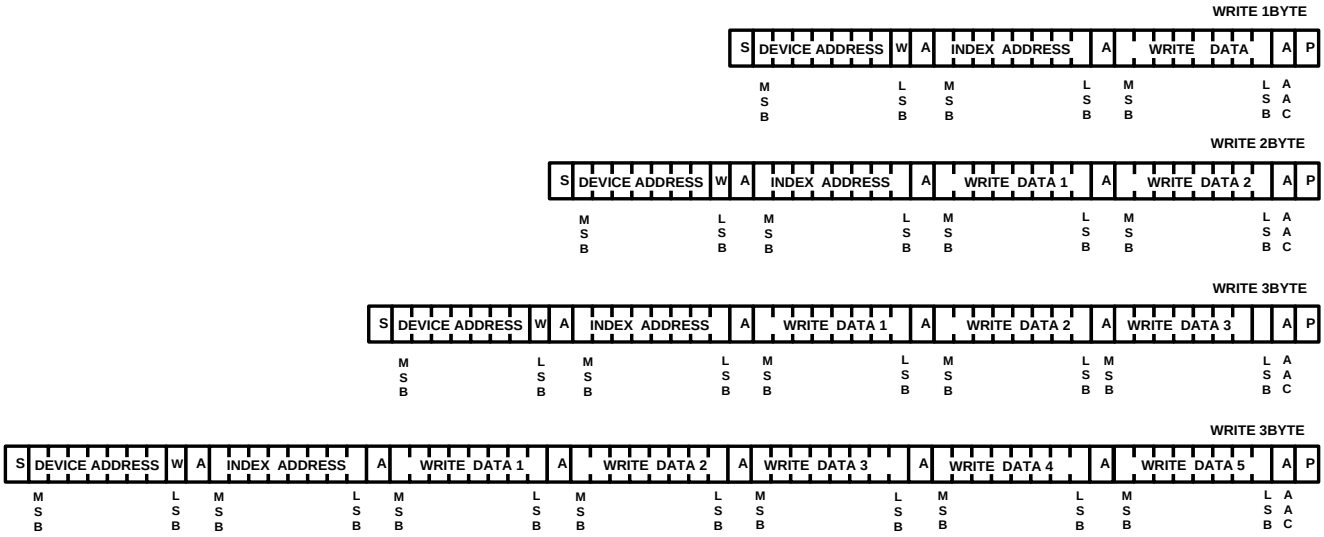


Figure 5-5 I2C Master Write Operation

- **Read Operation**

In order to access a random register to read the register value, " Dummy Write" needs to be performed. This is because internal address register automatically increases after the transmission is complete. In order to read data from a certain address register, write index address first to read the data at the relevant register. The blue dotted line in the figure below shows that in dummy write, STOP condition may be output after the index address has been sent, or the START condition may be output without the STOP condition. The function mentioned above is carried out by internal register settings. I2C master built in CP8210 can read a maximum of 2 Bytes in series.

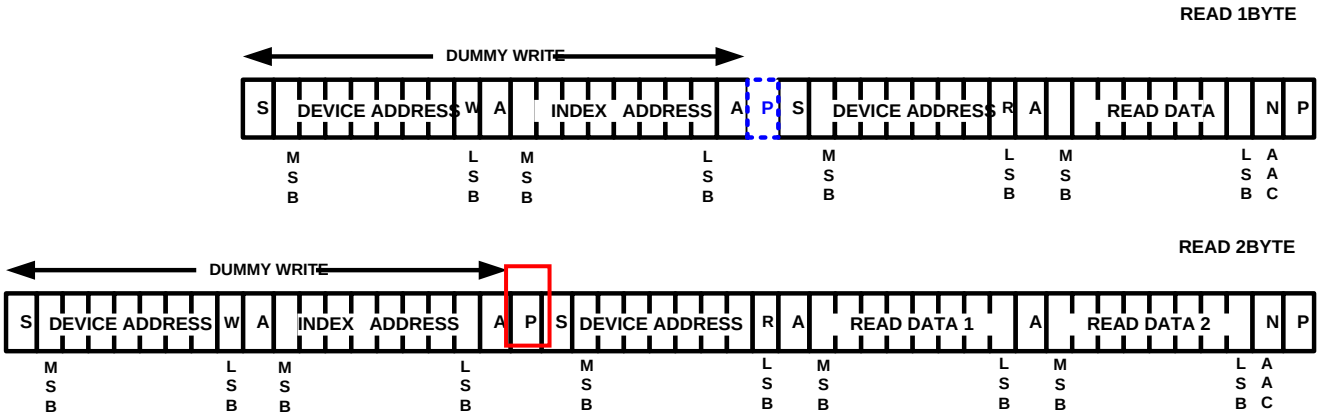


Figure 5-6 I2C Master Read Operation

5.3.3. I2C Slave Operation

CP8210 operates as slave through I2C interface SCL_S, SDA_S pin. Certain registers of CP8210 can be controlled through the I2C Slave interface. Program data can also be downloaded through the I2C Slave to the 8051 Program Memory within. MCU Code Memory Data of CP8210 can be saved in byte units, and MCU is under Reset status while SRAM write takes place through.

- **Byte Write**

  Write operation is composed of three parts including Device Address, Index Address, and Write Data, and the success of the communication can be verified through Acknowledge Bit after the transmission of each parts. I2C slave only receives data when the Device Address matches its own.

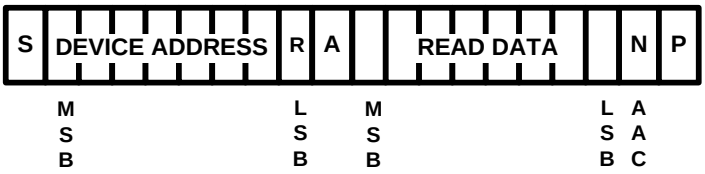
- **Random Read**

  In order to access a random register to read the register value " dummy" byte write needs to be performed. This is because internal address register automatically increases after the transmission is complete. In order to read data from a certain address register, write index address first to read the data at the relevant register.

- **Sequential Read**

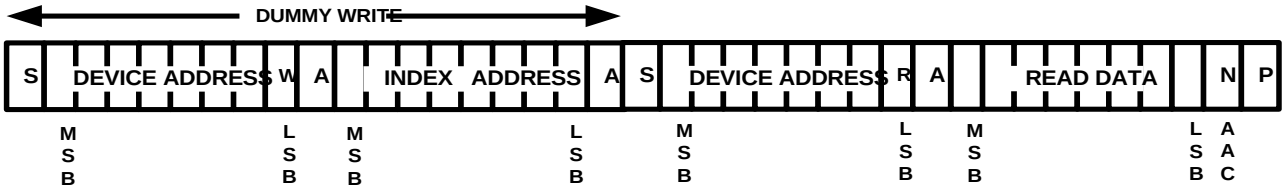
  Starts transmission together with initial Byte Read and data gets output continuously without the transmission of Device Address, Index Address to shorten communication time. I2C Master built in in CP8210 can read a maximum of 2 Bytes continuously and I2C Slave has no restrictions regarding this.

Byte Read Operation

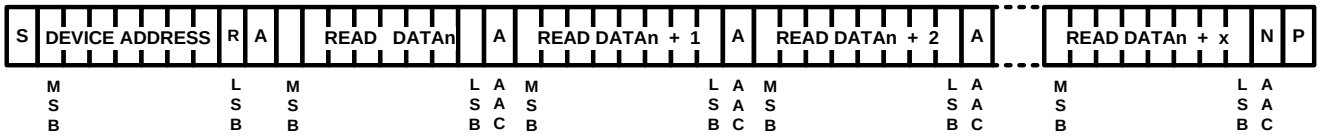


Byte Write Operation

Random Read Operation



Sequential Read Operation



S : Start Condition

P : Stop Condition

MSB : Most Significant Bit

LSB : Least Significant Bit

W : Write (1'b0)

R : Read (1'b1)

A : Acknowledge

N : No Acknowledge

AAC : Auto Address Increment

Figure 5-7 I2C Slave Read, Write Operation

5.4. GPIO, PWM Control Interface

CP8210 provides a maximum of 8 GPIOs and 4 PWMs in order to control the system control interface..

- **I/O control (system register 0x401f ~ 0x4023)**

  I/O control is used when sending output signals to external device, or when receiving input signal from external devices. A maximum of 8 ports can be used, and individual pull up/down control is possible through relevant registers.

- **PWM(Pulse Width Modulation control (system register 0x40a0 ~ 0x40c5)**

  PWM (Pulse Width Modulation) is used to control motor speed or light brightness. PWM can control the width of the pulse. These functions are analog characteristics but are possible by controlling digital pulse duty ratio and frequency divide value. In CP8210, duty ratio and frequency divide value can be controlled using 16bit control signals selected by register controls. Various PWM can be created based on main clock., and the duty cycle of each output wave can be controlled between 0%~100%.

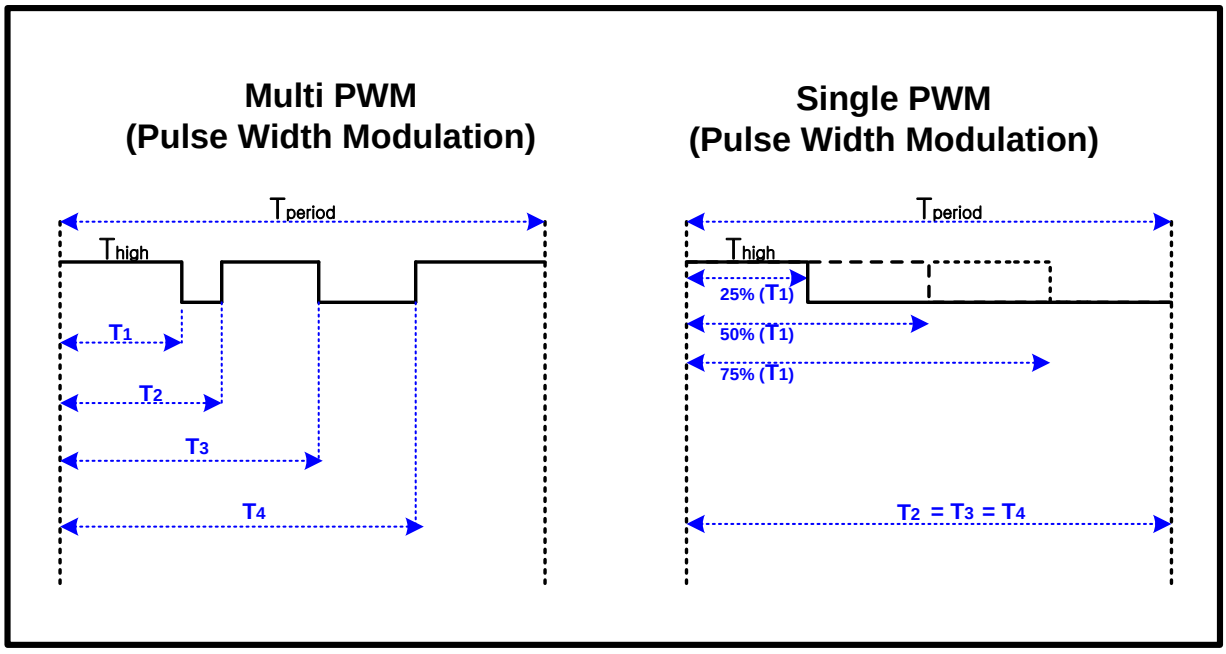


Figure 5-8 PWM Generation

5.5. PAD Control

- **GPIO1/PWM1, GPIO0/PWM0**

  GPIO1/PWM1, GPIO0/PWM0 pins can output GPIO[1:0] or PWM[1:0] using relevant register control.

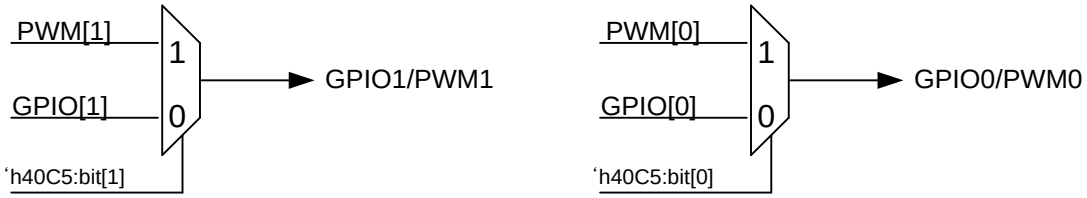


Figure 5-9 GPIO1/PWM1, GPIO0/PWM0 Control

- **PDATA Bus Control**

  PCLOCK, VSYNC, HSYNC, PDATA[9:0] pins are tri-state, pull-down control possible depending on the relevant register conditions. VSYNC, PCLOCK pins can be GPIO[3:2] or PWM[3:2] output through the register control. HSYNC, PDATA[2:0] pins can be GPIO[7:4] output through the register control.

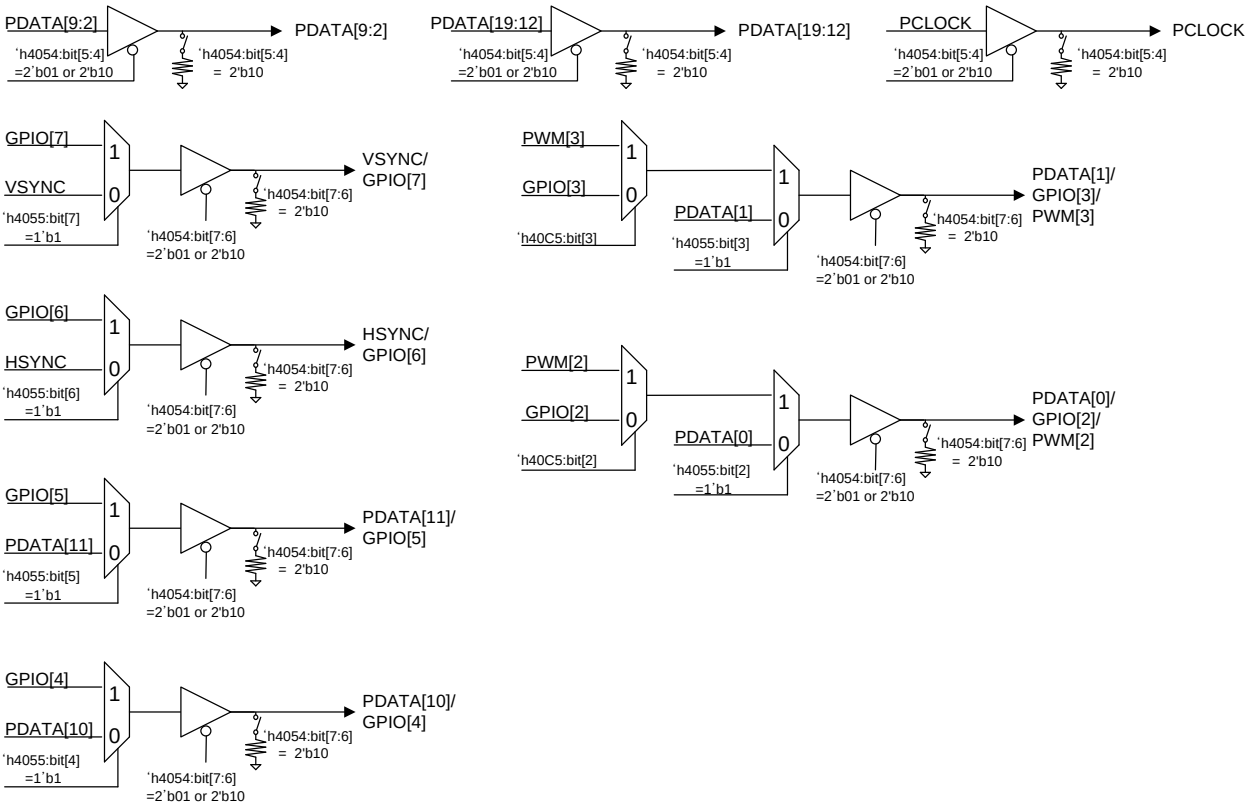


Figure 5-10 PDATA Bus Control

6. MCU interface

CP8210 has a 8bit MCU internally embedded. Memory map of the MCU block is as shown below. Code SRAM 24K byte, Data SRAM 2Kbyte are built in. CP8210 downloads the firmware using I2C master through an external EEPROM. Also, if no external EEPROM is available, the firmware can be downloaded through the system register 0x4024 ~0x4026 using I2C slave. Errors in firmware download can be checked through checksum register(0x4028 ~ 0x4029) or CRC register(0x402A ~ 0x402B). Only system register area can be accessed using I2C slave, and the other areas can be accessed using indirect mode when MCU is disabled, but the entire memory area of MCU is accessible. Interrupt Sources include VSYNC interrupt of internal Sensor and command register write interrupt.

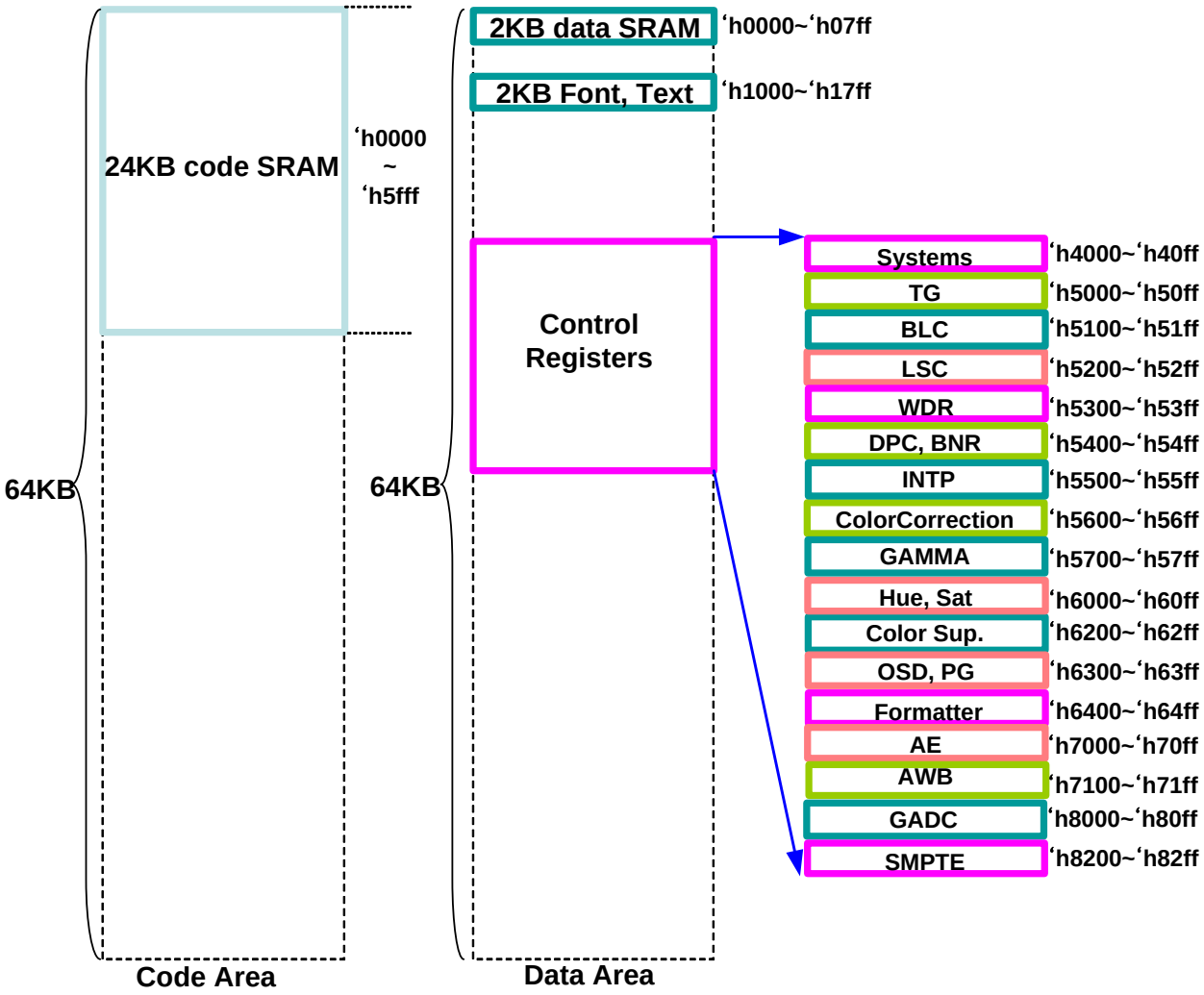


Figure 6-1 MCU Memory Map

7. EEPROM Boot Sequence

Code SRAM 24K byte and OSD Data SRAM 2Kbyte are embedded in CP8210. After initial power approval, firmware and OSD data is downloaded onto internal SRAM using I2C master through external EEPROM. Depending on the code written on certain parts of the firmware code, data size that downloaded 3 type mode can be controlled.

- **16Kbyte Code Only**

This mode uses 16K byte to code memory and does not use the OSD data. Of 16K code and address 0x3FFC and ox3FFD area of the write 0xAA and 0x55 to operate in this mode when it is.

- **24Kbyte Code Only**

This mode uses 24K byte to code memory and does not use the OSD data. Of 24K code and address 0x3FFC and 0x3FFD area does not have the write 0xAA and 0x55, address 0x5FFC and 0x5FFD area and the write 0xAA and 0x55 if it is to operate in this mode.

- **24Kbyte Code + 2Kbyte OSD**

This mode uses 24K byte to code memory and also uses 2K byte OSD data. Of 24K code and address 0x3FFC 0x3ffD area does not have the write 0xAA and 0x55, address 0x5FFC 0x5FFD area and if it is not the write 0xAA and 0x55 to operate in this mode. Since 24Kbyte data automatically for OSD data is write into SRAM 2Kbyte.

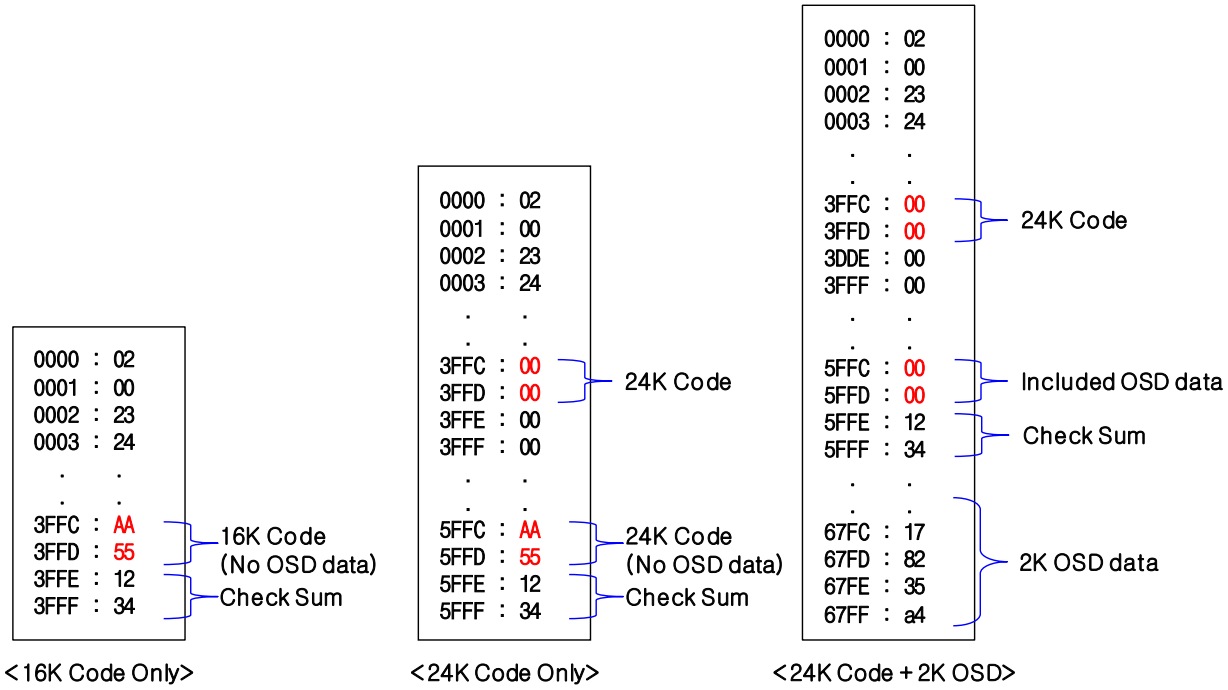


Figure 7-1 EEPROM Boot Sequence

8. Temperature Sensor Control

Main functions of Temperature sensor control block are below: .

- Generate Flag from TEMP80 input signal output from temperature sensor.
- Generate Flag if input is '1' more than 32 clock successive
- Set the temperature sensing range for each TEMP80

Temperature detection range of the TEMP80 can be set using TEMP_CON[2:0]

-TEMP80 range

000 : 40℃ 001 : 50℃

010 : 60℃ 011 : 70℃

100 : 80℃ 101 : 90℃

110 : 100℃ 111 : disable(default)

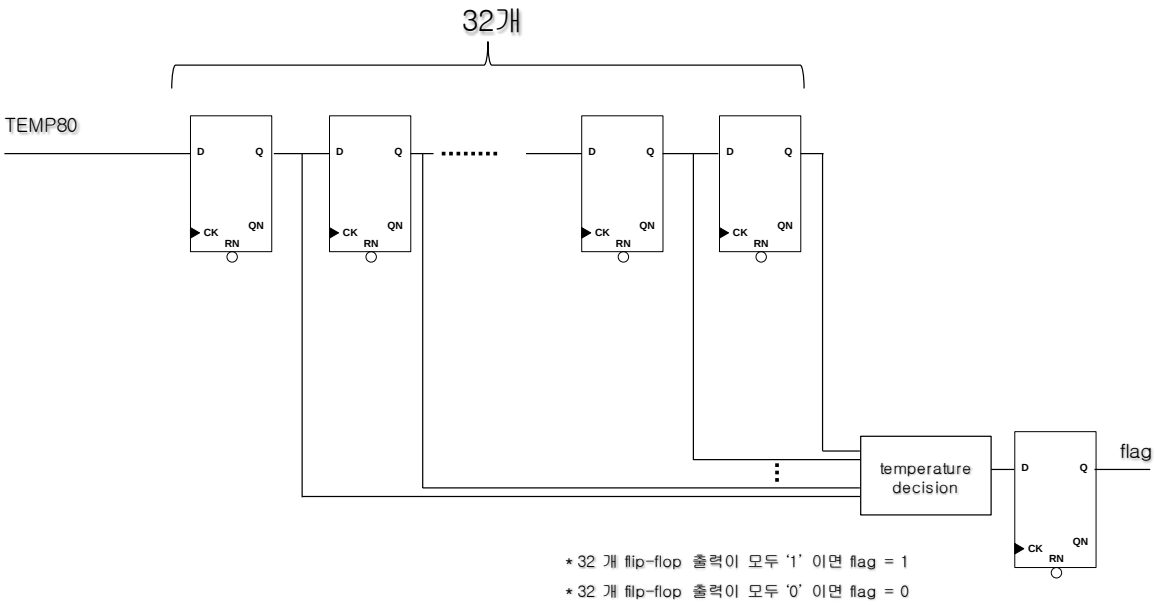


Figure 8-1 Temperature Sensor Control Block Diagram

8.1. Temperature Sensor Test Mode

In order to verity quality of temperature sensor a separate test mode is implemented.

TEST, SDA_M, SCL_M, SDA_S, SCL_S pin to give it applied to enter as shown in Figure 8-2, it can control the temperature sensor throught the PDATA pin and monitor the output.

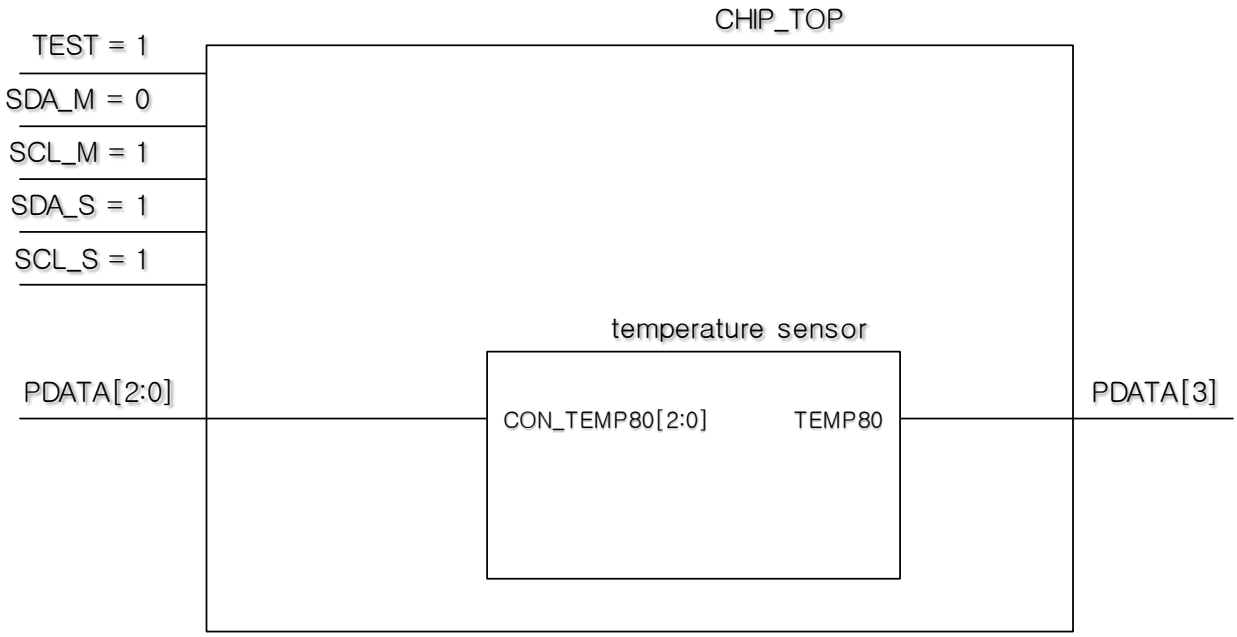


Figure 8-2 Temperature Sensor Test Mode

9. TG(Timing Generator)

This mode uses 24K byte to code memory and also uses 2K byte OSD data. Of 24K code and address 0x3FFC 0x3ffD area does not have the write 0xAA and 0x55, address 0x5FFC 0x5FFD area and if it is not the write 0xAA and 0x55 to operate in this mode. Since 24Kbyte data automatically for OSD data is write into SRAM 2Kbyte.

9.1. Analog/Digital Gain Control

9.1.1. Analog Gain

Analog gain can be controlled through the registers in Table 9-1. Used formula is a number of '1' of S_GAIN register/ a number of '1' of F_GAIN register. For example, if S_GAIN is 000_0000_0011 and F_GAIN is 000_0011_1100, the number of 1 of S_GAIN is 2 ad the one of F_GAIN is 4. Therefore 2/4=1/2 times gain is applied. Note that it can not be set in the same order digit. For example, if S_GAIN is 000_0000_0011 and F_GAIN is 000_0000_1111, these 2 bit settings are same order digit, therefore the setting is unacceptable. On the other hand, column gain can be set regardless of the order digit.

.

Register Name	RW	Bits	Register Description
L_A_F_GAIN1_H (Reg_0x5007)	RW	[2:0]	High byte of long data feedback cap enable for global gain 1
L_A_F_GAIN1_L (Reg_0x5008)	RW	[7:0]	Low byte of long data feedback cap enable for global gain 1
L_A_F_GAIN2_H (Reg_0x5009)	RW	[2:0]	High byte of long data feedback cap enable for global gain 2
L_A_F_GAIN2_L (Reg_0x500A)	RW	[7:0]	Low byte of long data feedback cap enable for global gain 2
S_A_F_GAIN1_H (Reg_0x500B)	RW	[2:0]	High byte of small pixel feedback cap enable for global gain 1
S_A_F_GAIN1_L (Reg_0x500C)	RW	[7:0]	Low byte of small pixel feedback cap enable for global gain 1
S_A_F_GAIN2_H (Reg_0x500D)	RW	[2:0]	High byte of small pixel feedback cap enable for global gain 2
S_A_F_GAIN2_L (Reg_0x500E)	RW	[7:0]	Low byte of small pixel feedback cap enable for global gain 2
L_A_S_GAIN1_H (Reg_0x500F)	RW	[2:0]	High byte of long data input cap enable for global gain 1
L_A_S_GAIN1_L (Reg_0x5010)	RW	[7:0]	Low byte of long data input cap enable for global gain 1
L_A_S_GAIN2_H (Reg_0x5011)	RW	[2:0]	High byte of long data input cap enable for global gain 2
L_A_S_GAIN2_L (Reg_0x5012)	RW	[7:0]	Low byte of long data input cap enable for global gain 2
S_A_S_GAIN1_H (Reg_0x5013)	RW	[2:0]	High byte of small pixel input cap enable for global gain 1
S_A_S_GAIN1_L (Reg_0x5014)	RW	[7:0]	Low byte of small pixel input cap enable for global gain 1

S_A_S_GAIN2_H (Reg_0x5015)	RW	[2:0]	High byte of small pixel input cap enable for global gain 2
S_A_S_GAIN2_L (Reg_0x5016)	RW	[7:0]	Low byte of small pixel input cap enable for global gain 2
A_F_GAIN3 (Reg_0x5017)	RW	[3:0]	feedback cap enable for column gain
A_S_GAIN3 (Reg_0x5018)	RW	[3:0]	input cap enable for column gain

Table 9-1 Analog Gain Control

global gain table(gain1)

S	---------->	1	2	3	4	5	6	7	8	9	10
F	1	1.00	0.50	0.33	0.25	0.20	0.17	0.14	0.13	0.11	0.10
	2	2.00	1.00	0.67	0.50	0.40	0.33	0.29	0.25	0.22	
	3	3.00	1.50	1.00	0.75	0.60	0.50	0.43	0.38		
	4	4.00	2.00	1.33	1.00	0.80	0.67	0.57			
	5	5.00	2.50	1.67	1.25	1.00	0.83				
	6	6.00	3.00	2.00	1.50	1.20					
	7	7.00	3.50	2.33	1.75						
	8	8.00	4.00	2.67							
	9	9.00	4.50								
	10	10.00									

global gain table(gain2)

S	---------->	1	2	3	4	5	6	7	8	9	10
F	1	1.00	0.50	0.33	0.25	0.20	0.17	0.14	0.13	0.11	0.10
	2	2.00	1.00	0.67	0.50	0.40	0.33	0.29	0.25	0.22	
	3	3.00	1.50	1.00	0.75	0.60	0.50	0.43	0.38		
	4	4.00	2.00	1.33	1.00	0.80	0.67	0.57			
	5	5.00	2.50	1.67	1.25	1.00	0.83				
	6	6.00	3.00	2.00	1.50	1.20					
	7	7.00	3.50	2.33	1.75						
	8	8.00	4.00	2.67							
	9	9.00	4.50								
	10	10.00									

pre_amp gain(gain3)

S	---------->	1	2	3	4
F	1	1.00	2.00	3.00	4.00
	2	0.50	1.00	1.50	2.00
	3	0.33	0.67	1.00	1.33
	4	0.25	0.50	0.75	1.00

Table 9-2 Analog Gain Table

9.1.2. Digital Gain

Digital gain can be controlled through the registers in Table 9-3.

Register Name	RW	Bits	Register Description	
			Field Name	Field Description
L_D_GAIN (Reg_0x500C)	Large Pixel Global Digital Gain control register **(Default 0x00)**			
	RW	[7:0]	**L_D_GAIN**	[7:5] : Large Pixel Global Digital Gain1 control [4:0] : Large Pixel Global Digital Gain2 control Gain = 2^L_D_GAIN[7:5]*(1 + L_D_GAIN[4:0]/32)
S_D_GAIN (Reg_0x500D)	Small Pixel Global Digital Gain control register **(Default 0x00)**			
	RW	[7:0]	**S_D_GAIN**	[7:5] : Small Pixel Global Digital Gain1 control [4:0] : Small Pixel Global Digital Gain2 control Gain = 2^S_D_GAIN[7:5]*(1 + S_D_GAIN[4:0]/32)

Table 9-3 Digital Gain Control

D_GAIN[7]	D_GAIN[6]	D_GAIN[5]	Digital Gain1 Output
0	0	0	x1
0	0	1	x2
0	1	0	x4
0	1	1	x8
1	X	X	x16

Table 9-4 Digital Gain 1 Table

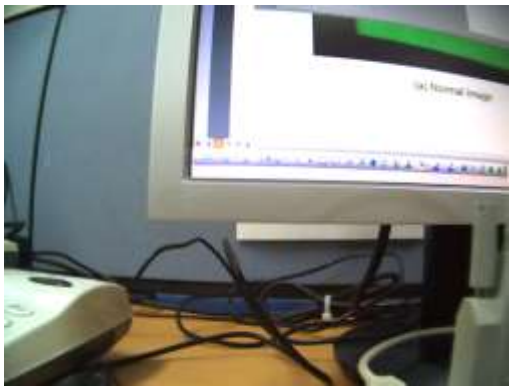
D_GAIN[4]	D_GAIN[3]	D_GAIN[2]	D_GAIN[1]	D_GAIN[0]	Digital Gain2 Output
0	0	0	0	0	x1.00
0	0	0	0	1	x1.03
0	0	0	1	0	x1.06
0	0	0	1	1	x1.09
0	0	1	0	0	x1.13
0	0	1	0	1	x1.16
0	0	1	1	0	x1.19
0	0	1	1	1	x1.22
0	1	0	0	0	x1.25
0	1	0	0	1	x1.28
0	1	0	1	0	x1.31
0	1	0	1	1	x1.34
0	1	1	0	0	x1.38
0	1	1	0	1	x1.41
0	1	1	1	0	x1.44
0	1	1	1	1	x1.47
1	0	0	0	0	x1.50
1	0	0	0	1	x1.53
1	0	0	1	0	x1.56
1	0	0	1	1	x1.59
1	0	1	0	0	x1.63
1	0	1	0	1	x1.66

1	0	1	1	0	x1.69
1	0	1	1	1	x1.72
1	1	0	0	0	x1.75
1	1	0	0	1	x1.78
1	1	0	1	0	x1.81
1	1	0	1	1	x1.84
1	1	1	0	0	x1.88
1	1	1	0	1	x1.91
1	1	1	1	0	x1.94
1	1	1	1	1	x1.97

Table 9-5 Digital Gain 2 Table

9.2. Mirror Control

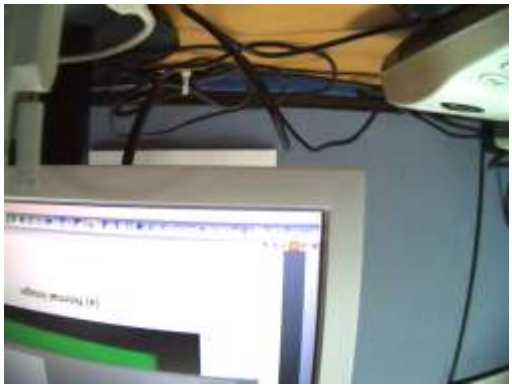
10. CP8210 can use the horizontal/vertical mirror function through the IMG_CON(0x501B) register. .Figure 9-1은 shows the image when mirror control is used.



(a) original image

(b) horizontal mirror image

(c) vertical mirror image



(b) horizontal/vertical mirror image

Figure 9-1 mirror control image

11. BLC(Black Level Compensation)

Various noises are created at the image sensor which converts light into electric signals. Among those are offset form noise from heat and noise from analog circuit which processes signals. In order to measure and remove the offset form noise, create a pixel area (optical black area) which is not affected by light due to metal blocking, and change the relevant pixel value to true ‘ 0’ . Such offset adjustment work is called BLC(Black Level Compensation).

12. ISP(Image Signal Processing)

12.1. Overview

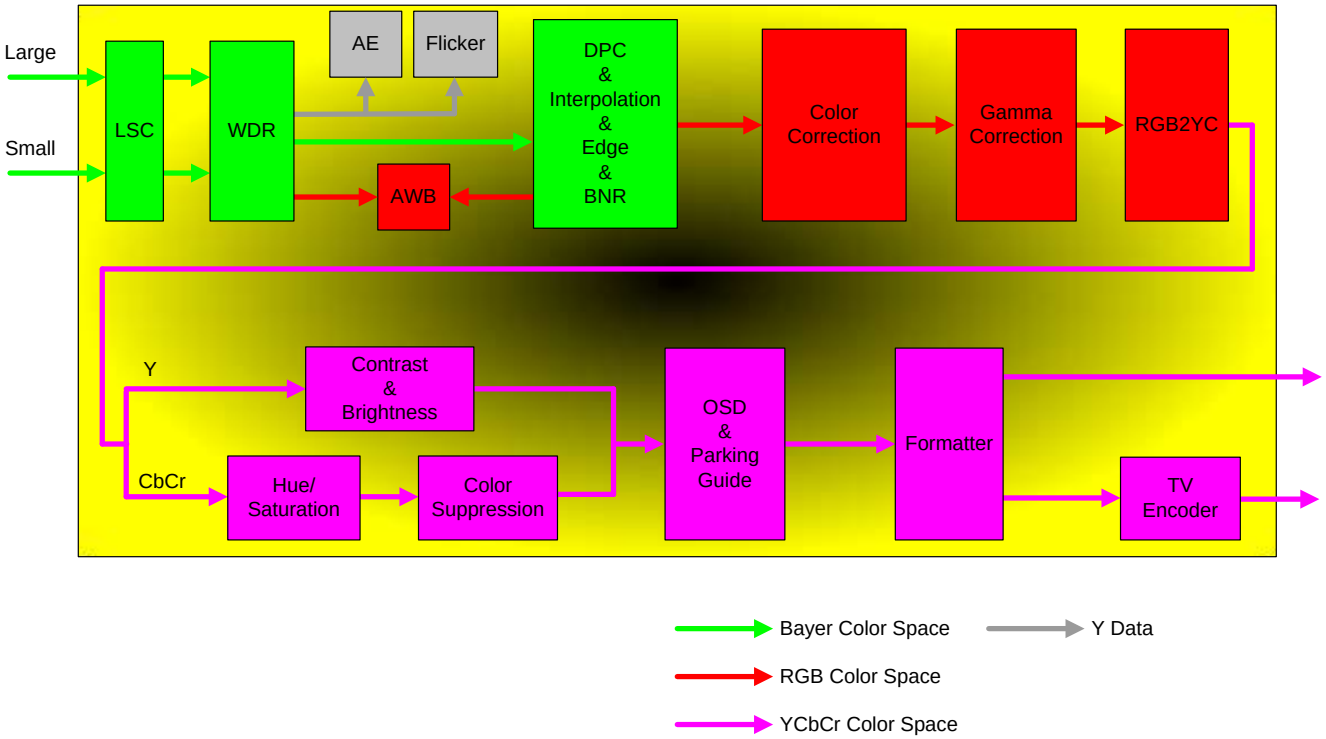


Figure 12-1 ISP Block Diagram

ISP (Image Signal Processing) carries out a function whereby the 10 bit data input from the sensor is converted into RGB and image processed to be output again. As shown in Figure 12-1 ISP Block Diagram, the input video data is processed together with Y and RGB data for Auto Exposer(AE) and Auto White Balance (AWB), through LSC and WDR blocks. Bayer format data goes through interpolation part to be converted to R[9:0], G[9:0], B[9:0].

R, G, B data interpolated are transformed into 8 bit data after color correction and gamma correction of each R, G, and B, and transformed R, G, B data are then transformed into brightness signal Y and color difference Cb, Cr signals. Therefore the bayer format video data input from the sensor is transformed into brightness and color difference singals, and that brightness (Y) and color difference(Cr/Cb) are used to enhance image quality per user request. Transformed data can be output in either of YCrCb 4:2:2, RGB565 or RGB555, Bayer formats.

12.2. LSC(Lens Shading Compensation)

As camera modules get smaller by trend, small external lens and large f number optical devices experience image distortion due to geometrical arrangement of pixel array.

Pixels of image sensor RGB Color Filter Array (CFA) center and edges are subject to light from different directions. These minute location differences cause illumination differences, and illumination differences also affect color due to light wave and micro lens curvature differences. As a result, color distortion that forming FCA and signal size decrease dependant on the pixel location inevitably happens, and this causes the image quality fall in the original image.

12.2.1. Gain for LSC

Lens shading correction performs correction of a lens shading distortion due to gradual brightness differences from the center to the edges. Lens shading correction gain uses the ar^2 function whereby r is a distance between the center and the relevant coordinates. Normally, the lens shading correction gain error increases from center to the edges. In CP8210, the two gains can be combined to compensate.

Gain control for adjusting CP8210 distortion can control each of R, Gr, Gb, B of large and small pixels. (LSC register : 0x5204 ~ 0x5217)

12.2.2. LSC Centering

LSC Centering 은 센서의 Pixel array 의 중심과 렌즈의 중심이 서로 상이할 경우 이를 보상해 준다.

LSC center 를 위한 register (LP:0x5201~0x5203, SP:0x5211~0x5213)를 제공해준다.

12.3. WDR(Wide Dynamic Range)

ynamic Range a scope of dynamics that can be expressed in one screen. The larger the dynamic range, the more likely the capture of outside/inside environments simultaneously. Figure 12-2 shows a comparison of capture with a normal sensor, and with WDR.

Figure 12-2 WDR Image Comparison

12.4. ISP1

ISP1 (Image Signal Processing1) receives Bayer format 10 bit data as input, converts it to RGB and outputs after image processing. Bayer format data passes through interpolation part and is converted into R[9:0], G[9:0], B[9:0]. RGB data is converted into YCbCr data through RGB2YCbCr block, and the Hue/Saturation block controls Hue, Saturation, Contrast and Brightness.

12.4.1. Defect Pixel Compensation(DPC)

DPC finds defect pixels, and corrects it using the surrounding pixels. DPC used in CP8210 determines defect pixels by comparing color of pixels in a 5x5 window with the center pixel to correct it.

12.4.2. Color Interpolation

Color Interpolation is a block which acquires color from surrounding pixels if a pixel only has a single color information. CP8210 Interpolation block, in addition to CP8210 Interpolation function has functions including YC noise reduction, Edge Enhancement, False Color Suppression, and RGB gain for White Balance..

12.4.3. YC Noise Reduction

YC noise reduction classifies between the plane section and edge section of a video to blur the plane section while maintaining the edge to reduce image noise. This function can be set on Register(0x5500).

12.4.4. Edge Enhancement

Edge Enhancement of CP8210 is controlled by Register 0x5508~0x5509 YMGAIN 뭉 YHGAIN.YMGAIN controls Gain of Middle Frequency Edge of Video, YHGAIN controls Gain of High Frequency Edge of Video. Corrding level is set on register(0x550A~0x550B) so that Edge Gain under Corring Level is not applied on the video.

12.4.5. Color Correction

Color Correction controls of color balance of acquired image to suit the target color checker. When AWB is performed, the image brightness ingredients changes and color correction needs to be performed as well.

$$\begin{bmatrix} Rout \\ Gout \\ Bout \end{bmatrix} = \begin{bmatrix} cc00 & cc01 & cc02 \\ cc10 & cc11 & cc12 \\ cc20 & cc21 & cc22 \end{bmatrix} x \begin{bmatrix} Rin \\ Gin \\ Bin \end{bmatrix}$$

Figure 12-3 Color Correction Matrix

The above equation is about the color correction. As shown above, the input color signals R_in, G_in, and B_in are adjusted to each offset values and are transformed by the color correction matrix. Each coefficient of the matrix can be set as negative value or positive value depending on the sign bit (MSB of

each coefficient). In case of a negative number, it is in a form of two's complement. The coefficients which are expressed in 6bit (except sign and overflow bytes) can be divided into 64, and each coefficient value range is -2 ~ 1.984. An appropriate coefficient is found and set depending on each image system lens, IR filter, and sensor type. When configuring each coefficients, CC_00 = {CC_01 + CC_02}, CC_11 = {CC_10 + CC_12}, CC_22 = {CC_20 + CC_21} need all to be set as same values to maintain white balance.

With actual CP8210, Color Correction Matrix of each light source are saved on the firmware and applied depending on the light source.

12.4.6. Gamma Correction

CP8210 supports the following GAMMA MODE. 19 registers are applied for gamma. Gamma control register is defined in 0x5710 ~0x574F.

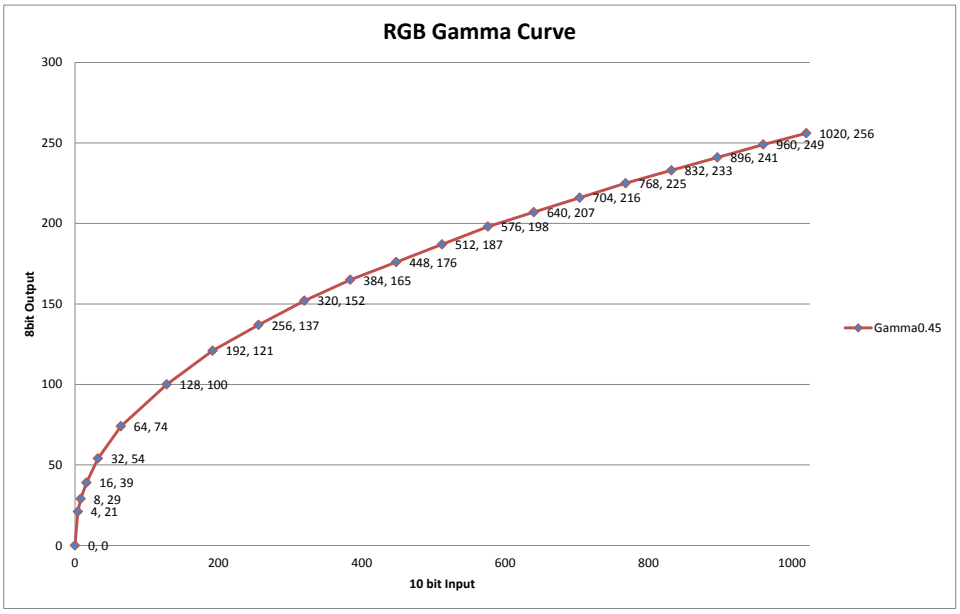


Figure 12-4 GAMMA register and GAMMA value

Figure 12-4 shows that 19 points on Y axis are mapped by the value entered in the register..

12.4.7. RGB to YCbCr

CP8210 RGB to YcbCr block converts RGB to Y, Cb, Cr values by under equation.

Y601 = 0.299*R + 0.587*G + 0.114*B

Cb = -0.169*R – 0.331*G + 0.500*B + 128

Cr = 0.500*R – 0.419*G – 0.081*B + 128

R,G,B are in 0~255 range

Y601 is in 0~255 range (0-255, offset=0)

Cb, Cr are in 0~255 range (+/- 127, offset=0)

Figure 12-5 SDI Equations

12.5. ISP2

ISP2 (Image Signal Processing2) receives output RGB format from ISP1 block as input. Input 8bit RGB data is transferred to brightness Y and color difference Cb, Cr data in RGB2YCbCr block. Data converted to YCbCr format go through image enhance functions to suit user demand including Hue, Saturation, Contrast, Edge control, and color suppression.

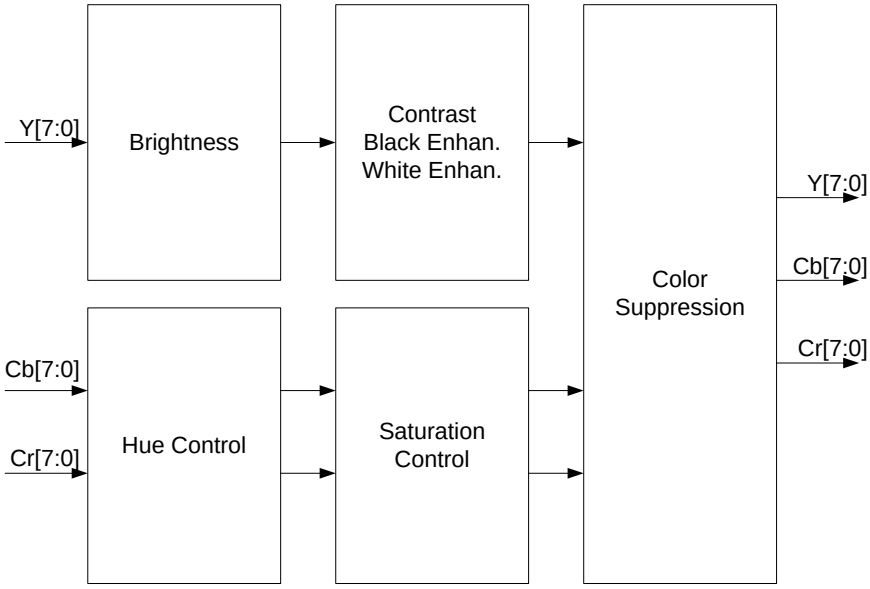


Figure 12-6 ISP2 Block Diagram

12.5.1. Brightness Control

Brightness control gives offset to the image luminance to control the brightness of the image, and the size of the offset can be chosen between -128~127.

12.5.2. Contrast Control

Contrast control block is based on the reference point luminance, and controls the contrast by reducing the luminance of areas where luminance is lower than the reference point, and increasing the luminance of areas where luminance is above the reference point. Reference point normally used is 128, and can be changed depending on the situation. Contrast gain can be applied in 0~2x ranges.

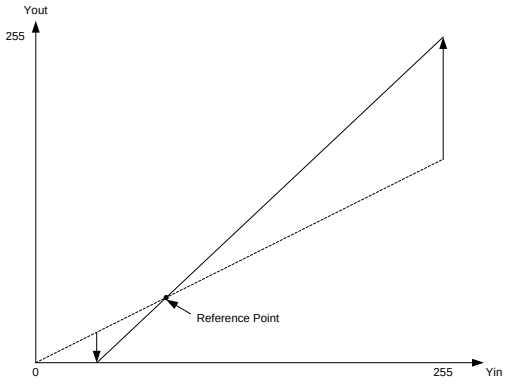


Figure 12-7 Contrast control

12.5.3. Cb/Cr Gain

Cb/Cr gain control moves current color difference information towards Cb axis or Cr axis by apply ing saturation gain on color coordinates. Cb/Cr gain can be applied in 0~2x ranges.

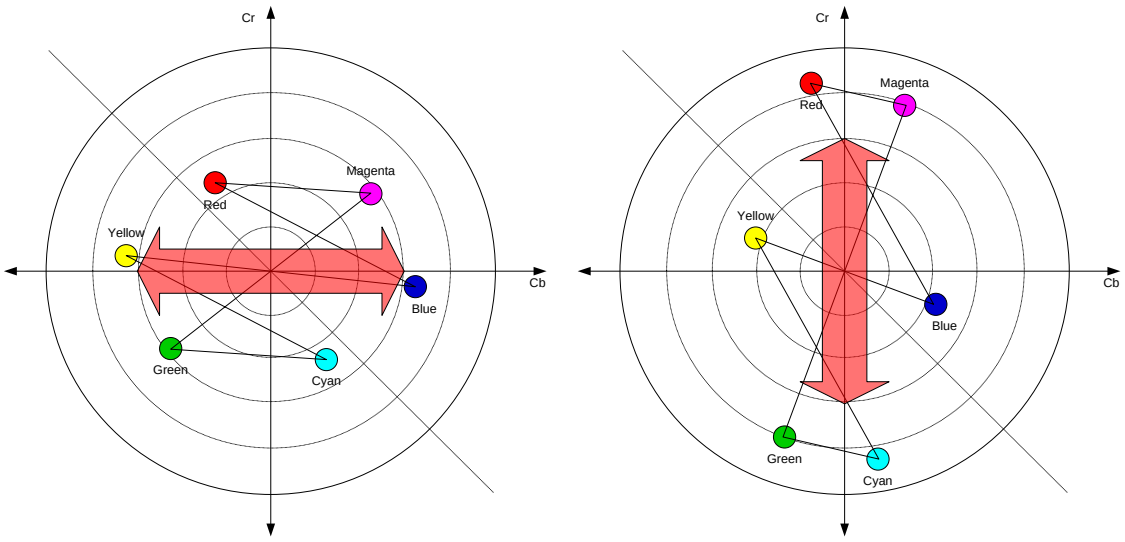


Figure 12-8 Cb/Cr gain control

12.5.4. Hue Control

Hue control is used for global or individual color information change. Hue can be changed betwe en −45°~+45° in 1° units and uses 2's complement.

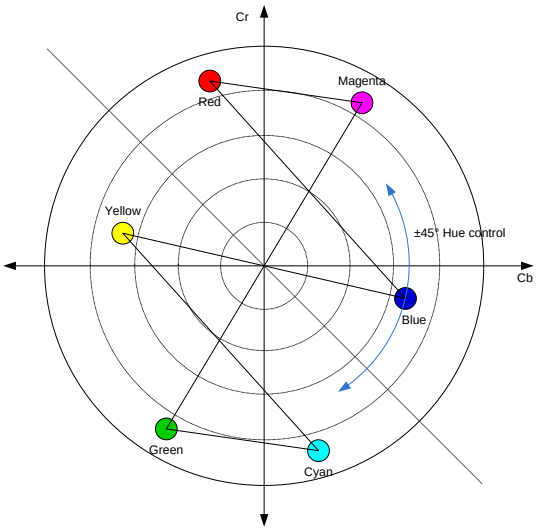


Figure 12-9 Hue control

12.5.5. Saturation Control

Saturation control is used to control the image saturation. Saturation gain can be applied in 0~2x

ranges.

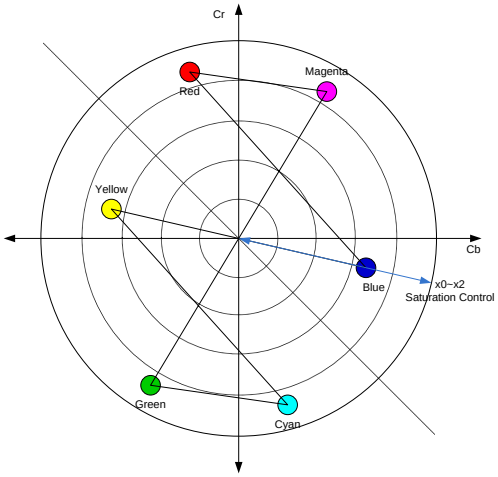


Figure 12-10 Saturation control

12.5.6. Black Enhancement

Black Enhancement makes dark areas of the image darker by making Black color level more Black, and it preserves data in the lighter areas than Contrast Control and can reduce the Minimum Black Level of the image.

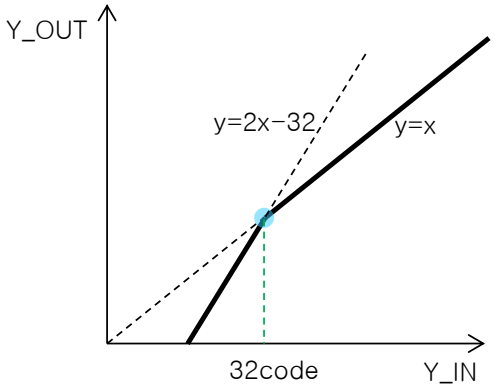


Figure 12-11 Black Enhancement Control

12.5.7. White Enhancement

White Enhancement makes bright areas of the image brighter by making White color level more White, and it preserves data in the darker areas than Contrast Control and can reduce the Minimum Black Level of the image.

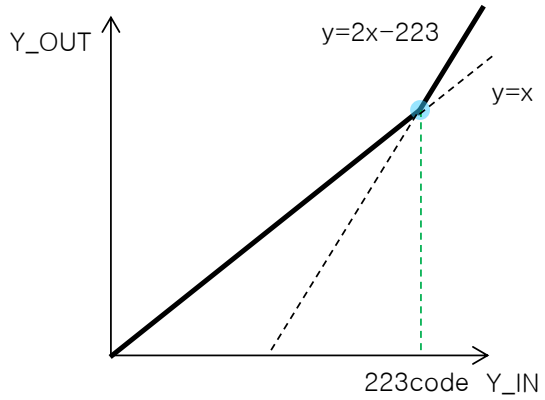


Figure 12-12 White Enhancement Control

12.5.8. Color Suppression

Color Suppression function is a function to reduce the color component when luminance is too high or low or if there is unwanted color noise.

Threshold value and gain control is possible on each of Cb and Cr

Cb => thresh hold low : ' h6213 thresh hold high : ' h6211
gain low : ' h6214 gain high : ' h6212

Cr => thresh hold low : ' h6218 thresh hold high : ' h6216
gain low : ' h6219 gain high : ' h6217

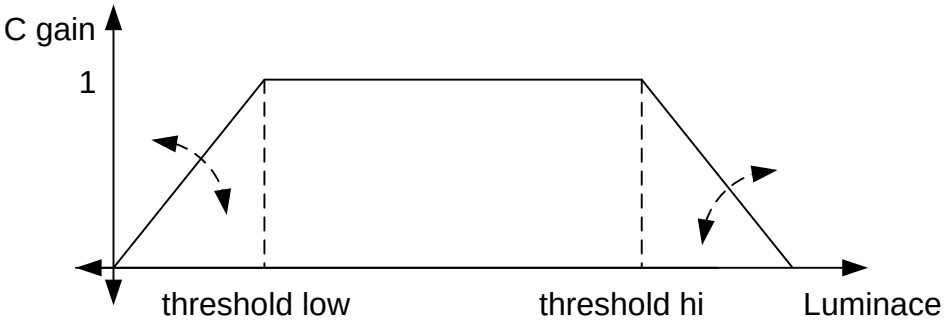


Figure 12-13 Applying Gain on Luminance Threshold

13. OSD(On Screen Display)

14. OSD(On Screen Display) is a function to display the information user needs directly on screen. CP8210 OSD is largely composed of three parts including text menu, parking guide, and privacy zone.
15. Text menu was designed for displaying text information for users to help product installation and optimization, and parking guide was designed for helping rear parking using rear-view camera, and privacy zone was designed for protecting privacy using CCTV.

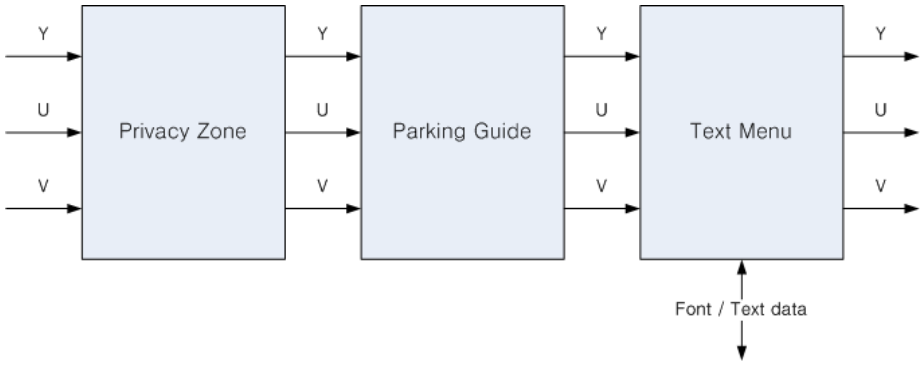


Figure 13-1 OSD block diagram

15.1. Privacy Zone

privacy zone were designed to protect privacy in using CCTV or others.

Rectangular masks are output instead of the sensor output at user designated locations. Up to 8 of these masks can be set, and when the different color masks overlap, the mask with the smaller internal mask number takes priority. Figure 13-2 is an example of a privacy zone set.

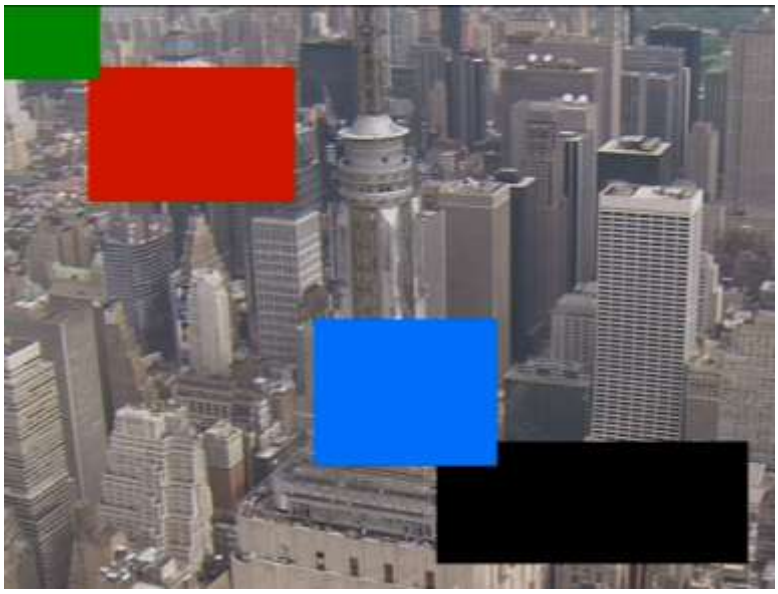


Figure 13-2 Privacy Zone Example

15.2. Parking Guide

Parking guide was designed to help rear parking using rear-view camera. The lines drawn on parking guide screen can be adjusted for their transparency, each line's width can be adjusted in pixel units, and the color information can be set with YUV. Figure 13-3 is an example of a parking guide which has been set following this method.

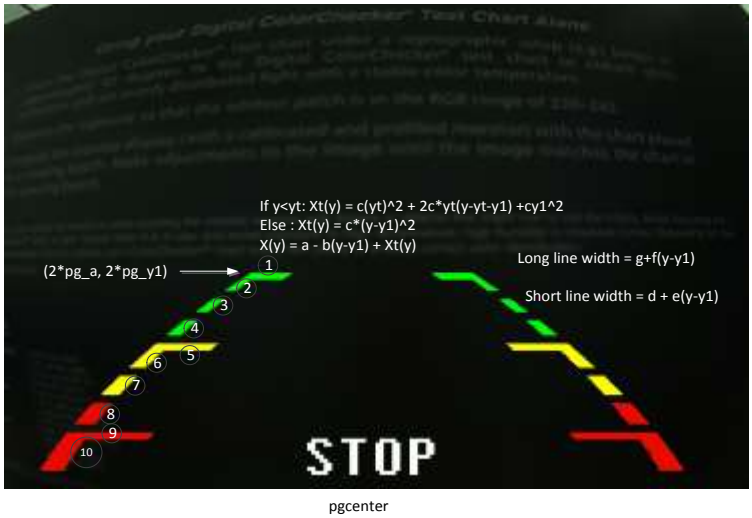


Figure 13-3 Parking Guide Example

15.3. Text Menu

Text menu was designed for displaying text information for users to help product installation and optimization. Text menu is consisted of character font information, character text information, line text information, line pointer information.

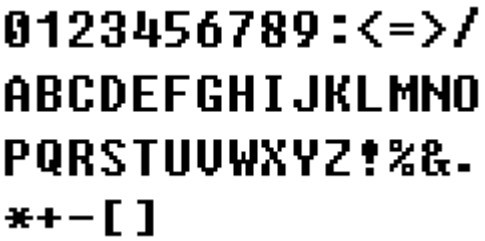


Figure 13-4 Character Font Information

Font information for a maximum of 51 characters can be saved simultaneously, and including the blank character provided as base a maximum of 52 font information is saved.

Figure 13-5 Text Menu Example

16. Formatter

16.1. Overview

Main functions of Formatter block are as below:

- Bayer 8/10 bit
- YCbCr 4:2:2
- RGB565/555
- Vsync/Hsync/pclock polarity control
- Hsync control in VBLANK
- OPB(Optical Black) data output control
- Pixel data sequence control
- Bit position control when the output data is 8 bit

CP8210 receives Y, C data and can output Bayer 8/10 bit, YCbCr 4:2:2 and RGB565/555 format digital data. Digital data can be output in 720x480, 640x480 modes and supports CCIR656 output. In addition the polarity of Vsync/Hsync/pclock signals can be controlled and the output data sequences can be set in a preferred order. When in 8 bit output mode, the 8bit data MSB location can be changed.

16.2. Timing Diagram

- YCbCr 4:2:2 mode

YCbCr 4:2:2 format data can be output through the PDATA[9:0] port. Since the final output is 8 bit, only 8 port out of the PDATA 10bit port is used and 8 bit data location can be changed using PDATA_CON[1:0] value. Also, depending on the DATA_FMT_CON[4:3] register value, the data sequence can be changed as shown in Figure 16-1

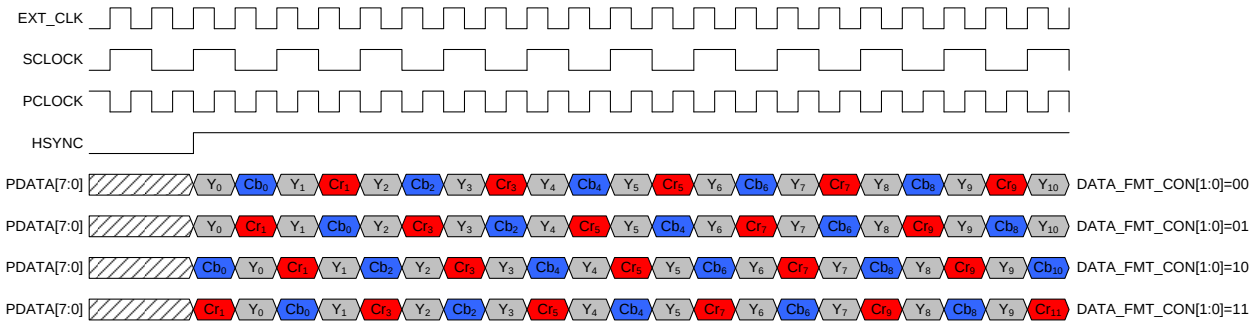
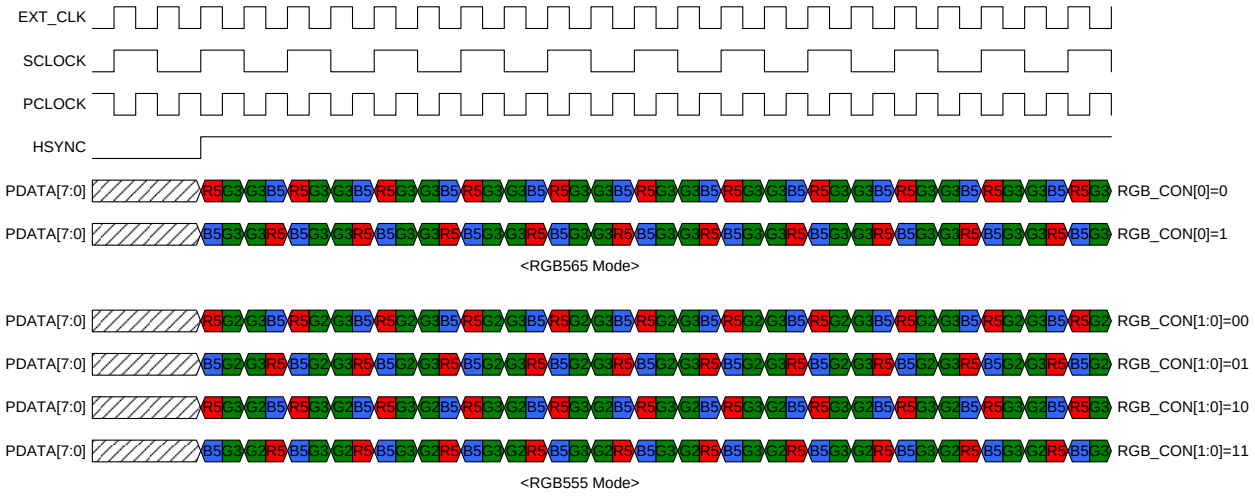


Figure 16-1 YCbCr Mode

- RGB565/555

RGB565/555 format data can be output through the PDATA[9:0] port. The final output is 8 bit in case of RGB565, and 8 or 7 bit in case of RGB555, and thus the output data location can be decided using the RGB_CON[1] value of the 10bit port PDATA. Also, depending on the RGB_CON[0] register value, the data sequence can be changed as shown below in Figure 16-2.



Mode	RGB_CON[1:0]	PDATA[7:0]
RGB555	00	0 $R_4R_3R_2R_1R_0G_4G_3$ $G_2G_1G_0B_4B_3B_2B_1B_0$
	01	0 $B_4B_3B_2B_1B_0G_4G_3$ $G_2G_1G_0R_4R_3R_2R_1R_0$
	10	$R_4R_3R_2R_1R_0G_4G_3G_2$ $G_1G_0B_4B_3B_2B_1B_0$ 0
	11	$B_4B_3B_2B_1B_0G_4G_3G_2$ $G_1G_0R_4R_3R_2R_1R_0$ 0

Figure 16-2 RGB565/555 Mode

- Bayer 8bit/10bit

Bayer 8 bit/10 bit format data can be output through the PDATA[9:0] port. Final output of Bayer 8 bit is 8 bit and so only 8 ports of 10 bit port PDATA is used and 8 bit data location can be decided using the PDATA_CON[1:0] value. Also, depending on the RGB_CON[3:2] register value, the data sequence can be changed as shown below in Figure 16-3

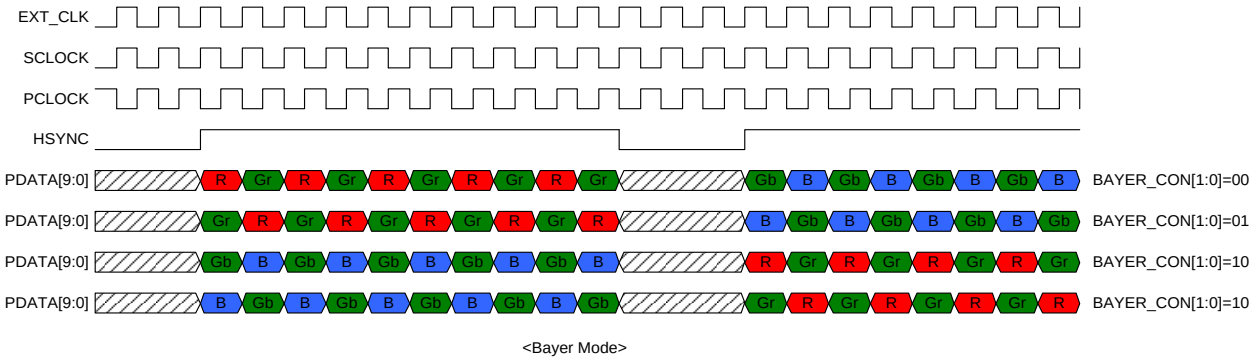


Figure 16-3 Bayer 8/10 bit Mode

17. Auto Control Function

CP8210 has auto control functions such as AE, Anti-Flicker, and AWB. These functions are not all processed in the ISP block, but transfers the information to the MCU that can operate the auto control algorithm. As shown in Figure 17-1 the brightness(Y) data for Anti-Flicker and RGB data for AWB are transferred to the MCU and depending on the calculation results of each algorithm, expose time, and RGB gain are performed.

.

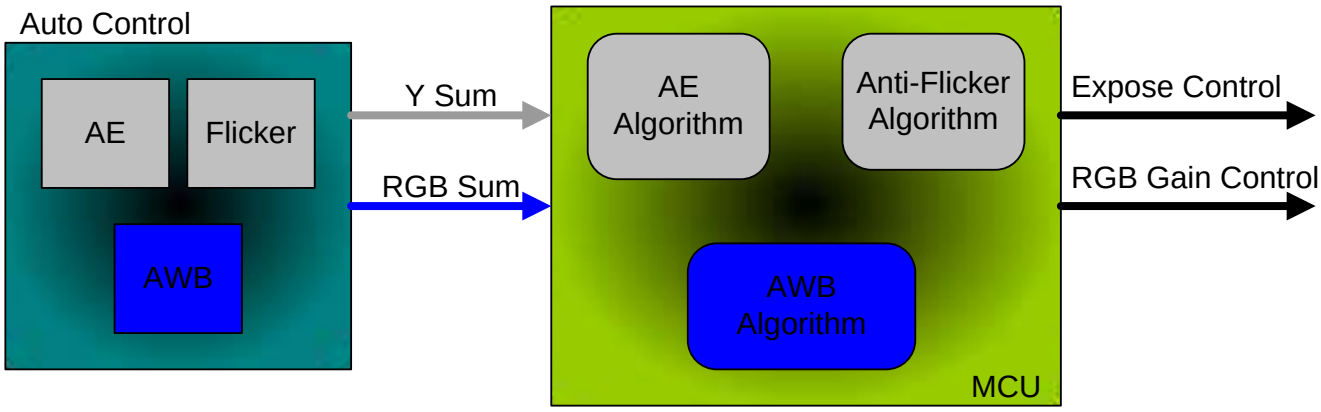


Figure 17-1 Auto Control Function

18. SMPTE 296M(HD size)

18.1. Overview

CP8210 supports SPMTE 296M, PDATA[19:10] is Y Channel, PDATA[9:0] is CbCr Channel. Data Format is YCbCr 4:2:2 format, Pixel Rate is 1280x720 60fps@74.25 MHz. Figure 18-1 and Figure 18-3 shows SMPTE 296M timing diagram. Bit width of each channels is default and 10 bit, Each channel bit width can be changed to 8bit by setting resigter. TRS(Timing Reference Sequence) contains information of a beginning and an end of video, information of VSYNC, HSYNC. CP8210 supports 60 fps, 50 fps that defined from SMPTE 296M, supports 30 fps, 25 fps by adjusting frame width of resister setting

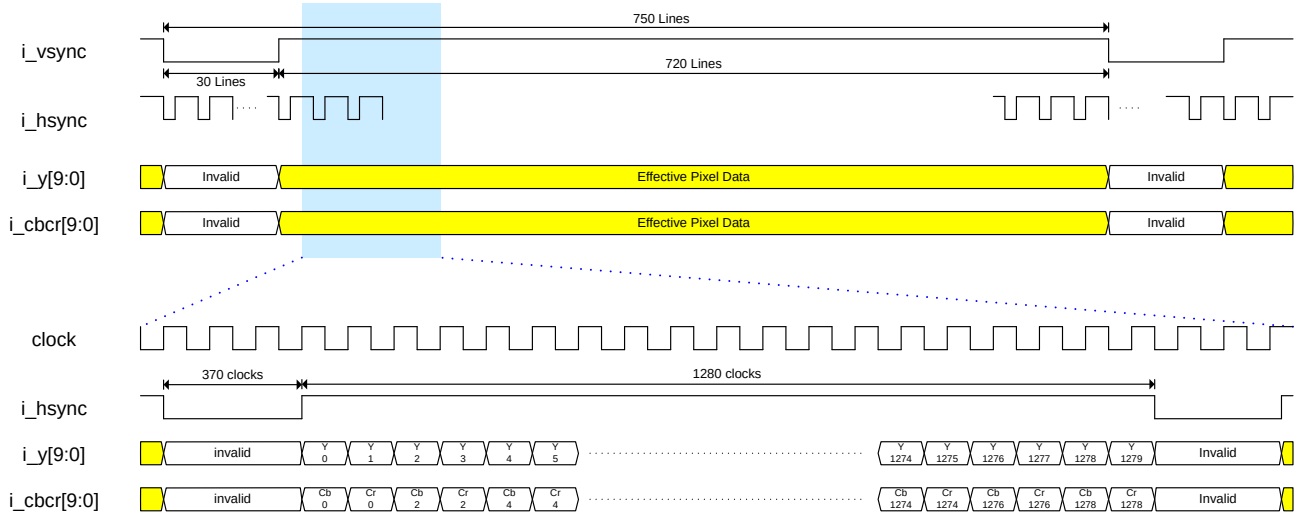


Figure 18-1 60 fps timing diagram

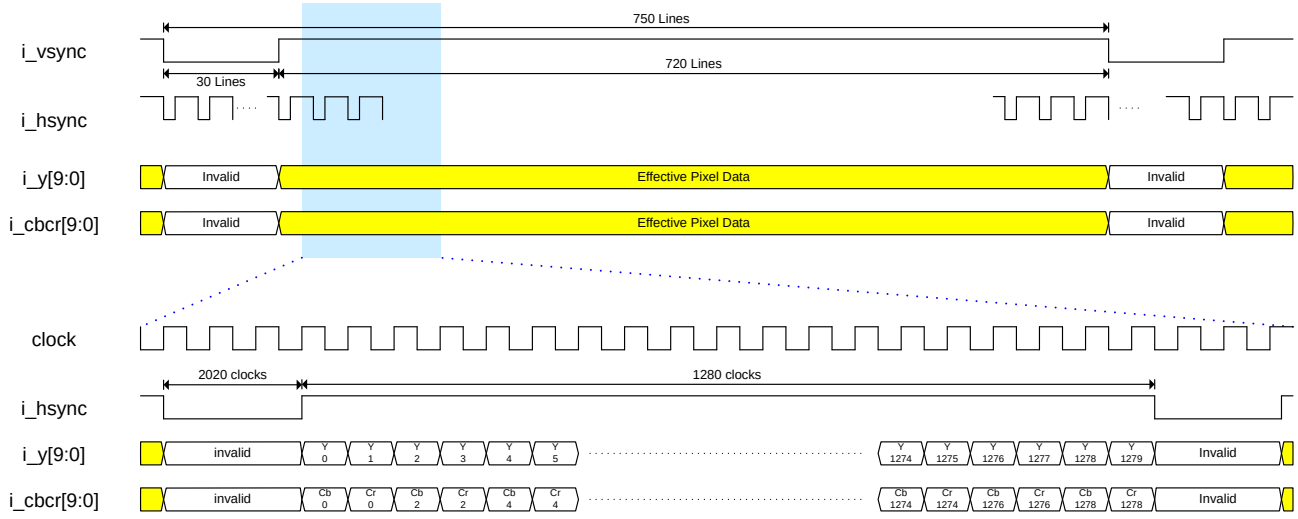


Figure 18-2 30 fps timing diagram

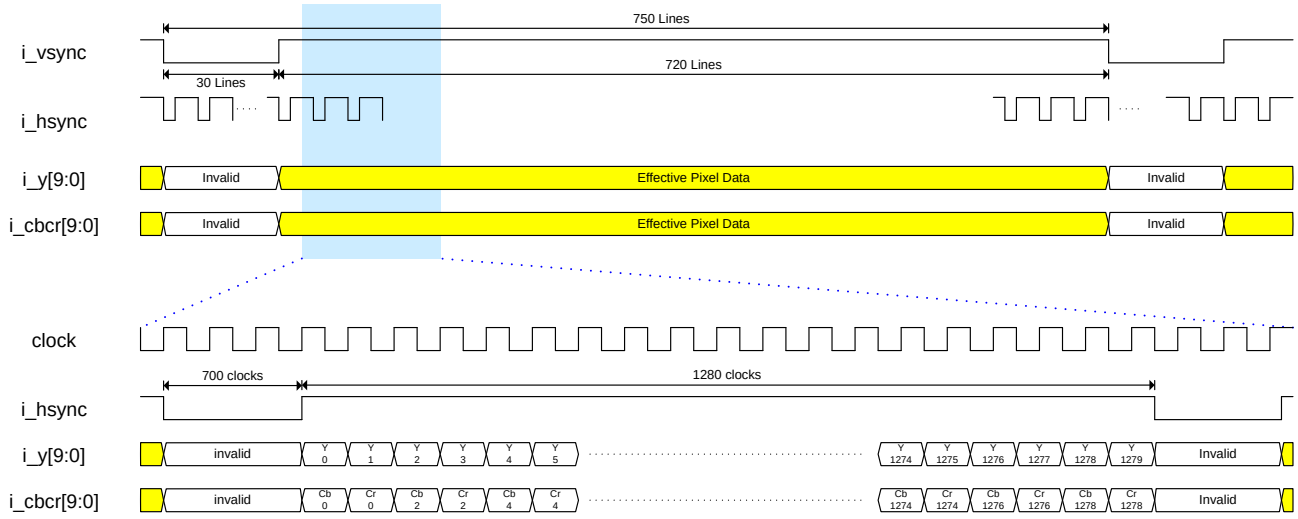


Figure 18-3 50 fps timing diagram

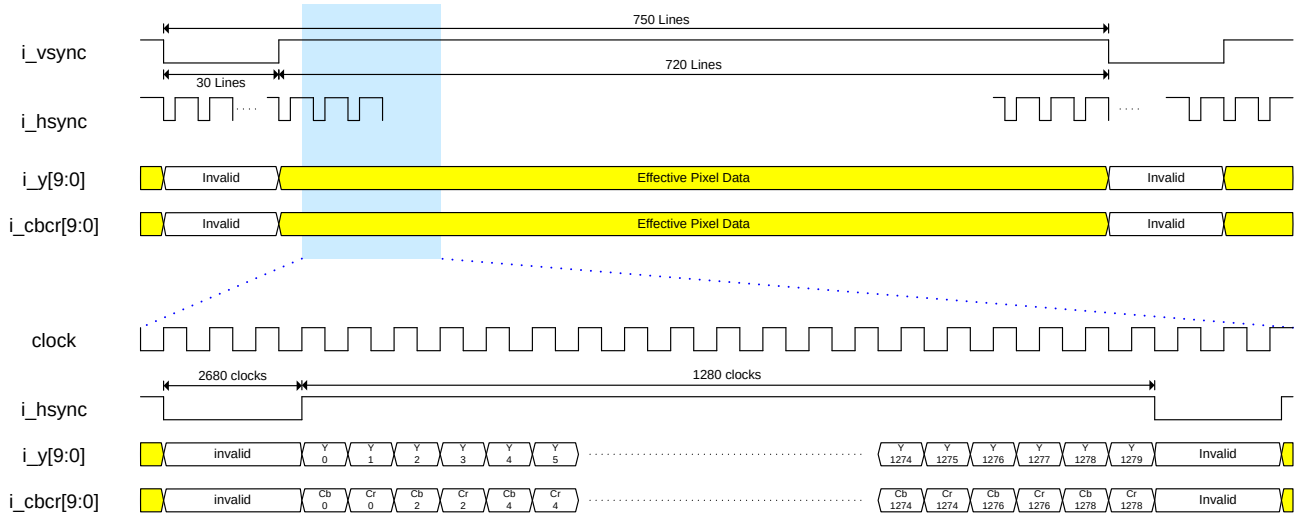


Figure 18-4 25 fps timing diagram

18.2. Video Timing

Ditigal video signal indicates a vlanking interval section of analog video signal as EVA(End of Acctive Video) and SAV(Start of Active Video). It provides a Vertical Blanking and Horizontal Blaking sections from a combination of EAV and SAV. It uses the following 3 information for status word which is the last data of EAV and SAV

.

1)V (Vertical blanking)
2)H (Horizontal blanking)
3)F (Field)

CP8210 is progressive and F(field) is always " 0"
EAV and SAV sequence is shown on Table 18-1, the status wors is as in the following.

1)F = " 0" for Filed 1 F = " 1" for Field 2
2)V = " 1" during vertical blanking
3)H = " 0" at SAV H = " 1" at EAV
4)P3 ~ P0 = protection bits :
i) P3 = V (+) H
ii) P2 = F (+) H
iii) P1 = F (+) V
iv) P0 = F (+) V (+) H

above are Exclusive OR function.

	8-bit Data								10-bit Data	
	D9 (MSB)	D8	D7	D6	D5	D4	D3	D2	D1	D0
preamble	1	1	1	1	1	1	1	1	1	1
	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0
status word	1	F	V	H	P3	P2	P1	P0	0	0

Table 18-1 EAV, SAV sequence

Vertical timing according to each fram rates shown at Image 1.3 and 1.4
Set the frame rate through H_DUMMY (0x50B8, 0x50B9) register. .

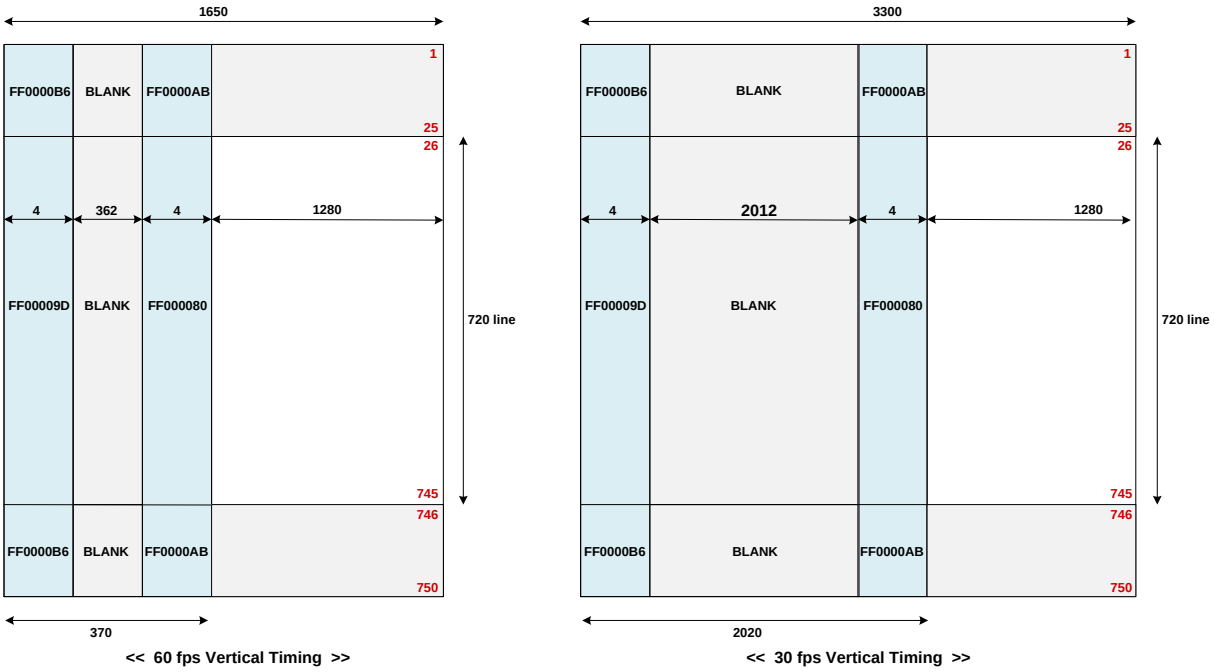


Figure 18-5 TRS & Display Timing Diagram @60fps, 30fps

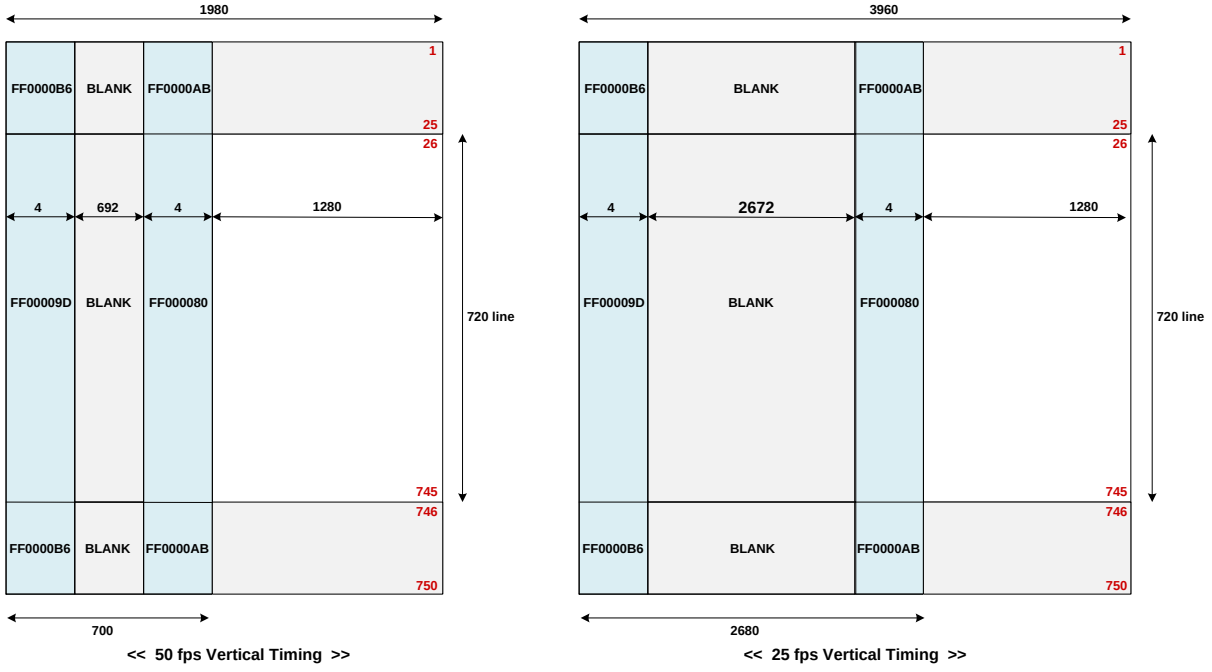


Figure 18-6 TRS & Display Timing Diagram @50fps, 25fps

19. Register definition

19.1. System

ADDRESS (HEX)	REGISTER NAME	R/W	DEFAULT (HEX)	DESCRIPTION
0x4000	PRODUCT_ID1	R	0x51	Product ID1
0x4001	PRODUCT_ID2	R	0x12	Product ID2
0x4002	PRODUCT_ID3	R	0xA0	Product ID3
0x4003	PIXEL_TYPE	R/W	0xA5	bit[7:0] : pixel type and revision number
0x4004	CLOCK_CONFIG	R/W	0xE5	[7] : crystal enable [6:5] : crystal output drive strength selection 00 : 1mA 01 : 2mA 10 : 4mA 11 : 8mA [4] : soft reset [3:2] : Sensor Clock 00 : Ext Clock 01 : Ext Clock / 2 10 : Ext Clock / 4 11 : reserved [1:0] : Main Clock 00 : Ext Clock 01 : Ext Clock / 2 10 : Ext Clock / 4 11 : reserved
0x4005	DEVICE_CONTROL	R/W	0x02	[7] : sleep [6] : power down mode selection [5] : pull down if powerdown at gpio & pbus [4] : reserved [3] : ISP enable [2] : TG enable [1] : MCU reset [0] : MCU enable
0x4006	I2C_SLAVE_ID	R/W	0x77	I2C Slave Device ID Value ID = [Value[7:1], R/W Flag[0]]
0x4007	I2C_SLAVE_LAST_INDEX	R	0x00	I2C Last Index address
0x4008	I2C_SLAVE_GLITCH	W	0x08	I2C slave glitch
0x4009	I2C_MASTER_START_REG	W	0x00	[7:1] : reserved [0] : i2c master start
0x400A	I2C_MASTER_STATUS	R	0x00	I2C Status register 0x00 : IDLE 0xAA : Transmit Success 0xBB : Transmit Fail 0xCC : I2C Line Busy
0x400B	I2C_MASTER_CONTROL	R/W	0xC0	I2C Master Control [2:0] : Transmit Byte Select 000 : 1 Byte Transfer 001 : 2 Byte Transfer 010 : 3 Byte Transfer 011 : 4 Byte Transfer 1xx : 5 Byte Transfer [3] : Dummy Write On [4] : Read Restart On [7:5] : I2C Clock Ratio Select [7:5] Trans act grap End

				3'b000 / 10'd100 / 10'd200 / 10'd300 / 10d'400 3'b001 / 10'd150 / 10'd300 / 10'd450 / 10d'600 3'b010 / 10'd200 / 10'd400 / 10'd600 / 10d'800 3'b011 / 10'd250 / 10'd500 / 10'd750 / 10d'1000 3'b100 / 10'd50 / 10'd100 / 10'd150 / 10d'200 3'b101 / 10'd25 / 10'd50 / 10'd75 / 10d'100 3'b110 / 10'd12 / 10'd24 / 10'd36 / 10d'48 3'b111 / 10'd6 / 10'd12 / 10'd18 / 10d'24
0x400C	I2C_TARGET_ADDRESS	R/W	0x00	I2C target device id
0x400D	I2C_TARGET_INDEX	R/W	0x00	I2C target Index
0x400E	I2C_TARGET_DATA1	R/W	0x00	I2C target data1
0x400F	I2C_TARGET_DATA2	R/W	0x00	I2C target data2
0x4010	I2C_TARGET_DATA3	R/W	0x00	I2C target data3
0x4011	I2C_TARGET_DATA4	R/W	0x00	I2C target data4
0x4012	I2C_TARGET_DATA5	R/W	0x00	I2C target data5
0x4013	EEPROM_CONFIG	R/W	0x00	[7:1] : reserved [0] : eeprom disable
0x4014	I2C_TARGET_RDATA_H	R	0x00	I2C target Read data[15:8]
0x4015	I2C_TARGET_RDATA_L	R	0x00	I2C target Read data[7:0]
0x4016	LUMP_INTERVAL	R/W	0x00	Interval[3:0] / Interval decision value 4'b1111 / 11'd50 4'b1110 / 11'd100 4'b1101 / 11'd150 4'b1100 / 11'd200 4'b1011 / 11'd250 4'b1010 / 11'd300 4'b1001 / 11'd350 4'b1000 / 11'd400 4'b0111 / 11'd450 4'b0110 / 11'd500 4'b0101 / 11'd550 4'b0100 / 11'd600 4'b0011 / 11'd700 4'b0010 / 11'd800 4'b0001 / 11'd900 4'b0000 / 11'd1023
0x4017	HOST_COMMAND_FLAGS	W	0x00	[7:0] : Host command flags When write, it generates MCU interrupt. When read, it clears MCU interrupt.
0x4018	HOST_COMMAND_DATA0	W	0x00	[7:0] : Host command data 0
0x4019	HOST_COMMAND_DATA1	W	0x00	[7:0] : Host command data 1
0x401A	HOST_COMMAND_DATA2	W	0x00	[7:0] : Host command data 2
0x401B	HOST_COMMAND_RESULT0	R/w	0x00	[7:0] :Command Result 0
0x401C	HOST_COMMAND_RESULT1	R/W	0x00	[7:0] :Command Result 1

0x401D	HOST_COMMAND_RESULT2	R/W	0x00	[7:0] :Command Result 2
0x401E	HOST_COMMAND_RESULT3	R/W	0x00	[7:0]: Command Result 3
0x401F	GPIO_DIRECTION_CONTROL	R/W	0xFF	[7:0] : GPIO[7:0] direction control 0 :output 1 : input
0x4020	GPIO_IN_OUT_DATA	R/W	0x00	[7:0] : GPIO[7:0] input/output data
0x4021	GPIO_PULL_UD_CON	R/W	0xFF	[7:0] : GPIO[7:0] pull up/down control 0 :disable 1 : enable
0x4022	GPIO_PULL_UD_SEL	R/W	0x00	[7:0] : GPIO[7:0] pull up/down selection 0 : pull-down 1 : pull-up
0x4023	GPIO_DRIVE_STRENGTH_SEL	R/W	0x55	[7:6] : GPIO[7:6] drive strength selection 00 : 1mA 01 : 2mA 10 : 4mA 11 : 8mA [5:4] : GPIO[5:4] drive strength selection 00 : 1mA 01 : 2mA 10 : 4mA 11 : 8mA [3:2] : GPIO[3:2] drive strength selection 00 : 1mA 01 : 2mA 10 : 4mA 11 : 8mA [1:0] : GPIO[1:0] drive strength selection 00 : 1mA 01 : 2mA 10 : 4mA 11 : 8mA
0x4024	MEM_ADDR_H	R/W	0x00	[7:0] : High byte of memory address
0x4025	MEM_ADDR_L	R/W	0x00	[7:0] : Low byte of memory address
0x4026	MEM_DATA	R/W	0x00	[7:0] : memory data
0x4027	MEM_CON	R/W	0x00	[7:4] : reserved [3] : fix index address (“1” -> i2c index address is fixed) [2] : reserved [1] : code memory write enable. [0] : code or data memory selection 0 : data 1 : code
0x4028	CHECK_SUM_H	R/W	0x00	[7:0] : High byte of code data check sum
0x4029	CHECK_SUM_L	R/W	0x00	[7:0] : High byte of code data check sum
0x402A	CRC_H	R/W	0x00	[7:0] : High byte of code data CRC
0x402B	CRC_L	R/W	0x00	[7:0] : Low byte of code data CRC
0x402C	CRC_CON	R/W	0x00	[7:1] : reserved [0] : CRC control 0 : disable 1 : enable
0x4054	PDATA_CON1	R/W	0xA0	[7:6] : P_1_0 control 00 : output PDATA[1:0] 01 : floating PDATA[1:0] 10 : floating & pull-down PDATA[1:0] 11 : reserved [5:4] : P_9_2 control 00 : output PDATA[9:2] 01 : floating PDATA[9:2] 10 : floating & pull-down PDATA[9:2] 11 : reserved [3] : PLL test mode [2:0]: reserved

0x4055	PDATA_CON2	R/W	0x01	[7] : GPIO[2] to PCLOCK 0 : disable 1 : enable [6] : GPIO[3] to VSYNC 0 : disable 1 : enable [5] : GPIO[4] to HSYNC 0 : disable 1 : enable [4] : GPIO[5] to PDATA[0] 0 : disable 1 : enable [3] : GPIO[6] to PDATA[1] 0 : disable 1 : enable [2] : GPIO[7] to PDATA[2] 0 : disable 1 : enable [1:0] : PDATA drive strength selection 00 : 1mA 01 : 2mA 10 : 4mA 11 : 8mA
0x4060	IMG_OUT_MUX	R/W	0x00	[7:0] : mux selection 0x00 : normal 0x01 : sensor_l 0x02 : sensor_s 0x03 : tg long or bypass 0x04 : tg short 0x05 : wdr 0x06 : intp R 0x07 : intp G 0x08 : intp B 0x09 : isp1, Y 0x0A : isp1, Cb 0x0B : isp1 Cr 0x0C : isp2, Y 0x0D : isp2, Cb 0x0E : isp2, Cr 0x0F : isp2, CbCr
0x4070	PLL_CON	R/W	0x01	[7:3] : reserved [2] : Reference Clock Bypass Enable 0 : disable 1 : enable [1] : FOUT Enable 0 : enable 1 : disable [0] : PLL Enable 0 : disable 1 : enable
0x4071	PLL_CAP2_EN	R/W	0x07	[7:0] : loop filter cap2 control
0x4072	PLL_CAP1_EN	R/W	0x00	[7:0] : loop filter cap1 control
0x4073	PLL_RES0_EN	R/W	0x38	[7:0] : loop filter resister control
0x4074	PLL_PFD_LOCK_DLY	R/W	0x18	[7:4] : PFD delay control [3:0] : LOCK delay control
0x4075	PLL_BCONT	R/W	0x27	[7:6] : reserved [5] : Bias control [4:0] : Charge pump bias control
0x4076	PLL_OD	R/W	0x01	[7:2] : reserved [1] : ADC divider value control [0] : VCOOUT Divider Value Control
0x4077	PLL_S_P	R/W	0x04	[7] : reserved [6:4] : Divider value control for Fout [3:0] : Reference Clock Divider Value Control Pin
0x4078	PLL_M	R/W	0x1E	[7:0] : Feedback Divider Value control
0x4079	PLL_CTRL_HIGH	R/W	0x00	[7:6] : reserved [5:0] : High level setting value for ADC Clock

0x407A	PLL_CTRL_PERIOD	R/W	0x01	[7:6] : reserved [5:0] : Divider setting value for ADC Clock
0x4080	RESULT_0	R/W	0x00	result 0
0x4081	RESULT_1	R/W	0x00	result 1
0x4082	RESULT_2	R/W	0x00	result 2
0x4083	RESULT_3	R/W	0x00	result 3
0x4084	RESULT_4	R/W	0x00	result 4
0x4085	RESULT_5	R/W	0x00	result 5
0x4086	RESULT_6	R/W	0x00	result 6
0x4087	RESULT_7	R/W	0x00	result 7
0x4088	RESULT_8	R/W	0x00	result 8
0x4089	RESULT_9	R/W	0x00	result 9
0x408A	RESULT_10	R/W	0x00	result 10
0x408B	RESULT_11	R/W	0x00	result 11
0x408C	RESULT_12	R/W	0x00	result 12
0x408D	RESULT_13	R/W	0x00	result 13
0x408E	RESULT_14	R/W	0x00	result 14
0x408F	RESULT_15	R/W	0x00	result 15
0x4090	RESULT_16	R/W	0x00	result 16
0x4091	RESULT_17	R/W	0x00	result 17
0x4092	RESULT_18	R/W	0x00	result 18
0x4093	RESULT_19	R/W	0x00	result 19
0x4094	RESULT_20	R/W	0x00	result 20
0x4095	RESULT_21	R/W	0x00	result 21
0x4096	RESULT_22	R/W	0x00	result 22
0x4097	RESULT_23	R/W	0x00	result 23
0x4098	RESULT _24	R/W	0x00	result 24
0x4099	RESULT_25	R/W	0x00	result 25
0x409A	RESULT_26	R/W	0x00	result 26
0x408B	RESULT_27	R/W	0x00	result 27
0x409C	RESULT_28	R/W	0x00	result 28
0x409D	RESULT_29	R/W	0x00	result 29
0x409E	RESULT_30	R/W	0x00	result 30
0x409F	RESULT_31	R/W	0x00	result 31
0x40A0	PWM_CON	R/W	0x00	[7] : PWM busy (read only) [6:5] : reserved [4] : PWM start. [3]: reserved [2] : PWM start synchronize VSYNC.falling edge. [1] : PWM loop [0] : PWM enable
0x40A1	PWM_CYC_NUM	R/W	0x00	[7:0]: PWM cycle number
0x40A2	PWM0_POINT1_H	R/W	0x00	[7:0] : High byte of PWM0 point 1
0x40A3	PWM0_POINT1_L	R/W	0x00	[7:0] : Low byte of PWM0 point 1
0x40A4	PWM0_POINT2_H	R/W	0x00	[7:0] : High byte of PWM0 point 2
0x40A5	PWM0_POINT2_L	R/W	0x00	[7:0] : Low byte of PWM0 point 2
0x40A6	PWM0_POINT3_H	R/W	0x00	[7:0] : High byte of PWM0 point 3

0x40A7	PWM0_POINT3_L	R/W	0x00	[7:0] : Low byte of PWM0 point 3
0x40A8	PWM0_POINT4_H	R/W	0x00	[7:0] : High byte of PWM0 point 4
0x40A9	PWM0_POINT4_L	R/W	0x00	[7:0] : Low byte of PWM0 point 4
0x40AA	PWM1_POINT1_H	R/W	0x00	[7:0] : High byte of PWM1 point 1
0x40AB	PWM1_POINT1_L	R/W	0x00	[7:0] : Low byte of PWM1 point 1
0x40AC	PWM1_POINT2_H	R/W	0x00	[7:0] : High byte of PWM1 point 2
0x40AD	PWM1_POINT2_L	R/W	0x00	[7:0] : Low byte of PWM1 point 2
0x40AE	PWM1_POINT3_H	R/W	0x00	[7:0] : High byte of PWM1 point 3
0x40AF	PWM1_POINT3_L	R/W	0x00	[7:0] : Low byte of PWM1 point 3
0x40B0	PWM1_POINT4_H	R/W	0x00	[7:0] : High byte of PWM1 point 4
0x40B1	PWM1_POINT4_L	R/W	0x00	[7:0] : Low byte of PWM1 point 4
0x40B2	PWM2_POINT1_H	R/W	0x00	[7:0] : High byte of PWM2 point 1
0x40B3	PWM2_POINT1_L	R/W	0x00	[7:0] : Low byte of PWM2 point 1
0x40B4	PWM2_POINT2_H	R/W	0x00	[7:0] : High byte of PWM2 point 2
0x40B5	PWM2_POINT2_L	R/W	0x00	[7:0] : Low byte of PWM2 point 2
0x40B6	PWM2_POINT3_H	R/W	0x00	[7:0] : High byte of PWM2 point 3
0x40B7	PWM2_POINT3_L	R/W	0x00	[7:0] : Low byte of PWM2 point 3
0x40B8	PWM2_POINT4_H	R/W	0x00	[7:0] : High byte of PWM2 point 4
0x40B9	PWM2_POINT4_L	R/W	0x00	[7:0] : Low byte of PWM2 point 4
0x40BA	PWM3_POINT1_H	R/W	0x00	[7:0] : High byte of PWM3 point 1
0x40BB	PWM3_POINT1_L	R/W	0x00	[7:0] : Low byte of PWM3 point 1
0x40BC	PWM3_POINT2_H	R/W	0x00	[7:0] : High byte of PWM3 point 2
0x40BD	PWM3_POINT2_L	R/W	0x00	[7:0] : Low byte of PWM3 point 2
0x40BE	PWM3_POINT3_H	R/W	0x00	[7:0] : High byte of PWM3 point 3
0x40BF	PWM3_POINT3_L	R/W	0x00	[7:0] : Low byte of PWM3 point 3
0x40C0	PWM3_POINT4_H	R/W	0x00	[7:0] : High byte of PWM3 point 4
0x40C1	PWM3_POINT4_L	R/W	0x00	[7:0] : Low byte of PWM3 point 4
0x40C2	PWM_WIDTH_H	R/W	0x00	[7:0] : High byte of PWM width
0x40C3	PWM_WIDTH_L	R/W	0x00	[7:0] : Low byte of PWM width
0x40C5	PWM2GPIO	R/W	0x00	[7] : Inverting PWM3 [6] : Inverting PWM2 [5] : Inverting PWM1 [4] : Inverting PWM0 [3] : assign PWM3 to GPIO[3] [2] : assign PWM2 to GPIO[2] [1] : assign PWM1 to GPIO[1] [0] : assign PWM0 to GPIO[0]

19.2. TG, BLC

ADDRESS (HEX)	REGISTER NAME	R/W	DEFAULT (HEX)	DESCRIPTION
TG	**(VSYNC SYNCHRONIZED)**			
0x5000	L_INT_TIME_H	R/W	0x04	[7:0] : High byte of Large pixel Integration(Exposure) time
0x5001	L_INT_TIME_L	R/W	0x10	[7:0] : Low byte of Large pixel Integration(Exposure) time
0x5002	S_INT_TIME_H	R/W	0x02	[7:0] : High byte of Small pixel Integration(Exposure) time
0x5003	S_INT_TIME_L	R/W	0x08	[7:0] : Low byte of Small pixel Integration(Exposure) time
0x5004	HBLANK	R/W	0x5F	[7:0] : Horizontal blank blank time = HBLANK[7:0]*4
0x5005	VBLANK	R/W	0x08	[7:0] : Vertical blank 960p : 0x08 720p : 0x02
0x5006	VDUMMY	R/W	0x02	[7:0] : Vertical dummy
0x5007	L_A_F_GAIN1_H	R/W	0x00	[7:3] : reserved [2:0] : High byte of Large pixel feedback cap enable for global gain 1
0x5008	L_A_F_GAIN1_L	R/W	0x02	[7:0] : Low byte of Large pixel feedback cap enable for global gain 1
0x5009	L_A_F_GAIN2_H	R/W	0x00	[7:3] : reserved [2:0] : High byte of Large pixel feedback cap enable for global gain 2
0x500A	L_A_F_GAIN2_L	R/W	0x02	[7:0] : Low byte of Large pixel feedback cap enable for global gain 2
0x500B	S_A_F_GAIN1_H	R/W	0x00	[7:3] : reserved [2:0] : High byte of Small pixel feedback cap enable for global gain 1
0x500C	S_A_F_GAIN1_L	R/W	0x02	[7:0] : Low byte of Small pixel feedback cap enable for global gain 1
0x500D	S_A_F_GAIN2_H	R/W	0x00	[7:3] : reserved [2:0] : High byte of Small pixel feedback cap enable for global gain 2
0x500E	S_A_F_GAIN2_L	R/W	0x02	[7:0] : Low byte of Small pixel feedback cap enable for global gain 2
0x500F	L_A_S_GAIN1_H	R/W	0x00	[7:3] : reserved [2:0] : High byte of Large pixel input cap enable for global gain 1
0x5010	L_A_S_GAIN1_L	R/W	0x01	[7:0] : Low byte of Large pixel input cap enable for global gain 1
0x5011	L_A_S_GAIN2_H	R/W	0x00	[7:3] : reserved [2:0] : High byte of Large pixel input cap enable for global gain 2
0x5012	L_A_S_GAIN2_L	R/W	0x01	[7:0] : Low byte of Large pixel input cap enable for global gain 2
0x5013	S_A_S_GAIN1_H	R/W	0x00	[7:3] : reserved [2:0] : High byte of Small pixel input cap enable for global gain 1
0x5014	S_A_S_GAIN1_L	R/W	0x01	[7:0] : Low byte of Small pixel input cap enable for global gain 1
0x5015	S_A_S_GAIN2_H	R/W	0x00	[7:3] : reserved [2:0] : High byte of Small pixel input cap enable for global gain 2
0x5016	S_A_S_GAIN2_L	R/W	0x01	[7:0] : Low byte of Small pixel input cap enable for global gain 2
0x5017	A_F_GAIN3	R/W	0x11	[7:4] : Large feedback cap enable for column gain [3:0] : Small feedback cap enable for column gain
0x5018	A_S_GAIN3	R/W	0x11	[7:4] : Large input cap enable for column gain [3:0] : Small input cap enable for column gain
0X5019	L_D_GAIN	R/W	0x00	[7:5] : Large Pixel Global Digital Gain1 control [4:0] : Large Pixel Global Digital Gain2 control Gain = 2^L_D_GAIN[7:5]*(1 + L_D_GAIN[4:0]/32)
0x501A	S_D_GAIN	R/W	0x00	[7:5] : Small Pixel Global Digital Gain1 control [4:0] : Small Pixel Global Digital Gain2 control Gain = 2^S_D_GAIN[7:5]*(1 + S_D_GAIN[4:0]/32)
0x501B	IMG_CON	R/W	0x00	[7:3] : reserved [2] : Scan mode selection 0 : 960 line scan 1 : 720 line scan [1] : Vertical mirror [0] : Horizontal mirror
0x501C	720_SCAN_ST_LINE	R/W	0x78	[7:0] : 720 scan start line
0x50C0	TP_IMG_CON	R/W	0x00	[7:6] : reserved

				[5] : Test Image Enable (0 : disable, 1 : enable) [4:3] : Test Image Data Select 00 : read out address 01 : large int. address 1x : small int. address [2:0] : Test Image Type 000 : diagonal 001 : horizontal 010 : vertical 011 : single color 100 : color bar 101 : gray chart 110 : gray chart for wdr
0x50C1	TP_IMG_HI	R/W	0x03	[7:6] : High byte of R color for test image [5:4] : High byte of Gr color for test image [3:2] : High byte of Gb color for test image [1:0] : High byte of B color for test image
0x50C2	TP_IMG_R_LO	R/W	0x00	[7:0] : Low byte of R color value for test image
0x50C3	TP_IMG_Gr_LO	R/W	0x00	[7:0] : Low byte of Gr color value for test image
0x50C4	TP_IMG_Gb_LO	R/W	0x00	[7:0] : Low byte of Gb color value for test image
0x50C5	TP_IMG_B_LO	R/W	0xFF	[7:0] : Low byte of B color value for test image
0x50C6	SYNC_REG_UP_CON	R/W	0x02	[7:2] : reserved [1] : first frame vsync signal mask control 0 : mask disable 1 : mask enable [0] : synchronous register update control 0 : vsync rising time update 1 : immediately update
BLC **(VSYNC SYNCHRONIZED)**				
0x5100	BLC_MODE1	R/W	0x37	[7] : reserved [6] : bypass [5] : OB2 DPC Enable (Row BLC Area) [4] : OB1 DPC Enable (ABLC, DBLC Area) [3] : Digital Row BLC Enable [2] : Digital BLC Enable [1] : OS Enable [0] : RST Enable
0x5101	BLC_MODE2	R/W	0x13	[7:5] : Reserved [4]: Gain Change Detection Enable [3] : OS 1step down enable [2] : Hold Enable [1] : DBLC Threshold Enable [0] : ABLC Threshold Enable
0x5102	BLC_MODE3	R/W	0x00	[7:6] : Reserved [5:4] : dblc moving average frame count 00 : 1frame 01: 8frame 10:16frame 11:32frame [3:2] : os moving average frame count 00 : 1frame 01: 8frame 10:16frame 11:32frame [1:0] : rst moving average frame count 00 : 1frame 01: 8frame 10:16frame 11:32frame
0x5105	ABLC_TGT	R/W	0x04	[7:0] : ABLC Target
0x5106	DBLC_TGT	R/W	0x00	[7:0] : DBLC Target

19.3. LSC, WDR

ADDRESS (HEX)	REGISTER NAME	R/W	DEFAULT (HEX)	DESCRIPTION
LENS SHADING CONTROL				
0x5200	LSC_CON	R/W	0x00	[7:2] : Reserved [1] : Small LSC enable 1'b0: Disable 1'b1: Enable [0] : Large LSC enable 1'b0: Disable 1'b1: Enable
0x5201	L_CENTER_H	R/W	0x0A	[7:3] : Reserved [2] : Long pixel High byte of y position [1:0] : Long pixel High byte of x position
0x5202	L_CENTER_X_L	R/W	0x80	[7:0] : Long pixel Low byte of x position
0x5203	L_CENTER_Y_L	R/W	0x68	[7:0] : Long pixel Low byte of y position
0x5204	L_C1_R	R/W	0x40	[7:0] : Long pixel R "c1"
0x5205	L_C1_GR	R/W	0x40	[7:0] : Long pixel Gr "c1"
0x5206	L_C1_GB	R/W	0x40	[7:0] : Long pixel Gb "c1"
0x5207	L_C1_B	R/W	0x40	[7:0] : Long pixel B "c1"
0x5208	L_OFFSET_R	R/W	0x00	[7:0] : Long pixel R offset(2's complement)
0x5209	L_OFFSET_GR	R/W	0x00	[7:0] : Long pixel Gr offset(2's complement)
0x520A	L_OFFSET_GB	R/W	0x00	[7:0] : Long pixel Gb offset(2's complement)
0x520B	L_OFFSET_B	R/W	0x00	[7:0] : Long pixel B offset(2's complement)
0x5211	S_CENTER_H	R/W	0x0A	[7:3] : Reserved [2] : Short pixel High byte of y position [1:0] : Short pixel High byte of x position
0x5212	S_CENTER_X_L	R/W	0x80	[7:0] : Short pixel Low byte of x position
0x5213	S_CENTER_Y_L	R/W	0x68	[7:0] : Short pixel Low byte of y position
0x5214	SL_C1_R	R/W	0x40	[7:0] : Short pixel R "c1"
0x5215	S_C1_GR	R/W	0x40	[7:0] : Short pixel Gr "c1"
0x5216	S_C1_GB	R/W	0x40	[7:0] : Short pixel Gb "c1"
0x5217	S_C1_B	R/W	0x40	[7:0] : Short pixel B "c1"
0x5218	S_OFFSET_R	R/W	0x00	[7:0] : Short pixel R offset(2's complement)
0x5219	S_OFFSET_GR	R/W	0x00	[7:0] : Short pixel Gr offset(2's complement)
0x521A	S_OFFSET_GB	R/W	0x00	[7:0] : Short pixel Gb offset(2's complement)
0x521B	S_OFFSET_B	R/W	0x00	[7:0] : Short pixel B offset(2's complement)
0x521C	COLOR_ORDER	R/W	0x00	[7:2] : Reserved [1:0] : First Color Selection 2'b00 : R 2'b01 : Gr 2'b01 : Gb 2'b01 : B
WDR (VSYNC SYNCHRONIZED)				
0x5300	LP_RATIO	R/W	0x80	[7:0] : LP Ratio for WDR Input Data (fraction 8bit)
0x5301	SP_RATIO	R/W	0x80	[7:0] : SP Ratio for WDR Input Data (fraction 8bit)
0x5302	WDR_GAIN_N	R/W	0x00	[7:0] : WDR Negative Gain (For Shadow Area)
0x5303	WDR_GAIN_P	R/W	0x00	[7:0] : WDR Positive Gain (For Highlight Area)
0x5304	WDR_REF_X	R/W	0x80	[7:0] : WDR X-axis Reference

0x5305	WDR_REF_Y	R/W	0x80	[7:0] : WDR Y-axis Reference
0x5306	WGT_LOW	R/W	0x80	[7:0] : Color Mapping Low Point
0x5307	WGT_HIGH	R/W	0xF0	[7:0] : Color Mapping High Point
0x5308	WDR_LMT_H	R/W	0xFF	[7:0] : WDR Shadow Area Gain Limit
0x5309	WDR_LMT_L	R/W	0x00	[7:0] : WDR Highlight Area Gain Limit
0x530A	SP_THR_UP	R/W	0x43	[7:0] : Sp Color Ratio Gain High Threshold (SP/WDR)
0x530B	SP_THR_DN	R/W	0x21	[7:0] : Sp Color Ratio Gain Low Threshold (SP/WDR)
0x530C	YG_MAP_UP	R/W	0xFF	[7:0] : Maximum Color Weight
0x530D	YG_MAP_DN	R/W	0x00	[7:0] : Minimum Color Weight
0x530E	WDR_CON	R/W	0x00	[7:3] : Reserved [2] : AWB data Selection 0 : RGB Blur Data sum 1 : RGB Center Data sum [1] : AWB Gain Mode sel 0 : Gain = Reg/128 + 1 1 : Gain = Reg/128 + 0.5 [0] : Median Filter Enable
0x530F	WDR_INOUT	R/W	0x03	<WDR Input Selection> [7:5] : Reserved [4] : Short Input Selection 0 : Short input <- Short Path 1 : Short input <- Long Path [3] : Long Input Selection 0 : Long input <- Long Path 1 : Long input <- Short Path <WDR Output Selection> [2:0] : Output Group 000 : WDR Image 001 : LP+SP Bayer Image 010 : SP Bayer Image 011 : LP Bayer Image 100 : WDR Gray Image 101 : LP+SP Gray Image 110 : SP Gray Image 111 : LP Gray Image
0x5311	WB_LR_GAIN	R/W	0x00	[7:0] : Long Red Pixel Gain for AWB
0x5312	WB_LGR_GAIN	R/W	0x00	[7:0] : Long Green(R) Pixel Gain for AWB
0x5313	WB_LGB_GAIN	R/W	0x00	[7:0] : Long Green(B) Pixel Gain for AWB
0x5314	WB_LB_GAIN	R/W	0x00	[7:0] : Long Blue Pixel Gain for AWB
0x5315	WB_SR_GAIN	R/W	0x00	[7:0] : Short Red Pixel Gain for AWB
0x5316	WB_SGR_GAIN	R/W	0x00	[7:0] : Short Green(R) Pixel Gain for AWB
0x5317	WB_SGB_GAIN	R/W	0x00	[7:0] : Short Green(B) Pixel Gain for AWB
0x5318	WB_SB_GAIN	R/W	0x00	[7:0] : Short Blue Pixel Gain for AWB
0x531A	LOCAL_RATIO	R/W	0x00	[7:1] : Reserved [0] : Local Ratio Enable 1'b0: Disable 1'b1: Enable
0x531B	SP_RATIO_LIMIT	R/W	0x80	[7:0] : Small Pixel Ratio Limit(fraction 8bit)
0x531C	RATIO_GAIN_H	R/W	0x03	[7:2] : Reserved [1:0] : High byte of Ratio Gain
0x531D	RATIO_GAIN_L	R/W	0xFF	[7:0] : Low byte of Ratio Gain
0x5320	CSAT_THR	R/W	0xF0	[7:0] : Pixel Saturation Threshold for Color error

0x5324	WDR_GAM_EN	R/W	0x02	[7:3] : Reserved [2] : Gamma Luminance Display [1] : LP/SP Gamma Selection 1'b0: SP Gamma 1'b1: LP Gamma [0] : Gamma enable
0x5326	MGR_SET	R/W	0x07	[7:6] : Reserved [5] : Vblank Hsync Out Disable [4] : Active Area Only Output Mode Enable [3] : Sensor Only Mode Enable [2] : Saturated LP color error fix Disable [1] : SP Gray Mapping Enable 1'b0: Differential Mode 1'b1: Ratio Mode [0] : LP Gray Mapping Enable 1'b0: Differential Mode 1'b1: Ratio Mode
0x5330	WDR_GAM_B0	R/W	0x1C	[7:0] : WDR Gamma Point 0 (8)
0x5331	WDR_GAM_B1	R/W	0x27	[7:0] : WDR Gamma Point 1 (16)
0x5332	WDR_GAM_B2	R/W	0x35	[7:0] : WDR Gamma Point 2 (32)
0x5333	WDR_GAM_B3	R/W	0x49	[7:0] : WDR Gamma Point 3 (64)
0x5334	WDR_GAM_B4	R/W	0x64	[7:0] : WDR Gamma Point 4 (128)
0x5335	WDR_GAM_B5	R/W	0x89	[7:0] : WDR Gamma Point 5 (255)
0x5336	WDR_GAM_B6	R/W	0xA4	[7:0] : WDR Gamma Point 6 (384)
0x5337	WDR_GAM_B7	R/W	0xBB	[7:0] : WDR Gamma Point 7 (512)
0x5338	WDR_GAM_B8	R/W	0xCF	[7:0] : WDR Gamma Point 8 (640)
0x5339	WDR_GAM_B9	R/W	0xE1	[7:0] : WDR Gamma Point 9 (768)
0x533A	WDR_GAM_B10	R/W	0xF1	[7:0] : WDR Gamma Point 10 (896)

19.4. ISP 1

ADDRESS (HEX)	REGISTER NAME	R/W	DEFAULT (HEX)	DESCRIPTION
DPC / COLOR INTPOLATION				
0x5400	DPC_CON	R/W	0x24	[7:2] : Reserved [1] : Compensation Data Selection 1’ b0: Neighborhood Similar Data 1’ b1: Neighborhood Median Data [0] : DPC Enable 1’ b0: Disable 1’ b1: Enable
0x5401	DPC_THR1_L	R/W	0xFF	[7:0] : DPC Threshold1
0x5402	DPC_THR2_L	R/W	0x20	[7:0] : DPC Threshold2
BAYER NOISE REDUCTION				
0x5420	BNR_CON	R/W	0x00	[7:6] : Reserved [5] : Pixel Position Selection [4] : Line Position Selection [3] : Red, Blue Pixel Average Type Selection 1’b0 : Average 1’b1 : Center pixel [2] : Green Pixel Average Type Selection 1’b0 : Average 1’b1 : Center pixel [1] : G_RB Position Test Enable 1’b0 : Disable 1’b1 : Enable [0] : Bayer Noise Reduction Enable 1’b0 : Disable 1’b1 : Enable
0x5421	BNR_STR	R/W	0x80	[7:0] : Strength
0x5422	BNR_THR_UPPER	R/W	0x20	[7:0] : Upper Threshold
0x5423	BNR_THR_LOWER	R/W	0x20	[7:0] : Lower Threshold
COLOR INTERPOLATION				
0x5500	INTP_CON	R/W	0x00	[7] : Reserved [6:5] : Color Interpolation Output Selection 2’b00: Normal Mode 2’b01: Red out 2’b10 : Green out 2’b11 : Blue out [4] : Bypass Enable [3] : Reserved [2] : Chrominance Noise Reduction Enable [1] : Luminance Noise Reduction Enable [0] : Adaptive False Color Suppression Enable
0x5501	Y_NR_GAIN	R/W	0x00	[7:2] : Reserved [1:0] : Luminance Noise Reduction Rate 2’b00 : 100% reduction 2’b01 : 50% reduction 2’b10 : 25% reduction 2’b11 : 12.5% reduction
0x5502	COLOR	R/W	0x00	[7:2] : Reserved [1:0] : First Color Selection 2’b00 : R 2’b01 : Gr

				2'b10 : Gb 2'b11 : B
0x5503	RGB_CLIP_H	R/W	0x03	[7:2] : Reserved [1:0] : High byte of RGB Clip Value
0x5504	RGB_CLIP_L	R/W	0xFF	[7:0] : Low byte of RGB Clip Value
0x5505	EDGE_TH_H	R/W	0x00	[7:2] : Reserved [1:0] : High byte of Edge Threshold
0x5506	EDGE_TH_L	R/W	0x80	[7:0] : Low byte of Edge Threshold
0x5507	Y_MID_COR	R/W	0x00	[7:0] : Middle Frequency Luminance Coring Value
0x5508	Y_HIGH_COR	R/W	0x00	[7:0] : High Frequency Luminance coring Value
0x5509	Y_MID_GAIN	R/W	0x60	[7:4] : Middle Frequency Luminance Coarse Gain(Integer 4bit) [3:0] : Middle Frequency Luminance Fine Gain(Fraction 4bit)
0x550A	Y_HIGH_GAIN	R/W	0x10	[7:4]: High Frequency Luminance Coarse Gain(Integer 4bit) [3:0]: High Frequency Luminance Fine Gain(Fraction 4bit)
0x550B	GRGB_OFFSET	R/W	0x00	[7:0]: Gr/Gb Offset
0x550C	FC_MID_SCL	R/W	0x80	[7:0]: Middle Frequency False Color Suppression Strength(Edge)
0x550D	FC_HIGH_SCL	R/W	0x80	[7:0]: High Frequency False Color Suppression Strength(Moiré)
COLOR CORRECTION				
0x5600	CC11	R/W	0x40	[7:0] : Coefficients of 1st row, 1st column in color correction matrix
0x5601	CC12	R/W	0x00	[7:0] : Coefficients of 1st row, 2nd column In color correction matrix
0x5602	CC13	R/W	0x00	[7:0] : Coefficients of 1st row, 3rd column In color correction matrix
0x5603	CC21	R/W	0x00	[7:0] : Coefficients of 2nd row, 1st column In color correction matrix
0x5604	CC22	R/W	0x40	[7:0] : Coefficients of 2nd row, 2nd column In color correction matrix
0x5605	CC23	R/W	0x00	[7:0] : Coefficients of 2nd row, 3rd column In color correction matrix
0x5606	CC31	R/W	0x00	[7:0] : Coefficients of 3rd row, 1st column In color correction matrix
0x5607	CC32	R/W	0x00	[7:0] : Coefficients of 3rd row, 2nd column In color correction matrix
0x5608	CC33	R/W	0x40	[7:0] : Coefficients of 3rd row, 3rd column in color correction matrix
GAMMA				
0x5700	GAMMA_CONTROL	R/W	0x00	[7:1] : reserved [0] : gamma enable 0 : disable 1 : enable
0x5710	GAMMA_0	R/W	0x15	[7:0] : gamma 0 (0~4)
0x5711	GAMMA_1	R/W	0x1D	[7:0] : gamma 1 (5~8)
0x5712	GAMMA_2	R/W	0x27	[7:0] : gamma 2 (9~16)
0x5713	GAMMA_3	R/W	0x36	[7:0] : gamma 3 (17~32)
0x5714	GAMMA_4	R/W	0x4A	[7:0] : gamma 4 (33~64)
0x5715	GAMMA_5	R/W	0x64	[7:0] : gamma 5 (65~128)
0x5716	GAMMA_6	R/W	0x79	[7:0] : gamma 6 (129~192)
0x5717	GAMMA_7	R/W	0x89	[7:0] : gamma 7 (193~256)
0x5718	GAMMA_8	R/W	0x98	[7:0] : gamma 8 (257~320)
0x5719	GAMMA_9	R/W	0xA5	[7:0] : gamma 9 (321~384)
0x571A	GAMMA_10	R/W	0xB0	[7:0] : gamma 10 (385~448)

0x571B	GAMMA_11	R/W	0xBB	[7:0] : gamma 11 (449~512)
0x571C	GAMMA_12	R/W	0xC6	[7:0] : gamma 12 (513~576)
0x571D	GAMMA_13	R/W	0xCF	[7:0] : gamma 13 (577~640)
0x571E	GAMMA_14	R/W	0xD8	[7:0] : gamma 14 (641~704)
0x571F	GAMMA_15	R/W	0xE1	[7:0] : gamma 15 (705~768)
0x5720	GAMMA_16	R/W	0xE9	[7:0] : gamma 16 (769~896)
0x5721	GAMMA_17	R/W	0xF1	[7:0] : gamma 17 (897~960)
0x5722	GAMMA_18	R/W	0xF9	[7:0] : gamma 18 (961~1023)

19.5. ISP 2

ADDRESS (HEX)	REGISTER NAME	R/W	DEFAULT (HEX)	DESCRIPTION
HUE / SATURATION / CONTRAST (VSYNC SYNCHRONIZED)				
0x6000	HS_CON	R/W	0x00	[7:5]: Reserved [4]: White Enhancement enable 1'b0: White Enhancement disable 1'b1: White Enhancement enable [3]: Black Enhancement enable 1'b0: Black Enhancement disable 1'b1: Black Enhancement enable [2]: Brightness enable 1'b0: Brightness disable 1'b1: Brightness enable [1]: Contrast enable 1'b0: Contrast disable 1'b1: Contrast enable [0]: Hue/Saturation enable 1'b0: Hue/ Saturation disable 1'b1: Hue/ Saturation enable
0x6001	HS_REF	R/W	0x80	[7:0]: Reference value of Hue/saturation control
0x6002	HS_Y_REF	R/W	0x80	[7:0]: Reference value of contrast
0x6003	HS_Y_CONTRAST	R/W	0x80	[7:0]: Contrast gain. Range x0(0x00)~x1.992(0xFF)
0x6004	HS_Y_BRIGHT	R/W	0x00	[7:0]: Brightness offset
0x6005	HS_SAT_CB	R/W	0x80	[7:0]: Saturation Cb gain. Range x0(0x00)~x1.992(0xFF)
0x6006	HS_SAT_CR	R/W	0x80	[7:0]: Saturation Cr gain. Range x0(0x00)~x1.992(0xFF)
0x6007	HS_SAT_MAG	R/W	0x80	[7:0]: Saturation Magenta gain. Range x0(0x00)~x1.992(0xFF)
0x6008	HS_SAT_RED	R/W	0x80	[7:0]: Saturation Red gain. Range x0(0x00)~x1.992(0xFF)
0x6009	HS_SAT_YEL	R/W	0x80	[7:0]: Saturation Yellow gain. Range x0(0x00)~x1.992(0xFF)
0x600A	HS_SAT_GRE	R/W	0x80	[7:0]: Saturation Green gain. Range x0(0x00)~x1.992(0xFF)
0x600B	HS_SAT_CYA	R/W	0x80	[7:0]: Saturation Cyan gain. Range x0(0x00)~x1.992(0xFF)
0x600C	HS_SAT_BLU	R/W	0x80	[7:0]: Saturation Blue gain. Range x0(0x00)~x1.992(0xFF)
0x600D	HS_HUE_MAG	R/W	0x00	[7:0]: Hue control(Magenta area) Range -45° ~ +45° (2's complement)
0x600E	HS_HUE_RED	R/W	0x00	[7:0]: Hue control(Red area) Range -45° ~ +45° (2's complement)
0x600F	HS_HUE_YEL	R/W	0x00	[7:0]: Hue control(Yellow area) Range -45° ~ +45° (2's complement)
0x6010	HS_HUE_GRE	R/W	0x00	[7:0]: Hue control(Green area) Range -45° ~ +45° (2's complement)
0x6011	HS_HUE_CYA	R/W	0x00	[7:0]: Hue control(Cyan area) Range -45° ~ +45° (2's complement)
0x6012	HS_HUE_BLU	R/W	0x00	[7:0]: Hue control(Blue area) Range -45° ~ +45° (2's complement)
Color Suppression (VSYNC SYNCHRONIZED)				
0x6210	COLOR_SUP_CON	R/W	0x00	[7:1] : Reserved [0] : Color suppress enable 1'b0: Disable 1'b1: Enable
0x6211	CB_UPPER_Y_THR	R/W	0xDC	[7:0] : Upper Threshold of Y for Cb
0x6212	CB_UPPER_SGAIN	R/W	0x20	[7:0] : Upper Suppression Gain for Cb
0x6213	CB_LOWER_Y_THR	R/W	0x40	[7:0] : Lower Threshold of Y for Cb
0x6214	CB_LOWER_SGAIN	R/W	0x20	[7:0] : Lower Suppression Gain for Cb
0x6215	CR_UPPER_Y_THR	R/W	0xDC	[7:0] : Upper Threshold of Y for Cr
0x6216	CR_UPPER_SGAIN	R/W	0x20	[7:0] : Upper Suppression Gain for Cr

0x6217	CR_LOWER_Y_THR	R/W	0x40	[7:0] : Lower Threshold of Y for Cr
0x6218	CR_LOWER_SGAIN	R/W	0x20	[7:0] : Lower Suppression Gain for Cr
0x6219	GRAY_LEVEL	R/W	0x00	[7:3] : reserved [2:0] : gray level, 111 -> full gray

19.6. FORMATTER

ADDRESS (HEX)	REGISTER NAME	R/W	DEFAULT (HEX)	DESCRIPTION
FORMATTER	**(VSYNC SYNCHRONIZED)**			
0x6400	DATA_FMAT_CON	R/W	0x00	[7:5] : reserved [4:3] : YCbCr Output Order Control 00 : YCbYCr 01 : YCrYCb 10 : CbYCrY 11 : CrYCbY [2:0] : DATA Format Selection 000 : YCbCr 4:2:2 001 : RGB565 010 : RGB555 011 : Bayer 8 bit 100 : Bayer 10 bit
0x6401	RGB_CON	R/W	0x00	[7:4] : reserved [3:2] : Bayer Output Order Control 00 : RGr-GbB 01 : GrR-BGb 10 : GbB-RGr 11 : BGb-GrR [1] : RGB555 Bit Position Control [0] : R/B Swap Control 0 : RG-GB 1 : BG-GR
0x6402	FMAT_PDATA_CON	R/W	0x00	[7] : reserved [6] : Hsync enable for Vblank [5] : OPB output enable (0 : disable, 1 : enable) [4] : pclock polarity inversion [3] : Vsync polarity inversion [2] : Hsync polarity inversion [1:0] : Bit Position Control 00 : xxPDATA[7:0] 01 : xPDATA[7:0]x 1x : PDATA[7:0]xx

19.7. CCP

ADDRESS (HEX)	REGISTER NAME	R/W	DEFAULT (HEX)	DESCRIPTION
AE	**(VSYNC SYNCHRONIZED)**			
0x7000	AE_WIN01_SEL	R/W	0x00	[7:4] : reserved [3] : AE window1 display enable (1:on) [2] : WDR Luminance data out [1] : LP Luminance data out [0] : SP Luminance data out
0x7001	AE_WIN02_SEL	R/W	0x00	[7:4] : reserved [3] : AE window2 display enable (1:on) [2] : WDR Luminance data out [1] : LP Luminance data out [0] : SP Luminance data out
0x7002	AE_WIN03_SEL	R/W	0x00	[7:4] : reserved [3] : AE window3 display enable (1:on) [2] : WDR Luminance data out [1] : LP Luminance data out [0] : SP Luminance data out
0x7003	AE_WIN04_SEL	R/W	0x00	[7:4] : reserved [3] : AE window4 display enable (1:on) [2] : WDR Luminance data out [1] : LP Luminance data out [0] : SP Luminance data out
0x7004	AE_WIN05_SEL	R/W	0x00	[7:4] : reserved [3] : AE window5 display enable (1:on) [2] : WDR Luminance data out [1] : LP Luminance data out [0] : SP Luminance data out
0x7005	AE_WIN06_SEL	R/W	0x00	[7:4] : reserved [3] : AE window6 display enable (1:on) [2] : WDR Luminance data out [1] : LP Luminance data out [0] : SP Luminance data out
0x700D	AE_SAT01_SEL	R/W	0x00	[7:4] : reserved [3] : SP saturation area selection 0 : LP saturation area 1 : SP whole area [2] : AE window21 sat.window1 win,rgn display enable [1] : AE window21 sat.window1 data sel (0:LP&SP,1:WDR) [0] : AE window21 sat.window1 enable
0x700E	AE_SAT02_SEL	R/W	0x00	[7:3] : reserved [2] : AE window22 sat.window2 win,rgn display enable [1] : AE window22 sat.window2 data sel (0:LP&SP,1:WDR) [0] : AE window22 sat.window2 enable
0x7020	AE_WIN01_LR	R/W	0x0F	[7:4] : Left value of AE window 1 [3:0] : Right value of AE window 1
0x7021	AE_WIN01_UD	R/W	0x0F	[7:4] : Up value of AE window 1 [3:0] : Down value of AE window 1
0x7022	AE_WIN02_LR	R/W	0x0F	[7:4] : Left value of AE window 2 [3:0] : Right value of AE window 2
0x7023	AE_WIN02_UD	R/W	0x0F	[7:4] : Up value of AE window 2 [3:0] : Down value of AE window 2
0x7024	AE_WIN03_LR	R/W	0x0F	[7:4] : Left value of AE window 3 [3:0] : Right value of AE window 3
0x7025	AE_WIN03_UD	R/W	0x0F	[7:4] : Up value of AE window 3

				[3:0] : Down value of AE window 3
0x7026	AE_WIN04_LR	R/W	0x0F	[7:4] : Left value of AE window 4 [3:0] : Right value of AE window 4
0x7027	AE_WIN04_UD	R/W	0x0F	[7:4] : Up value of AE window 4 [3:0] : Down value of AE window 4
0x7028	AE_WIN05_LR	R/W	0x0F	[7:4] : Left value of AE window 5 [3:0] : Right value of AE window 5
0x7029	AE_WIN05_UD	R/W	0x0F	[7:4] : Up value of AE window 5 [3:0] : Down value of AE window 5
0x702A	AE_WIN06_LR	R/W	0x0F	[7:4] : Left value of AE window 6 [3:0] : Right value of AE window 6
0x702B	AE_WIN06_UD	R/W	0x0F	[7:4] : Up value of AE window 6 [3:0] : Down value of AE window 6
0x7038	AE_WIN21_LR	R/W	0x0F	[7:4] : Left value of Saturation Window1 [3:0] : Right value of Saturation Window1
0x7039	AE_WIN21_UD	R/W	0x0F	[7:4] : Up value of Saturation Window1 [3:0] : Down value of Saturation Window1
0x703A	AE_WIN22_LR	R/W	0x0F	[7:4] : Left value of Saturation Window2 [3:0] : Right value of Saturation Window2
0x703B	AE_WIN22_UD	R/W	0x0F	[7:4] : Up value of Saturation Window2 [3:0] : Down value of Saturation Window2
0x7050	AE01_SUM3	R	0x00	[7:6] : Reserved [5:0] : Summation of Y data out in AE window 1[29:24]
0x7051	AE01_SUM2	R	0x00	[7:0] : Summation of Y data out in AE window 1[23:16]
0x7052	AE01_SUM1	R	0x00	[7:0] : Summation of Y data out in AE window 1[15:8]
0x7053	AE01_SUM0	R	0x00	[7:0] : Summation of Y data out in AE window 1[7:0]
0x7054	AE02_SUM3	R	0x00	[7:6] : Reserved [5:0] : Summation of Y data out in AE window 2[29:24]
0x7055	AE02_SUM2	R	0x00	[7:0] : Summation of Y data out in AE window 2[23:16]
0x7056	AE02_SUM1	R	0x00	[7:0] : Summation of Y data out in AE window 2[15:8]
0x7057	AE02_SUM0	R	0x00	[7:0] : Summation of Y data out in AE window 2[7:0]
0x7058	AE03_SUM3	R	0x00	[7:6] : Reserved [5:0] : Summation of Y data out in AE window 3[29:24]
0x7059	AE03_SUM2	R	0x00	[7:0] : Summation of Y data out in AE window 3[23:16]
0x705A	AE03_SUM1	R	0x00	[7:0] : Summation of Y data out in AE window 3[15:8]
0x705B	AE03_SUM0	R	0x00	[7:0] : Summation of Y data out in AE window 3[7:0]
0x705C	AE04_SUM3	R	0x00	[7:6] : Reserved [5:0] : Summation of Y data out in AE window 4[29:24]
0x705D	AE04_SUM2	R	0x00	[7:0] : Summation of Y data out in AE window 4[23:16]
0x705E	AE04_SUM1	R	0x00	[7:0] : Summation of Y data out in AE window 4[15:8]
0x705F	AE04_SUM0	R	0x00	[7:0] : Summation of Y data out in AE window 4[7:0]
0x7060	AE05_SUM3	R	0x00	[7:6] : Reserved [5:0] : Summation of Y data out in AE window 5[29:24]
0x7061	AE05_SUM2	R	0x00	[7:0] : Summation of Y data out in AE window 5[23:16]
0x7062	AE05_SUM1	R	0x00	[7:0] : Summation of Y data out in AE window 5[15:8]
0x7063	AE05_SUM0	R	0x00	[7:0] : Summation of Y data out in AE window 5[7:0]
0x7064	AE06_SUM3	R	0x00	[7:6] : Reserved [5:0] : Summation of Y data out in AE window 6[29:24]
0x7065	AE06_SUM2	R	0x00	[7:0] : Summation of Y data out in AE window 6[23:16]
0x7066	AE06_SUM1	R	0x00	[7:0] : Summation of Y data out in AE window 6[15:8]
0x7067	AE06_SUM0	R	0x00	[7:0] : Summation of Y data out in AE window 6[7:0]

0x7080	AE21_SP_SAT_HTHR	R/W	0xB0	[7:0] : Small Pixel Saturation Histogram High Threshold
0x7081	AE21_SP_SAT_LTHR	R/W	0x28	[7:0] : Small Pixel Saturation Histogram Low Threshold
0x7082	AE21_SP_SAT_HCNT2	R	0x00	[7:4] : Reserved [3:0] : High part of Small Pixel saturation count[19:16]
0x7083	AE21_SP_SAT_HCNT1	R	0x00	[7:0] : High part of Small Pixel saturation count[15:8]
0x7084	AE21_SP_SAT_HCNT0	R	0x00	[7:0] : High part of Small Pixel saturation count[7:0]
0x7085	AE21_SP_SAT_MCNT2	R	0x00	[7:4] : Reserved [3:0] : Middle part of Small Pixel saturation count[19:16]
0x7086	AE21_SP_SAT_MCNT1	R	0x00	[7:0] : Middle part of Small Pixel saturation count[15:8]
0x7087	AE21_SP_SAT_MCNT0	R	0x00	[7:0] : Middle part of Small Pixel saturation count[7:0]
0x7088	AE21_SP_SAT_LCNT2	R	0x00	[7:4] : Reserved [3:0] : Low part of Small Pixel saturation count[19:16]
0x7089	AE21_SP_SAT_LCNT1	R	0x00	[7:0] : Low part of Small Pixel saturation count[15:8]
0x708A	AE21_SP_SAT_LCNT0	R	0x00	[7:0] : Low part of Small Pixel saturation count[7:0]
0x70A0	AE21_LP_SAT_THR	R/W	0xF0	[7:0] : Large Pixel saturation threshold in saturation window1
0x70A1	AE21_LP_SAT_CNT2	R	0x00	[7:4] : Reserved [3:0] : Count of Large Pixel Y in SAT window 1[19:16]
0x70A2	AE21_LP_SAT_CNT1	R	0x00	[7:0] : Count of Large Pixel Y in SAT window 1[15:8]
0x70A3	AE21_LP_SAT_CNT0	R	0x00	[7:0] : Count of Large Pixel Y in SAT window 1[7:0]
0x70A4	AE21_LP_SAT_SUM3	R	0x00	[7:6] : Reserved [5:0] : Sum of Large Pixel Y in SAT window 1[29:24]
0x70A5	AE21_LP_SAT_SUM2	R	0x00	[7:0] : Sum of Large Pixel Y in SAT window 1[23:16]
0x70A6	AE21_LP_SAT_SUM1	R	0x00	[7:0] : Sum of Large Pixel Y in SAT window 1[15:8]
0x70A7	AE21_LP_SAT_SUM0	R	0x00	[7:0] : Sum of Large Pixel Y in SAT window 1[7:0]
0x70A8	AE21_SP_SAT_SUM3	R	0x00	[7:6] : Reserved [5:0] : Sum of Small Pixel Y in SAT window 1[29:24]
0x70A9	AE21_SP_SAT_SUM2	R	0x00	[7:0] : Sum of Small Pixel Y in SAT window 1[23:16]
0x70AA	AE21_SP_SAT_SUM1	R	0x00	[7:0] : Sum of Small Pixel Y in SAT window 1[15:8]
0x70AB	AE21_SP_SAT_SUM0	R	0x00	[7:0] : Sum of Small Pixel Y in SAT window 1[7:0]
0x70B0	AE22_LP_SAT_THR	R/W	0x8C	[7:0] : Large Pixel saturation threshold in saturation window2
0x70B1	AE22_LP_SAT_CNT2	R	0x00	[7:4] : Reserved [3:0] : Count of Large Pixel Y in SAT window 2[19:16]
0x70B2	AE22_LP_SAT_CNT1	R	0x00	[7:0] : Count of Large Pixel Y in SAT window 2[15:8]
0x70B3	AE22_LP_SAT_CNT0	R	0x00	[7:0] : Count of Large Pixel Y in SAT window 2[7:0]
0x70B4	AE22_LP_SAT_SUM3	R	0x00	[7:6] : Reserved [5:0] : Sum of Large Pixel Y in SAT window 2[29:24]
0x70B5	AE22_LP_SAT_SUM2	R	0x00	[7:0] : Sum of Large Pixel Y in SAT window 2[23:16]
0x70B6	AE22_LP_SAT_SUM1	R	0x00	[7:0] : Sum of Large Pixel Y in SAT window 2[15:8]
0x70B7	AE22_LP_SAT_SUM0	R	0x00	[7:0] : Sum of Large Pixel Y in SAT window 2[7:0]
0x70B8	AE22_SP_SAT_SUM3	R	0x00	[7:6] : Reserved [5:0] : Sum of Small Pixel Y in SAT window 2[29:24]
0x70B9	AE22_SP_SAT_SUM2	R	0x00	[7:0] : Sum of Small Pixel Y in SAT window 2[23:16]
0x70BA	AE22_SP_SAT_SUM1	R	0x00	[7:0] : Sum of Small Pixel Y in SAT window 2[15:8]
0x70BB	AE22_SP_SAT_SUM0	R	0x00	[7:0] : Sum of Small Pixel Y in SAT window 2[7:0]
AWB **(VSYNC SYNCHRONIZED)**				
0x7100	WB_BOUND_EN	R/W	0x00	[7] : reserved [6] : Using Long Pixel display enable(1:on) [5] : Using Short Pixel display enable(1:on) [4] : Long Pixel white count zone 1 disable(1:off) [3] : Long Pixel white count zone 2 disable(1:off)

				[2] : Short Pixel white count zone 1 disable(1:off) [1] : Short Pixel white count zone 2 disable(1:off) [0] : AWB window 1 display enable
0x7101	WB_WIN_X_START_END_H	R/W	0x01	[7:2] : reserved [1] : High byte of X position start value of AWB window [0] : High byte of X position end value of AWB window
0x7102	WB_WIN_X_START_L	R/W	0x00	[7:0] : X position start value of AWB window
0x7103	WB_WIN_X_END_L	R/W	0x3F	[7:0] : X position end value of AWB window
0x7104	WB_WIN_Y_START	R/W	0x00	[7:0] : Y position start value of AWB window
0x7105	WB_WIN_Y_END	R/W	0xB3	[7:0] : Y position end value of AWB window
0x7106	WB_LP_WZONE1_P1_X	R/W	0x4B	[7:0] : Long Pixel White pixel zone 1 P1_X
0x7107	WB_LP_WZONE1_P1_Y	R/W	0xAA	[7:0] : Long Pixel White pixel zone 1 P1_Y
0x7108	WB_LP_WZONE1_P1_X_OS	R/W	0x0F	[7:0] : Long Pixel White pixel zone 1 P1_X Offset
0x7109	WB_LP_WZONE1_P1_Y_OS	R/W	0x09	[7:0] : Long Pixel White pixel zone 1 P1_Y Offset
0x710A	WB_LP_WZONE1_P2_X	R/W	0x60	[7:0] : Long Pixel White pixel zone 1 P2_X
0x710B	WB_LP_WZONE1_P2_Y	R/W	0x7E	[7:0] : Long Pixel White pixel zone 1 P2_Y
0x710C	WB_LP_WZONE1_SLOPE	R/W	0xA0	[7:0] : Long Pixel White pixel zone 1 Slope
0x710D	WB_LP_WZONE2_P1_X	R/W	0x5C	[7:0] : Long Pixel White pixel zone 2 P1_X
0x710E	WB_LP_WZONE2_P1_Y	R/W	0x74	[7:0] : Long Pixel White pixel zone 2 P1_Y
0x710F	WB_LP_WZONE2_P1_X_OS	R/W	0x1F	[7:0] : Long Pixel White pixel zone 2 P1_X Offset
0x7110	WB_LP_WZONE2_P1_Y_OS	R/W	0x06	[7:0] : Long Pixel White pixel zone 2 P1_Y Offset
0x7111	WB_LP_WZONE2_P2_X	R/W	0x82	[7:0] : Long Pixel White pixel zone 2 P2_X
0x7112	WB_LP_WZONE2_P2_Y	R/W	0x64	[7:0] : Long Pixel White pixel zone 2 P2_Y
0x7113	WB_LP_WZONE2_SLOPE	R/W	0x1A	[7:0] : Long Pixel White pixel zone 2 Slope
0x7114	WB_LP_WZONE3_P1_X	R/W	0x50	[7:0] : Long Pixel White pixel zone 3 P1_X
0x7115	WB_LP_WZONE3_P1_Y	R/W	0x6A	[7:0] : Long Pixel White pixel zone 3 P1_Y
0x7116	WB_LP_WZONE3_P2_X	R/W	0x56	[7:0] : Long Pixel White pixel zone 3 P2_X
0x7117	WB_LP_WZONE3_P2_Y	R/W	0x62	[7:0] : Long Pixel White pixel zone 3 P2_Y
0x7118	WB_LP_WZONE4_P1_X	R/W	0x50	[7:0] : Long Pixel White pixel zone 4 P1_X
0x7119	WB_LP_WZONE4_P1_Y	R/W	0xAE	[7:0] : Long Pixel White pixel zone 4 P1_Y
0x711A	WB_LP_WZONE4_P2_X	R/W	0x58	[7:0] : Long Pixel White pixel zone 4 P2_X
0x711B	WB_LP_WZONE4_P2_Y	R/W	0xA4	[7:0] : Long Pixel White pixel zone 4 P2_Y
0x711C	WB_SP_WZONE1_P1_X	R/W	0x4B	[7:0] : Short Pixel White pixel zone 1 P1_X
0x711D	WB_SP_WZONE1_P1_Y	R/W	0xAA	[7:0] : Short Pixel White pixel zone 1 P1_Y
0x711E	WB_SP_WZONE1_P1_X_OS	R/W	0x0F	[7:0] : Short Pixel White pixel zone 1 P1_X Offset
0x711F	WB_SP_WZONE1_P1_Y_OS	R/W	0x09	[7:0] : Short Pixel White pixel zone 1 P1_Y Offset
0x7120	WB_SP_WZONE1_P2_X	R/W	0x60	[7:0] : Short Pixel White pixel zone 1 P2_X
0x7121	WB_SP_WZONE1_P2_Y	R/W	0x7E	[7:0] : Short Pixel White pixel zone 1 P2_Y
0x7122	WB_SP_WZONE1_SLOPE	R/W	0xA0	[7:0] : Short Pixel White pixel zone 1 Slope
0x7123	WB_SP_WZONE2_P1_X	R/W	0x5C	[7:0] : Short Pixel White pixel zone 2 P1_X
0x7124	WB_SP_WZONE2_P1_Y	R/W	0x74	[7:0] : Short Pixel White pixel zone 2 P1_Y
0x7125	WB_SP_WZONE2_P1_X_OS	R/W	0x1F	[7:0] : Short Pixel White pixel zone 2 P1_X Offset

0x7126	WB_SP_WZONE2_P1_Y_OS	R/W	0x06	[7:0] : Short Pixel White pixel zone 2 P1_Y Offset
0x7127	WB_SP_WZONE2_P2_X	R/W	0x82	[7:0] : Short Pixel White pixel zone 2 P2_X
0x7128	WB_SP_WZONE2_P2_Y	R/W	0x64	[7:0] : Short Pixel White pixel zone 2 P2_Y
0x7129	WB_SP_WZONE2_SLOPE	R/W	0x1A	[7:0] : Short Pixel White pixel zone 2 Slope
0x712A	WB_SP_WZONE3_P1_X	R/W	0x50	[7:0] : Short Pixel White pixel zone 3 P1_X
0x712B	WB_SP_WZONE3_P1_Y	R/W	0x6A	[7:0] : Short Pixel White pixel zone 3 P1_Y
0x712C	WB_SP_WZONE3_P2_X	R/W	0x56	[7:0] : Short Pixel White pixel zone 3 P2_X
0x712D	WB_SP_WZONE3_P2_Y	R/W	0x62	[7:0] : Short Pixel White pixel zone 3 P2_Y
0x712E	WB_SP_WZONE4_P1_X	R/W	0x50	[7:0] : Short Pixel White pixel zone 4 P1_X
0x712F	WB_SP_WZONE4_P1_Y	R/W	0xAE	[7:0] : Short Pixel White pixel zone 4 P1_Y
0x7130	WB_SP_WZONE4_P2_X	R/W	0x58	[7:0] : Short Pixel White pixel zone 4 P2_X
0x7131	WB_SP_WZONE4_P2_Y	R/W	0xA4	[7:0] : Short Pixel White pixel zone 4 P2_Y
0x7132	WB_LP_SAT_UP	R/W	0xC0	[7:0] : Up Threshold of Long Pixel RGB Data
0x7133	WB_LP_SAT_DN	R/W	0x04	[7:0] : Down Threshold of Long Pixel RGB Data
0x7134	WB_SP_SAT_UP	R/W	0xC0	[7:0] : Up Threshold of Short Pixel RGB Data
0x7135	WB_SP_SAT_DN	R/W	0x04	[7:0] : Down Threshold of Short Pixel RGB Data
0x7140	WB_LP_RSUM3	R	0x00	[30:24] : Summation of Long Pixel raw Red data out in WB window
0x7141	WB_LP_RSUM2	R	0x00	[23:16] : Summation of Long Pixel raw Red data out in WB window
0x7142	WB_LP_RSUM1	R	0x00	[15:8] : Summation of Long Pixel raw Red data out in WB window
0x7143	WB_LP_RSUM0	R	0x00	[7:0] : Summation of Long Pixel raw Red data out in WB window
0x7144	WB_LP_GSUM3	R	0x00	[30:24] : Summation of Long Pixel raw Green data out in WB window
0x7145	WB_LP_GSUM2	R	0x00	[23:16] : Summation of Long Pixel raw Green data out in WB window
0x7146	WB_LP_GSUM1	R	0x00	[15:8] : Summation of Long Pixel raw Green data out in WB window
0x7147	WB_LP_GSUM0	R	0x00	[7:0] : Summation of Long Pixel raw Green data out in WB window
0x7148	WB_LP_BSUM3	R	0x00	[30:24] : Summation of Long Pixel raw Blue data out in WB window
0x7149	WB_LP_BSUM2	R	0x00	[23:16] : Summation of Long Pixel raw Blue data out in WB window
0x714A	WB_LP_BSUM1	R	0x00	[15:8] : Summation of Long Pixel raw Blue data out in WB window
0x714B	WB_LP_BSUM0	R	0x00	[7:0] : Summation of Long Pixel raw Blue data out in WB window
0x714C	WB_SP_RSUM3	R	0x00	[30:24] : Summation of Short Pixel raw Red data out in WB window
0x714D	WB_SP_RSUM2	R	0x00	[23:16] : Summation of Short Pixel raw Red data out in WB window
0x714E	WB_SP_RSUM1	R	0x00	[15:8] : Summation of Short Pixel raw Red data out in WB window
0x714F	WB_SP_RSUM0	R	0x00	[7:0] : Summation of Short Pixel raw Red data out in WB window
0x7150	WB_SP_GSUM3	R	0x00	[30:24] : Summation of Short Pixel raw Green data out in WB window
0x7151	WB_SP_GSUM2	R	0x00	[23:16] : Summation of Short Pixel raw Green data out in WB window
0x7152	WB_SP_GSUM1	R	0x00	[15:8] : Summation of Short Pixel raw Green data out in WB window
0x7153	WB_SP_GSUM0	R	0x00	[7:0] : Summation of Short Pixel raw Green data out in WB window
0x7154	WB_SP_BSUM3	R	0x00	[30:24] : Summation of Short Pixel raw Blue data out in WB window
0x7155	WB_SP_BSUM2	R	0x00	[23:16] : Summation of Short Pixel raw Blue data out in WB window
0x7156	WB_SP_BSUM1	R	0x00	[15:8] : Summation of Short Pixel raw Blue data out in WB window
0x7157	WB_SP_BSUM0	R	0x00	[7:0] : Summation of Short Pixel raw Blue data out in WB window
0x7158	WB_LP_WCNT2	R	0x00	[20:16] : Count of Long Pixel white in WB window
0x7159	WB_LP_WCNT1	R	0x00	[15:8] : Count of Long Pixel white in WB window
0x715A	WB_LP_WCNT0	R	0x00	[7:0] : Count of Long Pixel white in WB window
0x715B	WB_SP_WCNT2	R	0x00	[20:16] : Count of Short Pixel white in WB window

0x715C	WB_SP_WCNT1	R	0x00	[15:8] : Count of Short Pixel white in WB window
0x715D	WB_SP_WCNT0	R	0x00	[7:0] : Count of Short Pixel white in WB window

19.8. GADC

ADDRESS (HEX)	REGISTER NAME	R/W	DEFAULT (HEX)	DESCRIPTION
GADC				
0x8000	GADC_CON	R/W	0x08	[7] : GADC interrupt mask [6] : GADC current control 2 [5] : GADC current control 1 [4] : GADC current control 0 [3] : GADC power down 0 : active 1 : power down [2] : GADC channel selection 0 : channel 0 1 : channel 1 [1] : GADC start control [0] : GADC end flag
0x8001	GADC_DATA	R	0x00	[7:0] : GADC data
0x8002	GADC_CLK	R/W	0x02	[7:2] : reserved [1:0] : GADC clock 00 : Ext Clock / 4 01 : Ext Clock / 8 10 : Ext Clock / 16 11 : reserved

19.9. SMPTE

ADDRESS (HEX)	REGISTER NAME	R/W	DEFAULT (HEX)	DESCRIPTION
SMPTE	**(VSYNC SYNCHRONIZED)**			
0x8200	SMPTE_CONT	R/W	0x00	[7:3] : reserved [2:1] : frame rate selection 00 : 60fps 01 : 30fps 10 : 50fps 11 : 25fps [0] : smpte_en

20. Spectral Response Of Color Filter

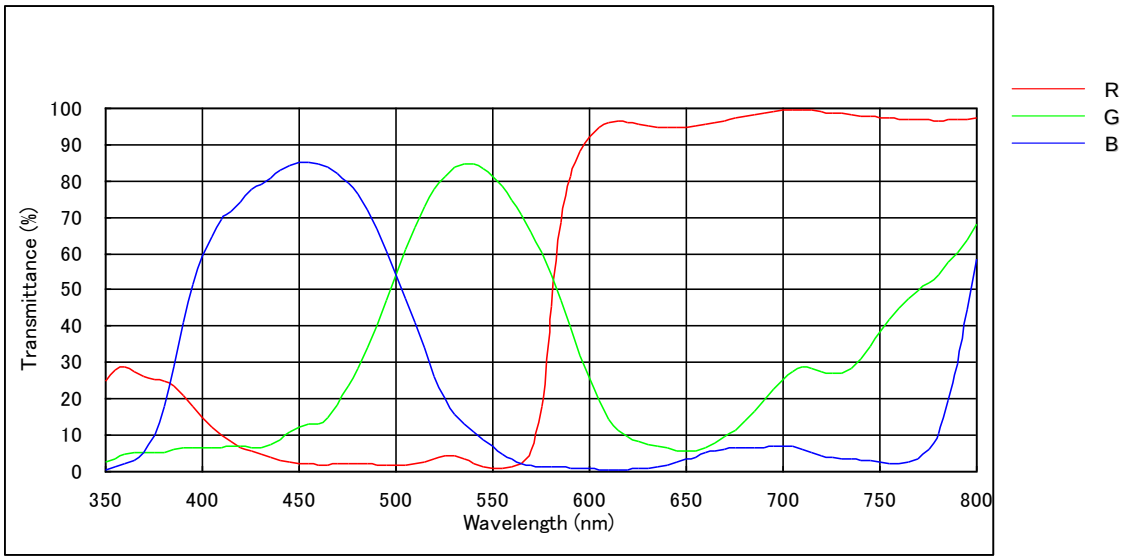


Figure 20-1 spectral response of color filter

21. Electrical Characteristics

Symbol	Parameter	Rating	Units
VDDIO	Supply Voltage for IO	4	V
VDDP	Supply Voltage for Analog	4	V
VDDD		4	V
VDDA		4	V
VDDL		4	V
VDD	Supply Voltage for Digital Core	2.4	V
T	Storage Temperature	-50 to 125	℃

Table 21-1 Absolute Maximum Ratings

Symbol	Parameter	Rating			Units
		MIN	TYP	MAX	
VDDIO	Supply Voltage for IO	2.97	3.3	3.63	V
VDDP	Supply Voltage for Analog	2.97	3.3	3.63	V
VDDD		2.97	3.3	3.63	V
VDDA		2.97	3.3	3.63	V
VDDL		2.97	3.3	3.63	V
VDD	Supply Voltage for Digital Core	1.35	1.5	1.65	V
T_A	Commercial Temperature Range	0 to 70			℃
	Industrial Temperature Range	-40 to 105			

Table 21-2 Recommended Operating Condition

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
IDDS	Quiescent Current	VDDIO = 3.3V VDD = 1.5V		[T.B.D]		mW
IDD	Dynamic IDD	VDDIO = 3.3V VDD = 1.5V EXT_CLK = 27MHz		[T.B.D]		mW

Table 21-3 Power Consumption

Items	VDDIO = 3.3V±10%			Unit
	MIN	TYP	MAX	
VIL			0.35*VDDIO	V
VIH	0.7*VDDIO			
IIH	-5		5	μA
IIL	-5		5	
VOL (PAD)			0.4	V
VOH (PAD)	VDDIO-0.4			
Schmitt trigger L to H Threshold	1.74		1.92	V
Schmitt trigger H to L Threshold	1.26		1.46	V

Table 21-4 DC Characteristics

22. PIN DESCRIPTION

CP8210 has two kinds of package, CP8210B and CP8210S.

CP8210B has only 10bit data output for BT601 interface and CP8210S 20bit data output for BT1120.

Caution] some pins are different from CP8110.

CP8210B PIN MAP is as below.

PIN#	PIN NAME (CURRENT)	PIN NAME (BEFORE)	Description (CURRENT)	Remark
PIN01	NC	PDATA18	No connection	
PIN02	NC	PDATA17	No connection	
PIN03	NC	PDATA16	No connection	
PIN04	NC	PDATA15	No connection	
PIN05	NC	PDATA14	No connection	
PIN06	NC	PDATA13	No connection	
PIN07	NC	PDATA12	No connection	
PIN08	NC	PDATA11	No connection	
PIN09	NC	PDATA10	No connection	
PIN10	NC	VSSIO	No connection	
PIN11	NC	VDDIO	No connection	
PIN12	PDATA9	PDATA9	Data [9] output port	
PIN13	PDATA8	PDATA8	Data [8] output port	
PIN14	PDATA7	PDATA7	Data [7] output port	
PIN15	PDATA6	PDATA6	Data [6] output port	
PIN16	PDATA5	PDATA5	Data [5] output port	
PIN17	PDATA4	PDATA4	Data [4] output port	
PIN18	VSSIO	VSSIO	Digital ground for I/O	
PIN19	VDDIO	VDDIO	Digital power for I/O	
PIN20	VSS	VSS	Digital core ground	
PIN21	VDD	VDD	Digital core power	
PIN22	PDATA3	PDATA3	Data [3] output port	
PIN23	PDATA2	PDATA2	Data [2] output port	
PIN24	PDATA1	PDATA1	Data [1] output port	
PIN25	PDATA0	PDATA0	Data [0] output port	
PIN26	HSYNC	HSYNC	Horizontal Sync output port	
PIN27	VSYNC	VSYNC	Vertical Sync output port	
PIN28	PCLOCK	PCLOCK	Pixel clock I/O	
PIN29	VSSIO	VSSIO	Digital ground for I/O	
PIN30	VDDIO	VDDIO	Digital power for I/O	
PIN31	VSS	VSS	Digital core ground	
PIN32	VDD	VDD	Digital core power	
PIN33	GPIO1	GPIO1	Gereral I/O port	
PIN34	GPIO0	GPIO0	Gereral I/O port	
PIN35	STDBY	STDBY	Standby input port	
PIN36	RST_N	RST_N	Reset input port	
PIN37	SCL_S	SCL_S	Slave Serial Clock port	
PIN38	SDA_S	SDA_S	Slave Serial Data port	
PIN39	SDA_M	SDA_M	Master Serial Clock port	
PIN40	SCL_M	SCL_M	Master Serial Data port	

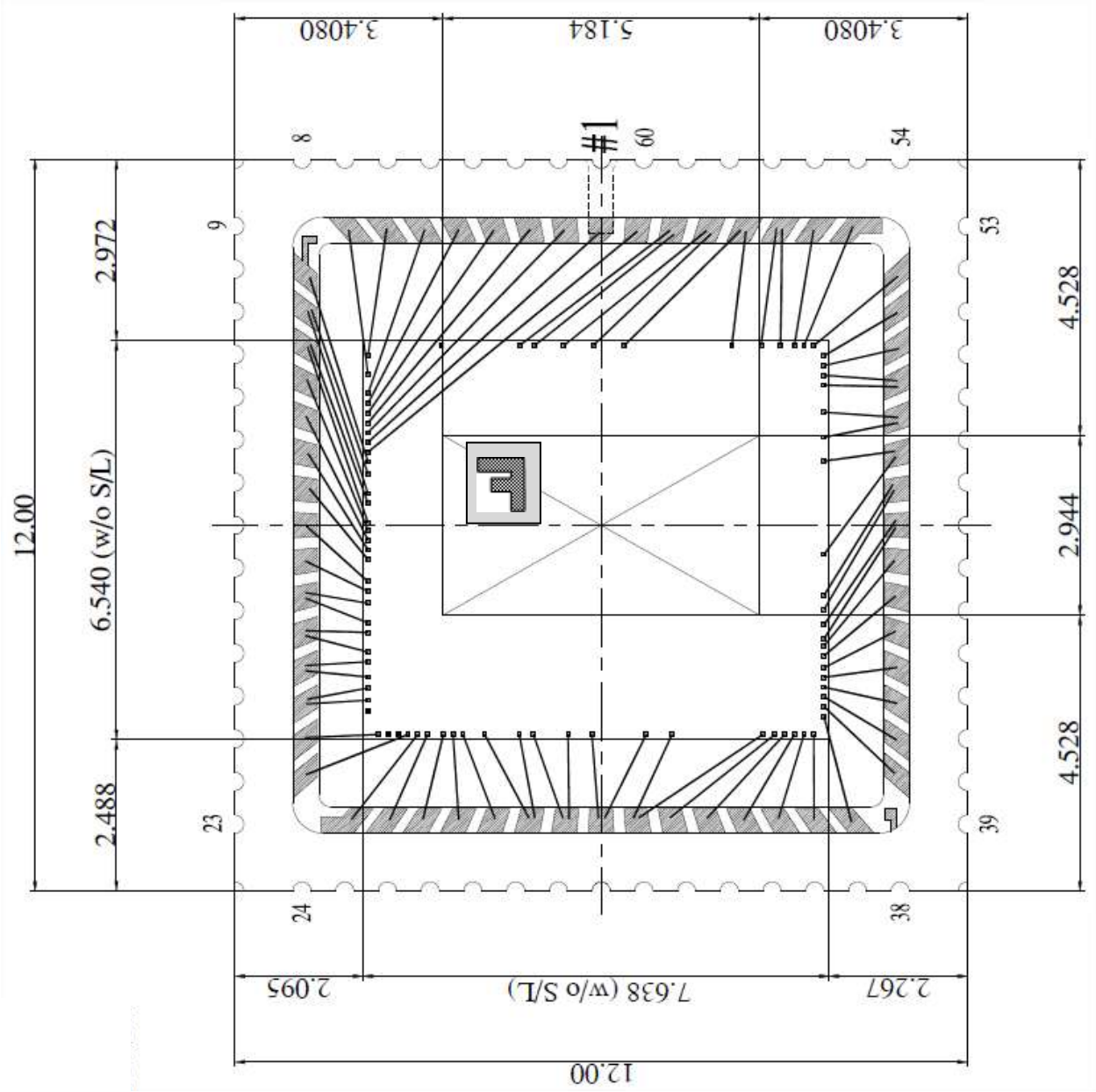
PIN41	SEL_CLK	SEL_CLK	Extern clock enable	
PIN42	XI	XI	XTAL/OSC input	
PIN43	XO	XO	XTAL output	
PIN44	VDD	VDD	Digital core power	
PIN45	VSS	VSS	Digital core ground	
PIN46	VSSL	VSSL	Analog digital ground	**PLL**
PIN47	VDDL	VDDL	Analog digital power	**PLL**
PIN48	VDDA	VDDA	Analog core power	
PIN49	VSSA	VSSA	Analog core ground	
PIN50	VSIG	VSIG	Vsig input port	
PIN51	MON0	MON0	Monitoring[0] output port	
PIN52	A0	A0	ADC[0] input port	
PIN53	VRST	VRST	Vrst input port	
PIN54	MON1	MON1	Monitoring[1] output port	
PIN55	A1	A1	ADC[1] input port	
PIN56	VDDP	VDDP	Pixel core power	
PIN57	VSSP	VSSP	Pixel core ground	
PIN58	VDDA	VDDA	Analog core power	
PIN59	VSSA	VSSA	Analog core ground	
PIN60	NC	PDATA19	No connection	

CP8210S PINMAP is as below.

PIN#	PIN NAME (CURRENT)	PIN NAME (BEFORE)	Description (CURRENT)	Remark
PIN01	NC	PDATA18	No connection	
PIN02	PDATA17	PDATA17	Data [17] output port	
PIN03	NC	PDATA16	No connection	
PIN04	PDATA15	PDATA15	Data [15] output port	
PIN05	PDATA14	PDATA14	Data [14] output port	
PIN06	PDATA13	PDATA13	Data [13] output port	
PIN07	PDATA12	PDATA12	Data [12] output port	
PIN08	PDATA11	PDATA11	Data [11] output port	
PIN09	PDATA16	PDATA10	Data [16] output port	
PIN10	PDATA18	VSSIO	Data [18] output port	
PIN11	PDATA10	VDDIO	Data [10] output port	
PIN12	PDATA9	PDATA9	Data [9] output port	
PIN13	PDATA8	PDATA8	Data [8] output port	
PIN14	PDATA7	PDATA7	Data [7] output port	
PIN15	PDATA6	PDATA6	Data [6] output port	
PIN16	PDATA5	PDATA5	Data [5] output port	
PIN17	PDATA4	PDATA4	Data [4] output port	
PIN18	VSSIO	VSSIO	Digital ground for I/O	
PIN19	VDDIO	VDDIO	Digital power for I/O	
PIN20	VSS	VSS	Digital core ground	
PIN21	VDD	VDD	Digital core power	
PIN22	PDATA3	PDATA3	Data [3] output port	
PIN23	PDATA2	PDATA2	Data [2] output port	
PIN24	PDATA1	PDATA1	Data [1] output port	
PIN25	PDATA0	PDATA0	Data [0] output port	

PIN26	HSYNC	HSYNC	Horizontal Sync output port	
PIN27	VSYNC	VSYNC	Vertical Sync output port	
PIN28	PCLOCK	PCLOCK	Pixel clock I/O	
PIN29	VSSIO	VSSIO	Digital ground for I/O	
PIN30	VDDIO	VDDIO	Digital power for I/O	
PIN31	VSS	VSS	Digital core ground	
PIN32	VDD	VDD	Digital core power	
PIN33	GPIO1	GPIO1	Gereral I/O port	
PIN34	GPIO0	GPIO0	Gereral I/O port	
PIN35	STDBY	STDBY	Standby input port	
PIN36	RST_N	RST_N	Reset input port	
PIN37	SCL_S	SCL_S	Slave Serial Clock port	
PIN38	SDA_S	SDA_S	Slave Serial Data port	
PIN39	SDA_M	SDA_M	Master Serial Clock port	
PIN40	SCL_M	SCL_M	Master Serial Data port	
PIN41	SEL_CLK	SEL_CLK	Extern clock enable	
PIN42	XI	XI	XTAL/OSC input	
PIN43	XO	XO	XTAL output	
PIN44	VDD	VDD	Digital core power	
PIN45	VSS	VSS	Digital core ground	
PIN46	VSSL	VSSL	Analog digital ground	**PLL**
PIN47	VDDL	VDDL	Analog digital power	**PLL**
PIN48	VDDA	VDDA	Analog core power	
PIN49	VSSA	VSSA	Analog core ground	
PIN50	VSIG	VSIG	Vsig input port	
PIN51	MON0	MON0	Monitoring[0] output port	
PIN52	A0	A0	ADC[0] input port	
PIN53	VRST	VRST	Vrst input port	
PIN54	MON1	MON1	Monitoring[1] output port	
PIN55	A1	A1	ADC[1] input port	
PIN56	VDDP	VDDP	Pixel core power	
PIN57	VSSP	VSSP	Pixel core ground	
PIN58	VDDA	VDDA	Analog core power	
PIN59	VSSA	VSSA	Analog core ground	
PIN60	PDATA19	PDATA19	Data [19] output port	

23. PKG Dimension



TOP VIEW

Figure 23-1 60 Pin CLCC PKG Image Center

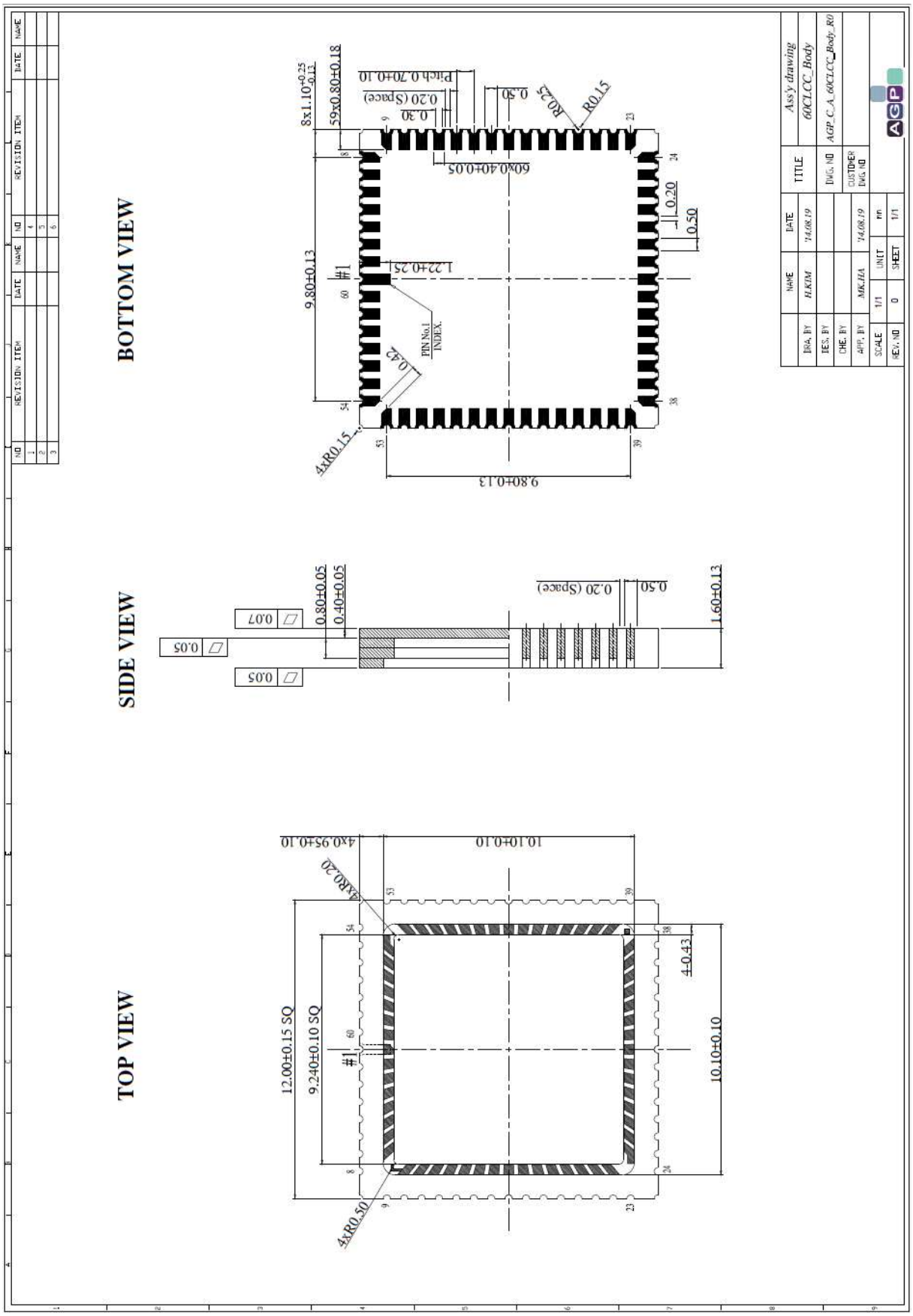


Figure 23-2 60 Pin CLCC PKG Dimension