

CPM2-1200-0040B

Silicon Carbide Power MOSFET
C2M™ MOSFET Technology
 N-Channel Enhancement Mode

V_{DS}	1200 V
$I_D @ 25^\circ\text{C}$	63 A
$R_{DS(on)}$	40 mΩ

Features

- C2M SiC MOSFET technology
- High Blocking Voltage with Low On-Resistance
- High Speed Switching with Low Capacitances
- Easy to Parallel and Simple to Drive
- Avalanche Ruggedness
- Resistant to Latch-Up
- Halogen Free, RoHS Compliant

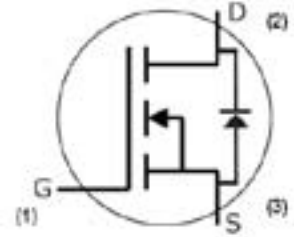
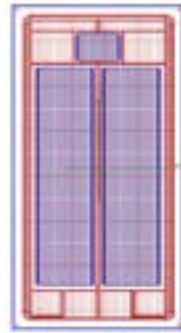
Benefits

- Higher System Efficiency
- Reduced Cooling Requirements
- Increased Power Density
- Increased System Switching Frequency

Applications

- Solar Inverters
- Switch Mode Power Supplies
- High Voltage DC/DC converters
- Battery Chargers
- Motor Drives
- Pulsed Power Applications

Chip Outline



Part Number	Die Size (mm)
CPM2-1200-0040B	3.10 x 5.90

Maximum Ratings ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{DSmax}	Drain - Source Voltage	1200	V	$V_{GS} = 0\text{ V}, I_b = 100\ \mu\text{A}$	
V_{GSmax}	Gate - Source Voltage (dynamic)	-10/+25	V	AC ($f > 1\text{ Hz}$)	Note 1
V_{GSop}	Gate - Source Voltage (static)	-5/+20	V	Static	Note 2
I_D	Continuous Drain Current	63	A	$V_{GS} = 20\text{ V}, T_c = 25^\circ\text{C}$	Note 3
		46		$V_{GS} = 20\text{ V}, T_c = 100^\circ\text{C}$	
$I_{D(pulse)}$	Pulsed Drain Current	160	A	Pulse width t_p limited by T_{jmax}	
T_J, T_{stg}	Operating Junction and Storage Temperature	-40 to +175	$^\circ\text{C}$		
T_{Proc}	Maximum Processing Temperature	325	$^\circ\text{C}$	10 min. maximum	

Note (1): When using MOSFET Body Diode $V_{GSmax} = -5\text{V}/+25\text{V}$

Note (2): MOSFET can also safely operate at 0/+20 V

Note (3): Assumes a $R_{\theta JC} < 0.38\text{ K/W}$



Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200			V	$V_{GS} = 0\text{ V}, I_D = 100\ \mu\text{A}$	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	2.6	4	V	$V_{DS} = V_{GS}, I_D = 10\text{mA}$	Fig. 11
			2.0		V	$V_{DS} = V_{GS}, I_D = 10\text{mA}, T_J = 175^\circ\text{C}$	
I_{DSS}	Zero Gate Voltage Drain Current		1	100	μA	$V_{DS} = 1200\text{ V}, V_{GS} = 0\text{ V}$	
I_{GSS}	Gate-Source Leakage Current			250	nA	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	
$R_{DS(on)}$	Drain-Source On-State Resistance		40	52	m Ω	$V_{GS} = 20\text{ V}, I_D = 40\text{ A}$	Fig. 4,5,6
			90			$V_{GS} = 20\text{ V}, I_D = 40\text{ A}, T_J = 175^\circ\text{C}$	
g_{fs}	Transconductance		23		S	$V_{DS} = 20\text{ V}, I_{DS} = 40\text{ A}$	Fig. 7
			19			$V_{DS} = 20\text{ V}, I_{DS} = 40\text{ A}, T_J = 175^\circ\text{C}$	
C_{iss}	Input Capacitance		1893		pF	$V_{GS} = 0\text{ V}$	Fig. 17,18
C_{oss}	Output Capacitance		150			$V_{DS} = 1000\text{ V}$	
C_{riss}	Reverse Transfer Capacitance		10			$f = 1\text{ MHz}$	
E_{oss}	C_{oss} Stored Energy		82		μJ	$V_{AC} = 25\text{ mV}$	Fig. 16
E_{AS}	Avalanche Energy, Single Pluse		2		J	$I_D = 40\text{ A}, V_{DD} = 50\text{ V}$	Fig. 29
E_{ON}	Turn-On Switching Energy		1.0		mJ	$V_{DS} = 800\text{ V}, V_{GS} = -5/20\text{ V}$	Fig. 25
E_{OFF}	Turn Off Switching Energy		0.4			$I_D = 40\text{ A}, R_{G(ext)} = 2.5\ \Omega, L = 80\ \mu\text{H}$	
$t_{d(on)}$	Turn-On Delay Time		15		ns	$V_{DD} = 800\text{ V}, V_{GS} = -5/20\text{ V}$ $I_D = 40\text{ A}$ $R_{G(ext)} = 2.5\ \Omega, R_L = 20\ \Omega$ Timing relative to V_{DS} Per IEC60747-8-4 pg 83	Fig. 27
t_r	Rise Time		52				
$t_{d(off)}$	Turn-Off Delay Time		26				
t_f	Fall Time		34				
$R_{G(int)}$	Internal Gate Resistance		1.8		Ω	$f = 1\text{ MHz}, V_{AC} = 25\text{ mV}$	
Q_{gs}	Gate to Source Charge		28		nC	$V_{DS} = 800\text{ V}, V_{GS} = -5/20\text{ V}$ $I_D = 40\text{ A}$ Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		37				
Q_g	Total Gate Charge		115				

Reverse Diode Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	4.1		V	$V_{GS} = -5\text{ V}, I_{SD} = 20\text{ A}, T_J = 25^\circ\text{C}$	Fig. 8, 9, 10
		3.5		V	$V_{GS} = -5\text{ V}, I_{SD} = 20\text{ A}, T_J = 175^\circ\text{C}$	
I_S	Continuous Diode Forward Current		60	A	$T_c = 25^\circ\text{C}$	Note 1
t_{rr}	Reverse Recovery Time	54		ns	$V_{GS} = -5\text{ V}, I_{SD} = 40\text{ A}, T_J = 25^\circ\text{C}$ $VR = 800\text{ V}$ $dif/dt = 1000\text{ A}/\mu\text{s}$	Note 1
Q_{rr}	Reverse Recovery Charge	283		nC		
I_{rrm}	Peak Reverse Recovery Current	15		A		

Note (4): For inductive and resistive switching data and waveforms please refer to datasheet for packaged device.
Part number C2M0040120D.

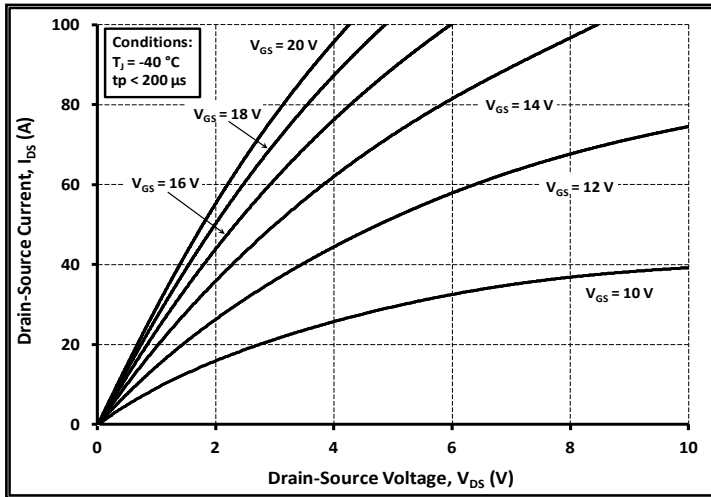


Figure 1. Output Characteristics $T_J = -40\text{ }^\circ\text{C}$

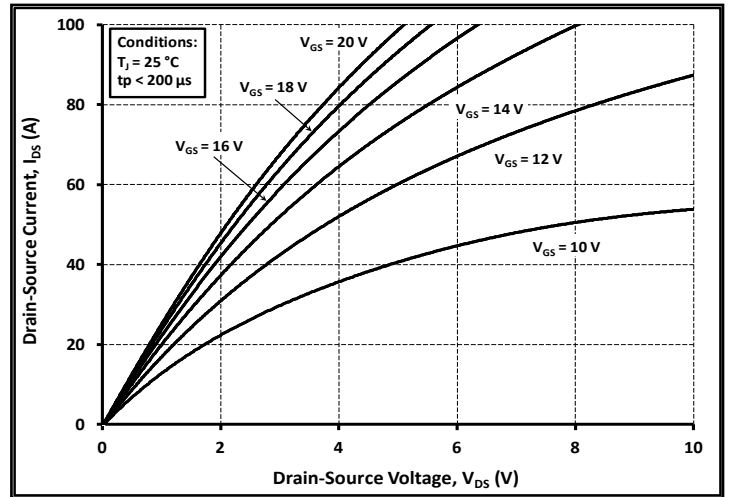


Figure 2. Output Characteristics $T_J = 25\text{ }^\circ\text{C}$

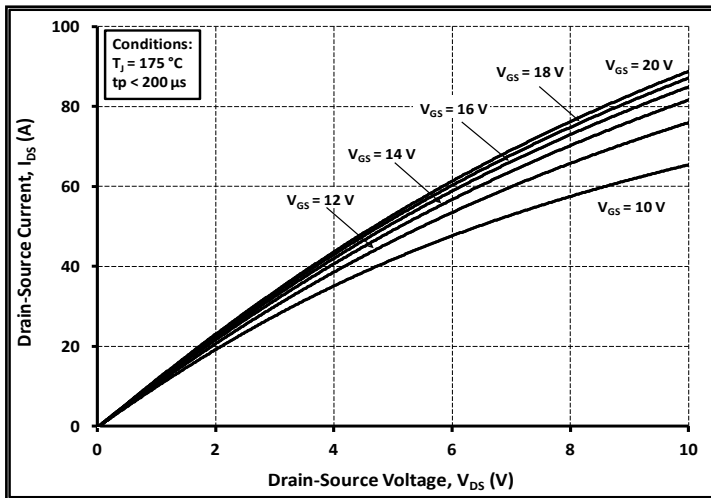


Figure 3. Output Characteristics $T_J = 175\text{ }^\circ\text{C}$

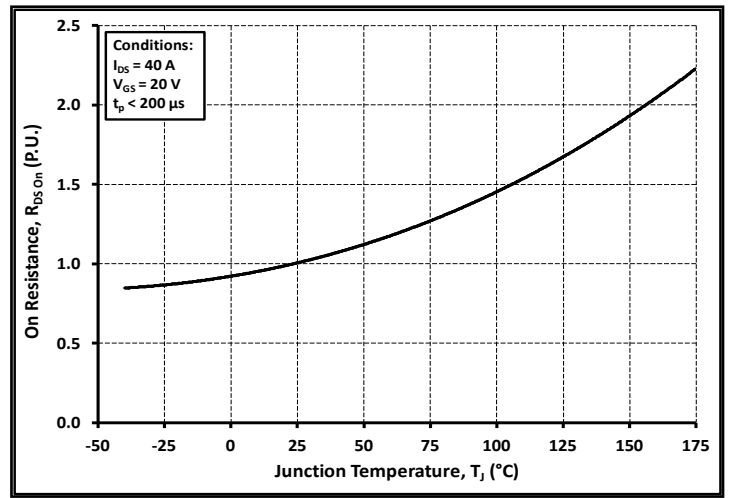


Figure 4. Normalized On-Resistance vs. Temperature

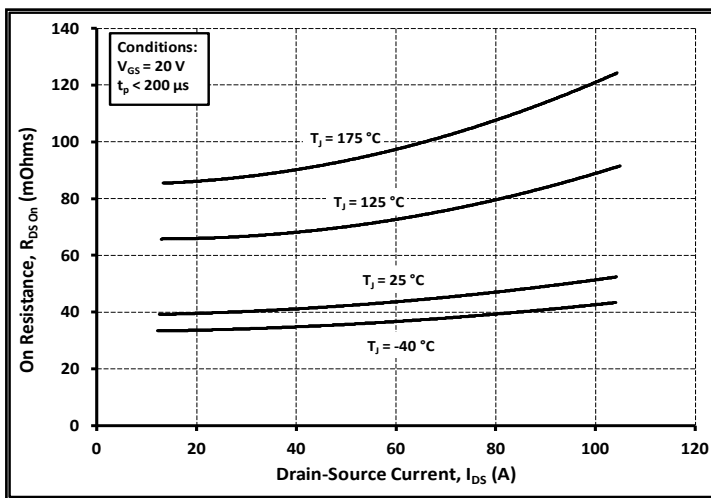


Figure 5. On-Resistance vs. Drain Current For Various Temperatures

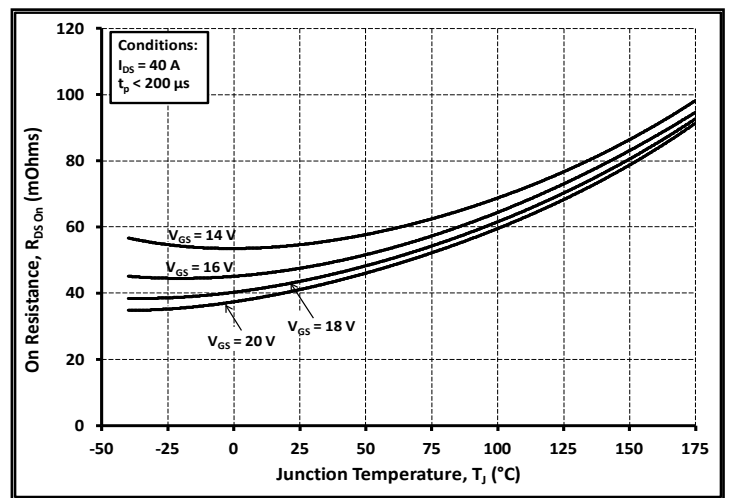


Figure 6. On-Resistance vs. Temperature For Various Gate Voltage

Typical Performance

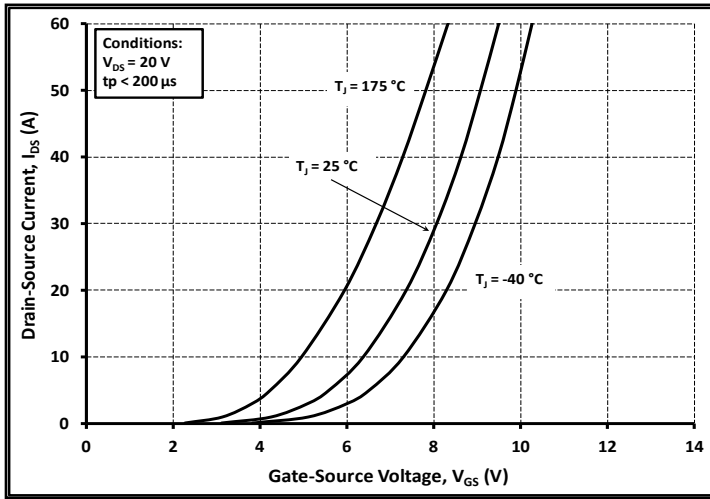


Figure 7. Transfer Characteristic for Various Junction Temperatures

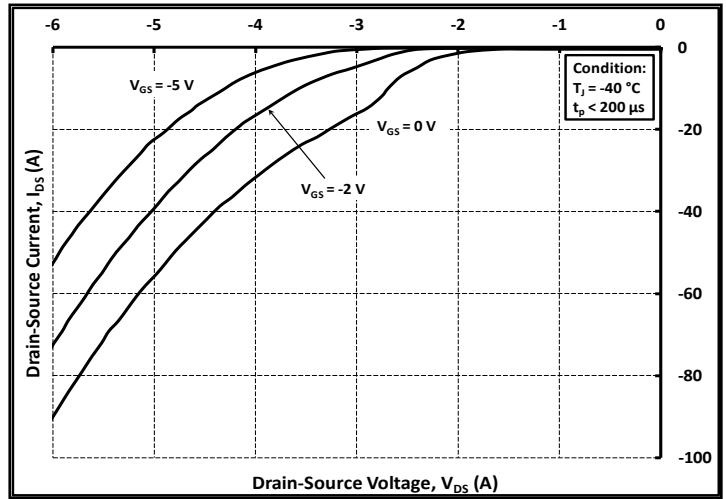


Figure 8. Body Diode Characteristic at -40 °C

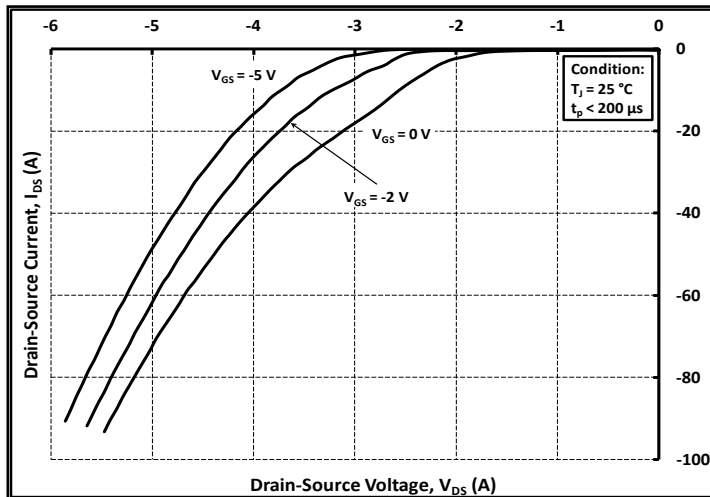


Figure 9. Body Diode Characteristic at 25 °C

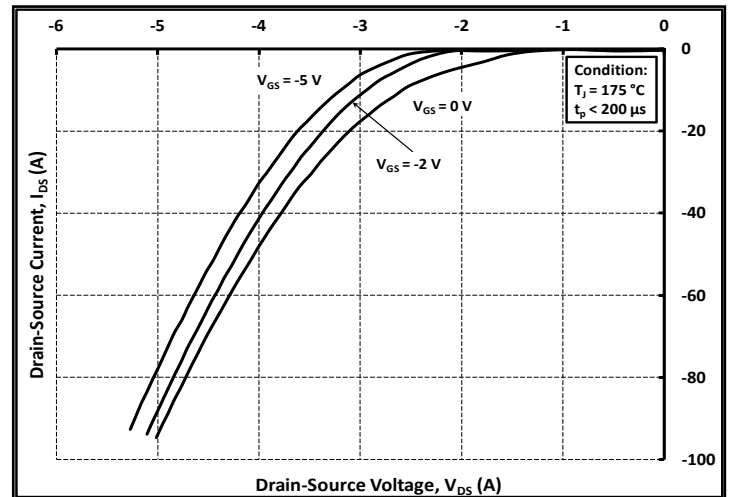


Figure 10. Body Diode Characteristic at 175 °C

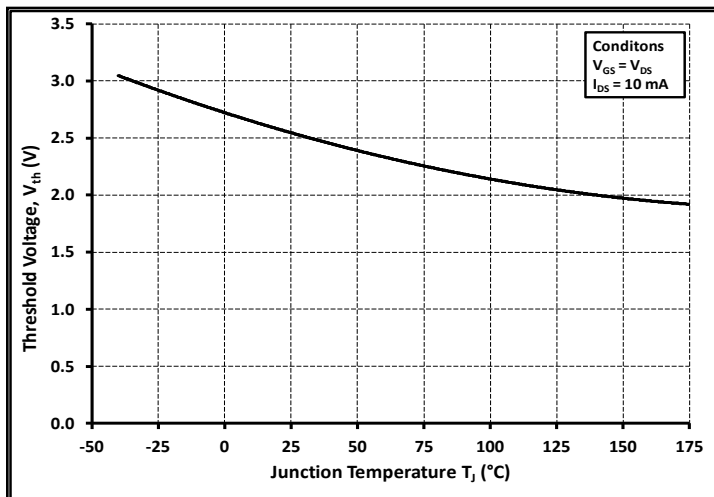


Figure 11. Threshold Voltage vs. Temperature

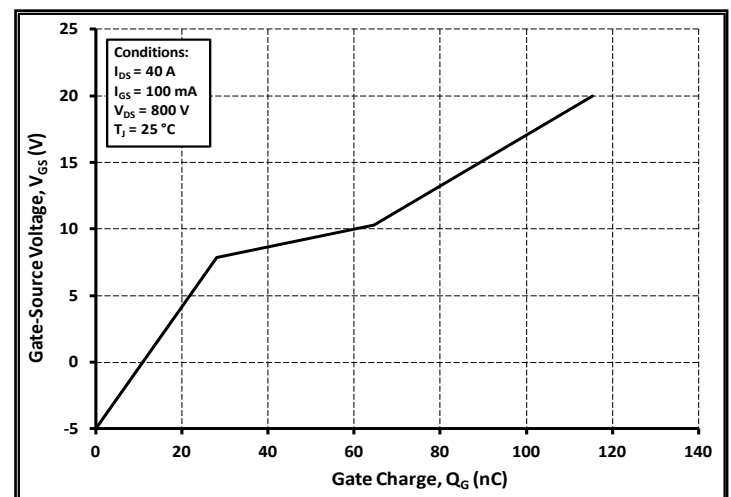


Figure 12. Gate Charge Characteristics

Typical Performance

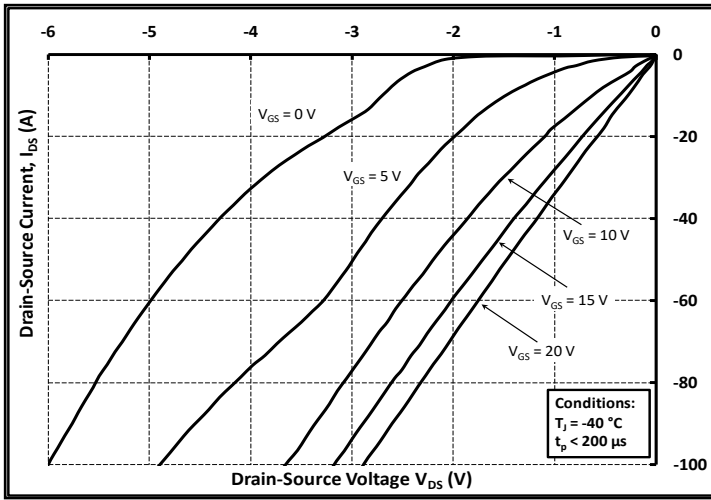


Figure 13. 3rd Quadrant Characteristic at -40 °C

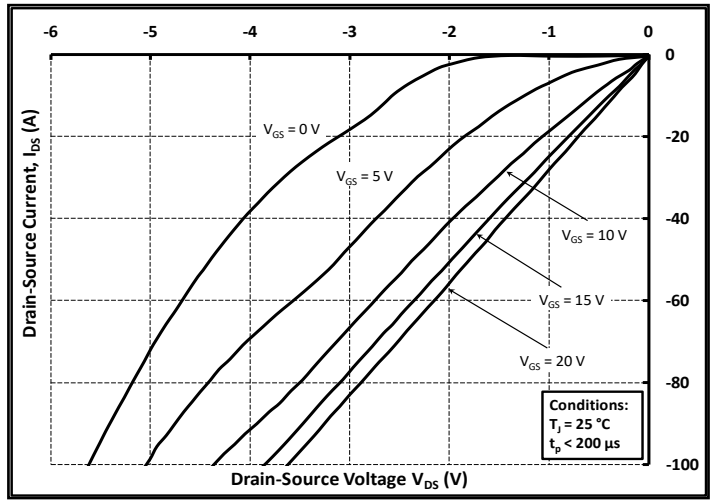


Figure 14. 3rd Quadrant Characteristic at 25 °C

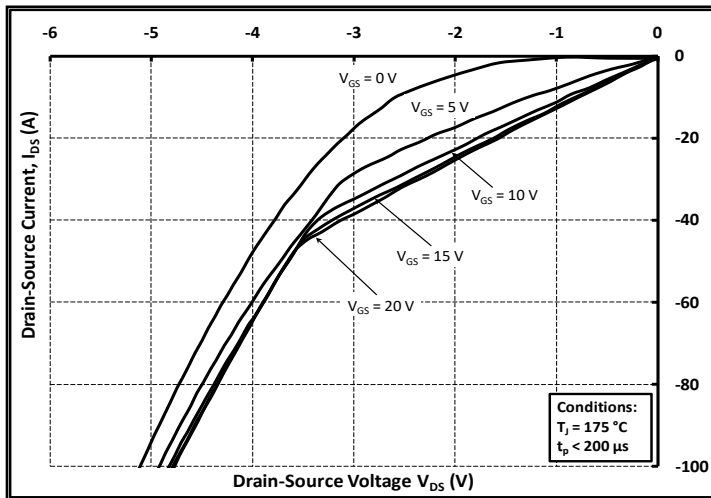


Figure 15. 3rd Quadrant Characteristic at 175 °C

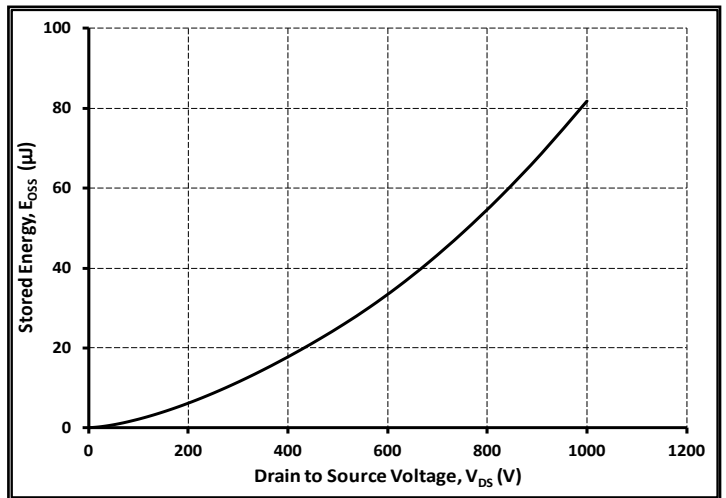


Figure 16. Output Capacitor Stored Energy

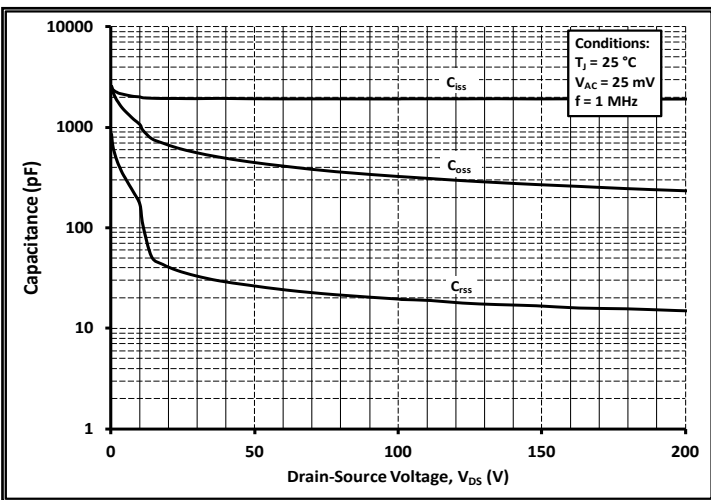


Figure 17. Capacitances vs. Drain-Source Voltage (0-200 V)

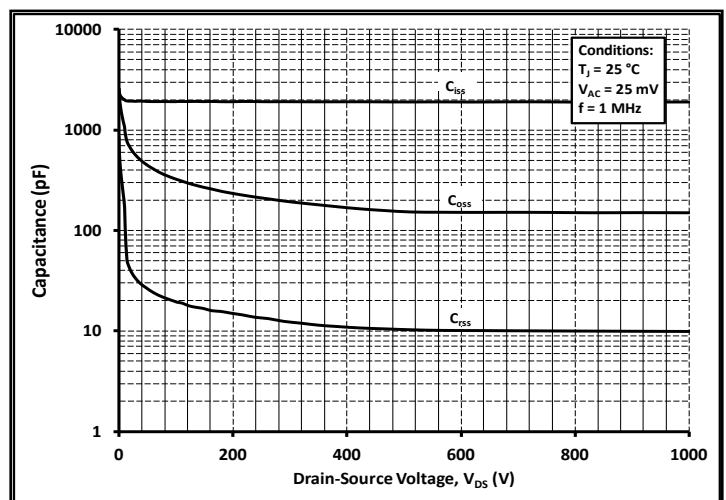
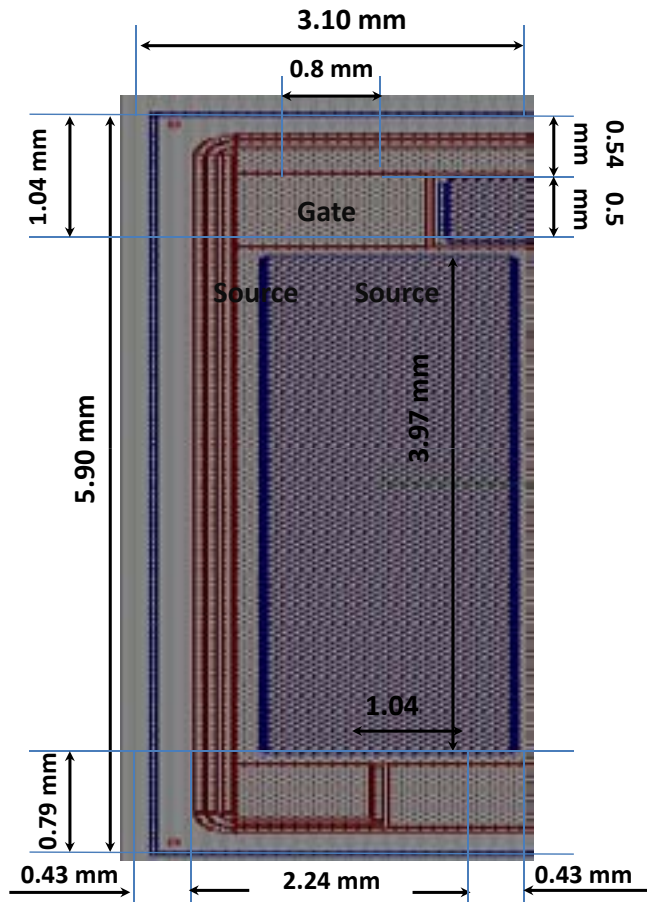


Figure 18. Capacitances vs. Drain-Source Voltage (0-1000 V)

Mechanical Parameters

Parameter	Typical Value	Unit
Die Dimensions (L x W)	3.10 x 5.90	mm
Exposed Source Pad Metal Dimensions (LxW) Each	1.04 x 3.97 (x2)	mm
Gate Pad Dimensions (L x W)	0.80 x 0.50	mm
Die Thickness	180 ± 40	µm
Top Side Source metallization (Al)	4	µm
Top Side Gate metallization (Al)	4	µm
Bottom Drain metallization (Ni/Ag)	0.8 / 0.6	µm

Chip Dimensions





Notes

- **RoHS Compliance**
The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS2), as implemented January 2, 2013. RoHS Declarations for this product can be obtained from your Cree representative or from the Product Documentation sections of www.wolfspeed.com.
- **REACH Compliance**
REACH substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact a Cree representative to insure you get the most up-to-date REACH SVHC Declaration. REACH banned substance information (REACH Article 67) is also available upon request.
- This product has not been designed or tested for use in, and is not intended for use in, applications implanted into the human body nor in applications in which failure of the product could lead to death, personal injury or property damage, including but not limited to equipment used in the operation of nuclear facilities, life-support machines, cardiac defibrillators or similar emergency medical equipment, aircraft navigation or communication or control systems, air traffic control systems.

Related Links

- C2M PSPICE Models: www.wolfspeed.com/power
- SiC MOSFET Isolated Gate Driver reference design: www.wolfspeed.com/power
- Application Considerations for Silicon-Carbide MOSFETs: www.wolfspeed.com/power