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CR5842B

High Voltage Green Mode PWM Controller with Brownout

FEATURES

- Built-in High Voltage Startup
- Patent High voltage startup technique
- Extra Low Standby (<50mW)
- Power on Soft Startup
- Frequency spreading to Minimize EMI
- Audio Noise Free Operation
- Fixed 65kHz Switching Frequency
- Brownout function
- 4000V HBM ESD
- DIP-8L Green Package
- Comprehensive Protection
  - VDD Under Voltage Lockout with Hysteresis (UVLO)
  - Cycle-by-cycle Over Current Protection (OCP)
  - Overload Protection (OLP) with Auto-recovery
  - Over Temperature Protection (OTP) with Auto-recovery
  - VDD Over Voltage Protection (OVP) with Auto-recovery

APPLICATIONS

Offline AC/DC Flyback Converter For

- AC/DC Adapter
- PDA Power Supplies
- Auxiliary Power Supply for PC and Server
- Open-frame SMPS

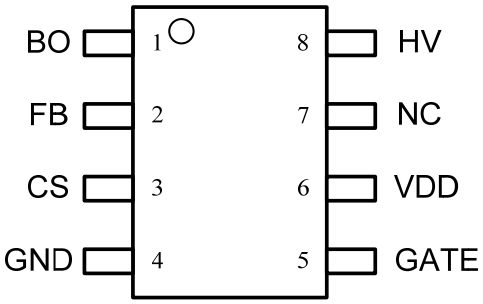
GENERAL DESCRIPTION

CR5842B is a highly integrated current mode PWM controller. It built in patent High voltage startup, optimized for high performance, exhibit extra low standby power consumption (<50mW) and costs effective offline flyback converter applications.

PWM switching frequency at normal operation is internally fixed. At no load or light load condition, it operates in burst mode to minimize switching loss. Less than 50mW standby power consumption and very high conversion efficiency is thus achieved. Patent high voltage startup is implemented in CR5842B, which features with short startup time and extra low standby current.

CR5842B offers rich protections with auto-recovery including Cycle-by-Cycle current limiting (OCP), over load protection (OLP), VDD under voltage lockout (UVLO), and over temperature protection (OTP), VDD over voltage protection (OVP). It also provides the protection with latched shut down including VDD over voltage protection. Excellent EMI performance is achieved with CR5842B proprietary frequency burst technique. The frequency at below 22kHz is minimized to avoid audible noise during operation.

PIN ASSIGNMENT

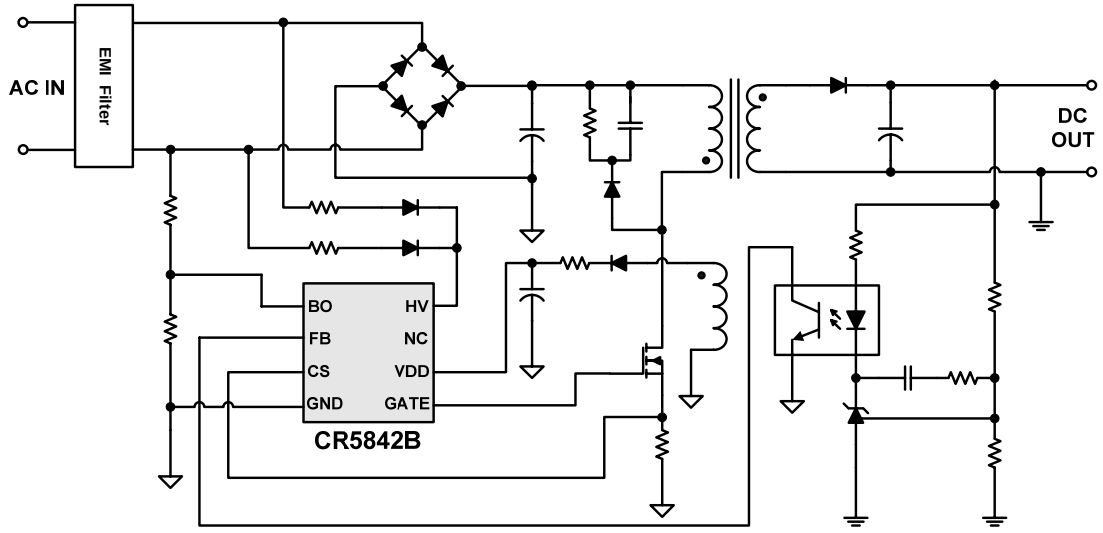


SOP-8L

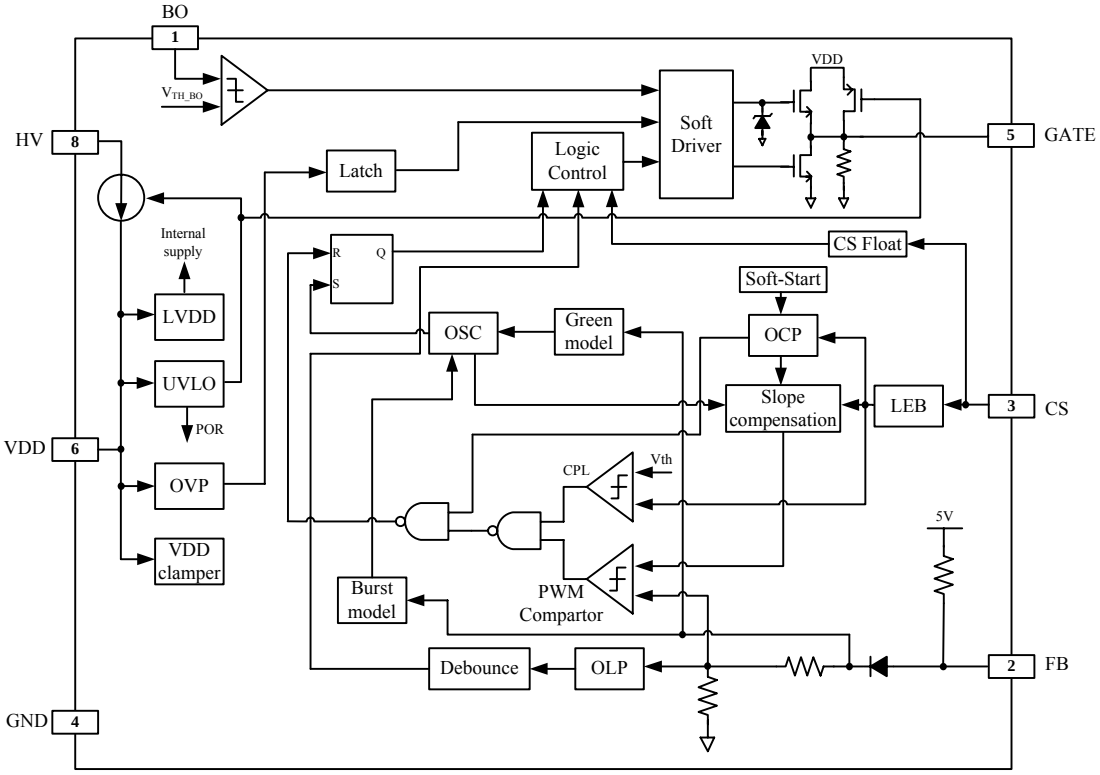
PIN DESCRIPTIONS

Pin No.	Symbol	Description
1	BO	Connected resistors for brownout protection
2	FB	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and the current-sense signal at CS pin.
3	CS	Current sense input.
4	GND	Ground
5	GATE	Gate driver output. Drive the power MOSFET.
6	VDD	Power Supply
7	NC	No Connect
8	HV	Connected to the line input or bulk capacitor via resistors for startup.

TYPICAL APPLICATION



BLOCK DIAGRAM



Simplified Internal Circuit Architecture

ABSOLUTE MAXIMUM PARAMETERS

Symbol	Parameter		Value	Unit
V_{DD}	Supply voltage Pin Voltage		30	V
V_{HV}	High-Voltage Pin Voltage		700	V
I_{OVP}	VDD OVP clamp current		10	mA
V_{FB}	Input Voltage to FB Pin		-0.3 to 6V	V
V_{CS}	input Voltage to CS Pin		-0.3 to 6V	V
V_{BO}	input Voltage to BO Pin		-0.3 to 6V	V
T_L	Lead Temperature (Soldering)	10s SOP-8L	260	℃
T_{STG}	Operating Junction Temperature Range		-55 to + 150	℃

RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Min. ~ Max.	Value
V_{DD}	VDD Supply Voltage	10~23	V
T_{OA}	Operation Ambient Temperature	-20~85	℃
P_O	Maximal Output Power	20～65	W

ELECTICAL CHARACTERISTICS

(TA=25℃ V_{DD} = 18V, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{HV}	Supply current from HV pin	VDD=2V, HV=100V		2		mA
$I_{HV\_leakage}$	HV pin leakage current after startup	VDD=18V, HV=500V			5	μA
Supply Voltage (VDD)						
I_{ST}	Start up Current			5	20	μA
I_{OP}	Operating Current	V_{FB}=3V		2	2.5	mA
	Burst Mode Current	VDD=15V, V_{FB}=1V		0.8	1	mA
$UVLO_{\_OFF}$	Turn-on Threshold Voltage		13.5	14.5	15.5	V
$UVLO_{\_ON}$	Turn-off Threshold Voltage		8	9	10	V
Vpull-up	Pull-up PMOS active			12		V
V_{DD_CLAMP}	VDD Clamp Voltage	I_{VDD}=10mA	30	32	34	V
V_{DD_OVP}	VDD OVP Voltage		24	26	28	V
Vth_recovery	Auto release threshold			5		V
Vth_latch	Latch release threshold			4.2		V
Feedback Input Section (FB Pin)						
I_{FB}	Short Circuit Current	V_{FB}=0V		0.2		mA
V_{FB}	Open Loop Voltage	V_{FB}=Open		5		V
Dmax	Maximum Duty Cycle PWM		75	80	85	%
V_{REF_GREEN}	Enter PFM REF Voltage			1.8		V
$V_{REF\_Burst\_H}$	Quit Burst Mode			1.2		V
$V_{REF\_Burst\_L}$	Enter Burst Mode			1.1		V
V_{OLP}	Enter OLP FB Voltage			3.7		V
T_{OLP}	OLP Delay Time		80	88	96	ms
Z_{FB}	Impedance			25		kohm
Current Sense Input (CS Pin)						
SST	Soft start time			4		ms
T_blanking	Leading edge blanking time			320		ns
Z_{CS}_IN	Input Impedance			40		kohm
T_{D_OC}	Delay to Output			60		ns
V_{TH_OC}	Current Limiting Threshold Voltage with zero duty cycle			0.75		V
$V_{OCP\_clamping}$	Current limiting threshold at maximum Duty			0.9		V
Oscillator						
F_{OSC}	PWM Normal Frequency		60	65	70	kHz

F_{PFM}	PFM Minimum Frequency			22		kHz
ΔF_{VDD}	Frequency VDD. Stability			1		%
ΔF_{TEMP}	Frequency Temp. Stability			1		%
F_{JITTER}	Frequency jitter			±4		%
$F_{shuffling}$	Shuffling frequency			32		Hz
Brownout protection						
$V_{TH\_BO\_L}$	Brownout threshold		0.75	0.8	0.85	V
$V_{TH\_BO\_H}$	Brownout release threshold		0.90	0.95	1.00	V
Td_brownout	Brownout debounce time		60		80	ms
Gate Drive Section (GATE Pin)						
V_{OL}	Output Low Level	VDD=15V, I_O=20mA			1	V
V_{OH}	Output High Level	VDD=15V, I_O=20mA	8			V
V_{G_CLAMP}	Output Clamp Voltage Level	VDD=20V		15		V
$T_{\_R}$	Output Rising Time	C_L=1nF		70		ns
$T_{\_F}$	Output Falling Time	C_L=1nF		30		ns
On Chip OTP						
OTP	Over temperature protection trip point with Recommended PCB layout.			150		℃

OPERATION DESCRIPTION

CR5842B is a highly integrated current mode PWM controller optimized for high performance, extra low standby power consumption and cost effective offline flyback converter applications. The burst mode control greatly reduces the standby power consumption (less than 50mW) and helps the design easily to meet the international power conservation requirements.

Internal High Voltage Startup and Under Voltage Lockout (UVLO)

CR5842B integrates HV startup circuit. During power on state, it provides about 2mA current to charge the capacitor connecting between VDD and Ground from HV pin. When the voltage level at VDD is higher than UVLO_OFF, the charge current is switched off. At this moment, the VDD capacitor provides current to CR5842B until the auxiliary winding of the main transformer starts to provide the operation current. In general application, a 51kΩ (typical) resistor is recommended to be placed in the high voltage path to limit the current.

Operating Current

The operating current of CR5842B is 2mA. Good efficiency is achieved with this low operating current together with the burst mode control features. The operation current is greatly reduced at no/light conditions such that extra low standby (less than 50mW) can be achieved.

Soft Start

CR5842B features an internal typical 4ms soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power on sequence. As soon as VDD reaches UVLO_OFF, the primary winding current is controlled to be gradually increased to the maximum level. Every restart up is followed by a soft start.

Frequency spreading for EMI improvement

The frequency spreading (switching frequency modulation) is implemented in CR5842B. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.

Green-Mode Operation

CR5842B provides green-mode control to reduce the switching frequency in light-load and no-load conditions. VFB, which is derived from the voltage feedback loop, is taken as the reference. Once VFB is lower than the threshold voltage (VREF_GREEN), switching frequency is continuously decreased to the minimum green-mode frequency of around 22 kHz.

Burst Mode Operation

At light load or zero load condition, most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss and thus conserves the energy.

The switching frequency is internally adjusted at no load or light load condition. The switching frequency is reduced at light/no load condition to improve the conversion efficiency. At light load or no load condition, the FB input drops below burst mode threshold voltage (VREF_Burst_L) and device enters burst mode control. The gate driver output switches only when FB voltage is higher than the threshold voltage (VREF_Burst_H) to output an on state. Otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend.

The switching frequency control also eliminates the audible noise at any load conditions.

Oscillator Operation

The switching frequency is internally fixed at 65kHz. No external frequency setting components are needed for PCB design simplification.

Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in CR5842B current mode PWM control. The switching current is detected by a sense resistor connected to the CS pin. An internal leading edge blanking circuit chops off the sensed voltage spikes due to snubber diode reverse recovery and surge gate current of power MOSFET at initial power MOSFET on state. The current limiting comparator is disabled and cannot turn off the power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and eliminates the sub-harmonic oscillation and thus reduces the output ripple voltage.

Driver

The power MOSFET out of CR5842B is driven by a dedicated gate driver for power switching control. Too weak the gate driver results in higher conduction and switch loss of power MOSFET while too strong gate driver results in the compromise of EMI.

A good tradeoff is achieved through the built-in totem pole gate design with well controlled output strength and dead time control. The low idle loss and good EMI system design is achieved with this dedicated control scheme.

Protection Controls

Good power supply system reliability is achieved with auto-recovery protection features including Cycle-by-Cycle current limiting (OCP), Over Load Protection (OLP), over temperature protection (OTP), Under Voltage Lockout on VDD (UVLO), and latched shutdown features

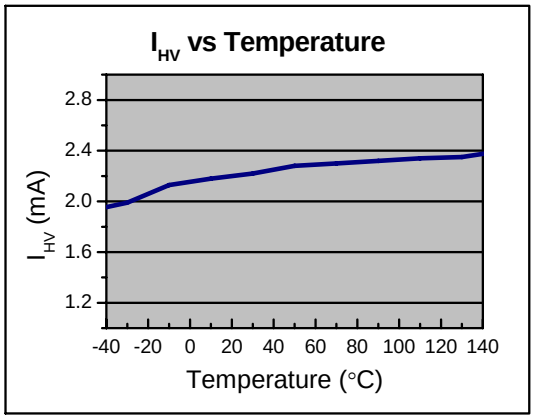
including VDD over voltage protection (OVP).

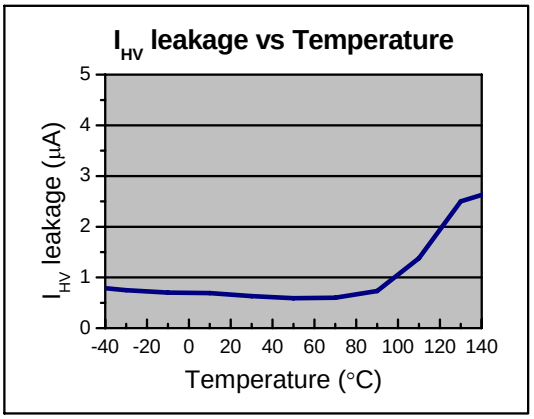
The OCP is line voltage compensated to achieve constant output power limit over the universal input voltage range.

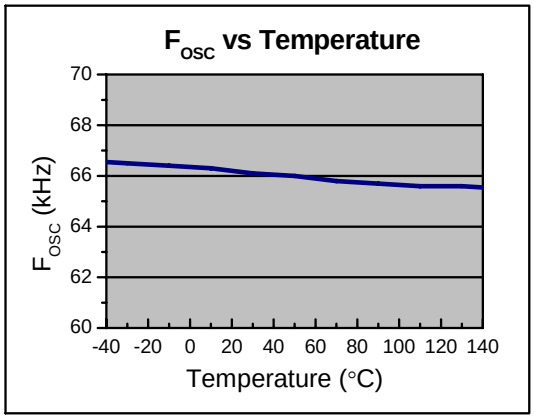
At overload condition, when FB input voltage exceeds power limit threshold value for more than TOLP, control circuit shuts down the converter. It restarts when VDD voltage drops below Vth_recovery.

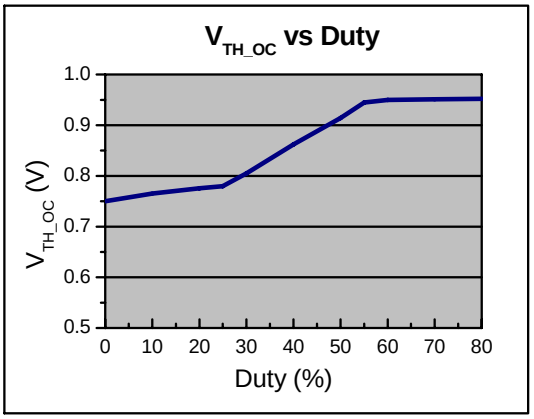
CHARACTERIZATION PLOTS

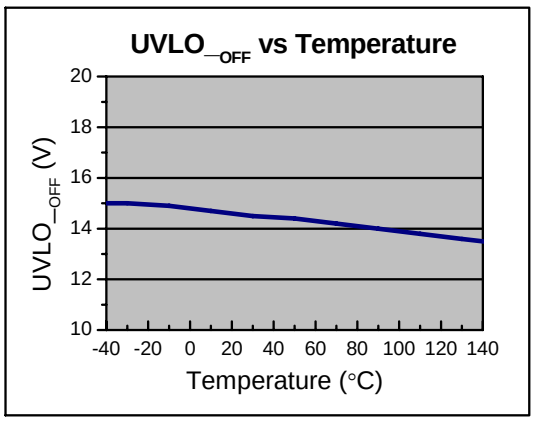
(VDD=18V, TA=25℃)

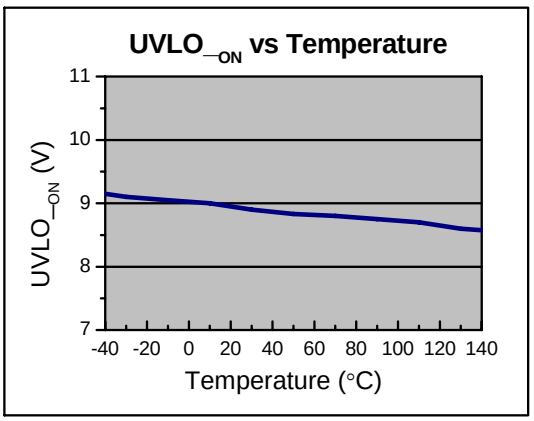




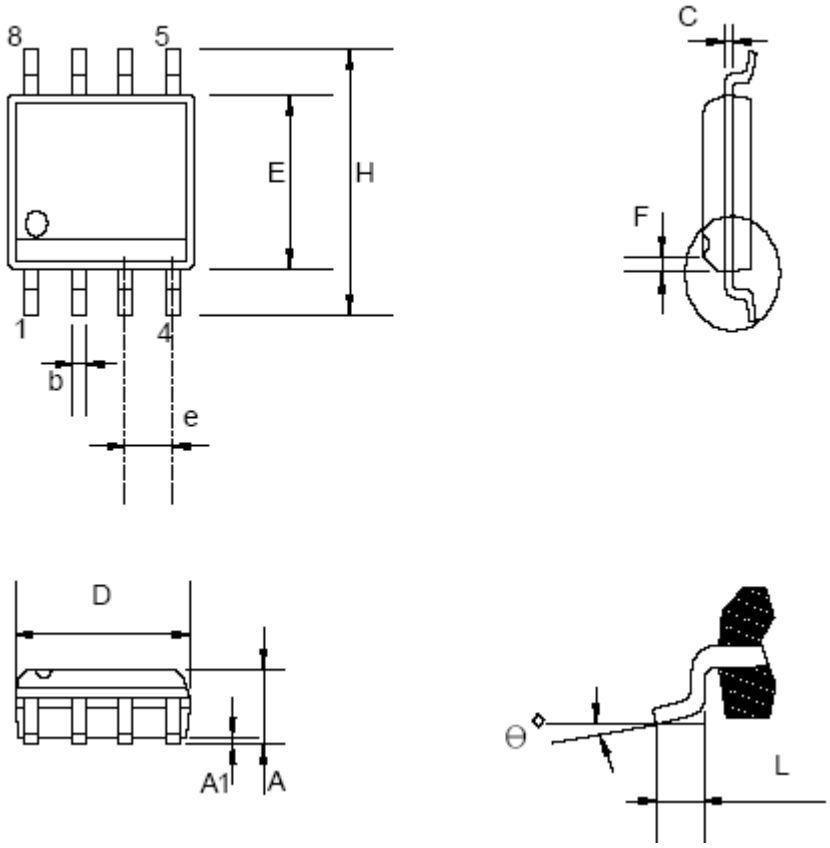






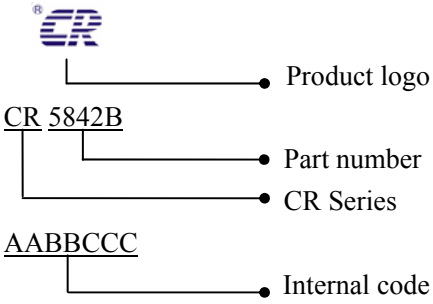


PACKAGE OUTLINE DIMENSIONS
SOP-8L



Symbol	Millimeter			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.346		1.752	0.053		0.069
A1	0.101		0.254	0.004		0.010
b	0.38		0.510	0.015		0.020
c	0.17		0.230	0.007	0.008	0.009
D	4.648		5.050	0.183		0.199
E	3.810		3.987	0.150		0.157
e	1.016	1.270	1.524	0.040	0.050	0.060
F		0.381X45°			0.015X45°	
H	5.791		6.197	0.228		0.244
L	0.406		1.270	0.016		0.050
θ°	0°		8°	0°		8°

PRINTING INFORMATION



ORDERING INFORMATION

Part number	package	Packaging Material	One plate	One box	One case
CR5842B	SOP-8L	Tube	100	10000	100000

The product minimum order quantity is 10,000, the quantity of one box.