8-Bit Microcontroller

DATA SHEET

=========CR80P200=========

Crescenic Technology Corporation

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CR80P200 Data Sheet

Table of Contents

1. General Description

The CR80P200 is an EPROM microcontroller with 8 bits, which takes advantage of a thorough CMOS technology improved with low cost, high speed, and high noise immunity. Preferably, integrated into this single chip are a Watchdog Timer, a RAM, an EPROM, a tri-state I/O port, a power-down mode, and a real time programmable clock/counter. CR80P200 works with 48 instructions, wherein all of them are single instruction cycles except that the program branches take 2 cycles.

1.1 Device options included in this data sheet:

CR80P200A
CR80P200B
CR80P200D
CR80P200E

1.2 Features

- Full CMOS static design.
- Very flexible 4 comparators application
- Better noise immunity
- Additional instructions BCTR and BRTC for easy use of transferring between Carry bit and Register bit
- Operating voltage range: 2.3V to 5.5V (without using comparator mode application)
  3.0 V to 5.5 V (with using comparator mode application)
- Operating temperature ranging from 0℃~70℃
- Operating frequency at 0 up to 20M Hz, Vdd = 5 V, in a high frequency crystal mode; (An additional product operating at a higher frequency is provided for customers to choose; please contact our local sales for said specification if necessary.)
- 8-bit data bus
- Internal EPROM with 2K words in size
- 72-byte internal RAM with Bank control
- 16 special purpose registers
- Both 22 general purpose I/O pins and 1 counter input pin for I/O pins
- 5-level stacks of a program counter
- Four types of event vectors, including 3 interrupt vectors and 1 reset vector
- Three interrupt sources:

a Port A interrupt
a Timer/counter interrupt
and a Watchdog timer timeout interrupt

- Bonding options:
  - Multiple Vref. comparator or single Vref. Comparator
  - Parallel programming or serial programming

- Configure options:

-- 4 oscillator types selected by code option:
RC -- RC oscillator
LFXT -- Low frequency crystal oscillator
XTAL -- Crystal oscillator
HFXT -- High frequency crystal oscillator

-- 4 oscillator start-up time selected by code option:
172μs, 22ms, 44ms, and 88ms

--Watchdog timer: enabled, disabled, and disabled during sleep, selected by code option

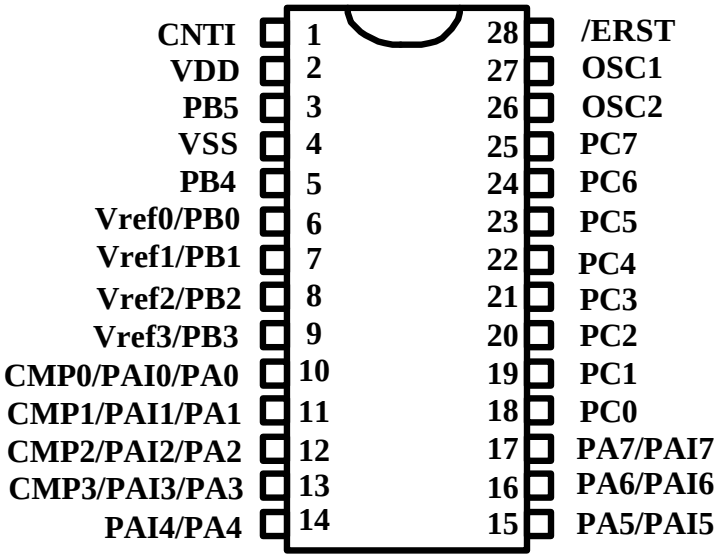
Serial programming needs only 5 pins (Vdd, Vss, CNTI, PA0, PA1) to program EPROM and configurations. It is suitable for on-board programming or packages with fewer pins.

2. Pins Assignment

The package patterns of CR80P200, corresponding to the programming mode for EPROM and the reference voltage of comparators, are respectively divided as follows:
CR80P200A for single Vref. in parallel programming mode
CR80P200B for multiple Vref. in parallel programming mode
CR80P200D for single Vref. in serial programming mode
CR80P200E for multiple Vref. in serial programming mode
Illustrated as below are the package patterns mentioned above and said pins configuration.

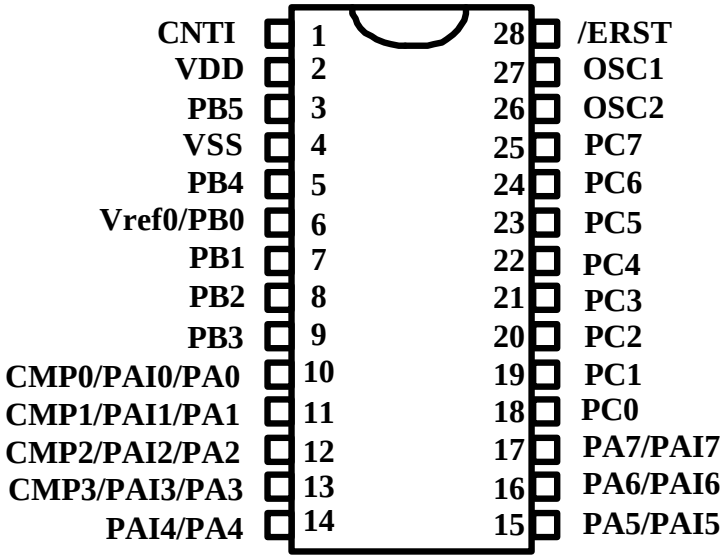
1. CR80P200BN28/CR80P200EN28 (for 28-pin package)

SOP, SSOP, PDIP, and Skinny PDIP



2. CR80P200AN28/CR80P200DN28 (for 28-pin package)

SOP, SSOP, PDIP, and Skinny PDIP



2.1 Pins Description

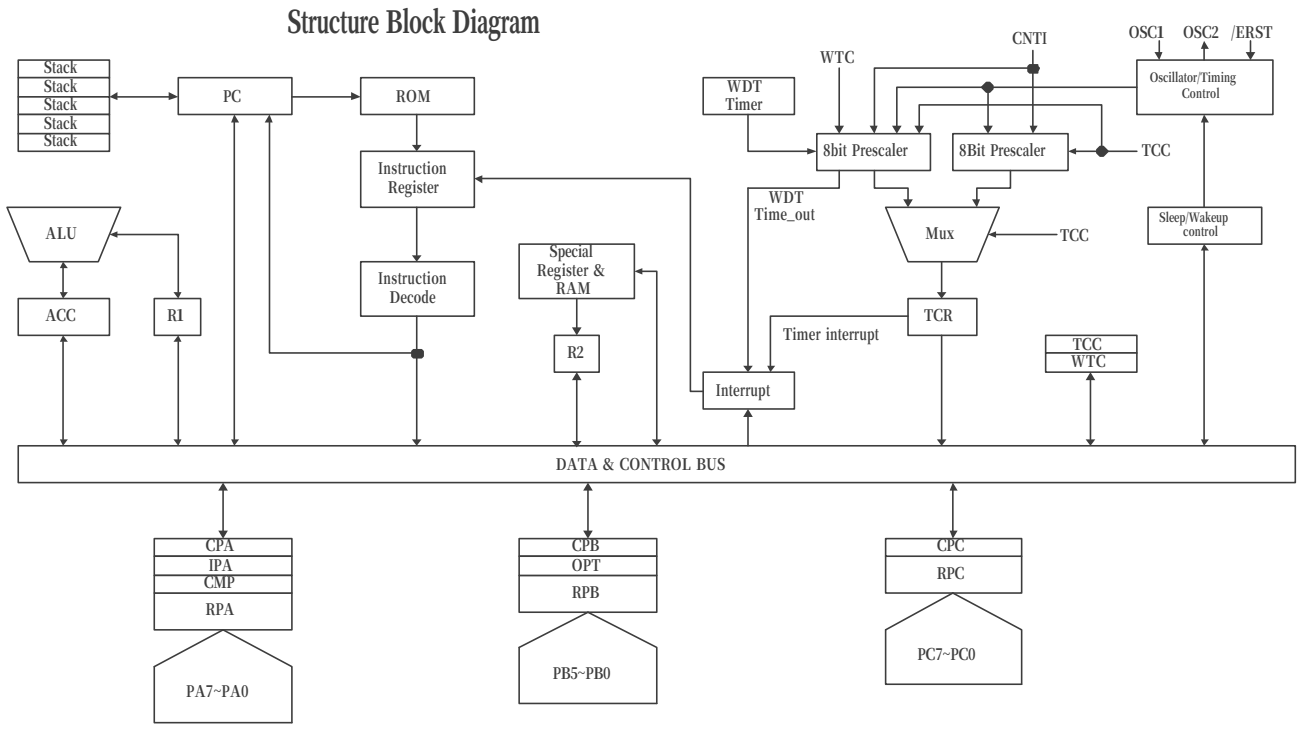
2.1.1 CR80P200BN28/CR80P200EN28 (for 28-pin package)

Name	No.	I/O Type	Input Level	Description
PA0/CMP0/PAI0	10	I/O	TTL	PA0 - - PA3 are bi-directional I/O ports. CMP0- -CMP3 are comparator inputs. PAI0 - - PAI3 are port A interrupt inputs.
PA1/CMP1/PAI1	11	I/O	TTL	
PA2/CMP2/PAI2	12	I/O	TTL	
PA3/CMP3/PAI3	13	I/O	TTL	
PA4/PAI4	14	I/O	TTL	PA4 - - PA7 are bi-directional I/O ports. PAI4 - - PAI7 are port A interrupt inputs.
PA5/PAI5	15	I/O	TTL	
PA6/PAI6	16	I/O	TTL	
PA7/PAI7	17	I/O	TTL	
PB0/VREF0	6	I/O	TTL	PB0 - - PB5 are bi-directional I/O ports. Vref0 - - Vref3 are comparator reference inputs.
PB1/VREF1	7	I/O	TTL	
PB2/VREF2	8	I/O	TTL	
PB3/VREF3	9	I/O	TTL	
PB4	5	I/O	TTL	
PB5	3	I/O	TTL	
PC0	18	I/O	TTL	PC0 - - PC7 are bi-directional I/O ports.
PC1	19	I/O	TTL	
PC2	20	I/O	TTL	
PC3	21	I/O	TTL	
PC4	22	I/O	TTL	
PC5	23	I/O	TTL	
PC6	24	I/O	TTL	
PC7	25	I/O	TTL	
CNTI	1	I	Schmitt Trigger	A clock input to TCR; in order to avoid the leakage current, this pin must be tied to pull-high or pull-low.
/ERST	28	I	Schmitt Trigger	An external reset input pin; this pin is an active-low reset to the device. A built-in pull high resistor
OSC1	27	I	-	An input pin of oscillator crystal input/external clock source Input pin for RC oscillator
OSC2	26	O	-	Oscillator crystal output 1/4 Fosc1 output for RC oscillator
VDD	2	P	-	Power supply
VSS	4	P	-	Ground

2.1.2 CR80P200AN28/CR80P200DN28 (for 28-pin package)

Name	No.	I/O Type	Input Level	Description
PA0/CMP0/PAI0	10	I/O	TTL	PA0 - - PA3 are bi-directional I/O ports. CMP0- -CMP3 are comparator inputs. PAI0- -PAI3 are port A interrupt inputs.
PA1/CMP1/PAI1	11	I/O	TTL	
PA2/CMP2/PAI2	12	I/O	TTL	
PA3/CMP3/PAI3	13	I/O	TTL	
PA4/PAI4	14	I/O	TTL	PA4 - - PA7 are bi-directional I/O ports. PAI4- -PAI7 are port A interrupt inputs.
PA5/PAI5	15	I/O	TTL	
PA6/PAI6	16	I/O	TTL	
PA7/PAI7	17	I/O	TTL	
PB0/Vref0	6	I/O	TTL	PB0 - - PB5 are bi-directional I/O ports. Vref0 is a comparator reference input.
PB1	7	I/O	TTL	
PB2	8	I/O	TTL	
PB3	9	I/O	TTL	
PB4	5	I/O	TTL	
PB5	3	I/O	TTL	
PC0	18	I/O	TTL	PC0 - - PC7 are bi-directional I/O ports.
PC1	19	I/O	TTL	
PC2	20	I/O	TTL	
PC3	21	I/O	TTL	
PC4	22	I/O	TTL	
PC5	23	I/O	TTL	
PC6	24	I/O	TTL	
PC7	25	I/O	TTL	
CNTI	1	I	Schmitt Trigger	A clock input to TCR; in order to avoid the leakage current, this pin must be tied to pull-high or pull-low.
/ERST	28	I	Schmitt Trigger	An external reset input pin; this pin is an active-low reset to the device. A built-in pull high resistor
OSC1	27	I	-	An input pin of oscillator crystal input/external clock source Input pin for RC oscillator
OSC2	26	O	-	Oscillator crystal output 1/4 Fosc1 output for RC oscillator
VDD	2	P	-	Power supply
VSS	4	P	-	Ground

3. Block Diagram of Structure



4. Memory mapping

4.1 Special Register & Internal RAM

00 INDirect addressing register (IND)
{CTRLR 00/h => Watchdog Timer Control register, WTC}
01 Timer/Counter Register (TCR)
{CTRLR 01/h => Timer/Counter Control register, TCC}
02 Program Counter, Low byte (PCL)
{CTRLR 02/h => Port A Interrupt control register, IPA}
03 Status Flag Register (SFR)
{CTRLR 03/h => OPTion control register, OPT}
04 Memory Index Register (MIR)
{CTRLR 04/h => CoMParator control register, CMP}
05 Port A data Register (RPA)
{CTRLR 05/h => Port A Control register, CPA}

06 Port B data Register (RPB)
{CTRLR 06/h => Port B Control register, CPB}
07 Port C data Register (RPC)
{CTRLR 07/h => Port C Control register, CPC}

Note: CTRLR is one of the RISC instructions for writing or reading these special control registers.

08		Internal RAM
09		Internal RAM
0A		Internal RAM
0B		Internal RAM
0C		Internal RAM
0D		Internal RAM
0E		Internal RAM
0F		Internal RAM
10	1F	Internal RAM
20	2F	Internal RAM (Bank Disabled) / Mapping to 10 1F(Bank Enabled)
30	3F	Internal RAM
40	4F	Internal RAM (Bank Disabled) / Mapping to 10 1F(Bank Enabled)
50	5F	None (Bank Disabled) / Internal RAM (Bank Enabled)
60	6F	None (Bank Disabled) / Mapping to 10 1F(Bank Enabled)
70	7F	None (Bank Disabled) / Internal RAM (Bank Enabled)

Hint:

If you don't understand the description above very well, please refer to the memory map shown below and the special function registers in chapter 5.1.

- **No Memory Bank (OPT bit7=0)**

Memory address = 00~4FH (continuous memory addressing mode)

• **Memory Bank (OPT bit7=1), illustrated in the form of table below:**

Address	Description			
MIR<6:5>	Bank 0 00	Bank 1 01	Bank 2 10	Bank 3 11
00h	IND			
01h	TCR			
02h	PCL			
03h	SFR			
04h	MIR			
05h	RPA		Address map back to address in bank 0	
06h	RPB			
07h	RPC			
08h~0Fh	General Purpose Register			
	10h~1Fh General Purpose Register	30h~3Fh General Purpose Register	50h~5Fh General Purpose Register	70h~7Fh General Purpose Register

5. Function Control Registers

5.1 Special Function Control Registers

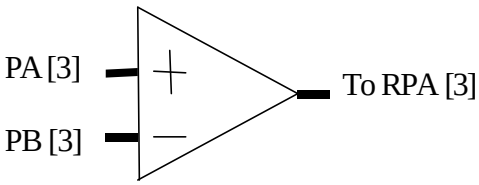
Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	**IND**	Use contents of MIR to address data memory (not a physical register)							
01h	**TCR**	8 bits of real-time clock/counter							
02h	**PCL**	Program counter with low byte							
03h	**SFR**	GB	PP1	PP0	/WD	/SP	Z	AC	C
04h	**MIR**	Indirect data memory address pointer							
05h	**RPA**	RPA7	RPA6	RPA5	RPA4	RPA3	RPA2	RPA1	RPA0
06h	**RPB**	-	-	RPB5	RPB4	RPB3	RPB2	RPB1	RPB0
07h	**RPC**	RPC7	RPC6	RPC5	RPC4	RPC3	RPC2	RPC1	RPC0

Note:

1. Access to these control registers can be executed in normal direct or indirect addressing mode.
2. GB does not defined as a specified function and can be used as a general purpose memory bit .
3. Bit 7 of MIR is an unimplemented bit, always read as ' 1' .
4. The symbol "-" means an unimplemented bit, always read as ' 0' .
5. Legend: GB = General memory Bit PP1, PP0 = Program memory page bits
   /WD = WatchDog flag /SP = SleeP flag
   AC = Auxiliary Carry flag C = Carry flag

Z = Zero flag

5.2 Implicit Function Control Registers

CTRLR Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	WTC	CNTI	WDTI	TCLK	EGTY	PSCA	PSC2	PSC1	PSC0
01h	TCC	TCEI	TCEN	PSCS	PSCC	TPSC	PSC2	PSC1	PSC0
02h	IPA	Port A interrupt control register							
		A '1' in this register will allow a low pulse applied to the corresponding pin of port A to generate an interrupt and wake up the MPU. The interrupt and wake-up function are valid only while the pin is not defined as an output pin.							
03h	OPT	RAMB	IOWM	-	-	-	-	-	-
		<RAMB> RAM Bank enable bit "0" for disabling RAM bank function "1" for enabling RAM bank function (default) <IOWM> I/O port write mode for read-then-write instruction. "0" for reading the latch → operation → write (default) "1" for reading the interface → operation → write							
04h	CMP	VRF3	VRF2	VRF1	VRF0	CMP3	CMP2	CMP1	CMP0
		<CMP3:CMP2:CMP1:CMP0> Define RPA bit[3:0] input function 0 Digital input 1 Comparator input <VRF3:VRF2:VRF1:VRF0> CMP[3:0] reference voltage select For multiple Vref mode: 0 1/2 VDD internal Vref 1 External Vref input RPB[3:0] For single Vref mode: 0 1/2 VDD internal Vref 1 External Vref input RPB[3:0] e.g. if CMP[3] and VRF[3], respectively, is set for comparator and external Vref., then PB[3] is assigned as a voltage reference of PA[3].  (*Please turn to page 26 for said additional description*.)							
05h	CPA	Port A control register							
		A '0' in this register will set the corresponding pin of port A to an output.							

06h	**CPB**	-	-	Port B control register
		A '0' in this register will set the corresponding pin of port B to an output. Bit [7:6] are unimplemented and always read as '0'.		
07h	**CPC**	Port C control register		
		A '0' in this register will set the corresponding pin of port C to an output.		

Note:

1. Access to these control registers is only executed by the instruction "CTRLR".

2. The symbol " - " means an unimplemented bit and always read as '0' .

5.3 Program Memory and Reset&Interrupt Vectors

000-7FB for program memory

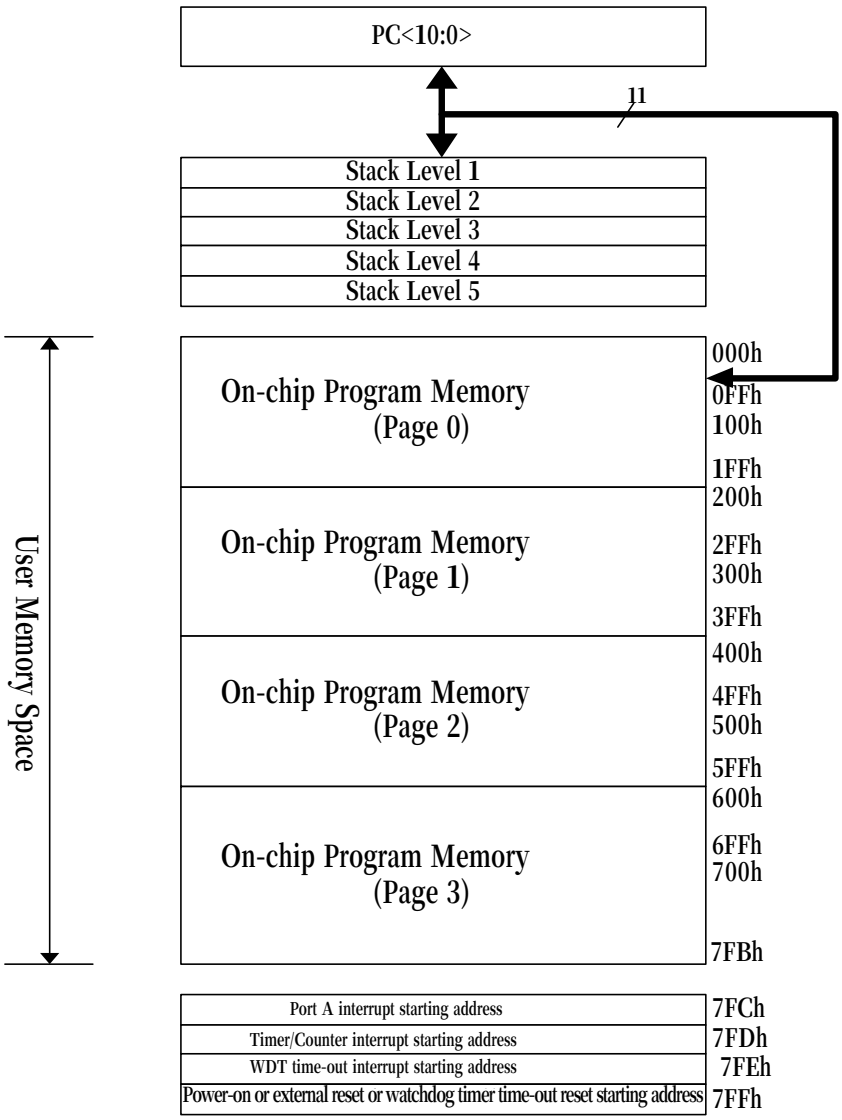
7FC for port A interrupt starting address

7FD for timer/counter interrupt starting address

7FE for watchdog timer time-out interrupt starting address

7FF for power-on or external reset or watchdog timer time-out reset starting address

6. Program Memory Map and Stack



6.1 Special Registers

1) 00H [7:0] **< IND > INDirect addressing register {RW}**

Description:

Not serving as a physical register, this register is used as an indirect address pointer. Reading or writing this address will have access to the register of the address defined by the 04H (MIR).

MIR (04H) = 0 indicates that the result=00H will appear if IND (00H) is read, and the operation will be being executed as a NOP (No OPeration), maybe affecting C, AC, or Z flag, if IND (00H) is written in.

2) 01H [7:0] **< TCR > Timer/Counter Register {RW}**

Description:

If a timer/counter is enabled, after powered on, the counter will start to count up. An interrupt, if enabled, will be generated while the counter reaches 255; unless otherwise an interrupt is disabled, the counter will not continue to count until a new value is loaded.

3) 02H [7:0] **< PCL > Program Counter Low byte {RW}**

Description:

This register is a low byte of the PC (program counter). Writing this register will change the PC.

4) 03H [7:0] **< SFR > Status Flag Register {RW}**

Description:

[0] = < C > Carry flag

Carry flag represents the operational results of addition and subtraction, wherein "0" indicates that the result of operation does not generate a carryout in the MSB and "1" indicates that the result of operation generates a carryout in the MSB. A subtraction is executed by adding the 2's complement of the operand. By the way, please refer to instruction set for other affected flags.

C	*Yes*	*No*
Carry (Addition)	1	0
Borrow (Subtraction)	0	1

[1]= < AC > Auxiliary Carry flag

"0" indicates that the result of operation does not generate a carryout in bit3;

"1" indicates that the result of operation generates a carryout in bit3.

Auxiliary Carry flag feature about operates addition and subtraction

AC	*Yes*	*No*
Carry from b3 (Addition)	1	0
Borrow for b3 (Subtraction)	0	1

[2]= < Z > Zero flag

"0" indicates that the result of operation is not zero;

"1" indicates that the result of operation is zero.

[3]= < /SP > SleeP flag

"0" for a bit coming after SLEEP or STDBY instruction. (The status bit can't be recovered to '1' automatically, so you have to set this bit manually after SLEEP or STDBY.);

"1" for power-up or the execution of CLRWT instruction

[4]= < /WT > Watchdog Timer flag

"0" for watchdog timer timeout;

"1" for power-up or the execution of CLRWT, SLEEP, and STDBY instructions

[6:5] = <PP1:PP0 > Program memory Page bits

[7] = < GB > General register Bit

GB does not defined as a specified function and can be used as a general purpose memory bit .

EVENT	***/WT***	***/SP***
SLEEP, STDBY	1	0
CLRWT instruction	1	1
Power up	1	1
Watchdog timeout	0	*

*: unaffected

/WT	***/SP***	***DESCRIPTION***
0	0	Watchdog timer timeout reset or interrupt during SLEEP, STDBY
0	1	Watchdog timer timeout reset or interrupt not during SLEEP, STDBY
1	0	External reset, Port A, Timer/Counter interrupt during SLEEP, STDBY
1	1	Power-on reset
u	u	External reset, Port A, Timer/Counter interrupt not during SLEEP, STDBY

u: unchanged

PP0, PP1:

Below shown is a table illustrating PP0 and PP1 status.

PP1	*PP0*	*Program segment address*
0	0	000 7FFH == 000 7FFH
0	1	000 1FFH == 200 3FFH
1	0	000 1FFH == 400 5FFH
1	1	000 1FFH == 600 7FFH

(1) [PP1:PP0] == 00 (default)

⊙ JUMP aADDR ; aADDR = A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0

↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓

PC = A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0

⊙ CALL aADDR ; aADDR = A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0

↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓

PC = A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0

⊙ WRITE PCL ; PC = A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0

Data 8 Bits = B7 B6 B5 B4 B3 B2 B1 B0

Operation result = D7 D6 D5 D4 D3 D2 D1 D0

PP1 PP0

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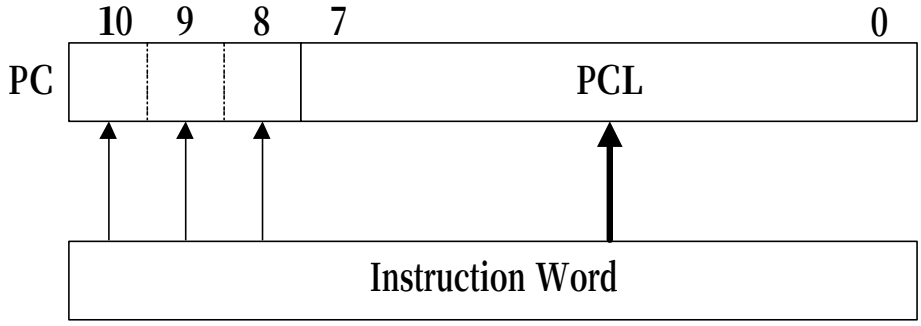
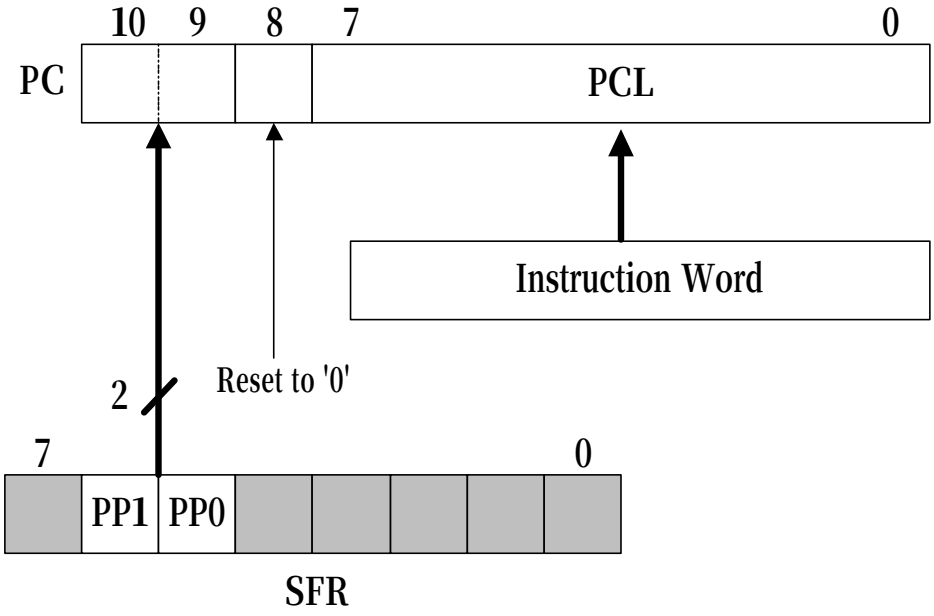
PC = 0 0 0 D7 D6 D5 D4 D3 D2 D1 D0

JUMP or CALL Instruction



WRITE Instruction



(2) [PP1:PP0] ≠ 00

⊙ JUMP aADDR ; aADDR = A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0

PP1 PP0

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PC = PP1 PP0 A8 A7 A6 A5 A4 A3 A2 A1 A0

⊙ CALL aADDR ; aADDR = A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0

PP1 PP0

↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓

PC = PP1 PP0 0 A7 A6 A5 A4 A3 A2 A1 A0

⊙ WRITE PCL ; PC = A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0

Data 8 Bits = B7 B6 B5 B4 B3 B2 B1 B0

Operation result = D7 D6 D5 D4 D3 D2 D1 D0

PP1 PP0

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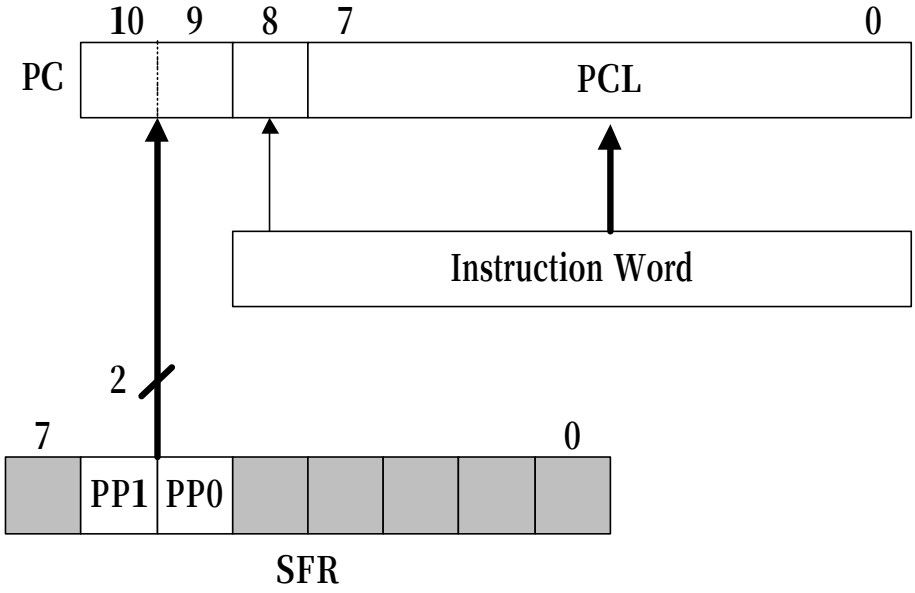
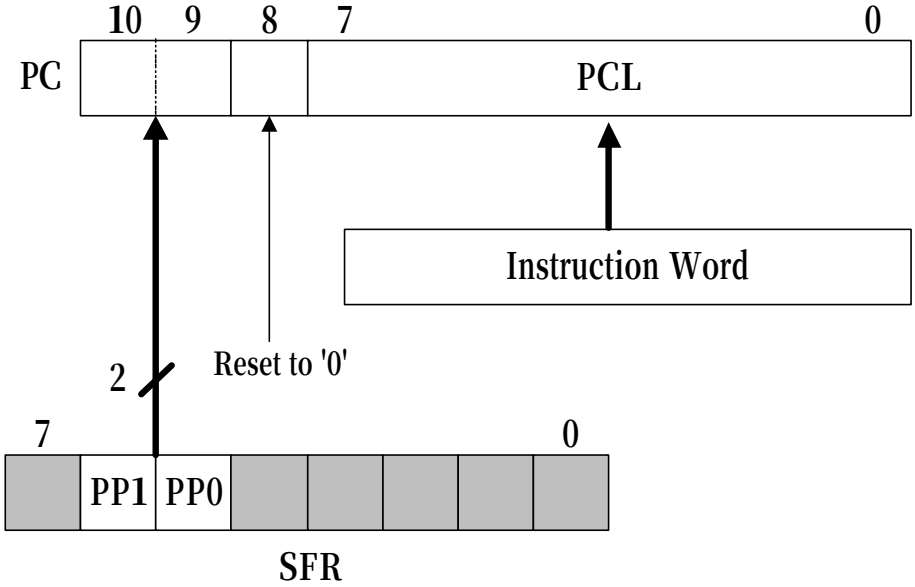
PC = PP1 PP0 0 D7 D6 D5 D4 D3 D2 D1 D0

JUMP Instruction



CALL or WRITE Instruction



5) 04H [7:0] **< MIR > Memory Index Register {RW}**

Description:

[6:0] indicates that this register used in the indirect addressing mode defines which register will be selected during the instruction to read/write 00H.

[7]=< unimplemented > always read as ' 1'

(1) [RAMB](b7 of OPT) == 0

⊙ MIR[6:0] → 00 4FH ≡ 00 4FH

[RAMB] (b7 of OPT) == 1 (default)

⊙ MIR [6:5] = Memory Bank select bit

⊙ ALL Case → MIR[4:0] 00 0FH ≡ 00 0FH

(Addresses mapping back to the addresses in Bank 0)

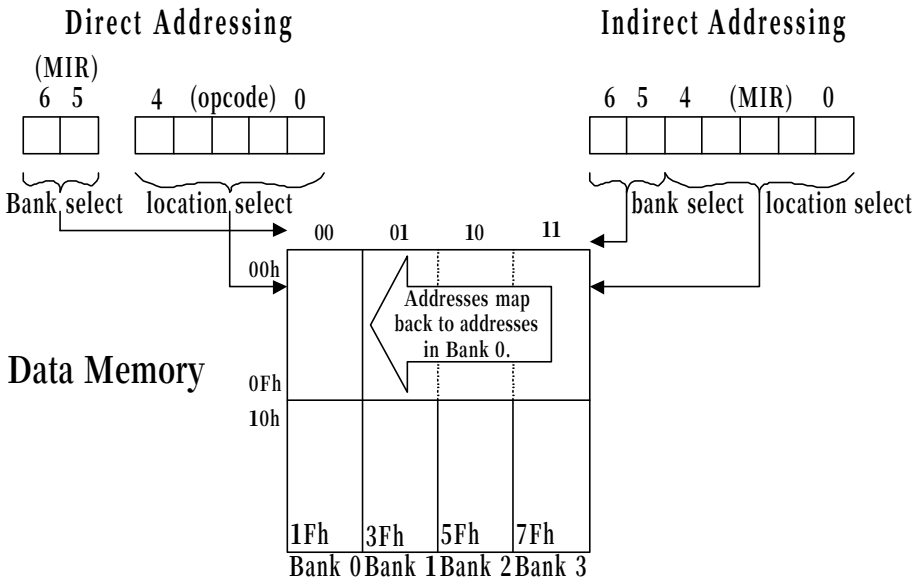
⊙ MIR [6:5] == 0 && MIR [4:0]= 10 1FH => Physical RAM

⊙ MIR [6:5] == 1 && MIR [4:0]= 10 1FH => Physical RAM

⊙ MIR [6:5] == 2 && MIR [4:0]= 10 1FH => Physical RAM

⊙ MIR [6:5] == 3 && MIR [4:0]= 10 1FH => Physical RAM

that is,



6) 05H [7:0] **< RPA > Port A data Register {RW}**

Description:

This register is an 8-bit I/O register.

7) 06H [5:0] **< RPB > Port B data Register {RW}**

Description:

Bits 5-0 are I/O register, while bits 7-6 are always read as '0'.

8) 07H [7:0] **< RPC > Port C data register {RW}**

Description:

This register is an 8-bit I/O register.

6.2 Implicit Registers

9) 00H [7:0] **< WTC > Watchdog Timer Control register {RW}**

[2:0] = < PSC2:PSC1:PSC0 > TCR | WDT PreSCaler rate bits

PSC2	*PSC1*	*PSC0*	*TCR rate*	*WDT rate*
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

[3] = < PSCA > PreSCaler Assigned bit

"0" is assigned to TCR;

"1" is assigned to WDT (default).

If one bit of the prescaler is assigned to WDT, it will be reset after the execution of CLRWT instruction.

[4] = < EGTY > CNTI input edge select

"0" for an increment of counter at a rising edge on CNTI pin

"1" for an increment of counter at a falling edge on CNTI pin (default)

[5] = < TCLK > Timer/Counter CLocK source

"0" for internal clock (instruction cycle clock, i.e. System clock /4)

"1" for transition on CNTI pin (default)

[6]= < WDTI > WatchDog Timer timeout interrupt control in the case of the enabled WDT in code option configuration

"0" indicates that reset MPU without interrupt in the case of WatchDog Timer timeout (default);

"1" indicates that enable WatchDog Timer timeout Interrupt.

[7] = < CNTI > State on CNTI pin {Ro}

10) 01H [7:0] **< TCC > Timer/Counter Control register {RW}**

Description:

[2:0] = < TPS2: TPS1: TPS0 > TCR PreScaler rate bits

TPS2	*TPS1*	*TPS0*	*TCR rate*
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

[3] = < TPSC > Control Timer/Counter prescaler of TCC register

"0" for disable (default)

"1" for enable

[4]= < PSCC > Clear prescaler of Timer/Counter automatically when TCR or prescaler rate is changed.

"0" for disable

"1" for enable (default)

[5] = < PSCS > Timer/Counter prescaler selection

"0" for TCR rate Controlled by WTC register [3] (default)

"1" for Timer/Counter using its own prescaler defined by TCC register [4:0].

[6] = < TCEN > Timer/Counter ENable control

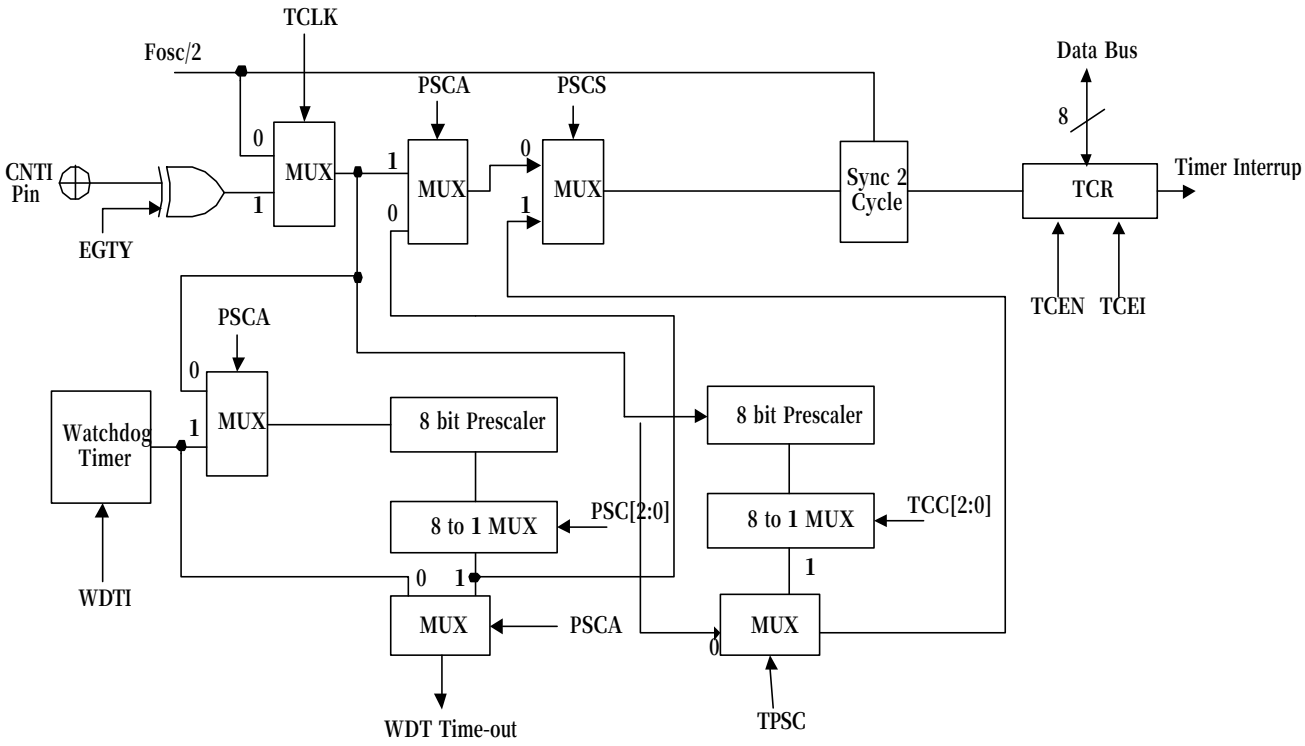
"0" indicates that the Timer/Counter is disabled.

"1" indicates that the Timer/Counter (default) is enabled.

[7] = < TCEI > Timer/Counter Interrupt control

"0" indicates that the Timer/Counter interrupt (default) is disabled.

"1" indicates that the Timer/Counter interrupt is enabled.



TCR Prescale control

10) 02H [7:0] **< IPA > Port A Interrupt control register {RW}**

Description:

A '1' in this register will allow a low pulse applied to the corresponding pin of port A to generate an interrupt and wake up the MPU, wherein the interrupt and wake-up functions are valid only while the pin is defined as an input pin.

12) 03H [7:6] **< OPT > OPTion control register {RW}**

Description:

[6] = < IOWM > I/O port Write Mode for read-then-write instructions.

"0" for reading the latches → operation → write (default)

"1" for reading the interface → operation → write

[7] = < RAMB > RAM Bank enable bit.

"0" for disabling RAM bank function

"1" for enabling RAM bank function (default)

13) 04H [7:0] **< CMP > CoMParator control register {RW}**

Description:

If Port A [3:0] is set for comparator, then the CPA [3:0] must be set for an input function.

[0] = < CMP0 > Define RPA bit 0 input function

"0" for digital input

"1" for comparator input

[1] = < CMP1 > Define RPA bit 1 input function

"0" for digital input

"1" for comparator input

[2] = < CMP2 > Define RPA bit 2 input function

"0" for digital input

"1" for comparator input

[3] = < CMP3 > Define RPA bit 3 input function

"0" for digital input

"1" for comparator input

[4] = < VRF0 > CMP0 reference voltage select

"0" for 1 / 2 VDD internal Vref

"1" for external Vref input (PB [0])

[5] = < VRF1 > CMP1 reference voltage select

"0" for 1 / 2 VDD internal Vref

"1" for external Vref input (PB [1]), if Multiple Vref input mode is selected

for external Vref input (PB[0]) , if Single Vref input mode is selected

[6] = < VRF2 > CMP2 reference voltage select

"0" for 1 / 2 VDD internal Vref

"1" for external Vref input (PB [2]), if Multiple Vref input mode is selected

for external Vref input (PB[0]), if Single Vref input mode is selected

[7] = < VRF3 > CMP3 reference voltage select

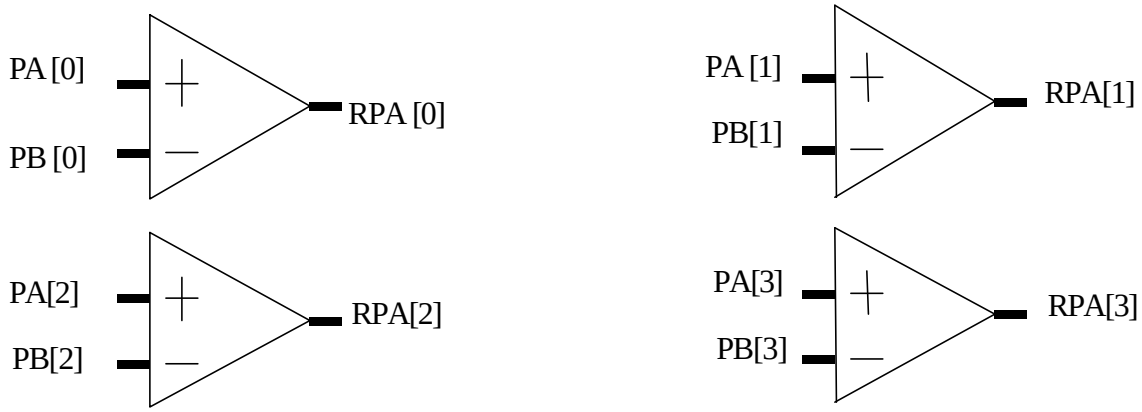
"0" for 1 / 2 VDD internal Vref

"1" for external Vref input (PB [3]), if Multiple Vref input mode is selected

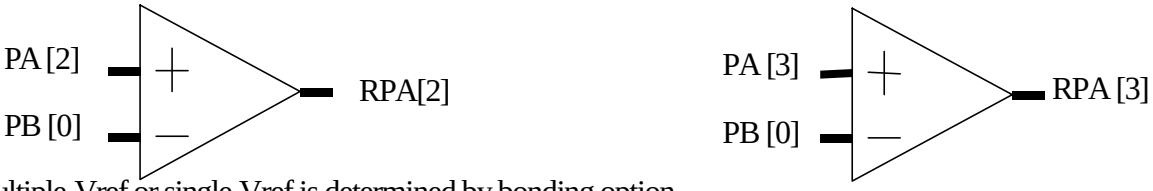
for external Vref input (PB[0]), if Single Vref input mode is selected

If CMP0 (、CMP1、CMP2、CMP3) is set for Comparator and if VRF0 (、VRF1、VRF2、VRF3) selects External Vref, then PB bit0 (、bit1、bit2、bit3) is assigned as Vref input. Please see the illustration shown below:

Multiple Vref.:



Single Vref.:



* Multiple Vref or single Vref is determined by bonding option.

14) 05H [7:0] **< CPA > Port A Control register {RW}**

Description:

A '0' in this register will set the corresponding pin of port A to an output. In the conditions of power-on and reset, all default "1" is input. If the program enables the comparator function, you must set the corresponding Port A pins to an input.

15) 06H [5:0] **< CPB > Port B Control register {RW}**

Description:

A '0' in this register will set the corresponding pin of port B to an output. In the conditions of power-on and reset, all [5:0] default "1" is input. Bits 7-6 are not implemented and always read as '0'. If the program enables the comparator function, you must set the corresponding PB pins to an input.

16) 07H [7:0] **< CPC > Port C Control register {RW}**

Description:

A '0' in this register will set the corresponding pin of port C to an output. All default '1' is input.

7. Absolute maximum ratings:

Operating temperature	-40 to 70℃
Storage temperature	-65 to 150℃
Supply voltage	7 V
Input voltage	-0.6 to Vdd+0.6 V
Total power dissipation	500 mW
Max. current out of VSS pin	100 mA
Max. current into VDD pin	100 mA
Max. output current sourced by a single port	50 mA
Max. output current sunk by a single port	50 mA

8. Electrical characteristics (operating temperature at 25℃):

Sym	Description	Conditions	Min.	Typ.	Max.	Unit
Vdd	Operating voltage	Without using comparator Using comparator	2.3 3.0		5.5 5.5	V V
Vref	Reference voltage		Vss+0.5		Vdd-1	V
Vin	Input voltage range for comparator inputs		0.2		Vdd-0.8	V
Vofs	Offset voltage between comparator inputs				20	mV
ViH	High level input voltage PA , PB CNTI , /ERST	Vdd = 3 V	 1.6 2.0		 Vdd Vdd	 V V
	High level input voltage PA , PB CNTI , /ERST	Vdd = 5 V	 2.2 3.5		 Vdd Vdd	 V V
ViL	Low level input voltage PA , PB CNTI , /ERST	Vdd = 3 V	 Vss Vss		 0.8 0.8	 V V
	Low level input voltage PA , PB CNTI , /ERST	Vdd = 5 V	 Vss Vss		 1.2 1.2	 V V
VoH	High level output voltage	Vdd=3V, IoH = -3 mA Vdd=5V, IoH= -4.5mA		2.4 4.2		V V
VoL	Low level output voltage	Vdd=3V, IoL= 3 mA Vdd=5V, IoL=4.5mA		0.2 0.3		V V
IiL	Input low leakage current PA,PB, CNTI /ERST	Vdd=3V			 -1 -6.5	 µA µA
	Input low leakage current PA,PB, CNTI /ERST	Vdd=5V			 -1 -18	 µA µA
IiH	Input high leakage current PA,PB, CNTI /ERST	Vdd=3V			 +1 +1	 µA µA
	Input low leakage current PA,PB, CNTI /ERST	Vdd=5V			 +1 +1	 µA µA
Tcy	Instruction cycle time	Vdd>=2.3V		200		nS

Sym	Description	Conditions	Min.	Typ.	Max.	Unit
Tost	Basic time-out period for watchdog timer	Vdd=3.0V Vdd=5.0V		25 22		mS mS
Idds	Sleep current (WDT disable)	Vdd=3.0 V All input pins level =Vdd or Vss No loading current for all output ports	0.2	1	10	µA
Idds	Sleep current (WDT enable)	Vdd=3.0 V All input pins level =Vdd or Vss No loading current for all output ports	10	15	25	µA
Idd	Operating Current	Vdd=3.0V, XT mode, 4MHz Vdd=5.0V, XT mode, 4MHz No loading current for all output ports The current will vary if a load is changed.		0.8 1.5		mA mA

9. Instruction Set

Binary Code	Syntax	Description	Operation	Status Affected
000 000 00000000	NOP	No Operation	None	None
000 000 00000010	SLEEP	Sleep mode	Stop OSC	SP=0
000 000 00000011	CLRWT	Clear watchdog timer	0→WT	SP=1
000 000 00000100	RETI	Return from interrupt	Stack→PC	IF=1
000 000 00000101	RET	Return from subroutine	Stack→PC	None
000 000 00000110	CLRIF	Clear interrupt flag	None	IF=1
000 000 00000111	STDBY	Stand-by mode	Stop Clock	SP=0
000 000 00001000	CLRA	Clear Acc.	0 → A	Z
000 000 00001001 | 000 000 01111111	None	None	None	None
000 000 1 rrrrrrr	STAR r	Store Acc. in Reg..	A → r	None
000 001 0xxxdrrr	CTRLR r, d	Store Acc in Reg. or store Reg. in Acc..	r = WTC(00h), TCC(01h) IPA(02h) OPT(03h) CMP(04h) CPA(05h) CPB(06h) CPC(07h) d = 0 r → A d = 1 A → r	CTRLR r,d
000 001 1 rrrrrrr	CLRR r	Clear Reg.	0 → r	Z
000 010 d rrrrrrr	IORAR r, d	Incl. OR Acc. and Reg.	r ˇ A → d	Z
000 011 d rrrrrrr	XORAR r, d	Excl. OR Acc. and Reg.	r⊕A → d	Z
000 100 d rrrrrrr	ANDAR r, d	AND Acc. and Reg.	r & A → d	Z
000 101 d rrrrrrr	ADDAR r, d	Add Acc. and Reg.	A + r → d	C,AC,Z
000 110 d rrrrrrr	SUBAR r, d	Subtract Acc. from Reg.	r – A → d	C,AC,Z
000 111 d rrrrrrr	LDR r, d	Load Reg. into destination	r → d	Z
001 0bb b rrrrrrr	BCR r, b	Clear bit of Reg.	0 → r[b]	
001 1bb b rrrrrrr	BTRSC r, b	Test bit of Reg., skip if cleared	Skip if r[b]=0	

010 000 d rrrrrr	COMR r, d	Complement Reg.	/R → d	Z
010 001 d rrrrrr	DECR r, d	Decrement Reg.	r-1 → d	Z
010 010 d rrrrrr	DRSZ r, d	Decrement Reg., skip if zero	r-1 → d	None
010 011 d rrrrrr	INCR r, d	Increment Reg.	r+1→ d	Z
010 100 d rrrrrr	IRSZ r, d	Increment Reg., skip if zero	r+1 → d	None
010 101 d rrrrrr	SWAPR r, d	Swap halves Reg.	r[0:3] <—> r[4:7] → d	None
010 110 d rrrrrr	RLR r, d	Rotate Reg. left	r[b] → r[b+1] C → r[0] r[7] → C	C
010 111 d rrrrrr	RRR r, d	Rotate reg. right	r[b] → r[b-1] C → r[7] r[0] → C	C
011 0bb b rrrrrr	BSR r, b	Set bit of Reg.	1 → r[b]	None
011 1bb b rrrrrr	BTRSS r, b	Test bit of Reg., skip if set	Skip if r[b]=1	None
100 i i i i i i i i i i i	JUMP i	Jump to address	i → PC	None
101 i i i i i i i i i i i	CALL i	Call subroutine	i → PC PC+1→ stack	None
110 000 d rrrrrr	ADCAR r, d	Add Acc, Reg., and carry	A+r+C → d	C,AC,Z
110 001 d rrrrrr	SBCAR r, d	Subtract Acc from Reg. with borrow	r-A-/C → A	C,AC,Z
110 010 d rrrrrr	SRR r, d	Shift Reg. right	r[b] → r[b-1] r[0] → C 0 → r[7]	C
110 011 d rrrrrr	SLR r, d	Shift Reg. left	r[b] → r[b+1] r[7] → C 0 → r[0]	C
110 100 d rrrrrr	DAR r, d	Decimal Adjustment	if r[3:0]>9 or AC=1, then r[7:0]+6→d[7:0] if r[7:4]>9 or C=1, then r[7:4]+6→ d[7:4]	C,AC
110 101 0 rrrrrr	XCHAR r	Exchange Reg. and	r <—> A	None

		Acc		
110 101 1 rrrrrrr	CMPAR r	Compare Acc with Reg.	r-A	C,Z
110 110 bbbrrrrr	BCTR r, b	Carry flag written into Bit [b] of Reg. Reg. address range 00H~1FH	C → r[b]	None
110 111 bbbrrrrr	BRTC r, b	Bit[b] of Reg. written into carry flag Reg. address range 00H~1FH	r[b] → C	C
111 000 i i i i i i i i	LDIA i	Load immediate into Acc.	i → A	None
111 001 i i i i i i i i	CMPIA i	Compare immediate with Acc	i - A	C,Z
111 010 i i i i i i i i	IORIA i	Incl. OR Acc and immediate	i ˅ A→ A	Z
111 011 i i i i i i i i	XORIA i	Excl. OR Acc and immediate	i⊕A → A	Z
111 100 i i i i i i i i	RTIA i	Return and place immediate into Acc	Stack → PC i → Acc	None
111 101 i i i i i i i i	ADCIA i	Add Acc and immediate and carry	A+i+C → A	C,AC,Z
111 110 i i i i i i i i	SBCIA i	Subtract Acc from immediate with borrow	i-A-/C → A	C,AC,Z
111 111 i i i i i i i i	ANDIA i	AND Acc and immediate	i & A→ A	Z

Notes to syntax:

ACC : Accumulator
A : Accumulator
Reg. : General register
WT: watchdog timer
X : Don't care
SP: Sleep flag
Incl.: Inclusive
Excl.: Exclusive
Z: Zero flag

r: General register address
d: Destination
d = 1: General register
d = 0 : Accumulator
b: Bit position
i: Immediate data
C: Carry flag
AC: Auxiliary
IF: Interrupt flag

/: Complement

10. Special Register Condition

Registers	*Power-on Reset*	*External or Watchdog reset*	*Watchdog interrupt*	*Timer/Counter or Port Interrupt*
01H (**TCR**)	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu
02H (**PCL**)	1111 1111	1111 1111	1111 1110	by starting address
03H (**SFR**)	0001 1xxx	000? ?uuu	uuu0 ?uuu	uuuu ?uuu
04H (**MIR**)	1xxx xxxx	1uuu uuuu	1uuu uuuu	1uuu uuuu
05H (**RPA**)	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu
06H (**RPB**)	- - xx xxxx	- - uu uuuu	- - uu uuuu	- - uu uuuu
07H (RPC)	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu
00H (**WTC**)	*011 1111	*u11 1111	*uuu uuuu	*uuu uuuu
01H (**TCC**)	0101 0111	0101 0111	uuuu uuuu	uuuu uuuu
02H (**IPA**)	0000 0000	0000 0000	uuuu uuuu	uuuu uuuu
03H (**OPT**)	10 - - - - - -	10 - - - - - -	uu - - - - - -	uu - - - - - -
04H (**CMP**)	0000 0000	0000 0000	uuuu uuuu	uuuu uuuu
05H (**CPA**)	1111 1111	1111 1111	uuuu uuuu	uuuu uuuu
06H (**CPB**)	- - 11 1111	- - 11 1111	- -uu uuuu	- -uu uuuu
07H (**CPC**)	1111 1111	1111 1111	uuuu uuuu	uuuu uuuu

Note:

x : unknown

u: unchanged

- : unimplemented, read as ' 0'

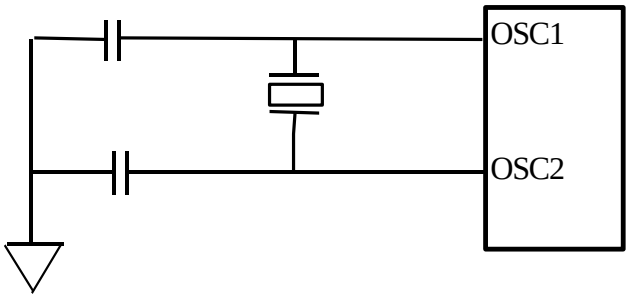
* : state of CNTI pin

? : states of /WT and /SP, illustrated in the form of a table below

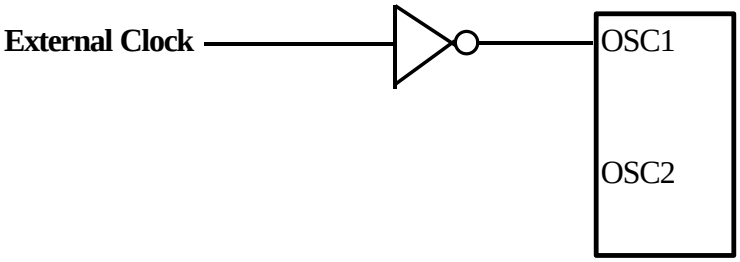
/WT	*/SP*	*DESCRIPTION*
0	0	Watchdog timer timeout reset or interrupt during SLEEP, STDBY
0	1	Watchdog timer timeout reset or interrupt not during SLEEP, STDBY
1	0	External reset, Port A, Timer/Counter interrupt during SLEEP, STDBY
1	1	Power-on reset
u	u	External reset, Port A, Timer/Counter interrupt not during SLEEP, STDBY

11. Oscillator Configurations

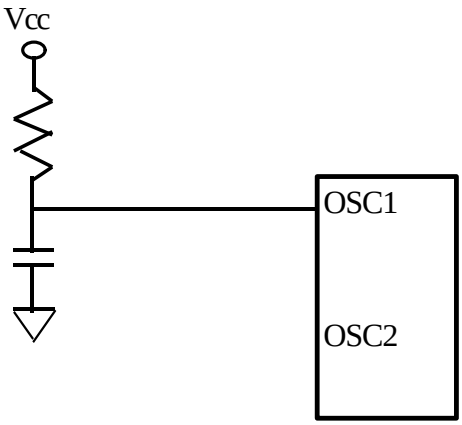
11.1 Crystal operation for LFXT, XTAL and HFXT types.



11.2 External clock input for LFXT, XTAL and HFXT



11.3 RC oscillator for RC only



Annex 1

Interrupt function:

Timer/counter interrupt: Timer/counter reaching 255 will generate an interrupt and go directly to address 7FD/h and can jump to the Timer Interrupt Service Routine (e.g. by JUMP instruction . .).

If the interrupt happened during the ISR (Interrupt Service Routine) of other interrupt (Port A interrupt or watchdog timer timeout interrupt), this interrupt will be held and then execute its own ISR after the end of the previous ISR generated by other source.

Port A interrupt: A low pulse (at least one instruction cycle long) applied to the corresponding pin (which is in an input mode) will generate an interrupt and go directly to address 7FC/h and can jump to the Port A Interrupt Service Routine. If the interrupt happened during the ISR of other interrupt (timer/counter interrupt or watchdog timer timeout interrupt), this interrupt will be held and then execute its own ISR after the end of the previous ISR generated by other source.

Watchdog timer timeout interrupt: Watchdog timer timeout will generate an interrupt and go directly to address 7FE/h (in the case of <WTC> Watchdog timer Control register bit 6="1") and can jump to the WDT Interrupt Service Routine. This interrupt has the highest priority and can execute its ISR immediately, whether or not having happened during another ISR (generated by timer/counter or Port A). If both timer/counter interrupt and port A interrupt happened during the execution period of watchdog timer timeout ISR, timer/counter ISR will be executed first after the return of watchdog timer timeout ISR.

The interrupt structure is two-level deep. But only watchdog timer timeout could be the most recently generated interrupt.

In interrupt service routine, the programmer has to save the accumulator and status registers first and restore the accumulator and status registers before exit. The following instructions are recommended.

In the beginning of ISR:

```
STAR    SAVE_A
LDR     03H,A
```

```
        STAR        SAVE_S
```

Before exit from ISR:

```
        LDR         SAVE_S,A
        STAR        03H,R
        XCHAR       SAVE_A
        RETI
```

Watchdog timer:

The basic timeout period of watchdog timer is Twdt (about 22 ms). By setting the post-scaler rate, 2.8 seconds of timeout period can be present. The CLRWT, SLEEP, or STDBY instruction will reset the watchdog timer and the post-scaler.

To clear interrupt flag:

Normally, the interrupt routine must be returned by RETI. If returning to the original address is not wanted, then CLRIF must be executed once. Otherwise, a next interrupt will not be allowed. The CLRIF instruction only clear the implicit interrupt enable flag and all the other register will not be affected.

Instruction cycle:

One instruction cycle consists of four oscillator periods. All instructions are executed within one instruction cycle except that a condition test is true or the program counter is changed into a result of an instruction. In this case, the instruction takes two instruction cycles.

Start-up Vector:

After a power-on or reset condition is applied, the program counter will first go to start-up vector " 7FF/h" to execute the instruction at said address.

Configuration byte (EPROM options):

Bit 1-0 for Watchdog timer control

=x0 for watchdog timer disabled all the time

=01 for watchdog timer disabled during sleep or stand-by mode

=11 for watchdog timer enabled all the time

3-2 for oscillator type

=00 for RC oscillator

=01 for LFXT oscillator
=10 for XTAL oscillator
=11 for HFXT oscillator

5-4 for Oscillator start-up time select
=00 for Twdt/128 (about 172μs)
=01 for Twdt x 1 (about 22ms)
=10 for Twdt x 2 (about 44ms)
=11 for Twdt x 4 (about 88ms)

This start-up time is generated by an internal RC oscillator and will vary from chip to chip. The operating voltage and temperature also will affect it. The above values are measured at Vdd=5V.

Setting for boosting wake-up speed from sleep:

For some low-power or special applications the shortest wake-up time is necessary, so we arrange some combinative settings for bypassing OST(oscillator start-up time) to shorten the time from Watch-dog wake-up during Sleep to program starting as soon as possible.

The combinative settings are listed below:

1. OST=22ms and WDT rate (defined in WTC)= 1:1
2. OST=44ms and WDT rate (defined in WTC)= 1:2
3. OST=88ms and WDT rate (defined in WTC)= 1:4

* These settings just change the wake-up time by watch-dog interrupt (Not including watch-dog reset) during sleep. They don't affect the start-up time right after power-on and wake-up time caused by other interrupts.

Bonding Option:

In consideration of the different purposes, the EPROM programming manners may be divided into a parallel programming mode and a serial programming mode. We can determine one of the two options just by different bonding diagrams:

- Parallel programming v.s. serial programming
  1. Parallel programming:

     The pins listed below are necessary: (the pins in the bracket are needed extra for writer programming)

Vss, OSC1, CNTI, PA0, PA1, PA2, PA3, PA5, PA6, PA7, Vdd, PB0, PB2, PB3, and (OSC2, /ERST)

2. Serial programming:

The pins listed below are necessary: (the pin in the bracket is needed extra for writer programming)

Vss, CNTI, PA0, PA1, Vdd, and (OSC2)

- Single Vref v.s. Multiple Vref

Annex 2

Package type available

Part number	package type	pin count	package size
CR80P200AN28P	PDIP	28 pins	600 mil
CR80P200AN28S	SOP	28 pins	300 mil
CR80P200AN28SP	Skinny PDIP	28 pins	300 mil
CR80P200AN28SS	SSOP	28 pins	209 mil
CR80P200BN28P	PDIP	28 pins	600 mil
CR80P200BN28S	SOP	28 pins	300 mil
CR80P200BN28SP	Skinny PDIP	28 pins	300 mil
CR80P200BN28SS	SSOP	28 pins	209 mil
CR80P200DN28P	PDIP	28 pins	600 mil
CR80P200DN28S	SOP	28 pins	300 mil
CR80P200DN28SP	Skinny PDIP	28 pins	300 mil
CR80P200DN28SS	SSOP	28 pins	209 mil
CR80P200EN28P	PDIP	28 pins	600 mil
CR80P200EN28S	SOP	28 pins	300 mil
CR80P200EN28SP	Skinny PDIP	28 pins	300 mil
CR80P200EN28SS	SSOP	28 pins	209 mil