

2 x 15 W CS4412 Digital Power Stage Reference Design

Features

- ◆ Pre-Configured for Stereo Full-Bridge Operation
 - Delivers 15 W/Ch into 8 Ω at 10 % THD+N
- ◆ Easily Configurable for Mono Parallel Full-Bridge Operation
 - Delivers 30 W into 4 Ω at 10 % THD+N
- ◆ Directly Connects to CRD4525 Digital Amplifier Reference Design
 - Implements a 2.1 Configuration
- ◆ Flexible I/O Provided
 - PWM Logic Level Signal Inputs
 - CS4412 Error and Warning Signals
- ◆ Operates from +9 V to +18 V and +3.3 V
- ◆ Demonstrates Recommended Layout and Grounding Arrangements
- ◆ Implements Recommended PWM Output Filtering

Description

The CRD4412 demonstrates the CS4412 digital amplifier power stage. This reference design is pre-configured as a two-channel full-bridge power stage which delivers 15 W per channel into 8 Ω loads using a single +18 V supply. The design can be easily configured to operate as a single channel parallel full-bridge power stage capable of delivering 30 W into a 4 Ω load from an +18 V supply. The CRD4412 can be powered from +9 V to +18 V

The CRD4412 is designed to operate in conjunction with the CRD4525. When connected, the combination implements a 2.1 configuration with the CRD4412 operating in mono parallel full-bridge mode.

The CRD4412 can also be operated without an attached CRD4525. In this configuration, all input/output connections are achieved through the CRD4412 interface header.

The PWM audio power outputs are routed through an inductor/capacitor 2nd order low-pass filter (LPF) to remove high frequency components from the output signal, effectively converting it from digital to analog.

ORDERING INFORMATION

CRD4412

CS4412 Reference Design

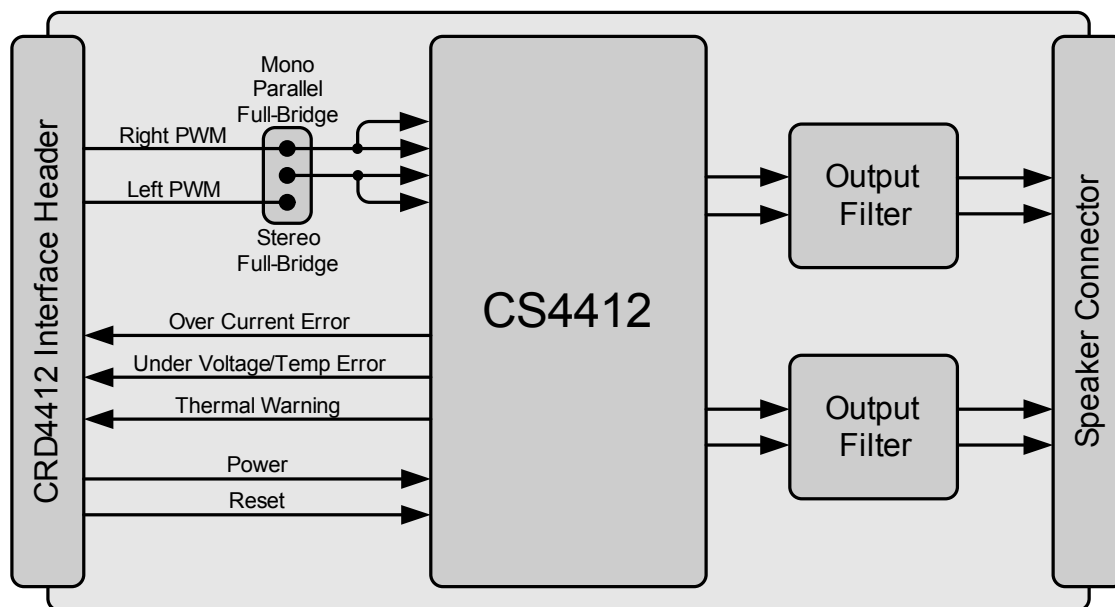


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1. SYSTEM OVERVIEW

The CRD4412 reference design is an excellent means for evaluating the CS4412 30 W digital amplifier power stage. The board is designed to connect directly to the CRD4525 digital amplifier reference design for easy evaluation. Alternatively, the CRD4412 may be used alone with all logic-level and power connections made through the CRD4412 interface header.

The CRD4412 schematic set is shown in [Figure 3](#) through [Figure 4](#). See the CRD4525 datasheet for more information about the features and connections of the CRD4525.

1.1 Power

Power (VD, VP) must be supplied to the evaluation board through the CS4412 interface header (J2). All voltage inputs must be referenced to ground, also provided through the CS4412 interface header.

See the [CRD4412 Interface Header Signal Assignments](#) table on [page 7](#) for signal to pin assignments.

WARNING: Please refer to the CS4412 data sheet for allowable voltage levels.

1.2 CS4412 Digital TV Amplifier

The CS4412 is a 30 W quad half-bridge digital amplifier power stage. A complete description of the CS4412 is included in the CS4412 product data sheet.

1.3 External Data Headers

The evaluation board has been designed to allow interfacing with external systems via the headers J2, J4, and J6. [Figure 3](#) shows the headers' electrical connections.

The 20-pin, 2 column header, J2, is included to interface with the CRD4525 digital amplifier reference design, and to interface with external sources when a CRD4525 is not connected. All necessary signals, power, and ground are presented on this header. See [Figure 3](#) for complete connectivity information.

The 4-pin, 2 column header, J4, provides access to the CS4412's thermal warning signal and the CS4525's DLY_SDIN/EX_TWR signal. When a CRD4525 is attached, a shunt can be placed across these signals to deliver the CS4412's thermal warning signal to the CS4525's external thermal warning input. Alternatively, this header can be used to connect the CS4412's thermal warning output to another device, and to drive an external serial audio data source into the CS4525. A single ground column is provided to maintain signal integrity in this configuration.

The 4-pin, 2 column header, J6, provides access to the CS4412's over-current error signals and the CS4525's DLY_SDOOUT signal. When a CRD4525 is attached, this header can be used to connect the CS4412's over-current error signals to another device, and to connect the CS4525's delay serial audio data output to an external device. A single ground column is provided to maintain signal integrity in this configuration.

1.4 Stereo/Mono Selection

A 3-pin header (J1) is included to select between stereo and mono operation. The position of the shunt placed across this header determines whether discrete PWM signals are routed to the full-bridge input pairs, or whether a single PWM signal is routed to both full-bridge input pairs.

It should be noted that when mono mode is selected, the outputs may be wired in parallel to achieve parallel full-bridge operation. See [Section 1.5](#) for more information.

1.5 Speaker Outputs

By default, the CS4412 power outputs are configured for stereo full-bridge operation. The outputs are routed through a 2nd order low-pass filter to remove high-frequency content from the output signals and then presented at the speaker wire crimp terminals (J5). The output filters are optimized for 8 Ω speaker loads. The speaker terminal connections are shown below.

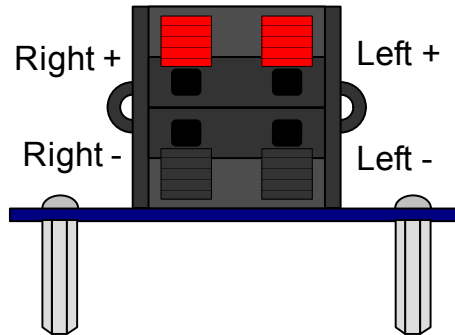


Figure 1. Stereo Full-Bridge Speaker Terminal Configuration

When the CS4412 is configured for mono operation via J1, the outputs must be connected in parallel as shown below. One wire is used to connect between the red terminals, and another is used to connect between the black terminals. This parallel connection adjusts the characteristic of the output filters, effectively optimizing them for 4 Ω speaker loads.

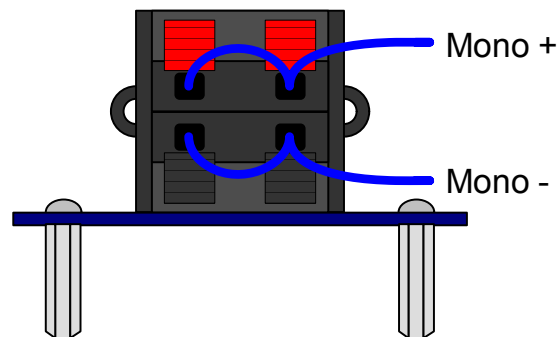


Figure 2. Mono Parallel Full-Bridge Speaker Terminal Configuration

2. OPERATING INSTRUCTIONS

The CRD4412 is designed to connect directly to the CRD4525 digital power amplifier reference design, and to interface with external signal sources. See the following sections for operation details with and without a CRD4525.

Note that the CRD4412 and CRD4525 must be connected and disconnected from one another while power is not applied to the CRD4525.

2.1 Operation With CRD4525

When the CRD4412 is attached to a CRD4525 via the CRD4412 interface header and the CRD4525 FlexGUI is launched, the CS4525 is automatically configured to enable its bass manager and route the subwoofer channel to the CRD4412. The CRD4412 amplifies the subwoofer signal in mono parallel full-bridge mode. Together, the CRD4412 and CRD4525 implement a 2.1 configuration.

To operate the CRD4412 and CRD4525 in this configuration:

1. Download and install the FlexGUI software from www.cirrus.com/msasoftware.
2. Connect the CRD4412 to the CRD4525 via the CRD4412 interface header.
3. Connect the CRD4525 to a host PC using the supplied USB cable.
4. Connect the 8 Ω stereo speakers to the speaker terminals on the CRD4525.
5. Wire the two red-terminal speaker outputs together on the CRD4412 as shown in [Figure 2](#).
6. Wire the two black-terminal speaker output together on the CRD4412 as shown in [Figure 2](#).
7. Connect the 4 Ω mono subwoofer between the red and black speaker terminals on the CRD4412.
8. Place a shunt across pins 2 and 3 of J1 to select mono mode.
9. Place a shunt across pins 1 and 2 of J4 to route the CS4412 thermal warning signal to the CS4525 external thermal warning input.
10. Connect an input source to the S/PDIF or analog input connectors.
11. Plug the input to the +18 V power supply (included with the CRD4525) into an available power outlet.
12. Plug the output of the +18 V power supply into the power input connector on the CRD4525.
13. Launch the FlexGUI software and select the CRD4525 + CRD4412 combination from the board selection list if necessary. *The GUI will load and be displayed.*
14. Un-check the "Power Down CS4525" check box to power-up the CS4525. *In this state, the CRD4525 and CRD4412 will convert and amplify the content present on the optical S/PDIF input.*

2.2 Stand-Alone Operation

The CRD4412 may be operated alone, without a connected CRD4525. In this mode of operation, all signals and power are supplied to the CRD4412 through the CRD4412 interface header.

To operate the CRD4412 in this configuration:

1. Connect ground to pins 7, 9, 11, 13, 15, and 16 of J2.
2. Connect a +3.3 V source to pin 2 of J2, but do not apply power.
3. Connect a +9 V to +18 V source to pins 17, 18, 19, and 20 of J2 but do not apply power.
4. Connect a reset input signal to pin 14 of J2.
5. Connect logic-level PWM input signals to pins 8 and 10 of J2. For mono mode, it is only necessary to connect a PWM input signal to pin 10 of J2.
6. Place a shunt across 2 pins of J1 to select stereo or mono mode as desired.
7. Connect the outputs and speaker load as discussed in [Section 1.5 on page 4](#).
8. Apply +3.3 V and +9 V to +18 V power.
9. Drive the reset input low and then high to reset the CS4412.

10. Begin PWM switching on the logic level PWM input signals. *In this state, the CRD4412 will amplify the content present on the logic level PWM input signals.*

3. GROUNDING AND POWER SUPPLY DECOUPLING

The CS4412 requires careful attention to power supply and grounding arrangements to optimize performance and heat dissipation and minimize radiated emissions. [Figure 5 on page 10](#) shows the component placement. [Figure 6 on page 11](#) shows the top layout. [Figure 9 on page 14](#) shows the bottom layout. The decoupling capacitors are located as close to the CS4412 as possible. Extensive use of ground plane fill in the evaluation board yields large reductions in radiated noise.

3.1 Power Supply Decoupling

Proper power supply decoupling is one key to maximizing the performance of a Class-D amplifier. Because the design uses an open loop output stage, noise on the power supply rail will be coupled to the output. Careful decoupling of the power stage supply rails is essential. [Figure 5 on page 10](#) demonstrates good decoupling capacitor placement. Notice that the small value decoupling capacitors are placed as close as physically possible to the power pins of the CS4412. The ground side of the capacitors is connected directly to top side ground plane, which is also used by the power supply return pins. This keeps the high frequency current loop small to minimize power supply variations and EMI. 470 μ F electrolytic capacitors are also located in close proximity to the power supply pins to supply the current locally for each channel. These are not required to be expensive low ESR capacitors. General purpose electrolytic capacitors that are specified to handle the ripple current can be used.

3.2 Electromagnetic Interference (EMI)

The EMI challenges that face a maker of Class-D amplifiers are largely the same challenges that have been faced by the switch mode power supply industry for many years. The numerous EMI consulting firms that have arisen and the many books that have been written on the subject indicate the scope of potential problems and available solutions. They should be considered a resource - most makers of switch mode equipment would benefit from developing a working relationship with a qualified EMI lab and from bringing their experience to bear on design issues, preferably early in the design process.

This reference design is a board level solution which is meant to control emissions by minimizing and suppressing them at the source in contrast to containing them in an enclosure.

The EMI requirements for an amplifier have added dimensions beyond those imposed on power supplies. Audio amplifiers are usually located in close proximity to radio receivers, particularly AM receivers which are notoriously sensitive to interference. Amplifiers also need to operate with speaker leads of unpredictable length and construction which make it possible for any high frequency currents that appear on the outputs to generate nuisance emissions. The criteria for judging successful EMI control is not as well defined for amplifier design as it is for power supplies. While the techniques of measuring conducted and radiated emissions are similar for both types of products, power supplies have a number of clearly defined (and legally imposed) thresholds that are useful mainly as guidelines when testing amplifiers.

3.2.1 Suppression of EMI at the Source

Several techniques are used in the circuit design and board layout to minimize high frequency fields in the immediate vicinity of the high power components. Specific techniques include the following:

- As mentioned in [Section 3.1](#), effective power supply decoupling of high frequency currents, and minimizing the loop area of the decoupling loop is one aspect of minimizing EMI.
- Each output of the CS4412 includes “snubbing” components. For example, OUT1 and OUT2 include snubber components R24 (20 Ω) and C23 (330 pF). These components serve to damp ringing on the

switching outputs in the 30-50 MHz range. The snubbing components should be as close as practical to the output pins to maximize their effectiveness.

- A separate ground plane with a solid electrical connection to the chassis and which surrounds the speaker output connector should be implemented. This allows the speaker outputs to be RF decoupled to the chassis just before they exit the chassis from the speaker connector.
- Make use of source termination resistors on all digital signals whose traces are longer than about 25 mm.

It is extremely critical that the layout of the power amplifier section of the CRD4412 be copied as exactly as possible to assure best RF/EMI performance.

4. SYSTEM CONNECTIONS AND JUMPERS

Connector Name	Reference Designator	Signal Direction	Connector Function
Speaker Connector	J5	Output	Analog output from CS4525.

Table 1. System Connections

Connector Name	Reference Designator	Header Function
CRD4412 I/F	J2	Connection to CRD4525 controller card.
-	J1	Selects between mono and stereo PWM input mode.
-	J4	Connects CS4412 thermal warning output to CRD4412 interface header. Allows direct access to CS4412 TWR and CS4525 DLY_SDIN signals when CRD4525 is connected.
-	J6	Allows direct access to CS4412 ERROC12/34 and CS4525 DLY_SDOUT signals when CRD4525 is connected.

Table 2. System Headers

Pin	Signal Name	Signal Function
1	SDA	I ² C serial data.
2	+3.3 V	Positive VD power.
3	SCL	I ² C serial clock.
4	DLY_SDIN/TWR	CS4525 delay port serial audio data input/CS4412 thermal warning output.
5	ERROC1234	CS4412 over-current error outputs.
6	DLY_SDOUT	CS4525 delay port serial audio data output.
7, 9, 11, 13, 15, 16	GND	Ground reference.
8	PWM_SIG1	Left channel logic level PWM input.
10	PWM_SIG2	Right channel/mono logic level PWM input.
12	ERRUVTE	CS4412 under-voltage/temperature error output.
14	RST	CS4412 reset input.
17, 18, 19, 20	+9 V to +18 V	High voltage VP power.

Table 3. CRD4412 Interface Header Signal Assignments

5. CRD SCHEMATICS

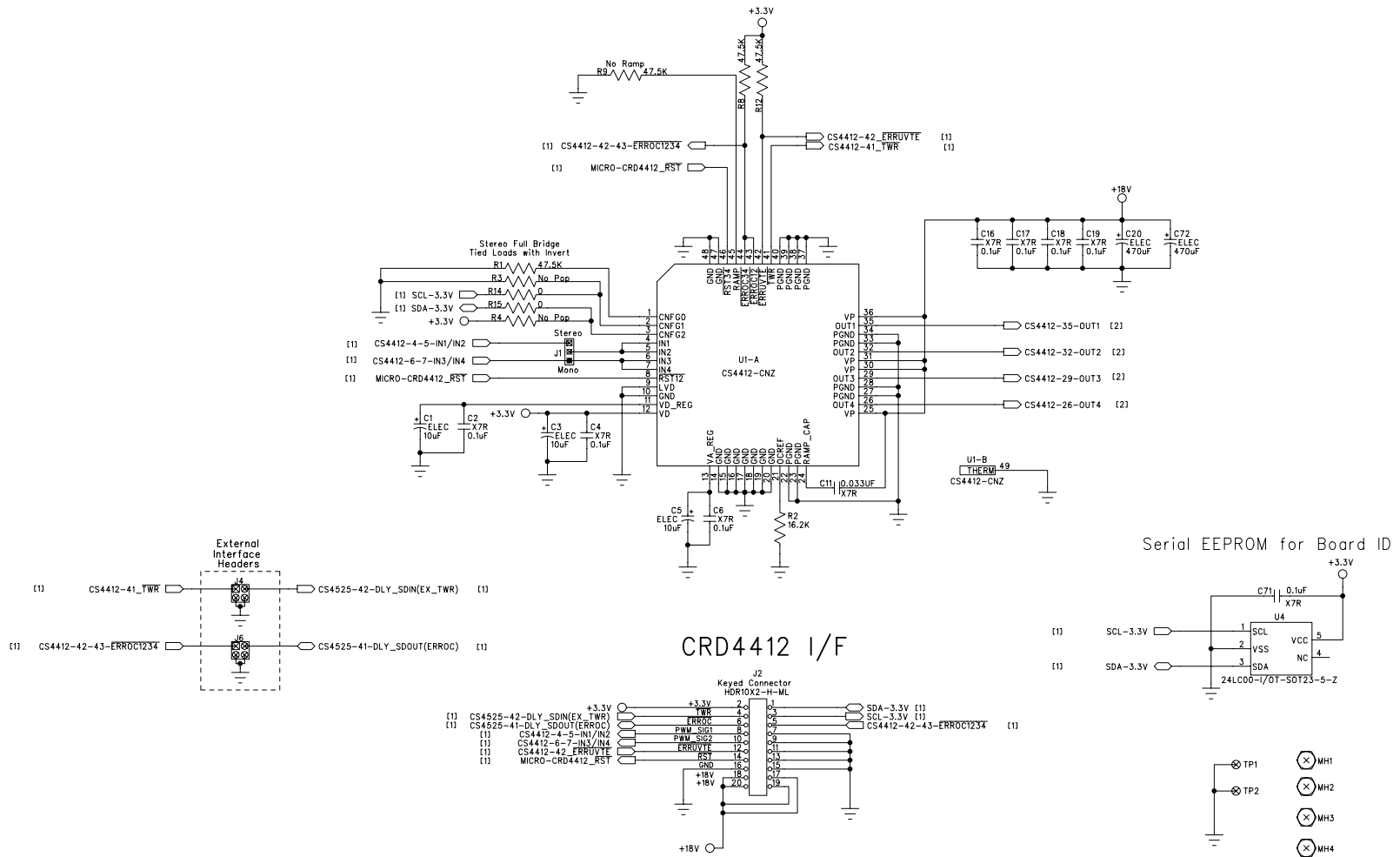


Figure 3. CS4525 - Schematic Page 1



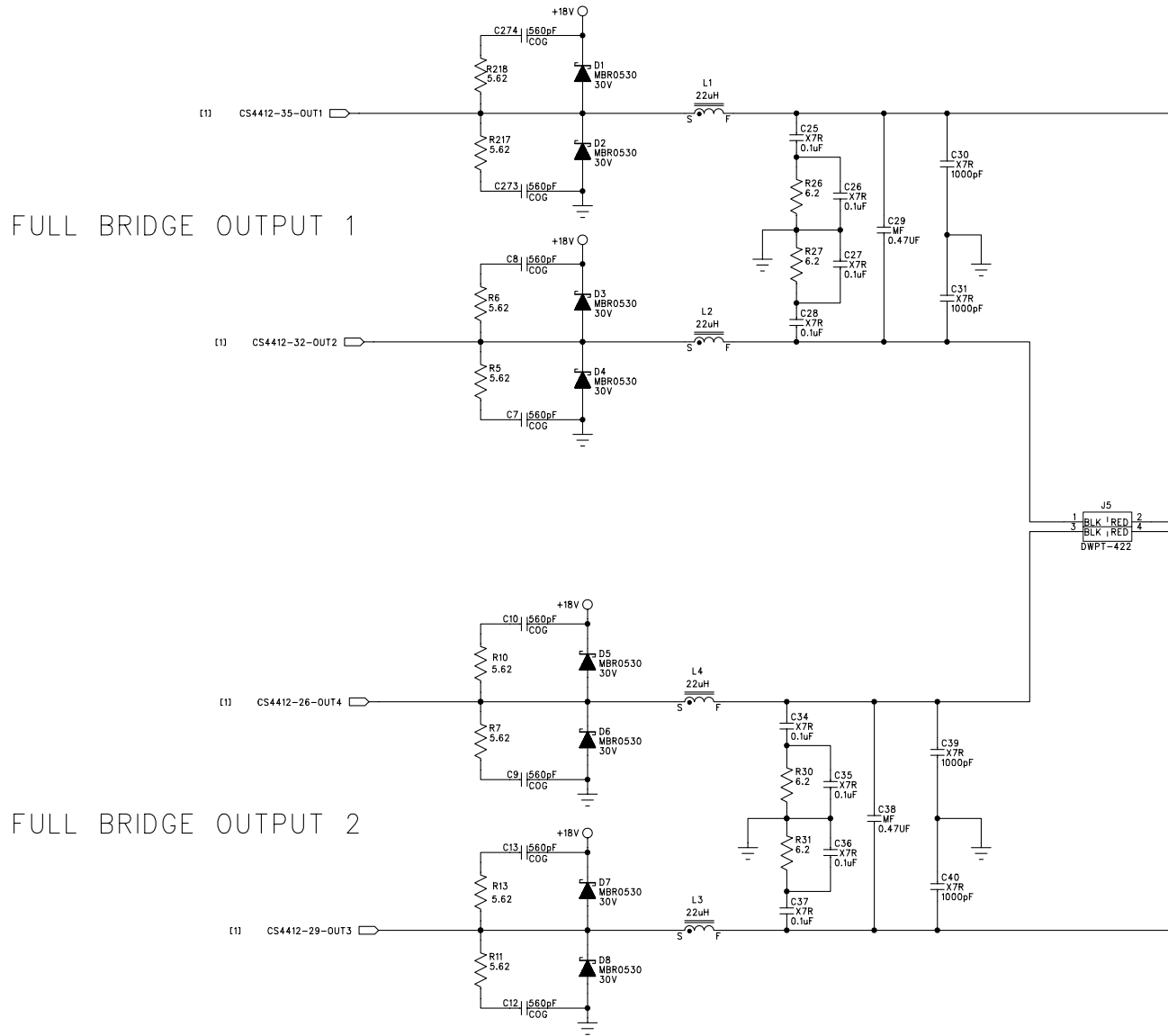


Figure 4. Power Outputs - Schematic Page 2



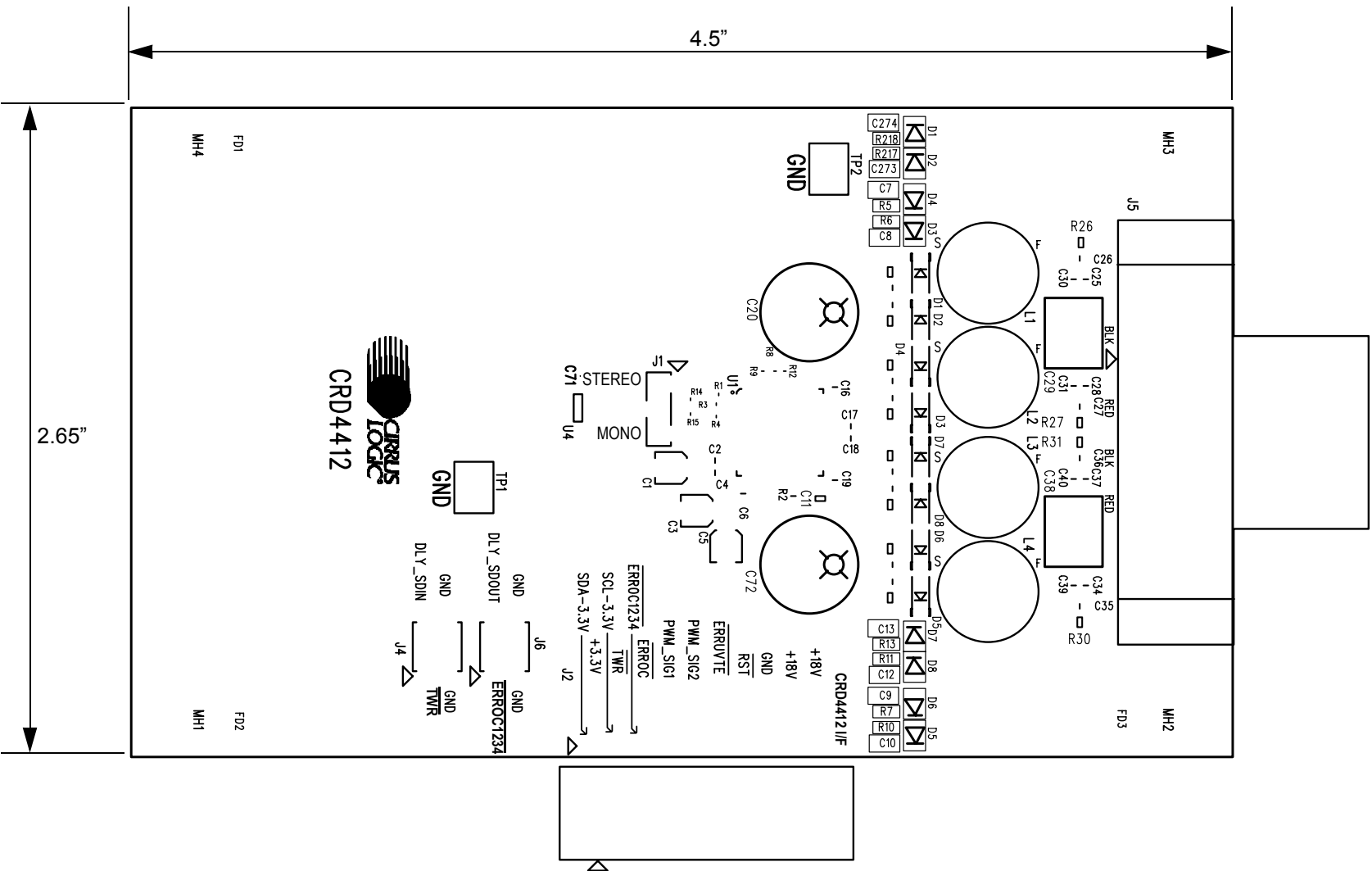


Figure 5. Silkscreen Top

6. CRD LAYOUT

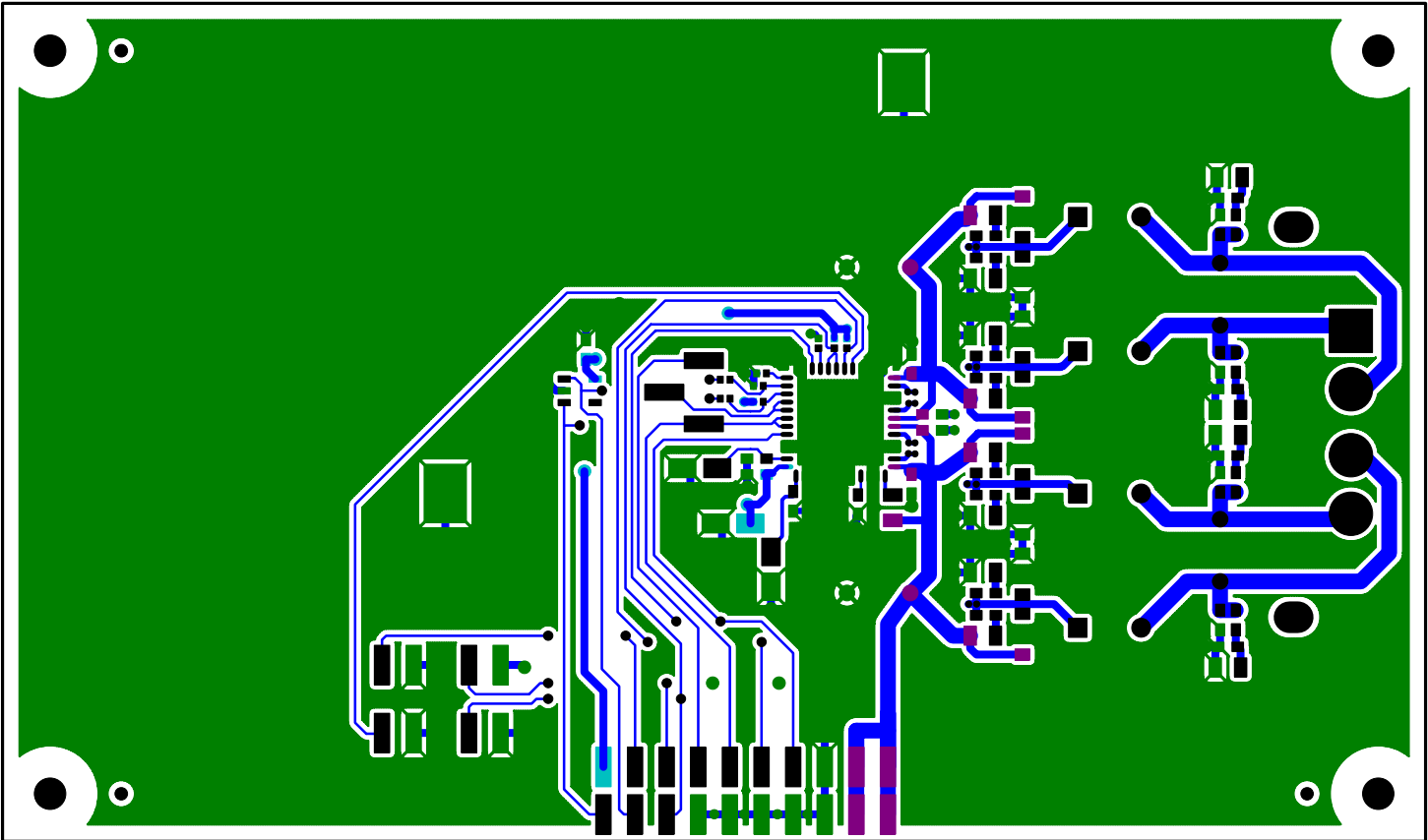


Figure 6. Topside Copper Layer

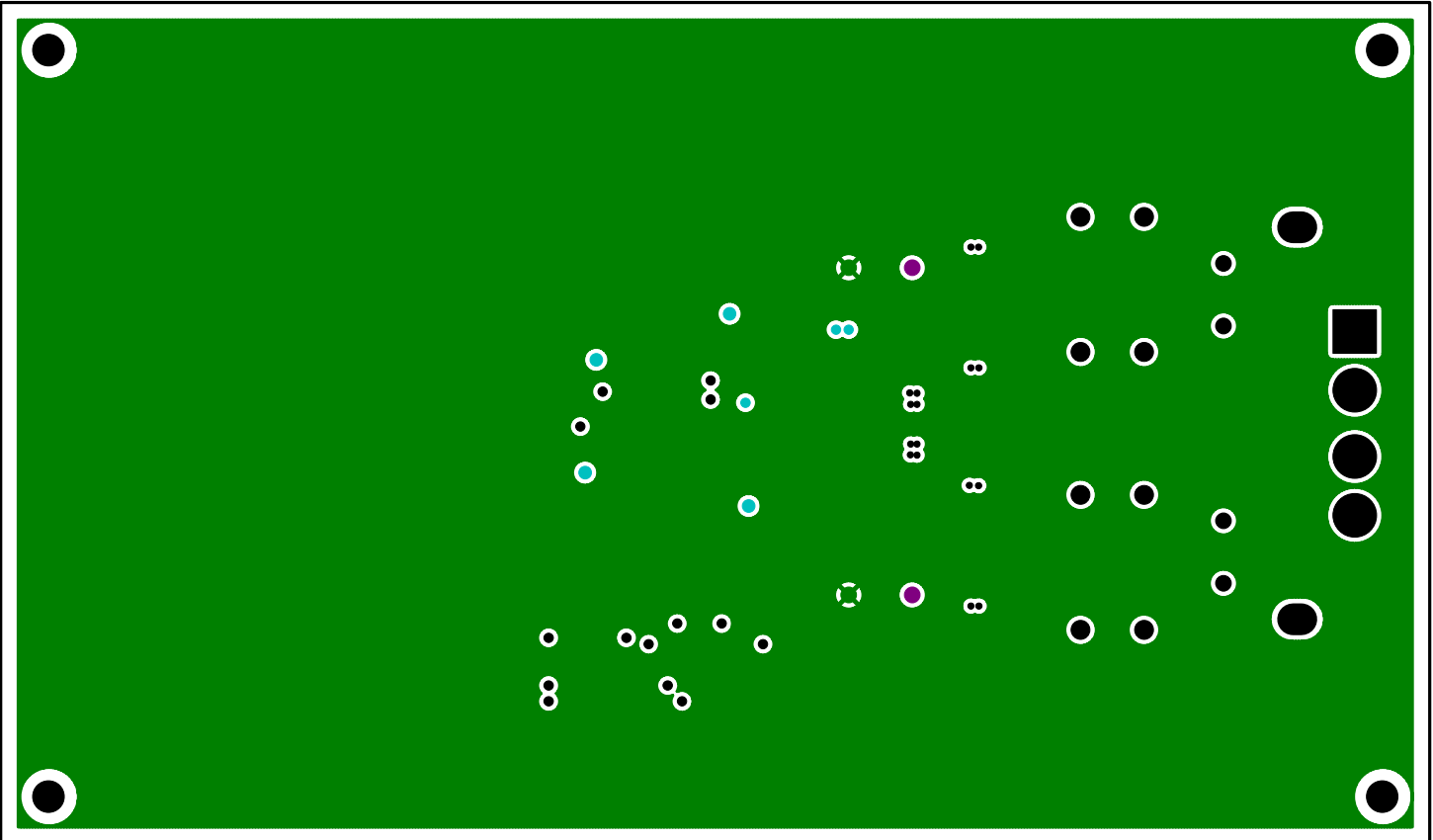


Figure 7. Inner Copper Layer 1

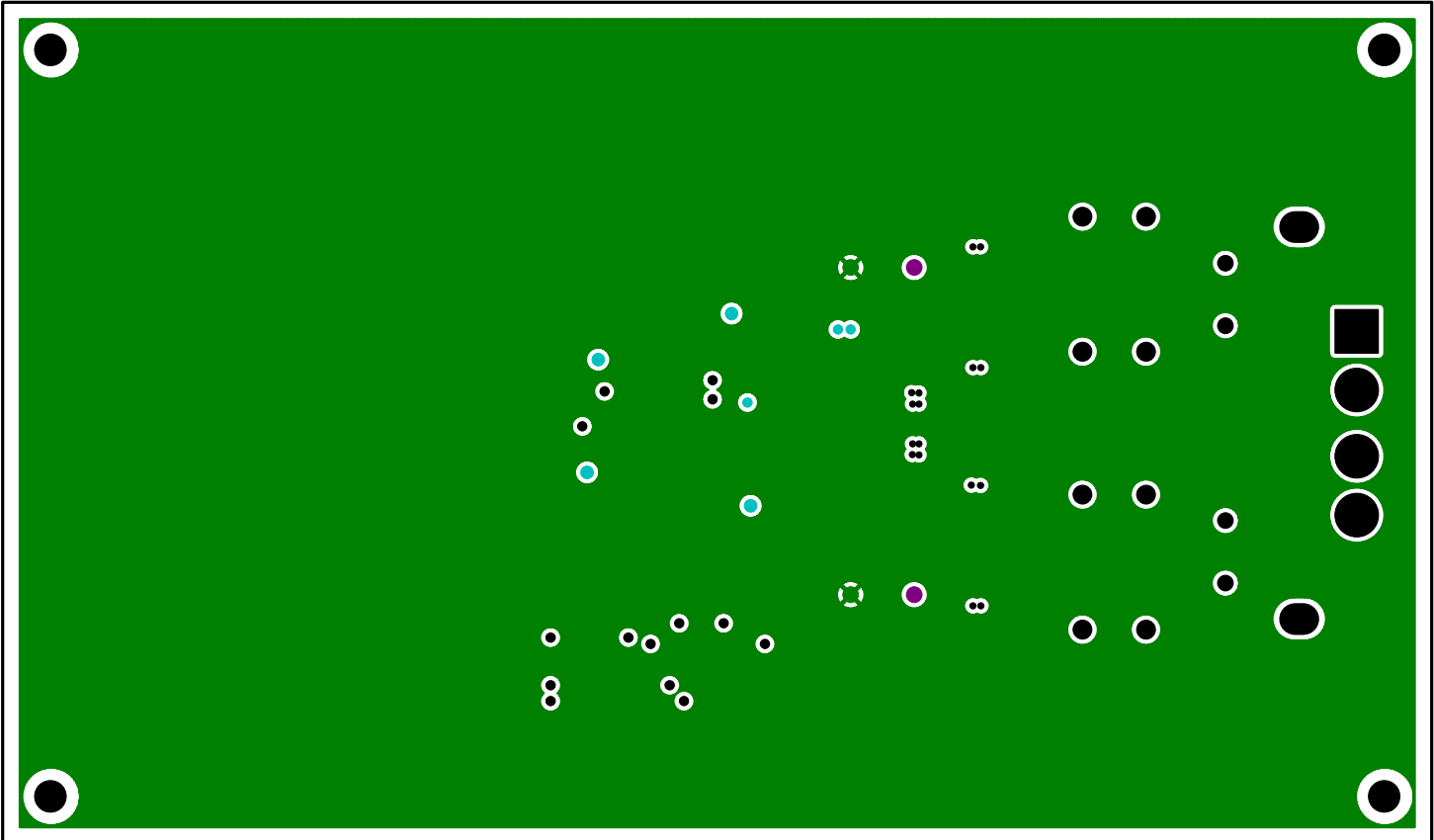


Figure 8. Inner Copper Layer 2

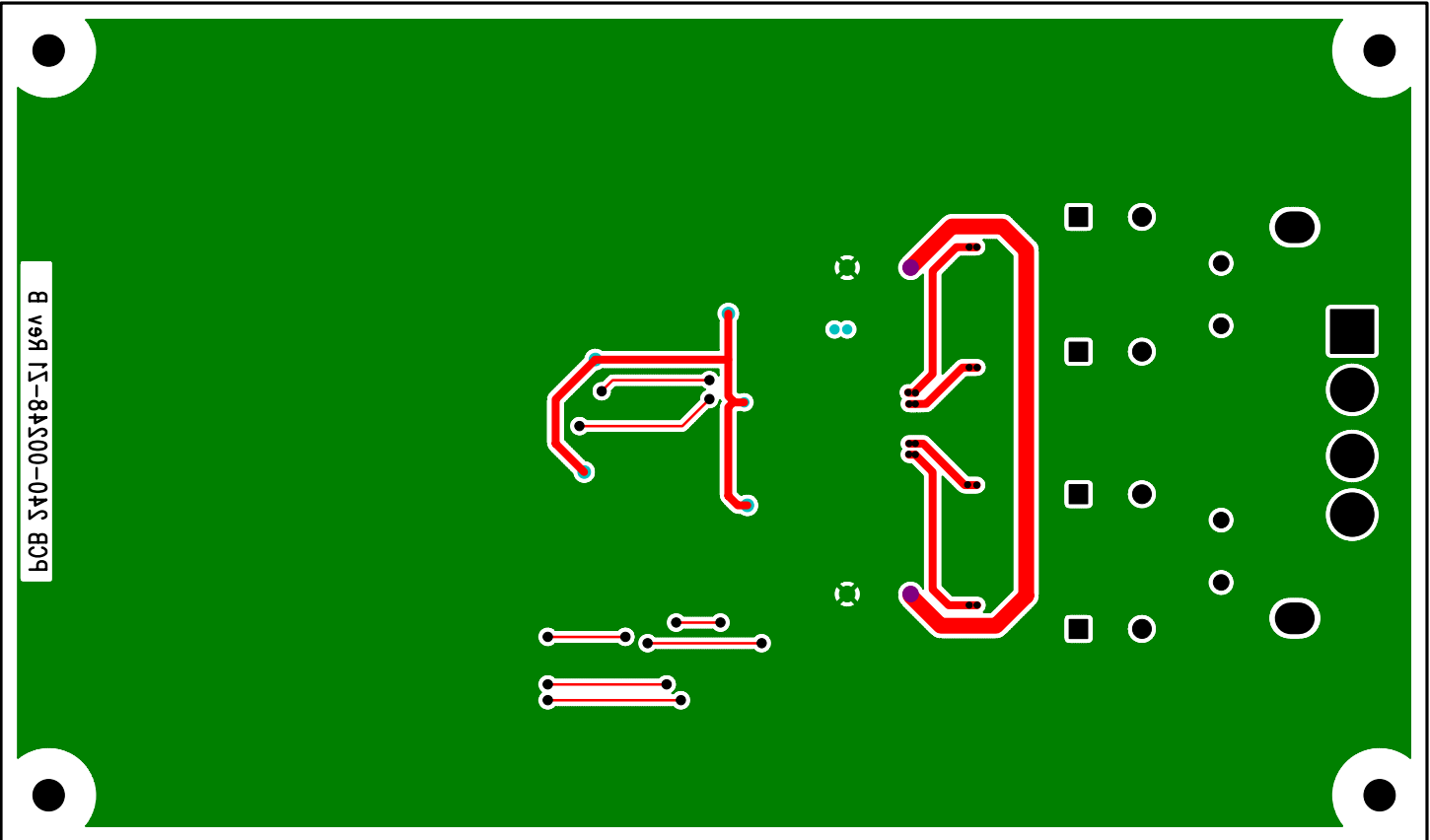


Figure 9. Bottom-side Copper Layer

7. REVISION HISTORY

Release	Changes
RD1	Initial Release

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