CRD5376

Multichannel Seismic Reference Design

Features

- Four Channel Seismic Acquisition Node
  - CS3301 geophone amplifiers (2x)
  - CS3302 hydrophone amplifiers (2x)
  - CS5372 dual ΔΣ modulators (2x)
  - CS5376A quad digital filter (1x)
  - CS4373A ΔΣ test DAC (1x)
  - Precision voltage reference
  - Clock recovery PLL
- On-board Microcontroller
  - SPI™ interface to digital filter
  - USB communication with PC
- PC Evaluation Software
  - Register setup & control
  - FFT frequency analysis
  - Time domain analysis
  - Noise histogram analysis

General Description

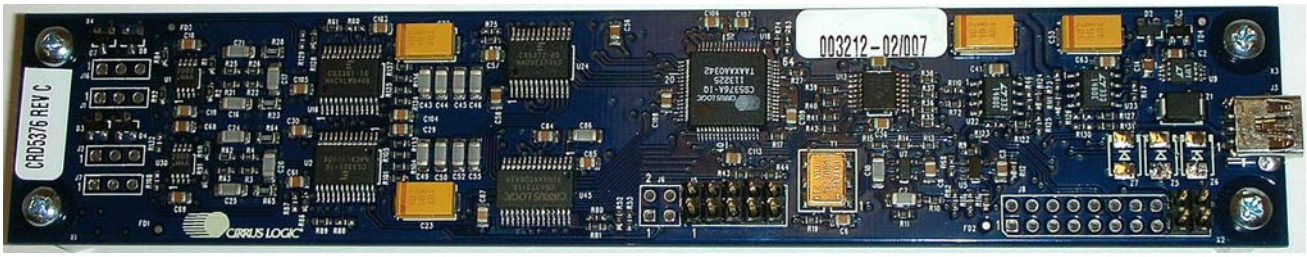
The CRD5376 board is a reference design for the Cirrus Logic multichannel seismic chip set. Data sheets for the CS3301, CS3302, CS4373A, CS5371/72, and CS5376A devices should be consulted when using the CRD5376 reference design.

Pin headers connect external differential geophone or hydrophone sensors to the analog inputs of the measurement channels. An on-board test DAC creates precision differential analog signals for in-circuit performance testing without an external signal source.

The reference design includes an 8051-type microcontroller with hardware SPI™ and USB serial interfaces. The microcontroller communicates with the digital filter via SPI and with the PC evaluation software via USB. The PC evaluation software controls register and coefficient initialization and performs time domain, histogram, and FFT frequency analysis on captured data.

ORDERING INFORMATION

CRD5376	Reference Design



Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find the one nearest to you go to www.cirrus.com

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1. INITIAL SETUP

1.1 Kit Contents

The CRD5376 reference design kit includes:

- CRD5376 reference design board
- USB cable (A to mini-B)
- Software download information card

The following are required to operate CRD5376, and are not included:

- Bipolar power supply with clip lead outputs (+/- 3.3 V @ 100 mA)
- PC running Windows 2000 or XP with an available USB port
- Internet access to download the evaluation software

1.2 Hardware Setup

To set up the CRD5376 reference design hardware:

- Verify all jumpers are in the default settings (see next section).
- With power off, connect the CRD5376 power inputs to the power supply outputs.
  - J8 pin 17 = -3.3 V
  - J8 pin 18 = 0 V
  - J8 pin 19 = +3.3 V
  - J8 pin 20 = 0 V
- Connect the USB cable between the CRD5376 USB connector and the PC USB port.
- Proceed to the Software Setup section to install the evaluation software and USB driver.

1.2.1 Default Jumper Settings

* indicates the default jumper installation for CRD5376.

Amplifier		CS3301	CS3302
CH1	**U16**	*R128 + *R84	R129
CH2	**U2**	*R86 + *R92	R87
CH3	**U33**	R95 + R132	*R94
CH4	**U3**	R58 + R100	*R59

Table 1. Amplifier Pin 13 Jumper Settings

CS5376A	uController	MCLK/2
SDTKI	*R74	R83

Table 2. SDTKI Input Jumper Settings

Component		NPWR	LPWR
U16	**CS3301**	*R61	R60
U2	**CS3301**	*R89	R88
U33	**CS3302**	*R97	R96
U3	**CS3302**	*R71	R70
U24	**CS5372**	*R76	R75
U29	**CS5372**	*R77	R78
U45	**CS4373A**	*R81	R80

Table 3. Analog Components LPWR Jumper Settings

Input Clock	Jumper
1.024 MHz	*R16
2.048 MHz	R18
4.096 MHz	R82

Table 4. PLL Clock Input Jumper Settings

1.3 Software Setup

1.3.1 PC Requirements

The PC hardware requirements for the Cirrus Seismic Evaluation system are:

- *Windows XP, Windows 2000, Windows NT*
- *Intel Pentium 600MHz or higher microprocessor*
- *VGA resolution or higher video card*
- *Minimum 64MB RAM*
- *Minimum 40MB free hard drive space*

1.3.2 Seismic Evaluation Software Installation

Important: For reliable USB communication, the USBXpress driver must be installed after the Seismic Evaluation Software installation but ***before*** launching the application. The USBXpress driver files are included in a sub-folder as part of the installation.

To install the Cirrus Logic Seismic Evaluation Software:

- Go to the Cirrus Logic Industrial Software web page (http://www.cirrus.com/industrialsoftware). Click the link for *"Cirrus Seismic Evaluation GUI"* to get to the download page and then click the link for *"Cirrus Seismic Evaluation GUI Release Vxx"* (*xx* indicates the version number).
- Read the software license terms and click *"Accept"* to download the *"SeismicEvalGUI_vxx.zip"* file to any directory on the PC.
- Unzip the downloaded file to any directory and a *"distribution"* sub-folder containing the installation application will automatically be created.
- Open the *"distribution"* sub-folder and run *"setup.exe"*. If the Seismic Evaluation Software has been previously installed, the uninstall wizard will automatically remove the previous version and you will need to run *"setup.exe"* again.
- Follow the instructions presented by the Cirrus Seismic Evaluation Installation Wizard. The default installation location is *"C:\Program Files\Cirrus Seismic Evaluation"*.

An application note, AN271 - *Cirrus Seismic Evaluation GUI Installation Guide*, is available from the Cirrus Logic web site with step-by-step instructions on installing the Seismic Evaluation Software.

1.3.3 USBXpress Driver Installation

Important: For reliable USB communication, the USBXpress driver must be installed after the Seismic Evaluation Software installation but ***before*** launching the application. The USBXpress driver files are included in a sub-folder as part of the installation.

The Cirrus Logic Seismic Evaluation Software communicates with CRD5376 via USB using the USBXpress driver from Silicon Laboratories (http://www.silabs.com). For convenience, the USBXpress driver files are included as part of the installation package.

To install the USBXpress driver (after installing the Seismic Evaluation Software):

- Connect CRD5376 to the PC through an available USB port and apply power. The PC will detect

CRD5376 as an unknown USB device.

- If prompted for a USB driver, skip to the next step. If not, using Windows Hardware Device Manager go to the properties of the unknown USB API device and select *"Update Driver"*.
- Select *"Install from a list or specific location"*, then select *"Include this location in the search"* and then browse to *"C:\Program Files\Cirrus Seismic Evaluation\Driver\"*. The PC will recognize and install the USBXpress device driver.
- After driver installation, cycle power to CRD5376. The PC will automatically detect it and add it as a USBXpress device in the Windows Hardware Device Manager.

An application note, AN271 - *Cirrus Seismic Evaluation GUI Installation Guide*, is available from the Cirrus Logic web site with step-by-step instructions on installing the USBXpress driver.

1.3.4 Launching the Seismic Evaluation Software

Important: For reliable USB communication, the USBXpress driver must be installed after the Seismic Evaluation Software installation but ***before*** launching the application. The USBXpress driver files are included in a sub-folder as part of the installation.

To launch the Cirrus Seismic Evaluation Software, go to:

- *Start ⇨ Programs ⇨ Cirrus Seismic Evaluation ⇨ Cirrus Seismic Evaluation*

or:

- *C:\Program Files\Cirrus Seismic Evaluation\SeismicGUI.exe*

For the most up-to-date information about the software, please refer to it's help file:

- Within the software: *Help ⇨ Contents*

or:

- Start ⇨ Programs ⇨ *Cirrus Seismic Evaluation ⇨ SEISMICGUI*

or:

- *C:\Program Files\Cirrus Seismic Evaluation\SEISMICGUI.HLP*

1.4 Self-Testing CRD5376

Noise and distortion self-tests can be performed once hardware and software setup is complete.

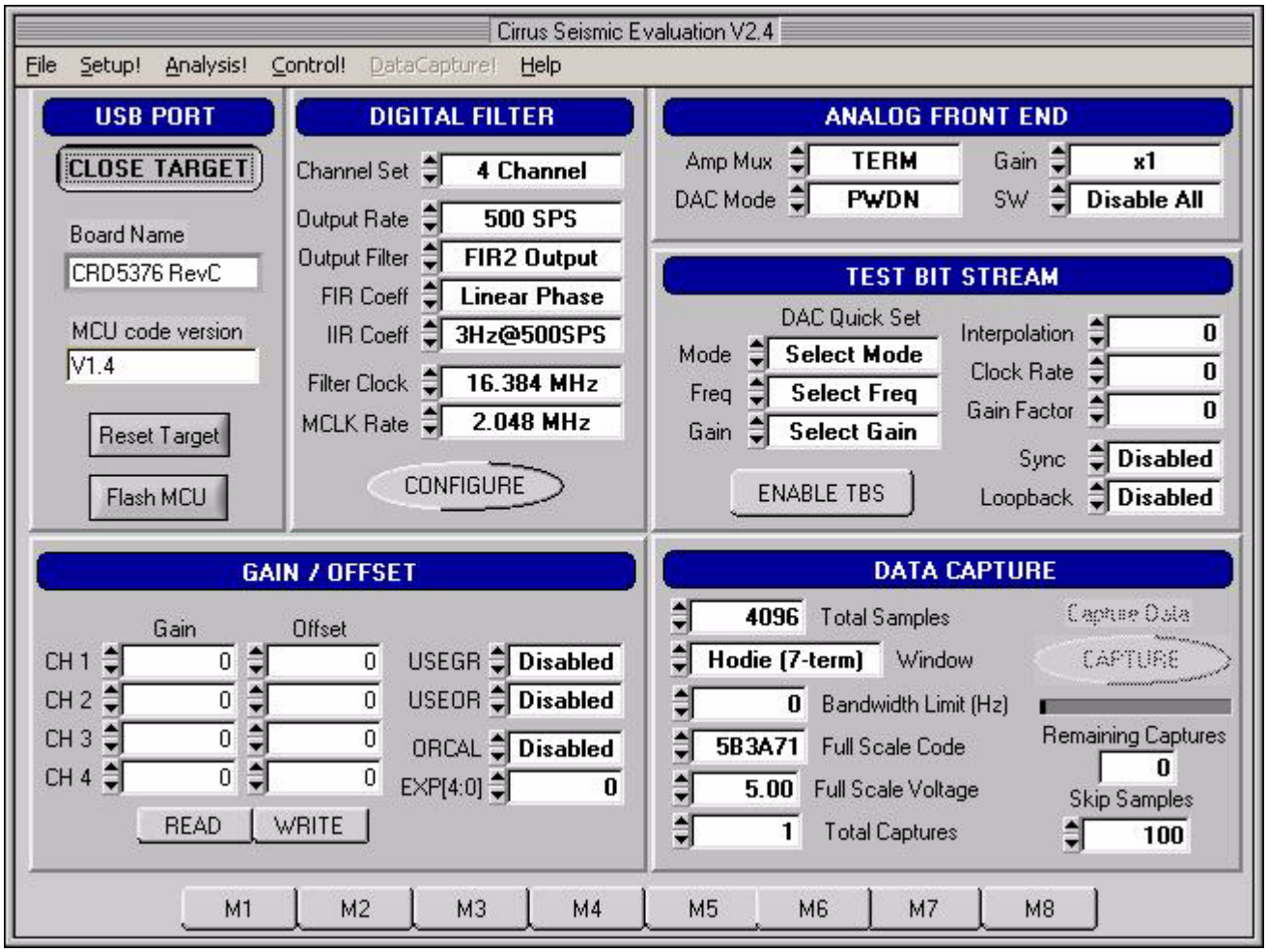
First, initialize the CRD5376 reference design:

- Launch the evaluation software and apply power to CRD5376.
- Click ‘OK’ on the **About** panel to get to the **Setup** panel.
- On the **Setup** panel, select *Open Target* on the **USB Port** sub-panel.
- When connected, the *Board Name* and *MCU code version* will be displayed.

1.4.1 Noise Test

Noise performance of the measurement channel can be tested as follows:

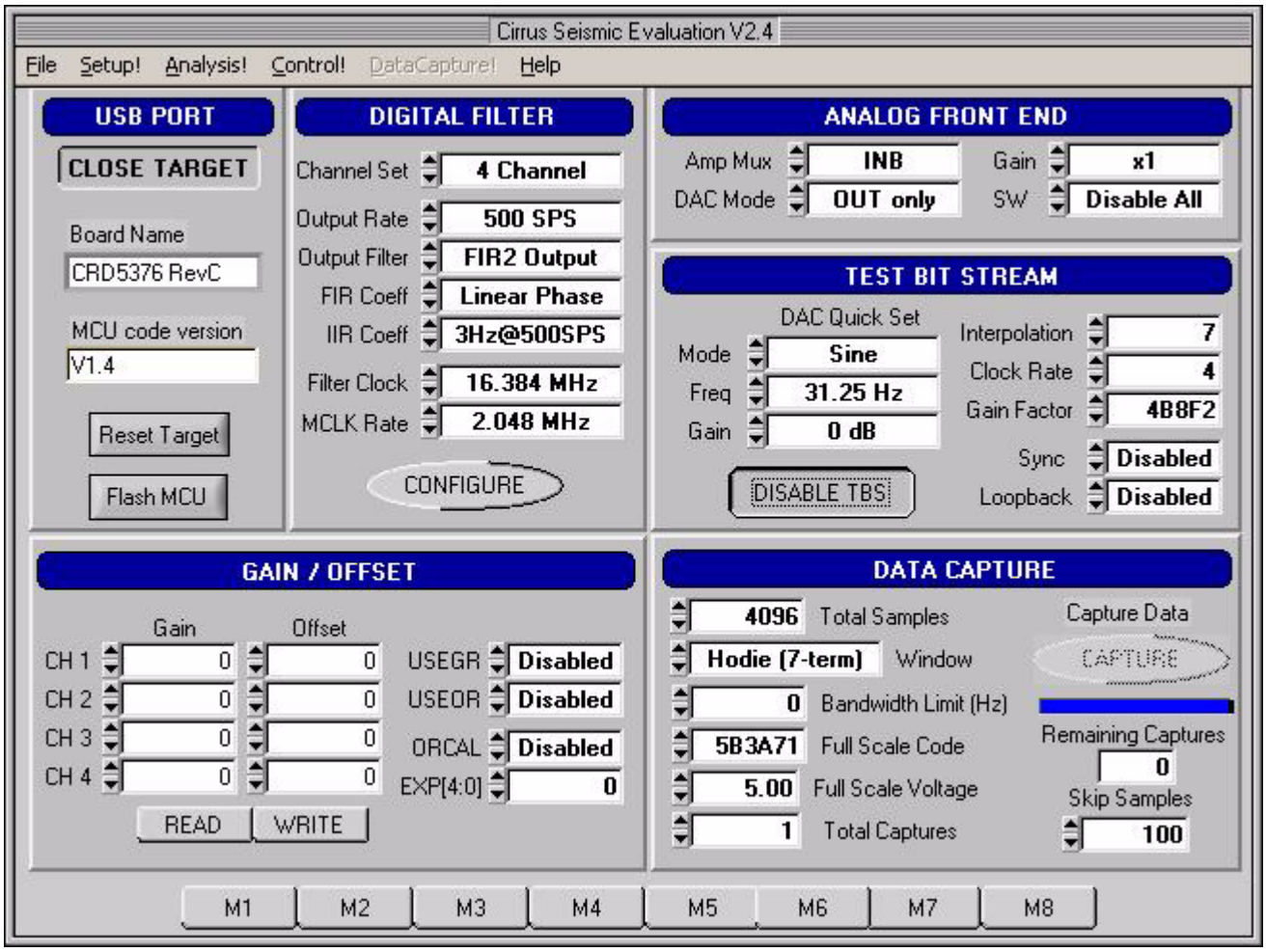
- Set the controls on the **Setup** panel to match the picture:



- Once the **Setup** panel is set, select *Configure* on the **Digital Filter** sub-panel.
- After digital filter configuration is complete, click *Capture* on the **Data Capture** sub-panel.
- Once the data record is collected, the **Analysis** panel is automatically displayed.
- Select *Noise FFT* from the *Test Select* control to display the calculated noise statistics.
- Verify the noise performance (S/N) is 124 dB or better.

1.4.2 Distortion Test

- Set the controls on the **Setup** panel to match the picture:



- Once the **Setup** panel is set, select *Configure* on the **Digital Filter** sub-panel.
- After digital filter configuration is complete, click *Capture* on the **Data Capture** sub-panel.
- Once the data record is collected, the **Analysis** panel is automatically displayed.
- Select *Signal FFT* from the *Test Select* control to display the calculated noise statistics.
- Verify the distortion performance (S/D) is 112 dB or better.

2. HARDWARE DESCRIPTION

2.1 Block Diagram

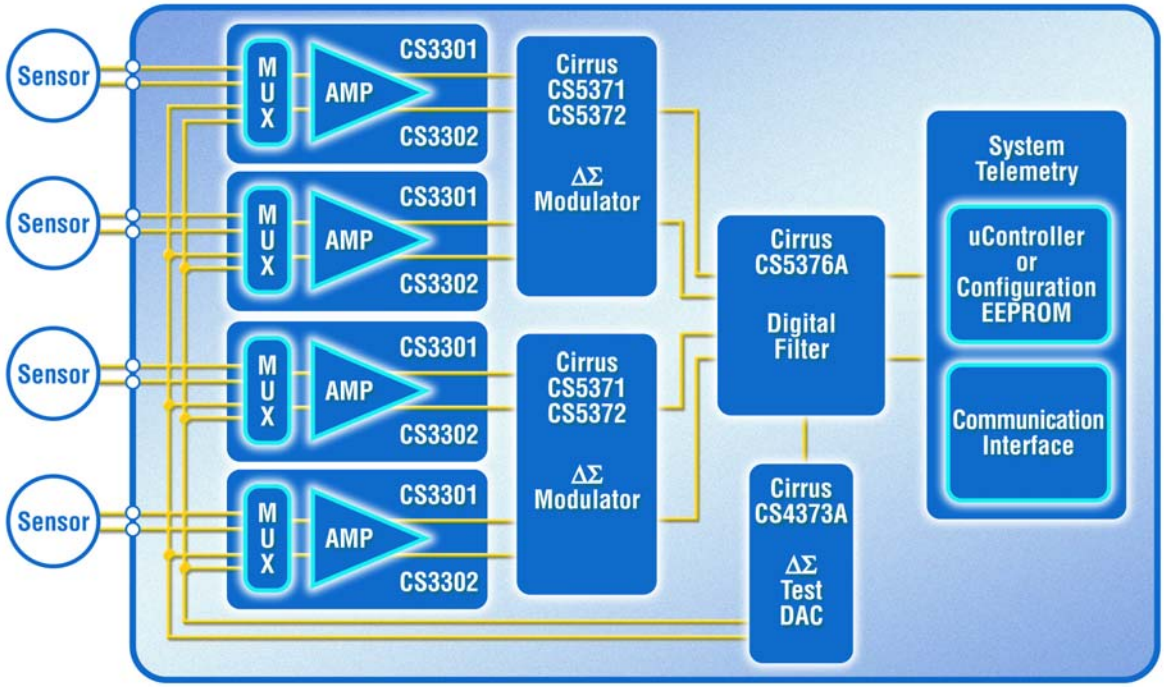


Figure 1. CRD5376 Block Diagram

Major blocks of the CRD5376 reference design include:

- **CS3301 Geophone Amplifier (2x)**
- **CS3302 Hydrophone Amplifier (2x)**
- **CS5372 Dual ΔΣ Modulators (2x)**
- **CS5376A Digital Filter**
- **CS4373A ΔΣ Test DAC**
- **Analog Switch Multiplexer**
- **Precision Voltage Reference**
- **Microcontroller with USB**
- **Phase Locked Loop**
- **RS-485 Transceivers**
- **Voltage Regulators**

2.2 Analog Hardware

2.2.1 Analog Inputs

2.2.1.1 External Inputs - INA

External signals into CRD5376 are from two major classes of sensors, moving coil geophones and piezo-electric hydrophones. Geophones are low-impedance sensors optimized to measure vibrations in land applications. Hydrophones are high-impedance sensors optimized to measure pressure in marine applications. Other sensors for earthquake monitoring and military applications are considered as geophones for this datasheet.

External signals connect to CRD5376 through 3-pin headers on the left side of the PCB. For each channel (CH1, CH2, CH3, CH4), these headers make connections to the differential INA amplifier inputs and to either a GND or GUARD signal for connection to the sensor cable shields, if present.

Signal Input	Pin Header
CH1 INA	J16
CH2 INA	J1
CH3 INA	J2
CH4 INA	J7

Table 5. Pin Header Input Connections

2.2.1.2 GUARD Output, GND Connection

The CS3302 hydrophone amplifier provides a GUARD signal output designed to actively drive the cable shield of a high impedance sensor with the common mode voltage of the sensor differential signal. This GUARD output on the cable shield minimizes leakage by minimizing the voltage differential between the sensor signal and the cable shield.

By default, the GUARD signal is output to pin 3 of the input signal headers on the left side of the PCB for channels 3 and 4, which use the CS3302 amplifier. There is no GUARD signal output for channels 1 and 2 since they use the CS3301 amplifier, so the GUARD pins for these channels are connected to GND through 0 Ω jumpers.

2.2.1.3 Internal Inputs - DAC_OUT, DAC_BUF

The CS4373A test DAC has two high performance differential test outputs, a precision output (DAC_OUT) and a buffered output (DAC_BUF). The DAC_OUT signal is wired directly to the INB inputs of the CS3301/02 amplifiers for testing the performance of the electronics channel. The DAC_BUF signal is wired to the INA inputs of the amplifiers through differential analog switches and is used to test the performance of the measurement channel with a sensor attached.

2.2.1.4 Input Protection

Sensor inputs must have circuitry to protect the analog electronics from voltage spikes. Geophone coils are susceptible to magnetic fields (especially from lightning) and hydrophones can produce large voltage spikes if located near an air gun source.

Discrete switching diodes quickly clamp the analog inputs to the power supply rails when the input voltage spikes. These diodes are reverse biased in normal operation and have low reverse bias leakage and capacitance characteristics to maintain high linearity on the analog inputs.

Specification	Value
Dual Series Switching Diode - ON Semiconductor	BAV99LT1
Surface Mount Package Type	SOT-23
Non-Repetitive Peak Forward Current (1 µs, 1 ms, 1 s)	2.0 A, 1.0 A, 500 mA
Reverse Bias Leakage (25 C to 85 C)	0.004 µA - 0.4 µA
Reverse Bias Capacitance (0 V to 5 V)	1.5 pF - 0.54 pF

Once a voltage spike is shunted to the power supply rail, a discharge path to ground must be present or the power supply will itself spike. Transient voltage suppressors clamp the ±2.5 V analog supply rails in the event of a voltage spike.

Specification	Value
Dual Surface Mount TVS - Diodes Inc.	MMBZ5V6AL-7
Surface Mount Package Type	SOT-23
Working Voltage, Leakage Current	3.0 V, 5 µA
Breakdown Voltage, Threshold Current	5.6 V, 20 mA
Clamp Voltage, Peak Current	8.0 V, 3.0 A

2.2.1.5 Input RC Filters

Following the diode clamps is an RC filter network that bandwidth limits the sensor inputs into the amplifiers to 'chop-the-tops-off' residual voltage spikes not clamped by the discrete diodes. In addition, all Cirrus Logic component ICs have built in ESD protection diodes guaranteed to 2000 V HBM / 200 V MM (JEDEC standard). The small physical size of these ESD diodes restricts their current capacity to 10 mA.

For land applications using the CS3301 amplifier (CRD5376 channels 1 and 2), the INA input has a common mode and differential RC filter. The common mode filter sets a low-pass corner to shunt very high frequency components to ground with minimal noise contribution. The differential filter sets a low-pass corner high enough not to affect the magnitude response of the measurement bandwidth.

For marine applications that use the CS3302 amplifier (CRD5376 channels 3 and 4), the inherent capacitance of the piezoelectric sensor is combined with large resistors connected to the input signal common mode to create an analog high-pass RC filter to eliminate the low-frequency components of ocean noise. Following the high-pass common mode filter is a differential low-pass filter to reject high frequency signals into the amplifier. The cutoff frequency for the low-pass filter is high enough not to affect the magnitude response of the measurement bandwidth.

Land Common Mode Filter Specification	Value
Common Mode Capacitance	10 nF ± 10%
Common Mode Resistance	200 Ω
Common Mode -3 dB Corner @ 6 dB/octave	80 kHz ± 10%

Land Differential Filter Specification	Value
Differential Capacitance	10 nF ± 10%
Differential Resistance	200 Ω + 200 Ω = 400 Ω
Differential -3 dB Corner @ 6 dB/octave	40 kHz ± 10%

Marine Common Mode Filter Specification	Value
Hydrophone Group Capacitance	128 nF ± 10%
Common Mode Resistance	825 kΩ || 825 kΩ = 412 kΩ
-3 dB Corner @ 6 dB/octave	3 Hz ± 10%

Marine Differential Filter Specification	Value
Differential Capacitance	10 nF ± 10%
Differential Resistance	200 Ω + 200 Ω = 400 Ω
-3 dB Corner @ 6 dB/octave	40 kHz ± 10%

2.2.1.6 Common Mode Bias

Differential analog signals into the CS3301/02 amplifiers are required to be biased to the center of the power supply voltage range, which for bipolar supplies is near ground potential. Resistors to create the common mode bias are selected based on the sensor impedance and may need to be modified from the CRD5376 defaults depending on the sensor to be used. Refer to the recommended operating bias conditions for the selected sensor, which are available from the sensor manufacturer.

Specification	Value
Geophone Sensor Bias Resistance	20 kΩ || 20 kΩ = 10 kΩ
Hydrophone Sensor Bias Resistance	18 MΩ || 18 MΩ = 9 MΩ

2.2.1.7 Analog Test Switches

Analog switches on CRD5376 connect the DAC_BUF test signal to the sensor. A two stage approach permits flexibility in switch operation while maximizing performance. First, control signals from the digital filter act as inputs to a 3-to-8 demultiplexer, selecting one of the eight outputs from the decoded GPIO input. Next, the demultiplexer creates level shifted control signals for the analog switches using the selected output and a pull-up / pull-down circuit on the analog power supplies. These level shifted signals control the analog switches to connect the test DAC buffered output (DAC_BUF) to the amplifier sensor input (INA).

Using this level-shifting 3-to-8 demultiplexer scheme allows flexible control of the analog switches without directly coupling them to the digital power supplies. With eight possible decoded outputs from three GPIO pins, multiple combinations of on / off analog switch arrangements are possible.

SW[2..0]	DAC_BUF to INA Connection
000	Channel 1 Only
001	Channel 2 Only
010	Channel 3 Only
011	Channel 4 Only
100	Even Channels Connected
101	Odd Channels Connected
110	All Channels Connected
111	All Channels Disconnected

Table 6. Analog Switch Settings

Independent dual analog switches for each differential channel helps to eliminate crosstalk between them.

Specification	**Value**
Analog Switch Mux - Texas Instruments	CD74HC4051PWR
Surface Mount Package Type	TSSOP-16
Power Supply Voltage, Current	±3.3V, 160 µA
Individual Switch Settings - Ch1, Ch2, Ch3, Ch4	000, 001, 010, 011
Even, Odd Switch Settings - Ch2+Ch4, Ch1+Ch3	100, 101
All On Switch Setting - Ch1+Ch2+Ch3+Ch4	110
All Off Switch Setting	111

Specification	**Value**
Analog Switch Selection - TI LittleLogic Dual-OR	SN74LVC2G32DCTR
Surface Mount Package Type	SSOP-8
Supply Voltage, Current	±2.5 V, 10 µA

Specification	**Value**
Dual SPST Analog Switches - Vishay	DG2003DS
Surface Mount Package Type	SOT23-8
On Resistance Match, + 5 V Supply	1.6 Ω
On Resistance Flatness, + 5 V Supply	0.2 Ω
Off Leakage Current	± 1 nA
Off Isolation @ 1 MHz	-61 dB
Channel Crosstalk @ 1 MHz	-67 dB
Supply Voltage, Power Consumption	±2.5 V, 5.5 µW

2.2.2 Differential Amplifiers

The CS3301/02 amplifiers act as a low-noise gain stage for internal or external differential analog signals.

Analog Signals	Description
INA	Sensor analog input
INB	Test DAC analog input
OUTR, OUTF	Analog rough / fine outputs
GUARD	CS3302 guard output (jumper selection)

Digital Signals	Description
MUX[0..1]	Input mux selection
GAIN[0..2]	Gain range selection
PWDN	Power down mode enable
CLK	CS3301 clock input (jumper selection)

2.2.2.1 MCLK/2 Input vs. GUARD Output

By default, channels 1 and 2 of CRD5376 use the CS3301 geophone amplifier while channels 3 and 4 use the CS3302 hydrophone amplifier. The CS3301 amplifier is chopper stabilized and connects pin 13 to a clock source (MCLK/2) to run the chopper circuitry synchronous to the modulator analog sampling clock. The CS3302 device is not chopper stabilized (with 1/f noise typically buried below the low-frequency ocean noise) to achieve very high input impedance. To minimize leakage from high impedance sensors connected to the CS3302 amplifier, pin 13 produces a GUARD signal output to actively drive a sensor cable shield with the common mode voltage of the sensor signal.

Comparing the CS3301 and CS3302 amplifiers, the functionality of pin 13 (CLK input vs. GUARD output) is the only external difference. CRD5376 can be converted to use any combination of CS3301 and CS3302 amplifiers by replacing the amplifier device and properly installing the pin 13 jumpers. Only one set of pin 13 jumpers should be installed per channel (either CS3301 or CS3302), and the others removed.

Amplifier		CS3301	CS3302
CH1	**U16**	R128 + R84	R129
CH2	**U2**	R86 + R92	R87
CH3	**U33**	R95 + R132	R94
CH4	**U3**	R58 + R100	R59

Table 7. Amplifier Pin 13 Jumper Settings

Common amplifier configurations for CRD5376 include 3x or 4x CS3301 amplifiers for land applications, 4x CS3302 amplifiers for marine streamer applications, and 3x CS3301 amplifiers plus 1x CS3302 amplifier for seabed reservoir monitoring applications. Replacement amplifiers can be requested as samples from the local Cirrus Logic sales representative.

2.2.2.2 Rough-Fine Outputs - OUTR, OUTF

The analog outputs of the CS3301/02 differential amplifiers are split into rough charge and fine charge signals for input to the CS5372 ΔΣ modulators. The amplifier outputs include integrated series resistors to create the anti-alias RC filters required to limit the modulator input signal bandwidth.

Analog signal traces out of the CS3301/02 amplifiers and into the CS5372 modulators are 4-wire INR+, INF+, INF-, INR- quad groups, and are routed with INF+ and INF- as a traditional differential pair and INR+ and INR- as guard traces outside the respective INF+ and INF- traces.

2.2.2.3 Anti-alias RC Filters

The CS5372 ΔΣ modulators are 4th order and high frequency input signals can cause instability. Simple single-pole anti-alias RC filters are required between the CS3301/02 amplifier outputs and the CS5372 modulator inputs to bandwidth limit analog signals into the modulator.

The CS3301/02 amplifier outputs include internal series resistors, so a differential anti-alias RC filter is created by connecting 20 nF of high linearity differential capacitance (2x 10 nF C0G) between each half of the rough and fine signals. External 0 Ω resistors are included in series with the amplifier internal anti-alias resistors to support testing of other anti-alias RC filter configurations.

2.2.3 Delta-Sigma Modulators

Each CS5372 dual modulator performs the A/D function for differential analog signals from two CS3301/02 amplifiers. The digital outputs are oversampled ΔΣ bit streams.

Analog Signals	Description
INR1, INF1	Channel 1 analog rough / fine inputs
INR2, INF2	Channel 2 analog rough / fine inputs
VREF	Voltage reference analog inputs

Digital Signals	Description
MDATA[1..2]	Modulator delta-sigma data outputs
MFLAG[1..2]	Modulator over-range flag outputs
MCLK	Modulator clock input
MSYNC	Modulator synchronization input
PWDN[1..2]	Power down mode enable
OFST	Internal offset enable (+VD when using CS3301/02)

2.2.3.1 Rough-Fine Inputs - INR, INF

The modulator analog inputs are separated into rough and fine signals, each of which has an anti-alias RC filter to limit the signal bandwidth into the modulator inputs.

2.2.3.2 Offset Enable - OFST

The CS5372 ΔΣ modulator requires differential offset to be enabled to eliminate idle tones for a terminated input. The use of internal offset to eliminate idle tones is described in the CS5372 data sheet. By default, OFST is enabled for the CS5372 modulators on CRD5376.

2.2.4 Delta-Sigma Test DAC

The CS4373A DAC creates differential analog signals for system tests. Multiple test modes are available and their use is described in the CS4373A data sheet.

Analog Signals	Description
OUT	Precision differential analog output
BUF	Buffered differential analog output
CAP	Capacitor connection for internal anti-alias filter
VREF	Voltage reference analog inputs

Digital Signals	Description
TDATA	Delta-sigma test data input
MCLK	Clock input
SYNC	Synchronization input
MODE[0..2]	Test mode selection
ATT[0..2]	Attenuation range selection

2.2.4.1 Precision Output - DAC_OUT

The CS4373A test DAC has a precision output (DAC_OUT) that is routed to the amplifier INB inputs of all channels. The input impedance of the CS3301/02 INB amplifier inputs are high enough that the precision output can be directly connected to the INB inputs of all channels simultaneously.

2.2.4.2 Buffered Output - DAC_BUF

The CS4373A test DAC has a buffered output (DAC_BUF) that is routed through differential analog switches to the amplifier INA inputs for each channel. This output is less sensitive to loading than the precision outputs, and can drive a sensor attached to the amplifier INA inputs provided the sensor meets the impedance requirements specified in the CS4373A data sheet.

2.2.5 Voltage Reference

A voltage reference on CRD5376 creates a precision voltage from the regulated analog supplies for the modulator and test DAC VREF inputs. Because the voltage reference output is generated relative to the negative analog power supply, VREF+ is near GND potential for bipolar power supplies.

Specification	Value
Precision Reference - Linear Tech	LT1019AIS8-2.5
Surface Mount Package Type	SO-8
Output Voltage Tolerance	+/- 0.05%
Temperature Drift	10 ppm / degC
Quiescent Current	0.65 mA
Output Voltage Noise, 10 Hz - 1 kHz	4 ppm_{RMS}
Ripple Rejection, 10 Hz - 200 Hz	> 100 dB

2.2.5.1 VREF_MOD12, VREF_MOD34, VREF_DAC

The voltage reference output is provided to the CS5372 ΔΣ modulators and the CS4373A test DAC through separate low pass RC filters. By separately filtering the voltage reference for each device, signal dependent sampling of VREF by one device is isolated from other devices. Each voltage reference signal is routed as a separate differential pair from the large RC filter capacitor to control the sensitive VREF source-return currents and keep them out of the ground plane. In addition to the RC filter function, the 100 uF filter capacitor provides a large charge-well to help settle voltage reference sampling transients.

2.3 Digital Hardware

2.3.1 Digital Filter

The CS5376A quad digital filter performs filtering and decimation of four delta-sigma bit streams from the CS5372 modulators. It also creates a delta-sigma bit stream output to create analog test signals in the CS4373A test DAC.

The CS5376A requires several control signal inputs from the external system.

Control Signals	Description
RESETz	Reset input, active low
BOOT	Microcontroller / EEPROM boot mode select
TIMEB	Time Break input, rising edge triggered
CLK	Master clock input, 32.768 MHz
SYNC	Master synchronization input, rising edge triggered

Configuration is completed through the SPI 1 port.

SPI1 Signals	Description
SSIz	Serial chip select input, active low
SCK1	Serial clock input
MISO	Master in / slave out serial data
MOSI	Master out / slave in serial data
SINTz	Serial acknowledge output, active low
SSOz	Serial chip select output (unused on CRD5376)

Data is collected through the SD port.

SD Port Signals	Description
SDTKI	Token input to initiate an SD port transaction
SDRDYz	Data ready acknowledge, active low
SDCLK	Serial clock input
SDDAT	Serial data output
SDTKO	Token output (unused on CRD5376)

Modulator ΔΣ data is input through the modulator interface.

Modulator Signals	Description
MCLK	Modulator clock output
MCLK/2	Modulator clock output, half-speed
MSYNC	Modulator synchronization output
MDATA[1..4]	Modulator delta-sigma data inputs
MFLAG[1..4]	Modulator over-range flag inputs

Test DAC ΔΣ data is generated by the test bit stream generator.

Test Bit Stream Signals	Description
TBSDATA	Test DAC delta-sigma data output
TBSCLK	Test DAC clock output (unused on CRD5376)

Amplifier, modulator, test DAC and analog switch digital pins are controlled by the GPIO port.

GPIO Signals	Description
GPIO[0..1]:MUX[0..1]	Amplifier input mux selection
GPIO[2..4]:GAIN[0..2]	Amplifier gain / test DAC attenuation
GPIO[5..7]:MODE[0..2]	Test DAC mode selection
GPIO[8]:PWDN	Amplifier / modulator power down
GPIO[9..11]:SW[0..2]	Analog switch control

The secondary serial port (SPI 2) and boundary scan JTAG port are unused on CRD5376.

SPI2 Signals	Description
SCK2	Serial clock output (unused on CRD5376)
SO	Serial data output (unused on CRD5376)
SI[1..4]	Serial data inputs (unused on CRD5376)

JTAG Signals	Description
TRSTz	JTAG reset (unused on CRD5376)
TMS	JTAG test mode select (unused on CRD5376)
TCK	JTAG test clock input (unused on CRD5376)
TDI	JTAG test data input (unused on CRD5376)
TDO	JTAG test data output (unused on CRD5376)

2.3.1.1 MCLK vs. MCLK/2 Usage

The CS5376A digital filter creates the analog sampling clock used by the CS5372 ΔΣ modulators and CS4373A test DAC. MCLK has strict jitter requirements to guarantee the accuracy of analog-to-digital and digital-to-analog conversion, and so is carefully routed between the digital filter and modulators / test DAC.

The CS3301 amplifier also requires an analog sampling clock to run the internal chopper stabilization circuitry, but without the strict jitter or speed requirement and so can run equally well from the full-speed MCLK or half-speed MCLK/2. Although MCLK could be used as the amplifier input clock, using MCLK/2 isolates the sensitive modulator / test DAC analog sampling clock from the amplifier clock.

2.3.1.2 Configuration - SPI 1 Port

Configuration of the CS5376A digital filter is through the SPI 1 port by the on-board 8051 microcontroller which receives commands from the PC evaluation software via the USB interface. Evaluation software commands can write/read digital filter registers, specify digital filter coefficients and test bit stream data, and start/stop digital filter operation.

How the digital filter receives configuration information, either from a microcontroller or configuration EEPROM, is selected by the BOOT signal. The BOOT signal is tied low on CRD5376 for microcontroller configuration.

2.3.1.3 Digital Control Signals

The reset, synchronization and timebreak signals to the CS5376A digital filter are generated by the on-board microcontroller and applied to the CS5376A digital filter RESET, SYNC, and TIMEB inputs.

Data collection transactions are initiated by a rising edge on the SDTKI input, as described in the CS5376A data sheet. Two options for providing the required SDTKI rising edge are available on CRD5376, as an input from the microcontroller to initiate data transactions on command or from the MCLK/2 clock to initiate data transactions automatically as soon as they are available from the digital filter.

CS5376A	uController	MCLK/2
SDTKI	R74	R83

Table 8. SDTKI Input Jumper Settings

The LPWR digital inputs to the analog components on CRD5376 reduce their power consumption at the expense of analog performance. Jumper options are provided to switch the analog components from normal operation at full specifications to low power operation with reduced specifications.

Component		NPWR	LPWR
U16	**CS3301**	R61	R60
U2	**CS3301**	R89	R88
U33	**CS3302**	R97	R96
U3	**CS3302**	R71	R70
U24	**CS5372**	R76	R75
U29	**CS5372**	R77	R78
U45	**CS4373A**	R81	R80

Table 9. Analog Components LPWR Jumper Settings

2.3.2 Microcontroller

Included on CRD5376 is an 8051-type microcontroller with integrated hardware SPI and USB interfaces. This C8051F320 microcontroller is a product of Silicon Laboratories (http://www.silabs.com/). Key features of the C8051F320 microcontroller are:

8051 compatibility - uses industry standard 8051 software development tools

In-circuit debugger - software development on the target hardware

Internal memory - 16k flash ROM and 2k static RAM included on-chip

Multiple serial connections - SPI, USB, I2C, and UART

High performance - 25 MIPS maximum

Low power - 0.6 mA @ 1 MHz w/o USB, 9 mA @ 12 MHz with USB

Small size - 32 pin LQFP package, 9mm x 9mm

Industrial temperature - full performance (including USB) from -40 C to +85 C

Internal temperature sensor - with range violation interrupt capability

Internal timers - four general purpose plus one extended capability

Power on reset - can supply a reset signal to external devices

Analog ADC - 10 bit, 200 ksps SAR with internal voltage reference

Analog comparators - arbitrary high/low voltage compare with interrupt capability

The exact use of the microcontroller features is controlled by embedded firmware.

C8051F320 has dedicated pins for power and the USB connection, plus 25 general purpose I/O pins that connect to the various internal resources through a programmable crossbar. Hardware connections on CRD5376 limit how the blocks can operate, so the port mapping of microcontroller resources is detailed below.

Pin #	Pin Name	Assignment	Description
1	P0.1	SDTKI	Token to start CS5376A data transaction
2	P0.0	SYNC_IO	SYNC signal from RS-485
3	GND		Ground
4	D+		USB differential data transceiver
5	D-		USB differential data transceiver
6	VDD		+3.3 V power supply input
7	REGIN		+5 V power supply input (unused on CRD5376)
8	VBUS		USB voltage sense input

Pin #	Pin Name	Assignment	Description
9	/RST C2CK	RESETz	Power on reset output, active low Clock input for debug interface
10	P3.0 C2D	GPIO	General purpose I/O Data in/out for debug interface
11	P2.7	AIN-	ADC input
12	P2.6	AIN+	ADC input
13	P2.5	SW0	Analog switch control
14	P2.4	MODE2	CS4373A mode control
15	P2.3	MODE1	CS4373A mode control
16	P2.2	MODE0	CS4373A mode control

Pin #	Pin Name	Assignment	Description
17	P2.1	TIMEB	Time Break signal to CS5376A
18	P2.0	SYNC	SYNC signal to CS5376A
19	P1.7	BYP_EN	I2C bypass switch control
20	P1.6	SDA_DE	I2C data driver enable
21	P1.5	SCL	I2C clock in/out
22	P1.4	SDA	I2C data in/out
23	P1.3	SSIz	SPI chip select output, active low
24	P1.2	MOSI	SPI master out / slave in

Pin #	Pin Name	Assignment	Assignment
25	P1.1	MISO	SPI master in / slave out
26	P1.0	SCK1	SPI serial clock
27	P0.7		Internal VREF bypass capacitors
28	P0.6	SINTz	Serial acknowledge from CS5376A, active low
29	P0.5	RX	UART receiver
30	P0.4	TX	UART transmitter
31	P0.3	4.096MHZ	External clock input
32	P0.2	SDRDYz	Data ready acknowledge from CS5376A, active low

Many connections to the C8051F320 microcontroller are inactive by default, but are provided for convenience during custom reprogramming. Listed below are the default active connections to the microcontroller and how they are used.

2.3.2.1 SPI Interface

The microcontroller SPI interface communicates with the CS5376A digital filter to write/read configuration information from the SPI 1 port and collect conversion data from the SD port. Detailed information about interfacing to the digital filter SPI 1 and SD ports can be found in the CS5376A data sheet.

2.3.2.2 USB Interface

The microcontroller USB interface communicates with the PC evaluation software to receive configuration commands and return collected conversion data. The USB interface uses the Silicon Laboratories API and Windows drivers, which are available free from the internet (http://www.silabs.com/).

2.3.2.3 Reset Source

By default, the C8051F320 microcontroller receives its reset signal from the internal power-on reset. This reset signal is also output to the CS5376A digital filter.

2.3.2.4 Clock Source

By default, the C8051F320 microcontroller uses an internally generated 12 MHz clock for compatibility with USB standards.

2.3.2.5 Timebreak Signal

By default, the C8051F320 microcontroller sends the TIMEB signal to the digital filter for the first collected sample of a data record. By default, 100 initial samples are skipped during data collection to ensure the CS5376A digital filters are fully settled, and the timebreak signal is automatically set for the first 'real' collected sample.

2.3.2.6 C2 Debug Interface

Through the PC evaluation software, the microcontroller default firmware can be automatically flashed to the latest version without connecting an external programmer. To flash custom firmware, software tools and an inexpensive hardware programmer that connects to the C2 Debug Interface on CRD5376 is available for purchase from Silicon Laboratories (DEBUGADPTR1-USB).

2.3.3 Phase Locked Loop

To make synchronous analog measurements throughout a distributed system, a synchronous system clock is required to be provided to each measurement node. CRD5376 can receive a lower frequency system clock through the external connector and create a synchronous higher frequency clock using an onboard PLL.

Specification	Value
Input Clock Frequency	1.024, 2.048, 4.096 MHz
Distributed Clock Synchronization	± 240 ns
Maximum Input Clock Jitter, RMS	1 ns

Specification	Value
PLL Output Clock Frequency	32.768 MHz
Maximum Output Jitter, RMS	300 ps
Oscillator Type	VCXO
Detector Architecture	Phase / Frequency

The expected input clock frequency to the external connector is set by jumper options. If no external clock is supplied to CRD5376, the PLL will free-run at the nominal output frequency. A jumper option is available to output the clock to the external connector, making it the system clock source.

Input Clock	Jumper
1.024 MHz	R16
2.048 MHz	R18
4.096 MHz	R82

Output Clock	Jumpers
1.024 MHz	R68 + R16
2.048 MHz	R68 + R18
4.096 MHz	R68 + R82

Table 10. Clock Input / Output Jumper Settings

The PLL on CRD5376 uses a voltage controlled crystal oscillator (VCXO) to minimize jitter, and has a single gate phase/frequency detector and clock divider to minimize size and power.

Specification	Value
Oscillator - Citizen 32.768 MHz VCXO	CSX750VBEL32.768MTR
Surface Mount Package Type	Leadless 6-Pin, 5x7 mm
Supply Voltage, Current	3.3 V, 11 mA
Frequency Stability, Pullability	± 50 ppm, ± 90 ppm
Startup Time	4 ms

Specification	Value
Phase Detector - TI LittleLogic XOR	SN74LVC1G86DBVR
Surface Mount Package Type	SOT23-5
Supply Voltage, Current	3.3 V, 10 µA

Specification	Value
Loop Filter Integrator - Linear Tech Op-Amp	LT1783IS5
Surface Mount Package Type	SOT23-5
Supply Voltage, Current	3.3 V, 375 µA

Specification	Value
Clock Divider - TI LittleLogic D-Flop	SN74LVC2G74DCTR
Surface Mount Package Type	SSOP8-199
Supply Voltage, Current	3.3 V, 10 µA

2.3.4 RS-485 Telemetry

By default, CRD5376 communicates with the PC evaluation software through the microcontroller USB port. Additional hardware is designed onto CRD5376 to use the microcontroller I2C port as a low-level local telemetry, but it is provided for custom programming convenience only and is not directly supported by the CRD5376 PC evaluation software or microcontroller firmware.

Telemetry signals enter CRD5376 through RS-485 transceivers, which are differential current mode transceivers that can reliably drive long distance communication. Data passes through the RS-485 transceivers to the microcontroller I2C interface and the clock and synchronization inputs.

Specification	Value
RS-485 Transceiver - Linear Tech	LTC1480IS8
Surface Mount Package Type	SOIC-8, 5mm x 6mm
Supply Voltage, Quiescent Current	3.3V, 600 µA
Maximum Data Rate	2.5 Mbps
Transmitter Delay, Receiver Delay	25 - 80 ns, 30 - 200 ns
Transmitter Current, Full Termination (60 Ω)	25 mA
Transmitter Current, Half Termination (120 Ω)	13 mA

2.3.4.1 CLK, SYNC

Clock and synchronization telemetry signals into CRD5376 are received through RS-485 twisted pairs. These signals are required to be distributed through the external system with minimal jitter and timing skew, and so are normally driven through high-speed bus connections.

Specification	Value
Synchronous Inputs, 2 wires each	CLK±, SYNC±

Specification	Value
Distributed SYNC Signal Synchronization	± 240 ns
Distributed Clock Synchronization	± 240 ns
Analog Sampling Synchronization Accuracy	± 480 ns

Synchronization of the measurement channel is critical to ensure simultaneous analog sampling across a network. Several options are available for connecting a SYNC signal through the RS-485 telemetry to the digital filter.

A direct connection is made when the SYNC_IO signal is received over the dedicated RS-485 twisted pair and sent directly to the digital filter SYNC pin through jumper R93. The incoming SYNC_IO signal must be synchronized to the network at the transmitter since no local timing adjustment is available.

A microcontroller hardware connection is made when the SYNC_IO signal is received over the dedicated RS-485 twisted pair and detected by a microcontroller interrupt. The microcontroller can then use an internal counter to re-time the SYNC signal output to the digital filter SYNC input as required.

A microcontroller software connection is made when the SYNC signal output is created by the microcontroller on command from the system telemetry. The microcontroller can use an internal counter to re-time the SYNC signal output to the digital filter SYNC input as required.

2.3.4.2 I2C - SCL, SDA, Bypass

The I2C telemetry connections to CRD5376 transmit and receive through RS-485 twisted pairs. Because signals passing through the transceivers are actively buffered, full I2C bus arbitration and error detection cannot be used (i.e. high-impedance NACK).

The I2C inputs and outputs can be externally wired to create either a daisy chain or a bus type network, depending how the telemetry system is to be implemented. Analog switches included on CRD5376 can bypass the I2C signals to create a bus network from a daisy chain network following address assignment.

Specification	Value
I2C Inputs, 2 wires each	SCL±, SDA±
I2C Outputs, 2 wires each	BYP_SCL±, BYP_SDA±
I2C Bypass Switch Control	BYP_EN

When CRD5376 is used in a distributed measurement network, each node must have a unique address. This address is used to transmit individual configuration commands and tag the source of returned con-

version data. Address assignment can be either dynamic or static, depending how the telemetry system is to be implemented.

Dynamic address assignment uses daisy-chained I2C connections to assign an address to each measurement node. Once a node receives an address, it enables the I2C bypass switches to the next node so it can be assigned an address.

Static address assignment has a serial number assigned to each node during manufacturing. When placed in the network the location is recorded and a master list of serial numbers vs. location is maintained. Alternately, a location dependent serial number can be assigned during installation.

2.3.5 UART Connection

A UART connection on CRD5376 provides a low-speed standardized connection for telemetry solutions not using I2C. UART connections are provided for custom programming convenience only and are not directly supported by the CRD5376 PC evaluation software or microcontroller firmware.

Specification	Value
UART Connections, 2 wires each	TX/GND, RX/GND

2.3.6 External Connector

Power supplies and telemetry signals route to a 20-pin double row connector with 0.1" spacing (J8). This header provides a compact standardized connection to the CRD5376 external signals.

Pins	Name	Signal
1, 2	CLK+, CLK-	Clock Input
3, 4	SYNC+, SYNC-	Synchronization Input
5, 6	SCL+, SCL-	I2C Clock
7, 8	SDA+, SDA-	I2C Data
9, 10	BYP_SDA+, BYP_SDA-	I2C Data Bypass
11, 12	BYP_SCL+, BYP_SCL-	I2C Clock Bypass
13, 14	TX, GND	UART transmit
15, 16	RX, GND	UART receive
17, 18	-3.3V, GND	Negative Power Supply
19, 20	+3.3V, GND	Positive Power Supply

2.4 Power Supplies

Power is supplied to CRD5376 through the +3.3 V and -3.3 V voltage inputs on the external connector (J8), which are typically from an external AC-DC or DC-DC converter. Digital circuitry on CRD5376 is driven directly from the +3.3 V input, while linear regulators create +2.5 V and - 2.5 V analog power supplies from +3.3 V and -3.3 V.

The +3.3 V and -3.3 V power supply inputs have zener protection diodes that limit the maximum input voltages to +5 V or -5 V with respect to ground. Each input also has 100 uF bulk capacitance for bypassing and to help settle transients and another 0.01 uF capacitor to bypass high frequency noise.

2.4.1 Analog Voltage Regulators

Linear voltage regulators create the positive and negative analog power supply voltages to the analog components on CRD5376. These regulate the +3.3 V and -3.3 V power supply inputs to create the +2.5 V and -2.5 V analog power supplies.

Specification	Value
Positive Analog Power Supply	+2.5 V
Low Noise Micropower Regulator - Linear Tech	LT1962ES8-2.5
Surface Mount Package Type	MSOP-8
Load Regulation, -40 C to +85 C	+/- 25 mV
Quiescent Current, Current @ 100 mA Load	30 µA, 2 mA
Output Voltage Noise, 10 Hz - 100 kHz	20 μV_{RMS}
Ripple Rejection, DC - 200 Hz	> 60 dB

Specification	Value
Negative Analog Supply	-2.5 V
Low Noise Micropower Regulator - Linear Tech	LT1964ES5-BYP
Surface Mount Package Type	SOT-23
Load Regulation, -40 C to +85 C	+/- 30 mV
Quiescent Current, Current @ 100 mA Load	30 µA, 1.3 mA
Output Voltage Noise, 10 Hz - 100 kHz	20 μV_{RMS}
Ripple Rejection, DC - 200 Hz	> 45 dB

The +2.5 V and -2.5 V power supplies to the analog components on CRD5376 include reverse biased Schottkey diodes to ground to protect against reverse voltages that could latch-up the CMOS analog components. Also included on +2.5 V and -2.5 V are several 100 uF bulk capacitors for bypassing and to help settle transients plus individual 0.1 uF bypass capacitors local to the power supply pins of each device.

2.5 PCB Layout

2.5.1 Layer Stack

CRD5376 layer 1 is dedicated for analog and digital routing. Critical analog signal routes for channels 1 and 2 are on this layer. Some digital routes for the digital filter are also included on this layer away from the analog signal routes.

CRD5376 layer 2 is a solid ground plane without splits or routing. A solid ground plane provides the best return path for bypassed noise to leave the system. No separate analog ground is required since analog signals on CRD5376 are differentially routed.

CRD5376 layer 3 is dedicated for power supply routing. Each power supply net includes at least 100 µF bulk capacitance as a charge well for settling transient currents.

CRD5376 layer 4 is dedicated as a digital routing layer with ground fill.

CRD5376 layer 5 is a solid ground plane without splits or routing. A solid ground plane provides the best return path for bypassed noise to leave the system. No separate analog ground is required since analog signals on CRD5376 are differentially routed.

CRD5376 layer 6 is dedicated for analog and digital routing. Critical analog signal routes for channels 3 and 4 are on this layer. Some digital routes for the microcontroller are also included on this layer away from the analog signal routes.

2.5.2 Differential Pairs

Analog signal routes on CRD5376 are differential with dedicated + and - traces. All source and return analog signal currents are constrained to the differential pair route and do not return through the ground plane. Differential traces are routed together with a minimal gap between them so that noise events affect them equally and are rejected as common mode noise.

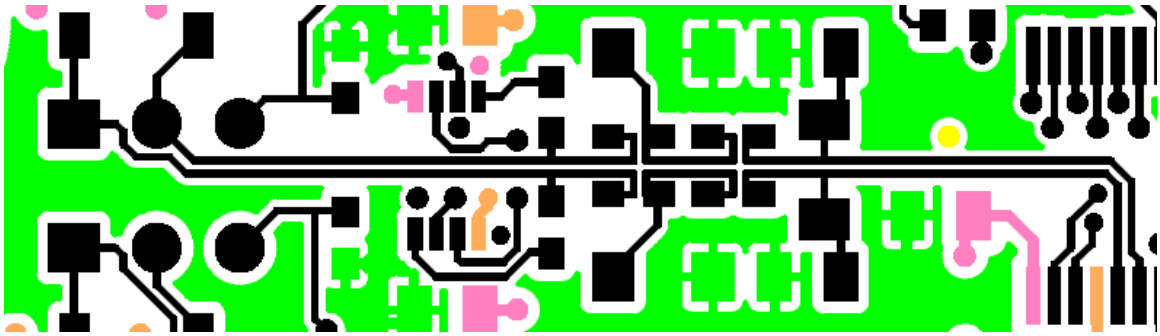


Figure 2. Differential Pair Routing

Analog signal connections into the CS3301/02 amplifiers are 2-wire IN+ and IN- differential pairs, and are routed as such. Analog signal connections out of the CS3301/02 amplifiers and into the CS5372 modulators are 4-wire INR+, INF+, INF-, INR- quad groups, and are routed with INF+ and INF- as a traditional differential pair and INR+ and INR- as guard traces outside the respective INF+ and INF- traces.

Figure 3. Quad Group Routing

2.5.3 Bypass Capacitors

Each device power supply pin includes 0.1 µF bypass capacitors placed as close as possible to the pin. Each power supply net includes at least 100 µF bulk capacitance as a charge well for transient current loads.

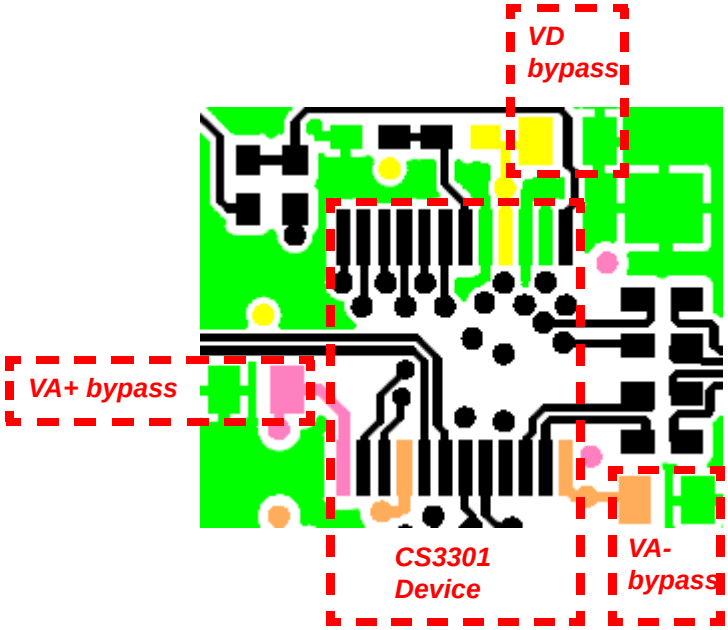
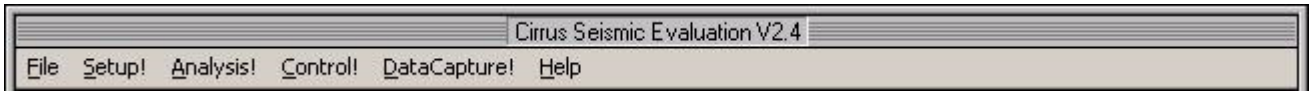


Figure 4. Bypass Capacitor Placement

3. SOFTWARE DESCRIPTION

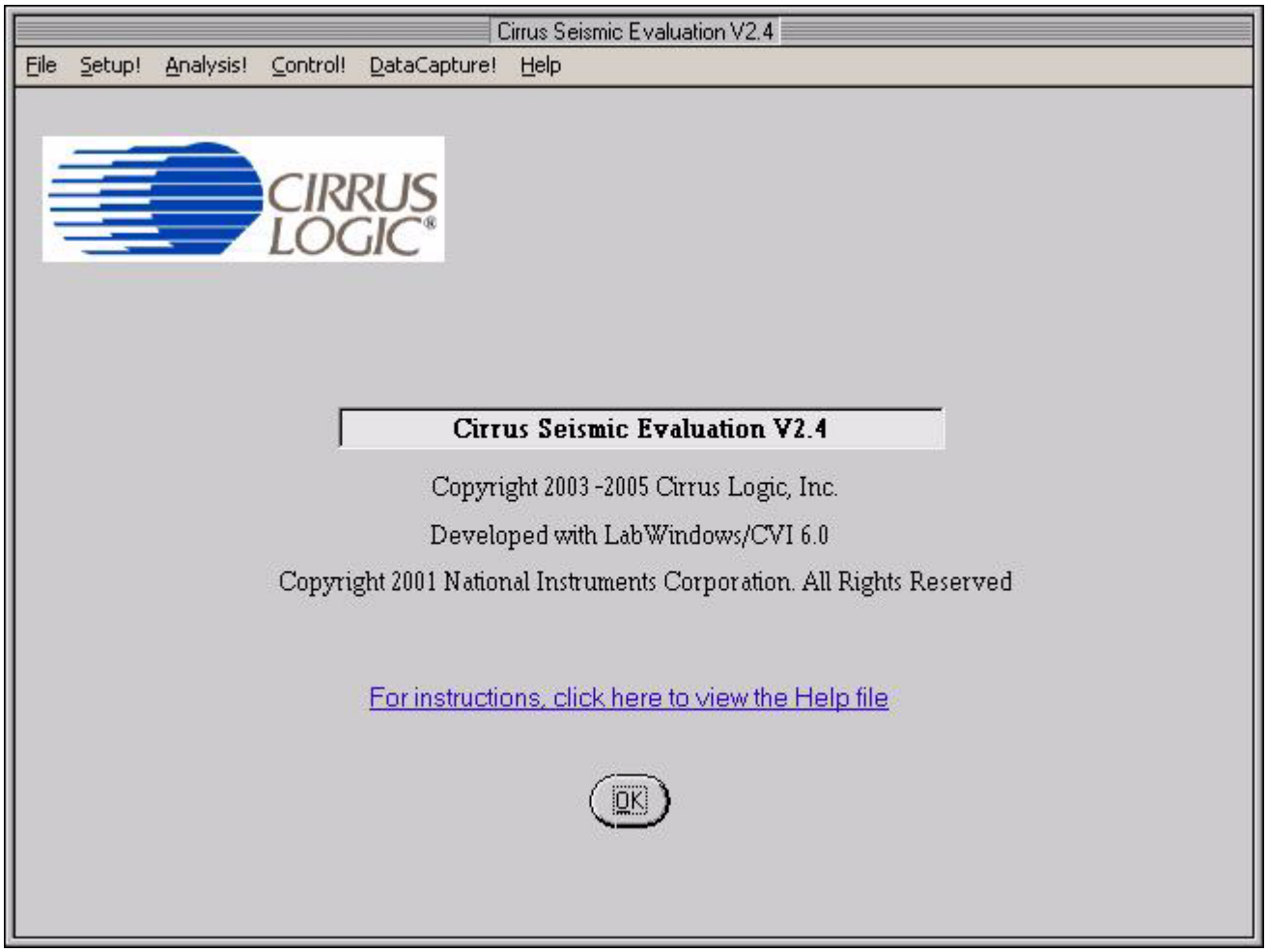
3.1 Menu Bar



The menu bar is always present at the top of the software panels and provides typical *File* and *Help* pull-down menus. The menu bar also selects the currently displayed panel.

Control	Description
File	
Load Data Set	Loads a data set from disk.
Save Data Set	Saves the current data set to disk.
Copy Panel to Clipboard	Copies a bitmap of the current panel to the clipboard.
Print Analysis Screen	Prints the full Analysis panel, including statistics fields.
Print Analysis Graph	Prints only the graph from the Analysis panel.
High Resolution Printing	Prints using the higher resolution of the printer.
Low Resolution Printing	Prints using the standard resolution of the screen.
Quit	Exits the application software.
Setup!	Displays the Setup Panel.
Analysis!	Displays the Analysis Panel.
Control!	Displays the Control Panel.
DataCapture!	Displays the Setup Panel and starts Data Capture.
Help	
Contents	Find help by topic.
Search for help on	Find help by keywords.
About	Displays the About Panel.

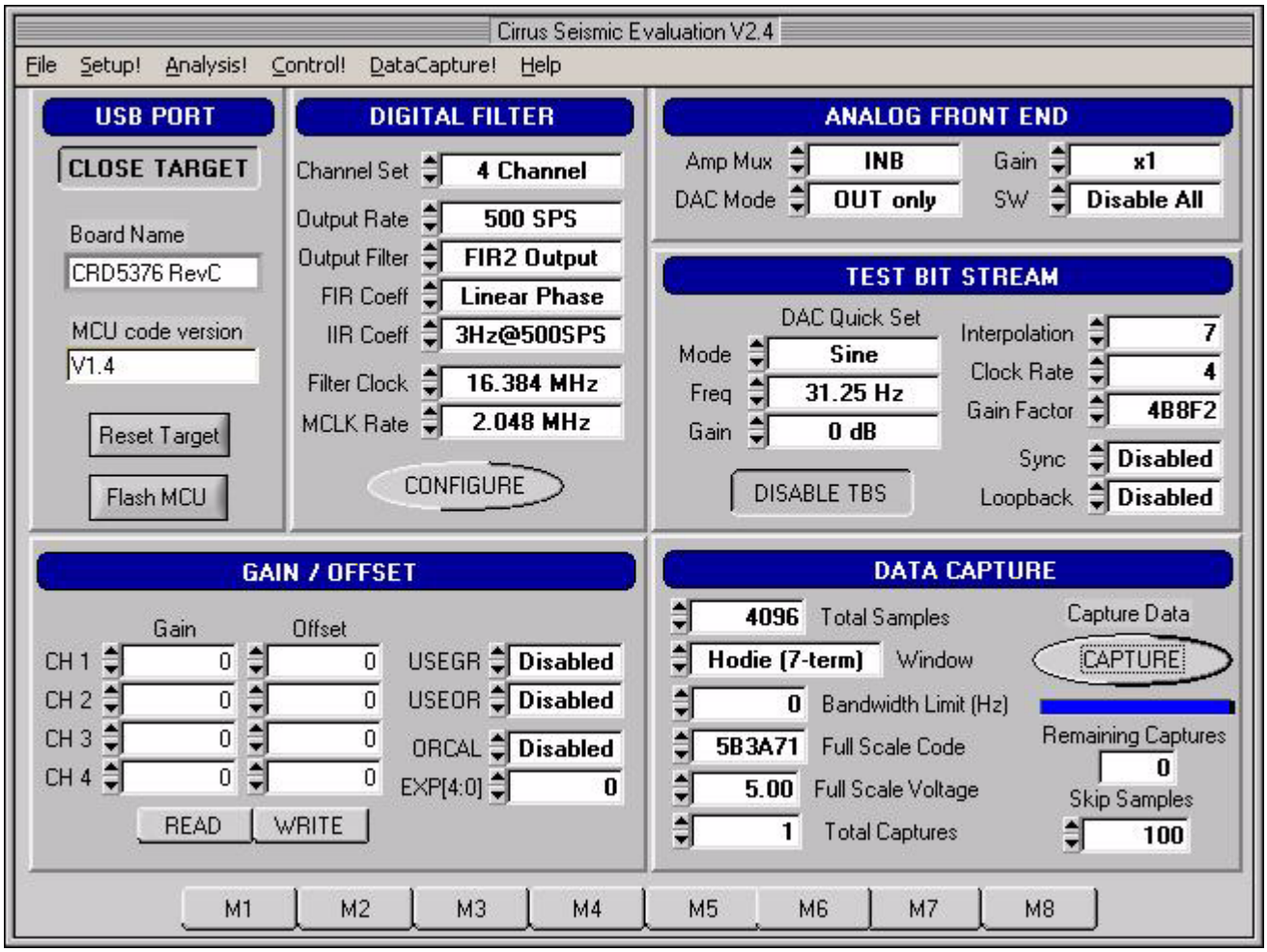
3.2 *About* Panel



The ***About*** panel displays copyright information for the Cirrus Seismic Evaluation software.

Click *OK* to exit this panel. Select *Help* ⇨ *About* from the menu bar to display this panel.

3.3 *Setup* Panel



The ***Setup*** panel initializes the evaluation system to perform data acquisition. It consists of the following sub-panels and controls.

- ***USB Port***
- ***Digital Filter***
- ***Analog Front End***
- ***Test Bit Stream***
- ***Gain/Offset***
- ***Data Capture***
- ***External Macros***

3.3.1 USB Port

The ***USB Port*** sub-panel sets up the USB communication interface between the PC and the target board.

Control	Description
Open Target	Open USB communication to the target board and read the board name and microcontroller firmware version. When communication is established, the name of this control changes to *'Close Target'* and ***Setup***, ***Analysis*** and ***Control*** panel access becomes available in the menu bar.
Close Target	Disconnects the previously established USB connection. On disconnection, this control changes to *'Open Target'* and the ***Setup***, ***Analysis*** and ***Control*** panel access becomes unavailable in the menu bar. The evaluation software constantly monitors the USB connection status and automatically disconnects if the target board is turned off or the USB cable is unplugged.
Board Name	Displays the type of target board currently connected.
MCU code version	Displays the version number of the microcontroller code on the connected target board.
Reset Target	Sends a software reset command to the target board.
Flash MCU	Programs the microcontroller code on the target board using the *.thx* file found in the *"C:\Program Files\Cirrus Seismic Evaluation"* directory. This feature permits reprogramming of the microcontroller (without using a hardware programmer) when a new version of the MCU code becomes available.

3.3.2 Digital Filter

The ***Digital Filter*** sub-panel sets up the digital filter configuration options.

By default the ***Digital Filter*** sub-panel configures the system to use on-chip coefficients and test bit stream data. The on-chip data can be overwritten by loading custom coefficients and test bit stream data from the ***Customize*** sub-panel on the ***Control*** panel.

Any changes made under this sub-panel will not be applied to the target board until the *Configure* button is pushed. The *Configure* button writes the new configuration to the target board and then enables the data *Capture* button.

Control	Description
Channel Set	Selects the number of channels that are enabled in the digital filter. For the CS5376A digital filter, from 1 to 4 channels can be enabled.
Output Rate	Selects the output word rate of the digital filter. Output word rates from 4000 SPS to 1 SPS (0.25 mS to 1 S) are available.
Output Filter	Selects the output filter stage from the digital filter. Sinc output, FIR1 output, FIR2 output, IIR 1st order output, IIR 2nd order output, or IIR 3rd order output can be selected. FIR2 output provides full decimation of the modulator data.
FIR Coeff	Selects the on-chip FIR coefficient set to use in the digital filter. Linear phase or minimum phase FIR coefficients can be selected.
IIR Coeff	Selects the on-chip IIR coefficient set to use in the digital filter. Coefficient sets producing a 3 Hz high-pass corner at 2000 SPS, 1000 SPS, 500 SPS, 333 SPS, and 250 SPS can be selected.
Filter Clock	Sets the digital filter internal clock rate. Lower internal clock rates can save power when using slow output word rates.
MCLK Rate	Sets the analog sample clock rate. The CS5372 modulators and CS4373A test DAC typically run with MCLK set to 2.048 MHz.
Configure	Writes all information from the ***Setup*** panel to the digital filter. The data *Capture* button becomes available once the configuration information is written to the target board.

3.3.3 Analog Front End

The ***Analog Front End*** sub-panel configures the amplifier, modulator, and test DAC pin options. Pin options are controlled through the GPIO outputs of the digital filter.

Any changes made under this sub-panel will not be applied to the target board until the *Configure* button is pushed. The *Configure* button writes the new configuration to the target board and then enables the data *Capture* button.

Control	Description
Amp Mux	Selects the input source for the CS3301/02 amplifiers. An internal termination, external INA inputs or external INB inputs can be selected.
DAC Mode	Selects the operational mode of the CS4373A test DAC. The test DAC operational modes are AC dual output (OUT&BUF), AC precision output (OUT only), AC buffered output (BUF only), DC common mode output (DC Common), DC differential output (DC Diff), or AC common mode output (AC Common). The test DAC can also be powered down (PWDN) when not in use to save power.
Gain	Sets the amplifier gain range and test DAC attenuation. Amplifier gain and DAC attenuation settings of 1x, 2x, 4x, 8x, 16x, 32x, or 64x can be selected and are controlled together.
Sw	Selects how the DAC_BUF to INA analog switches are enabled.

3.3.4 Test Bit Stream

The ***Test Bit Stream*** sub-panel configures test bit stream (TBS) generator parameters. The digitial filter data sheet describes TBS operation and options.

The *DAC Quick Set* controls automatically set the *Interpolation*, *Clock Rate*, and *Gain Factor* controls based on the selected *Mode*, *Freq*, and *Gain*. Additional configurations can be programmed by writing the *Interpolation*, *Clock Rate*, and *Gain Factor* controls manually.

Any changes made under this sub-panel will not be applied to the target board until the *Configure* button is pushed. The *Configure* button writes the new configuration to the target board and then enables the data *Capture* button.

Control	Description
DAC Quick Set	Automatically sets test bit stream options. *Mode* selects sine or impulse output mode, *Freq* selects the test signal frequency for sine mode, and *Gain* selects the test signal amplitude in dB.
Interpolation	Manual control for the data interpolation factor of the test bit stream generator.
Clock Rate	Manual control for the output clock and data rate of the test bit stream generator.
Gain Factor	Manual control to set the test bit stream signal amplitude.
Sync	Enables test bit stream synchronization by the MSYNC signal.
Loopback	Enables digital loopback from the test bit stream generator output to the digital filter input.

3.3.5 Gain/Offset

The ***Gain / Offset*** sub-panel controls the digital filter GAIN and OFFSET registers for each channel.

The OFFSET and GAIN registers can be manually written with any 24-bit 2's complement value from 0x800000 to 0x7FFFFF. The USEGR, USEOR, ORCAL, and EXP[4:0] values enable gain correction, offset correction, and offset calibration in the digital filter.

The offset calibration routine built into the digital filter is enabled by writing the ORCAL and EXP[4:0] bits. The EXP[4:0] value can range from 0x00 to 0x18 and represents an exponential shift of the calibration feedback, as described in the digital filter data sheet. Offset calibration results are automatically written to the OFFSET registers and remain there, even after offset calibration is disabled.

Control	Description
Gain	Displays the digital filter GAIN1 to GAIN4 registers.
Offset	Displays the digital filter OFFSET1 to OFFSET4 registers.
Read	Reads values from the GAIN and OFFSET registers.
Write	Writes values to the GAIN and OFFSET registers.
USEGR	Enables gain correction. When enabled, output samples are gained down by the value in the GAIN register.(Output = GAIN / 0x7FFFFF).
USEOR	Enables offset correction. When enabled, output samples are offset by the value in the OFFSET register. (Output = Sample - OFFSET).
ORCAL	Enables offset calibration using the exponent value from the EXP[4:0] control. Results are automatically written to the OFFSET registers as they are calculated.
EXP[4:0]	Sets the exponential value used by offset calibration.

3.3.6 Data Capture

The ***Data Capture*** sub-panel collects samples from the target board and sets analysis parameters.

When the *Capture* button is pressed, the requested number of samples are collected from the target board through the USB port and are split among the enabled channels. A four-channel system, for example, will collect (Total Samples / 4) samples per channel. The maximum number of samples that can be collected is 1,048,576 (1M). The number of samples per channel should be a power of two for the analysis FFT routines to work properly.

After data is collected, analysis is performed using the selected parameters and the results are displayed on the ***Analysis*** panel. The selected analysis *window*, *bandwidth limit*, *full scale code*, and *full scale voltage* parameters can be modified for the data set currently in memory and the analysis re-run by pressing the *REFRESH* button on the ***Analysis*** Panel.

Control	Description
Total Samples	Sets the total number of samples to be collected. Multichannel acquisitions split the requested number of samples among the channels. A maximum of 1,048,576 (1M) samples can be collected.
Window	Selects the type of analysis windowing function to be applied to the collected data set. Used to ensure proper analysis of discontinuous data sets.
Bandwidth Limit (Hz)	Sets the frequency range over which to perform analysis, used to exclude higher-frequency components. Default value of zero performs analysis for the full Nyquist frequency range.
Full Scale Code	Defines the maximum positive full-scale 24-bit code from the digital filter. Used during FFT noise analysis to set the 0 dB reference level.
Full Scale Voltage	Defines the maximum peak-to-peak input voltage for the nV/rtHz Spot Noise analysis.
Total Captures	Sets the number of data sets to be collected and averaged together in the FFT magnitude domain. The maximum number of data sets that can be averaged is 100.
Capture	Starts data collection from the target board through the USB port. After data collection, analysis is run using parameters from this sub-panel.
Remaining Captures	Indicates how many more data captures are remaining to complete the requested number of *Total Captures*. A zero value means that the current data capture is the last one.
Skip Samples	Sets the total number of samples to be skipped prior to data collection. A maximum of 64K samples can be skipped

3.3.7 External Macros

Macros are generated within the ***Macros*** sub-panel on the ***Control*** panel. Once a macro has been built it can either be saved with a unique macro name to be run within the ***Macros*** sub-panel, or saved as an external macro and be associated with one of the *External Macro* buttons.

A macro is saved as an *External Macro* by saving it in the *. /macros/* subdirectory using the name *'m1.mac'*, *'m2.mac'*, etc. Depending on the selected name the macro will be associated with the corresponding *External Macro* button *M1*, *M2*, etc.

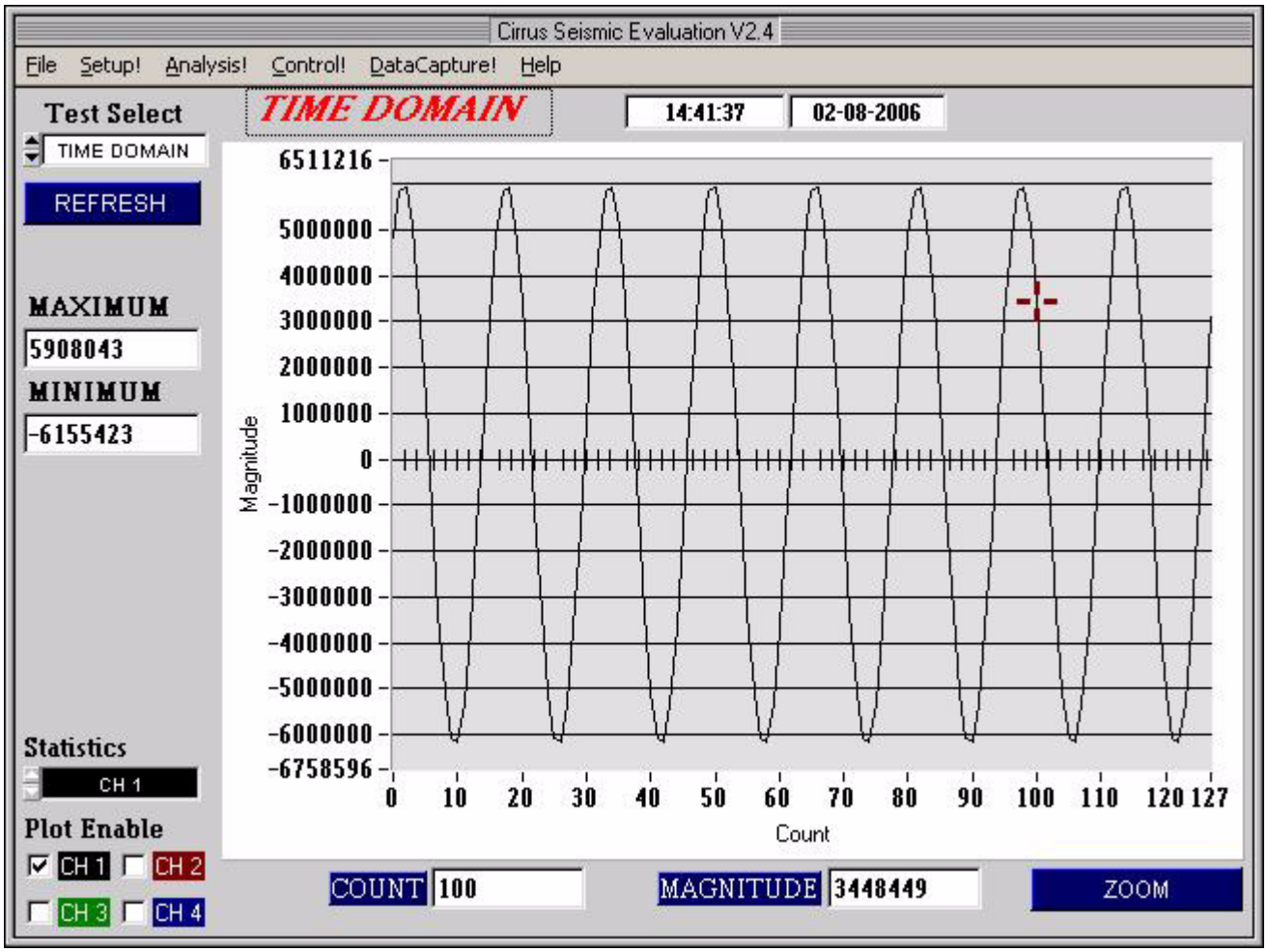
- M1 = . /macros/m1.mac
- M2 = . /macros/m2.mac
- etc.

External Macro buttons can be re-named on the panel by right clicking on them. The button name will change, but the macro associated with that button is always saved as '*m1.mac'*, *'m2.mac'*, etc., in the *. /macros/* subdirectory. The *External Macro* button names are stored in the file *'Mnames.txt'*, also in the *. /macros/* subdirectory.

*External Macro*s allow up to eight macros to be accessed quickly without having to load them into the ***Macros*** sub-panel on the ***Control*** panel. These *External Macro*s operate independently of the ***Macros*** sub-panel and are not affected by operations within it, except when a macro is saved to the *. /macros/* subdirectory to replace a currently existing *External Macro*.

Control	Description
M1 - M8	Runs the *External Macro* associated with that button.

3.4 *Analysis* Panel



The ***Analysis*** panel is used to display the analysis results on collected data. It consists of the following controls.

- ***Test Select***
- ***Statistics***
- ***Plot Enable***
- ***Cursor***
- ***Zoom***
- ***Refresh***
- ***Harmonics***
- ***Spot Noise***
- ***Plot Error***

3.4.1 Test Select

The *Test Select* control sets the type of analysis to be run on the collected data set.

Control	Description
Time Domain	Runs a min / max calculation on the collected data set and then plots sample data value vs. sample number.
Histogram	Runs a histogram calculation on the collected data set and then plots sample occurrence vs. sample value. Only valid for noise data since sine wave data varys over too many codes to plot as a histogram.
Signal FFT	Runs an FFT on the collected data set and then plots frequency magnitude vs. frequency. Statistics are calculated using the largest frequency bin as a full-scale signal reference.
Noise FFT	Runs an FFT on the collected data set and then plots frequency magnitude vs. frequency. Statistics are calculated using a simulated full-scale signal as a full-scale signal reference.
Phase	Runs an FFT on the collected data set and then plots phase vs. frequency. Limited usefulness for real collected data since noise has random phase.

3.4.2 Statistics

The *Statistics* control displays calculated statistics for the selected analysis channel. For multichannel data captures, only one channel of calculated statistics are displayed at a time and is selected using the *Statistics* channel control.

Errors that affect statistical calculations will cause the *Plot Error* control to appear. Information about errors on specific channels can be accessed by enabling the plot of the channel using the *Plot Enable* control and then accessing the *Plot Error* controls.

Control	Description
Time Domain	
Max	Maximum code of collected data set.
Min	Minimum code of collected data set.
Histogram	
Max	Maximum code of collected data set.
Min	Minimum code of collected data set.
Mean	Mean of collected data set.
Std Dev	Standard Deviation of collected data set.
Variance	Variance of collected data set.
Signal FFT	
S/N	Signal to Noise of calculated FFT.
S/PN	Signal to Peak Noise of calculated FFT.
S/D	Signal to Distortion of calculated FFT.
S/N+D	Signal to Noise plus Distortion of calculated FFT.
# of bins	Number of Bins covering the Nyquist frequency.
Noise FFT	
S/N	Signal to Noise of calculated FFT.
S/PN	Signal to Peak Noise of calculated FFT.
Spot Noise dB	Spot Noise in dB/Hz of calculated FFT.
Spot Noise nV	Spot Noise in nV/rtHz of calculated FFT.
# of bins	Number of Bins covering the Nyquist frequency.
Phase	
	No statistics are calculated.

3.4.3 Plot Enable

The *Plot Enable* control selects which channels are plotted for the current analysis. Multichannel plots are overlay plots with the highest number channel displayed as the top most plot. Only channels enabled by the *Plot Enable* control will report analysis error codes. Information about error codes can be accessed through the *Plot Error* controls.

3.4.4 Cursor

The *Cursor* control is used to identify a point on the graph using the mouse and then display its plot values. When any point within the plot area of the graph is clicked, the *Cursor* will snap to the closest plotted point and the plot values for that point display below the graph.

When using the *Zoom* function, the *Cursor* is used to select the corners of the area to zoom.

3.4.5 Zoom

The *ZOOM* function allows an area on the graph to be expanded.

To use the zoom function, click the *ZOOM* button and select the box corners of the area on the graph to expand. The graph will then expand to show the details of this area, and the plot axes will be re-scaled. While zoomed, you can zoom in farther by repeating the process.

To restore the graph to its original scale, click the *RESTORE* button that appears while zoomed. If multiple zooms have been initiated, the *RESTORE* button will return to the previously viewed plot scale. Repeated *RESTORE* will eventually return to the original plot scale. From within multiple zooms the original scale can be directly restored by clicking the *REFRESH* button.

3.4.6 Refresh

The *REFRESH* button will clear and re-plot the current data set. *Refresh* can be used to apply new analysis parameters from the ***Data Capture*** sub-panel, or to restore a *ZOOM* graph to its default plot scale.

3.4.7 Harmonics

The *HARMONICS* control is only visible during a Signal FFT analysis and highlights the fundamental and harmonic bins used to calculate the Signal FFT statistics. *HARMONICS* highlighting helps to understand the source of any Signal FFT plot errors.

3.4.8 Spot Noise

The *Spot Noise* control (labeled *dB* or *nV*) is only visible during a Noise FFT analysis and selects the units used for plotting the graph, either dB/Hz or nV/rtHz. The dB/Hz plot applies the *Full Scale Code* value from the ***Data Capture*** sub-panel on the ***Setup*** panel to determine the 0 dB point of the dB axis. The nV/rtHz plot applies the *Full Scale Voltage* value from the ***Data Capture*** sub-panel on the ***Setup*** panel to determine the absolute scaling of the nV axis.

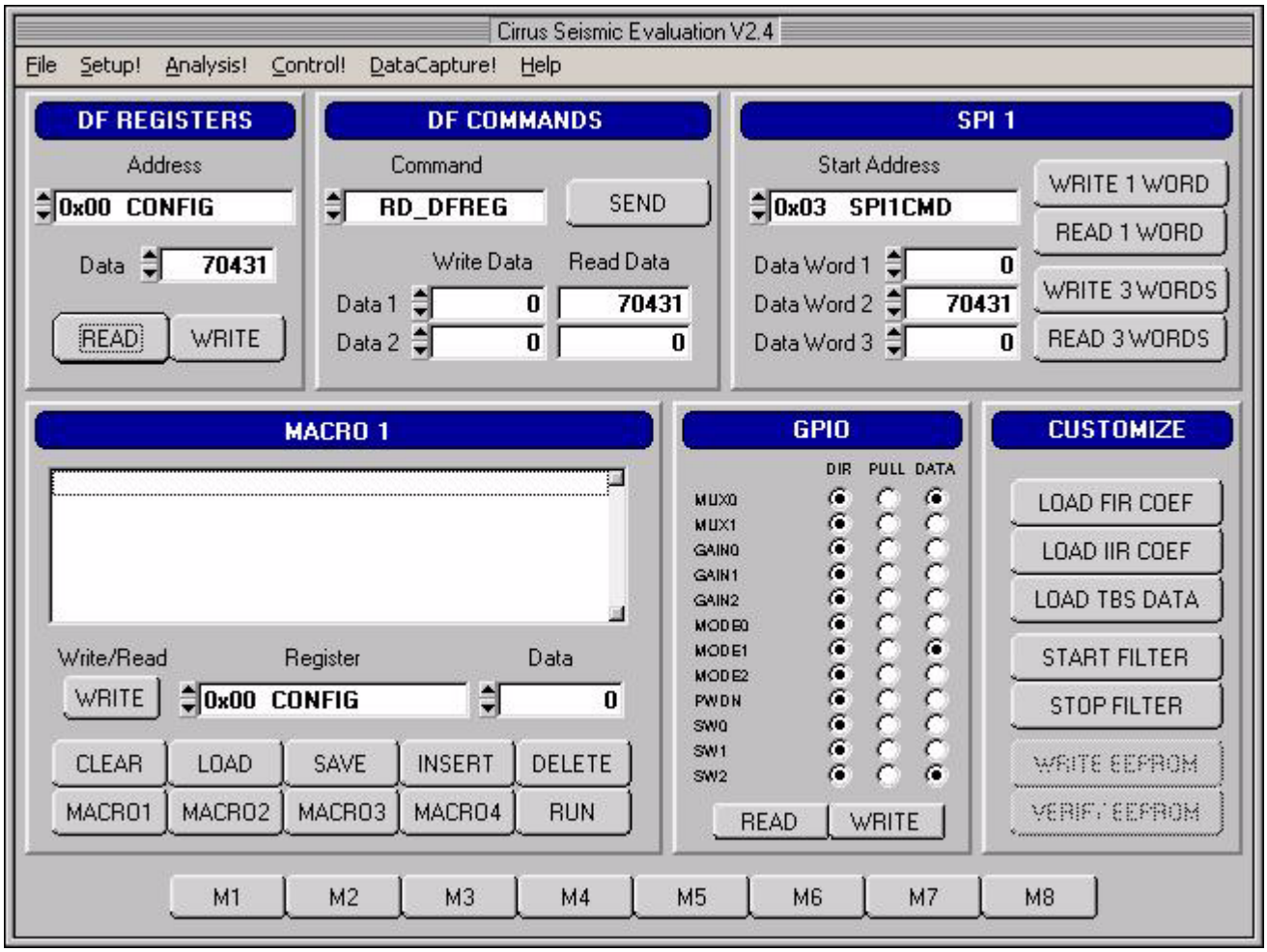
3.4.9 Plot Error

The *PLOT ERROR* control provides information about errors that occured during an analysis. Analysis errors are only reported if the channel that has the error is currently plotted.

An analysis error stores an error code in the numerical display box of the *PLOT ERROR* control. If more than one error occurs, all error codes are stored and the last error code is displayed. Any of the accumulated error codes can be displayed by clicking on the numerical box and selecting it.

Once an error code is displayed in the numerical box, a description can be displayed by clicking the *PLOT ERROR* button. This causes a dialog box to display showing the error number, the error channel, and a text error message.

3.5 *Control* Panel



The ***Control*** panel is used to write and read register settings and to send commands to the digital filter. It consists of the following sub-panels and controls.

- ***DF Registers***
- ***DF Commands***
- ***SPI1***
- ***Macros***
- ***GPIO***
- ***Customize***
- ***External Macros***

3.5.1 DF Registers

The ***DF Registers*** sub-panel writes and reads registers within the digital filter. Digital filter registers control operation of the digital filter and the included hardware peripherals, as described in the digital filter data sheet.

Control	Description
Address	Selects a digital filter register.
Data	Contains the data written to or read from the register.
Read	Initiates a register read.
Write	Initiates a register write.

3.5.2 DF Commands

The ***DF Commands*** sub-panel sends commands to the digital filter. The digital filter commands and their required parameters are described in the digital filter data sheet.

Not all commands require write data values, and not all commands will return read data values. Some commands require formatted data files for uploading custom coefficients or test bit stream data Example formatted data files are included in the SPI sub-directory of the software installation.

Control	Description
Command	Selects the command to be written to the digital filter.
Write Data 1	Contains the SPI1DAT1 data to be written to the digital filter.
Write Data 2	Contains the SPI1DAT2 data to be written to the digital filter.
Read Data 1	Contains the SPI1DAT1 data read from the digital filter.
Read Data 2	Contains the SPI1DAT2 data read from the digital filter.
Send	Initiates the digital filter command.

3.5.3 SPI

The ***SPI*** sub-panel writes and reads registers in the digital filter SPI register space. They can be used to check the SPI serial port status bits or to manually write commands to the digital filter.

Control	Description
Start Address	Selects the address to begin the SPI transaction.
Data Word 1	Contains the first data word written to or read from the SPI registers.
Data Word 2	Contains the second data word written to or read from the SPI registers.
Data Word 3	Contains the third data word written to or read from the SPI registers.
Read 1 Word	Initiates a 1 word SPI read transaction.
Read 3 Words	Initiates a 3 word SPI read transaction.
Write 1 Word	Initiates a 1 word SPI write transaction.
Write 3 Words	Initiates a 3 word SPI write transaction.

3.5.4 Macros

The ***Macros*** sub-panel is designed to write a large number of registers with a single command. This allows the target evaluation system to be quickly set into a specific state for testing.

The *Register* control gives access to both digital filter registers and SPI1 registers. These registers can be written with data from the *Data* control, or data can be read and output to a text window. The *Register* control can also select special commands to be executed, with the *Data* control used to define a parameter value for the special command, if necessary.

Control	Description
Write / Read	Selects the type of operation to be performed by the inserted macro command.
Register	Selects the target register for the inserted macro command. Also selects special commands that can be performed.
Data	Sets the register data value for the inserted macro command. Also sets the parameter value for special commands.
Clear	Clears the currently displayed macro.
Load	Loads a previously saved macro.
Save	Saves the currently displayed macro. Macros can be saved with unique names or can be saved as *External Macros*.
Insert	Inserts a macro command at the selected macro line. The macro command is built from the *Write/Read*, *Register*, and *Data* controls.
Delete	Deletes the macro command at the selected macro line.
Macro1 - Macro4	Selects which of the four working macros is displayed.
Run	Runs the currently displayed working macro.

3.5.5 GPIO

The ***GPIO*** sub-panel controls the digital filter GPIO pin configurations. GPIO pins have dedicated functions on the target board, but can be used in any manner for custom designs.

Control	Description
Direction	Sets the selected GPIO pin as an output (*) or input ( ).
Pull Up	Turns the pull up resistor for the selected GPIO pin on (*) or off ( ).
Data	Sets the selected output GPIO pin to a high (*) or low ( ) level.
Write	Initiates a write to GPIO registers.The *Direction*, *Pull Up* and *Data* controls are read to determine the register values to be written.
Read	Initiates a read from GPIO registers.The *Direction*, *Pull Up* and *Data* controls are updated based on the register values that are read.

3.5.6 Customize

The ***Customize*** sub-panel sends commands to upload custom FIR and IIR filter coefficients, upload custom test bit stream data, start the digital filter, stop the digital filter, and write/read custom EEPROM configuration files to the on-board boot EEPROM. Example data files are included in a sub-directory of the software installation.

Control	Description
Load FIR Coef	Write a set of FIR coefficients into the digital filter from a file.
Load IIR Coef	Write a set of IIR coefficients into the digital filter from a file.
Load TBS Data	Write a set of test bit stream data into the digital filter from a file.
Start Filter	Enables the digital filter by sending the *Start Filter* command.
Stop Filter	Disables the digital filter by sending the *Stop Filter* command.
Write EEPROM	Writes an EEPROM boot configuration file to the EEPROM memory.
Verify EEPROM	Verifies EEPROM memory against an EEPROM boot configuration file.

3.5.7 External Macros

Macros are generated within the ***Macros*** sub-panel on the ***Control*** panel. Once a macro has been built it can either be saved with a unique macro name to be run within the ***Macros*** sub-panel, or saved as an external macro and be associated with one of the *External Macro* buttons.

A macro is saved as an *External Macro* by saving it in the *. /macros/* subdirectory using the name *'m1.mac'*, *'m2.mac'*, etc. Depending on the selected name the macro will be associated with the corresponding *External Macro* button *M1*, *M2*, etc.

- M1 = . /macros/m1.mac
- M2 = . /macros/m2.mac
- etc.

External Macro buttons can be re-named on the panel by right clicking on them. The button name will change, but the macro associated with that button is always saved as *'m1.mac'*, *'m2.mac'*, etc., in the *. /macros/* subdirectory. The *External Macro* button names are stored in the file *'Mnames.txt'*, also in the *. /macros/* subdirectory.

*External Macro*s allow up to eight macros to be accessed quickly without having to load them into the ***Macros*** sub-panel on the ***Control*** panel. These *External Macro*s operate independently of the ***Macros*** sub-panel and are not affected by operations within it, except when a macro is saved to the *. /macros/* subdirectory to replace a currently existing *External Macro*.

Control	Description
M1 - M8	Runs the *External Macro* associated with that button.

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Item	Cirrus P/N	Rev	Description	Qty	Reference Designator	MFG	MFG P/N	Notes
1	001-04076-Z1	A	CAP 0.01uF ±10% 50V NPb X7R 0805	4	C1 C2 C13 C14	KEMET	C0805C103K5RAC	
2	001-04345-01	A	CAP 0.1uF ±10% 50V X7R 0805	71	C3 C6 C8 C9 C11 C12 C15 C18 C19 C20 C27 C28 C29 C30 C31 C32 C33 C34 C35 C36 C37 C38 C39 C40 C41 C42 C48 C56 C57 C58 C59 C60 C61 C62 C63 C64 C65 C66 C67 C68 C69 C71 C72 C76 C77 C78 C81 C82 C83 C84 C85 C87 C88 C89 C90 C91 C92 C93 C94 C99 C100 C101 C103 C104 C105 C106 C107 C108 C109 C110 C113	KEMET	C0805C104K5RAC	
3	004-00102-01	A	CAP 100uF ±10% 16V TANT CASE D	11	C4 C5 C22 C23 C51 C53 C54 C79 C102 C112 C114	KEMET	T491D107K016AS	
4	001-06603-01	A	CAP 0.01uF ±5% 25V C0G 1206	27	C7 C10 C16 C17 C21 C24 C25 C26 C43 C44 C45 C46 C47 C49 C50 C52 C55 C70 C73 C74 C75 C80 C86 C95 C96 C97 C98	KEMET	C1206C103J3GAC	
5	004-00068-Z1	A	CAP 4.7uF ±10% 10V NPb TANT CASE A	1	C111	KEMET	T491A475K010AS	
6	070-00010-01	A	DIODE SCHTKY BARRIER 30V 0.2A SOT23	2	D1 D2	PHILIPS SEMICONDUCTORS	BAT54	
7	070-00024-01	A	DIODE SWT 70V 215mA SOT-23	8	D3 D4 D5 D6 D7 D8 D9 D10	ON SEMI	BAV99LT1	
8	115-00009-01	A	HDR 3x1 ML .1"CTR 062BD ST GLD TH	4	J1 J2 J7 J16	SAMTEC	TSW-103-07-G-S	
9	110-00263-Z1	A	CON USB RCPT RA 5POS MINI-B NPb TH	1	J3	MOLEX	54819-0519	ECO333
10	115-00003-01	A	HDR 5x2 MLE .1"CTR S GLD	1	J5	SAMTEC	TSW-105-07-G-D	
11	115-00013-01	A	HDR 2x2 MLE .1"CTR .062BD S GLD	0	J6	SAMTEC	TSW-102-07-G-D	DO NOT POPULATE
12	115-00011-01	A	HDR 10x2 ML .1"CTR 062BD ST GLD TH	1	J8	SAMTEC	TSW-110-07-G-D	
13	020-01016-01	A	RES 1k OHM 1/10W ±1% 0603 FILM	10	R1 R2 R43 R44 R90 R91 R98 R99 R102 R103	DALE	CRCW06031001F	
14	020-00934-01	A	RES 200 OHM 1/10W ±1% 0603 FILM	19	R3 R4 R5 R6 R7 R8 R21 R22 R24 R25 R26 R29 R30 R54 R55 R62 R63 R66 R79	DALE	CRCW06032000F	
15	020-01130-Z1	A	RES 10k OHM 1/10W ±1% NPb 0603 FILM	17	R9 R10 R11 R14 R15 R17 R27 R32 R33 R36 R37 R38 R39 R40 R41 R42 R45	DALE	CRCW060310K0FKEA	
16	020-00788-01	A	RES 10 OHM 1/10W ±1% 0603 FILM	9	R12 R13 R19 R20 R34 R35 R48 R49 R85	DALE	CRCW0603310R0F	
17	020-00673-Z1	A	RES 0 OHM 1/10W ±5% NPb 0603 FILM	43	R16 R52 R59 R61 R71 R72 R74 R76 R77 R81 R84 R86 R89 R92 R94 R97 R111 R113 R115 R117 R118 R120 R122 R124 R127 R128 R131 R101 R104 R105 R133 R134 R135 R136 R137 R138 R139 R140 R141 R142 R143 R144 R145	DALE	CRCW0603000Z0EA	
18	000-00000-02	A	NO POP RES 0603	0	R18 R46 R47 R50 R51 R53 R58 R60 R68 R70 R73 R75 R78 R80 R82 R83 R87 R88 R93 R95 R96 R100 R110 R112 R114 R116 R119 R121 R123 R125 R126 R129 R130 R132	NO POP	NP-RES-0603	DO NOT POPULATE
19	020-01962-01	A	RES 20k OHM 1/8W ±1% 0805 FILM	4	R23 R28 R64 R65	DALE	CRCW08052002F	
20	020-01128-01	A	RES 9.53k OHM 1/10W ±1% 0603 FILM	1	R31	DALE	CRCW06039531F	
21	021-01391-01	A	RES 18M OHM 1/8W ±5% 0805	4	R56 R57 R67 R69	PANASONIC	ERJ6GEYK186V	
22	020-02949-01	A	RES 825k OHM 1/8W ±1% 1206 FILM	4	R106 R107 R108 R109	DALE	CRCW12068253F	
23	060-00195-01	A	IC LOW V DUAL SPST ANA SWITCH MSOP8	6	U1 U27 U28 U30 U31 U32	VISHAY	DG2003DQ	
24	065-00051-01	C	IC CRUS, 24 SSOP DIDO AMP	2	U2 U16	CIRRUS LOGIC	CS3301-IS\C	
25	065-00052-01	C	IC CRUS, 24 SSOP DIDO AMP	2	U3 U33	CIRRUS LOGIC	CS3302-IS\C	
26	061-00152-01	A	IC LOG DUAL 2-IN POS OR-GATE SSOP8	4	U4 U17 U19 U20	TEXAS INSTRUMENTS	SN74LVC2G32DCTR	
27	061-00061-01	A	IC LOG, LITTLE LOG 2IN XOR SOT-23-5	1	U5	TEXAS INSTRUMENTS	SN74LVC1G86DBVR	
28	061-00062-01	A	IC LOG, LITTLE LOG SNGLE D-FF SSOP8	5	U6 U11 U12 U14 U15	TEXAS INSTRUMENTS	SN74LVC2G74DCTR	
29	060-00175-01	A	IC 1.25MHz R-TO-R OP AMP SOT-23	1	U7	LINEAR TECH	LT1783IS5	
30	062-00079-01	A	IC PGM USB 16kB FLASH MCU LQFP32	1	U8	CYGNAL	C8051F320	
31	060-00163-01	A	IC LNR 300mA LNOISE LDO REG MSOP8	1	U9	LINEAR TECH	LT1962EMS8-2.5	
32	060-00063-01	A	IC LNR, V REG 200mA NEG ADJ SOT23-5	1	U10	LINEAR TECH	LT1964ES5-BYP	
33	061-00153-01	A	IC LOG CMOS ANA MUX / DEMUX TSSOP16	1	U13	TEXAS INSTRUMENTS	CD74HC4051PWR	
34	065-00056-01	A	IC CRUS, QUAD DIG FILTER, TQFP64	1	U18	CIRRUS LOGIC	CS5376A-IQ\A	
35	060-00162-01	A	IC 3.3V U LOW PWR RS485 XCVR SOIC8	4	U22 U23 U25 U26	LINEAR TECH	LTC1480IS8	
36	065-00174-Z1	G	IC CRUS, DUAL MODULATOR SSOP24 Npb	2	U24 U29	CIRRUS LOGIC	CS5372-BSZ\G	
37	060-00236-01	A	IC LNR PRC V REF 2.5V TC10 SO8-150	1	U35	LINEAR TECH	LT1019AIS8-2.5	
38	065-00173-Z1	D	IC CRUS, TEST DAC SSOP28 Npb	1	U45	CIRRUS LOGIC	CS4373-ISZ\D	

CIRRUS LOGIC
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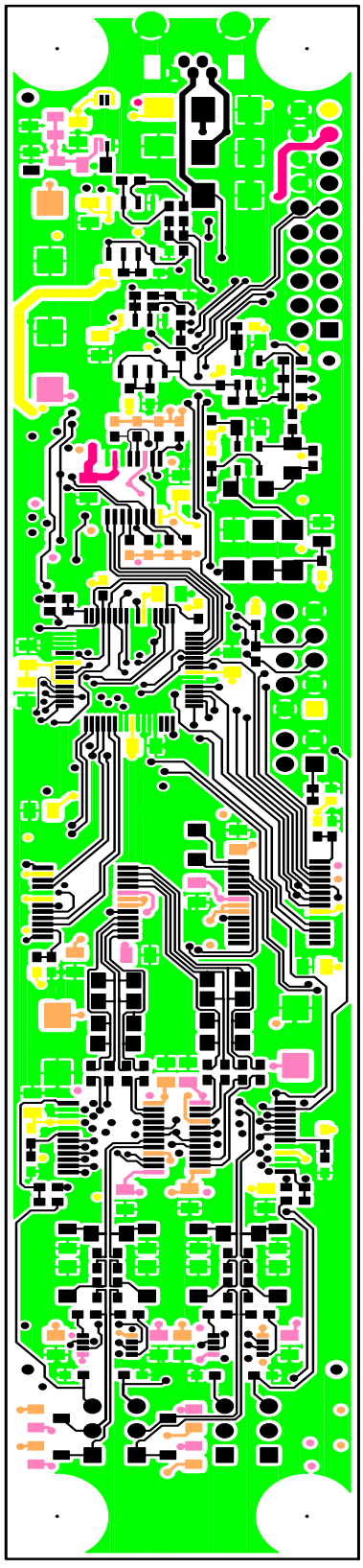
BILL OF MATERIAL

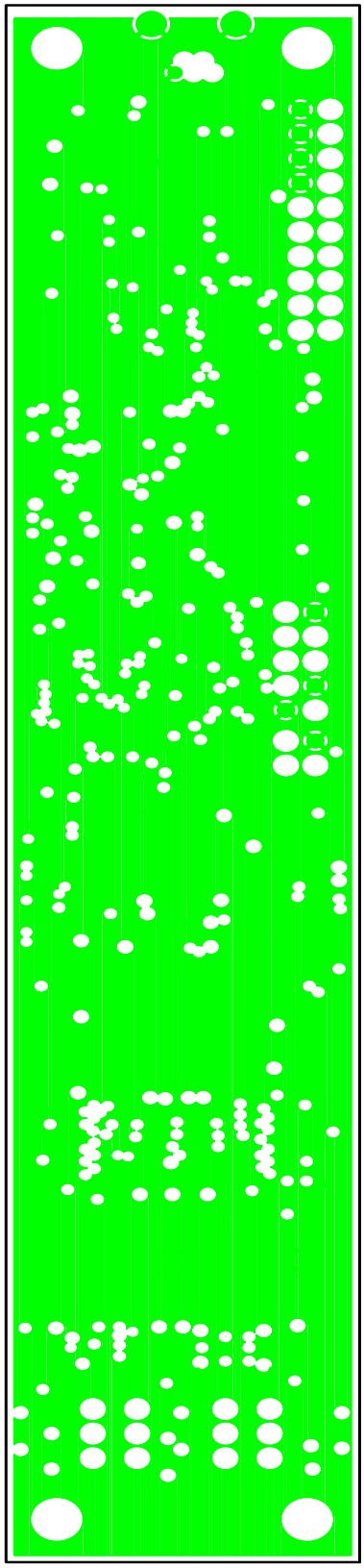
Item	Cirrus P/N	Rev	Description	Qty	Reference Designator	MFG	MFG P/N	Notes
39	304-00004-01	A	SPCR STANDOFF 4-40 THR .500"L	4	X1 X2 X3 X4	KEYSTONE	2203	REQUIRES 4-40- PAN HEAD SCREW
40	102-00017-02	A	OSC 32.768MHz 90ppm 3.3V V CNTL SMT	1	Y1	CITIZEN	CSX750VBEL32.768MTR	
41	070-00053-01	A	DIODE ZENER TR SUP 5V 600W PK SM	2	Z1 Z2	ON SEMICONDUCTOR	1SMB5.0AT3	
42	070-00050-01	A	DIODE 24W 40W PEAK PWR DUAL SOT-23	2	Z3 Z4	DIODES INC	MMBZ5V6AL-7	
43	600-00085-01	C4	SCHEM CRD5376	REF		CIRRUS LOGIC	600-00085-01	
44	240-00085-01	C	PCB CRD5376	1		CIRRUS LOGIC	240-00085-01	
45	603-00085-01	C	ASSY DWG PWA CRD5376	REF		CIRRUS LOGIC	603-00085-01	
47	300-00001-01	A	SCREW 4-40X5/16" PH STEEL	4		BUILDING FASTERNERS	PMS 440 0031 PH	USED TO INSTALL X1,X2,X3,X4
48	070-00053-01	A	DIODE ZENER TR SUP 5V 600W PK SM	0	Z5 Z6 Z7	ON SEMICONDUCTOR	1SMB5.0AT3	DO NOT POPULATE

5. LAYER PLOTS



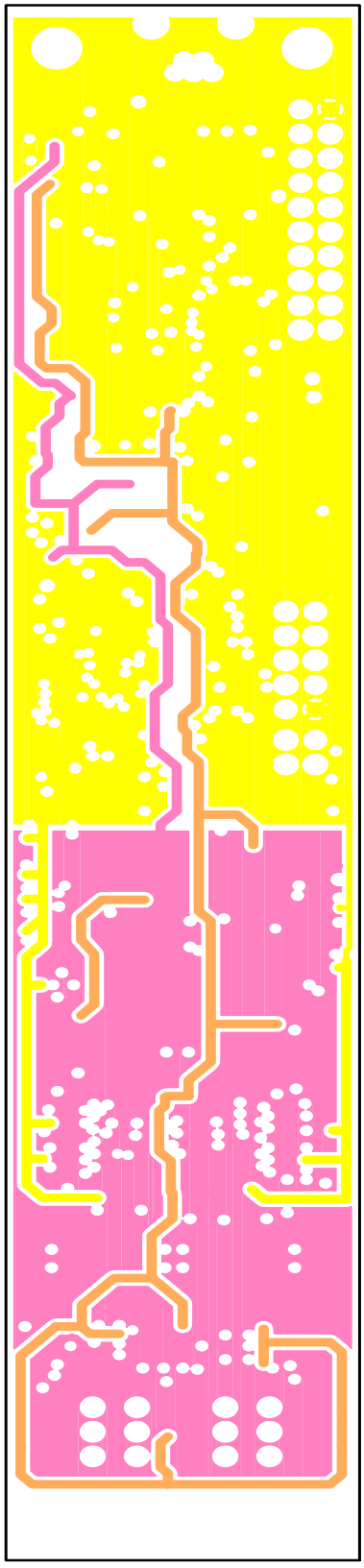
CRD5376 (240-00085-01 REV_C

TOP SIDE



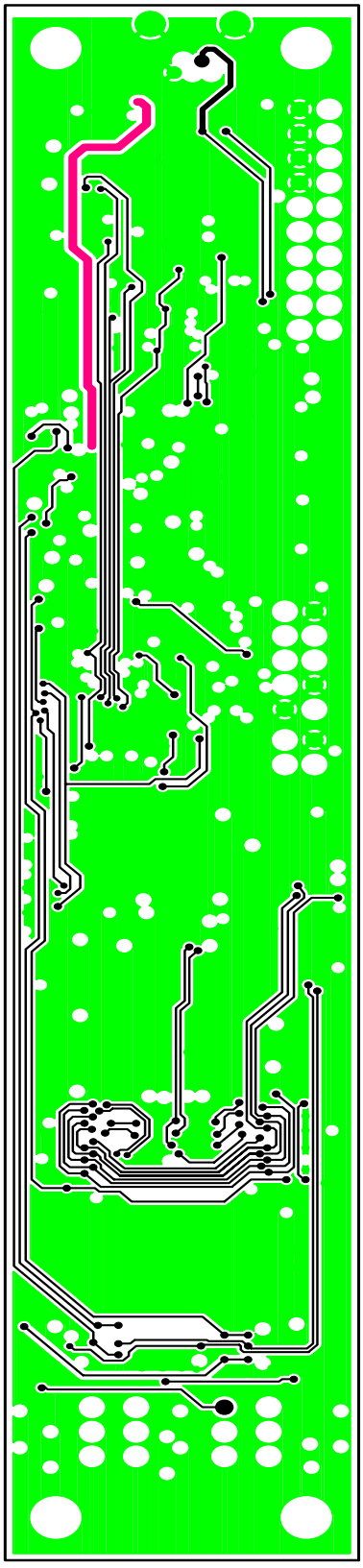
CRD5376 (240-00085-01 REV_C

LAYER2 GND PLANE



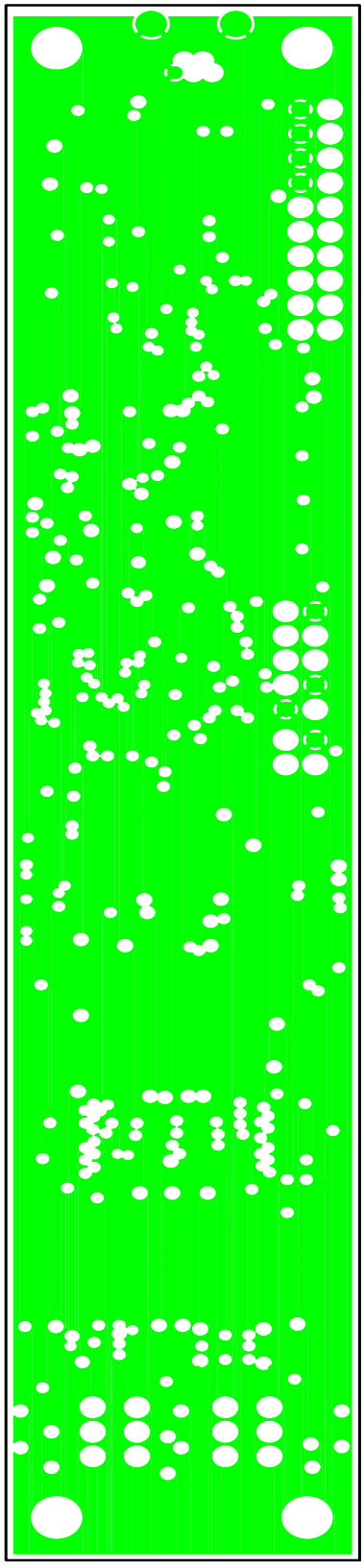
CRD5376 (240-00085-01 REV_C

LAYER3 PWR PLANE



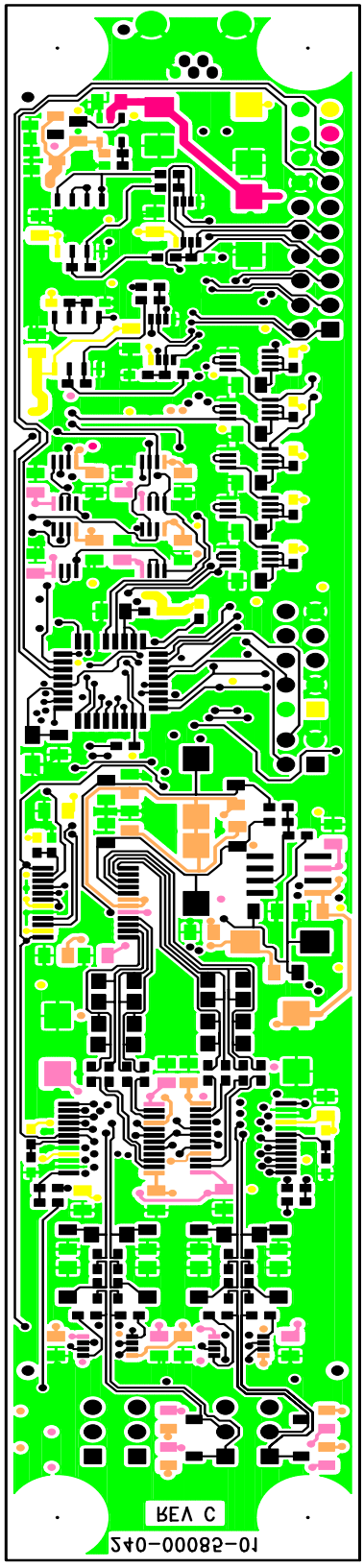
CRD5376 (240-00085-01 REV_C

LAYER4



CRD5376 (240-00085-01 REV_C

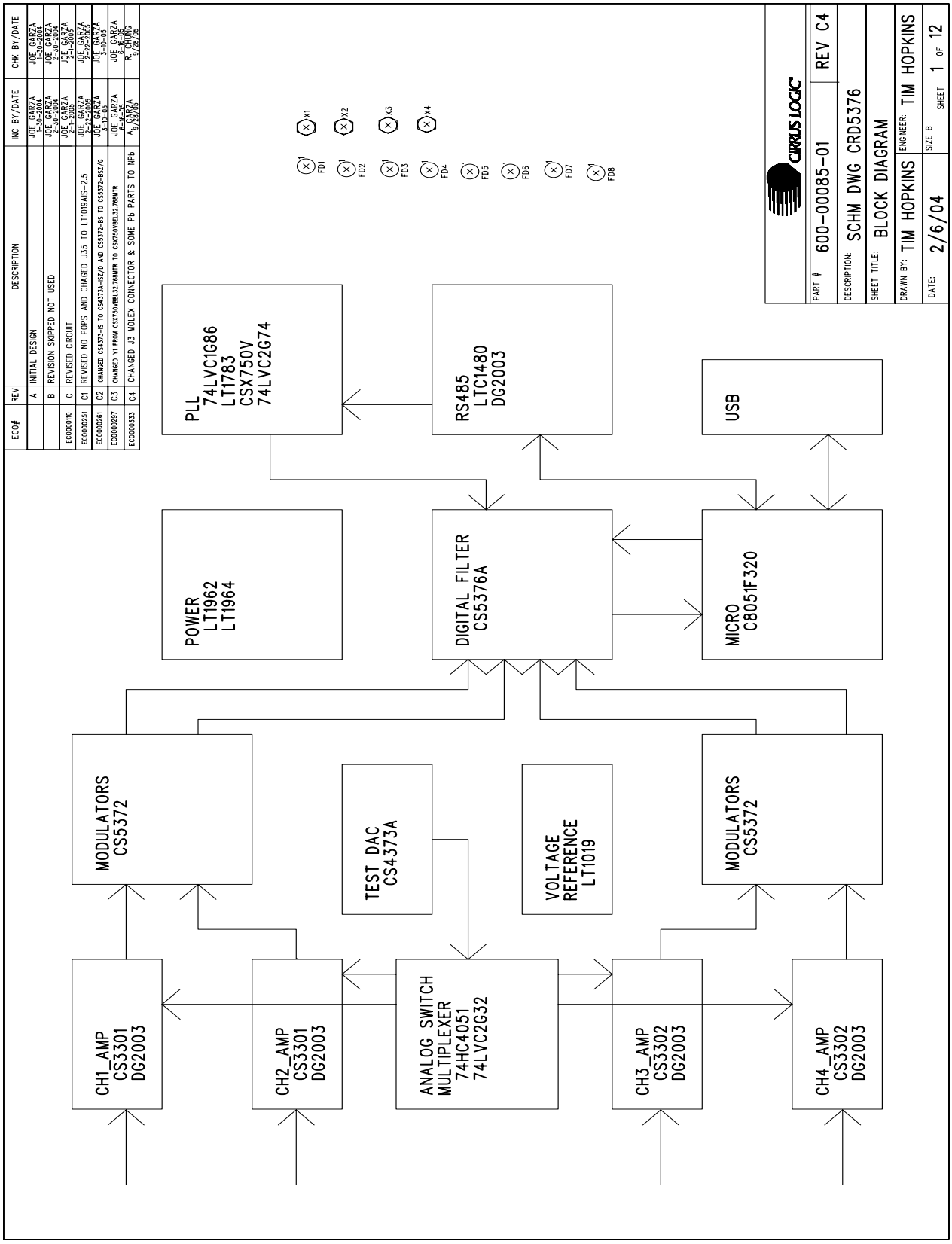
LAYER5 GND

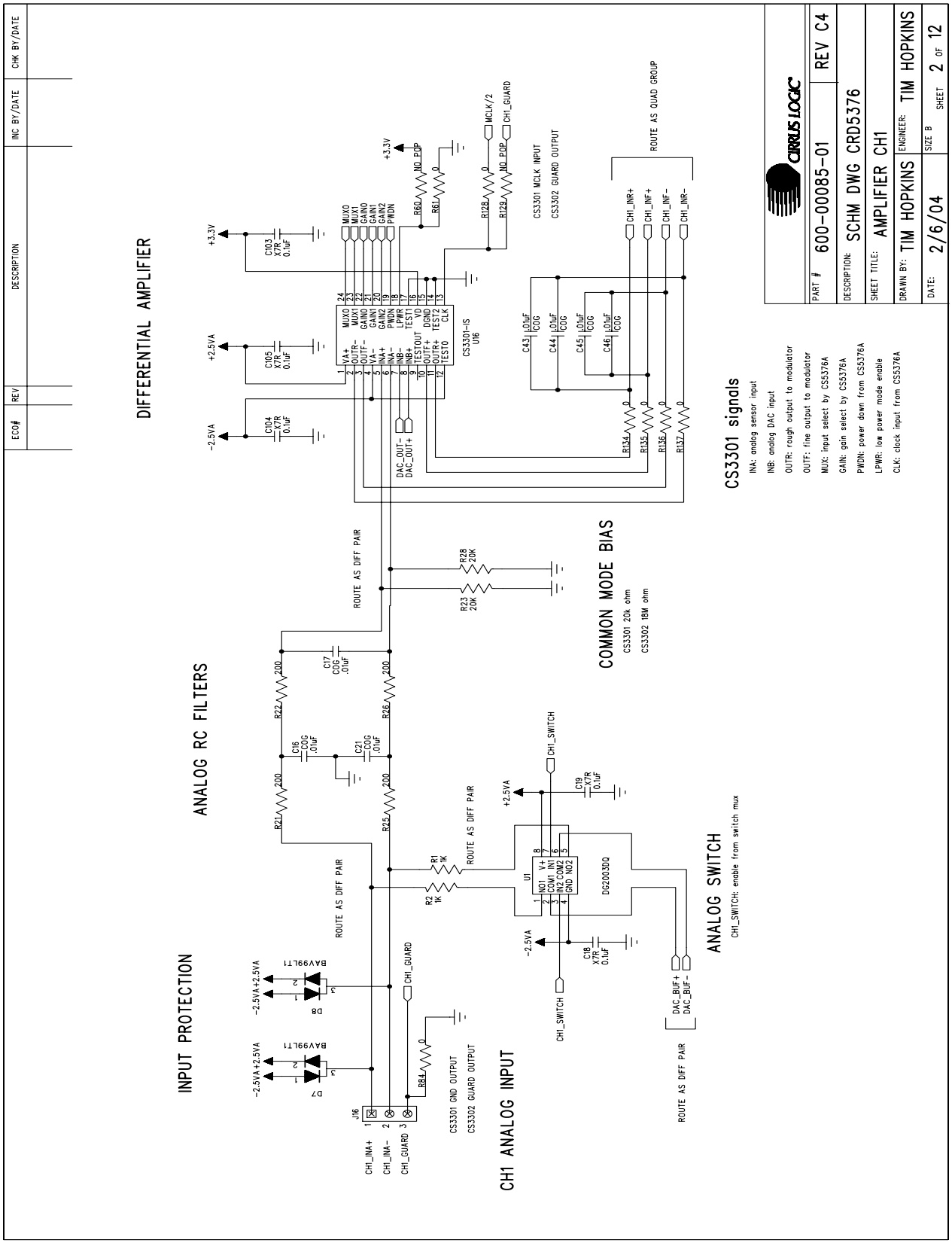


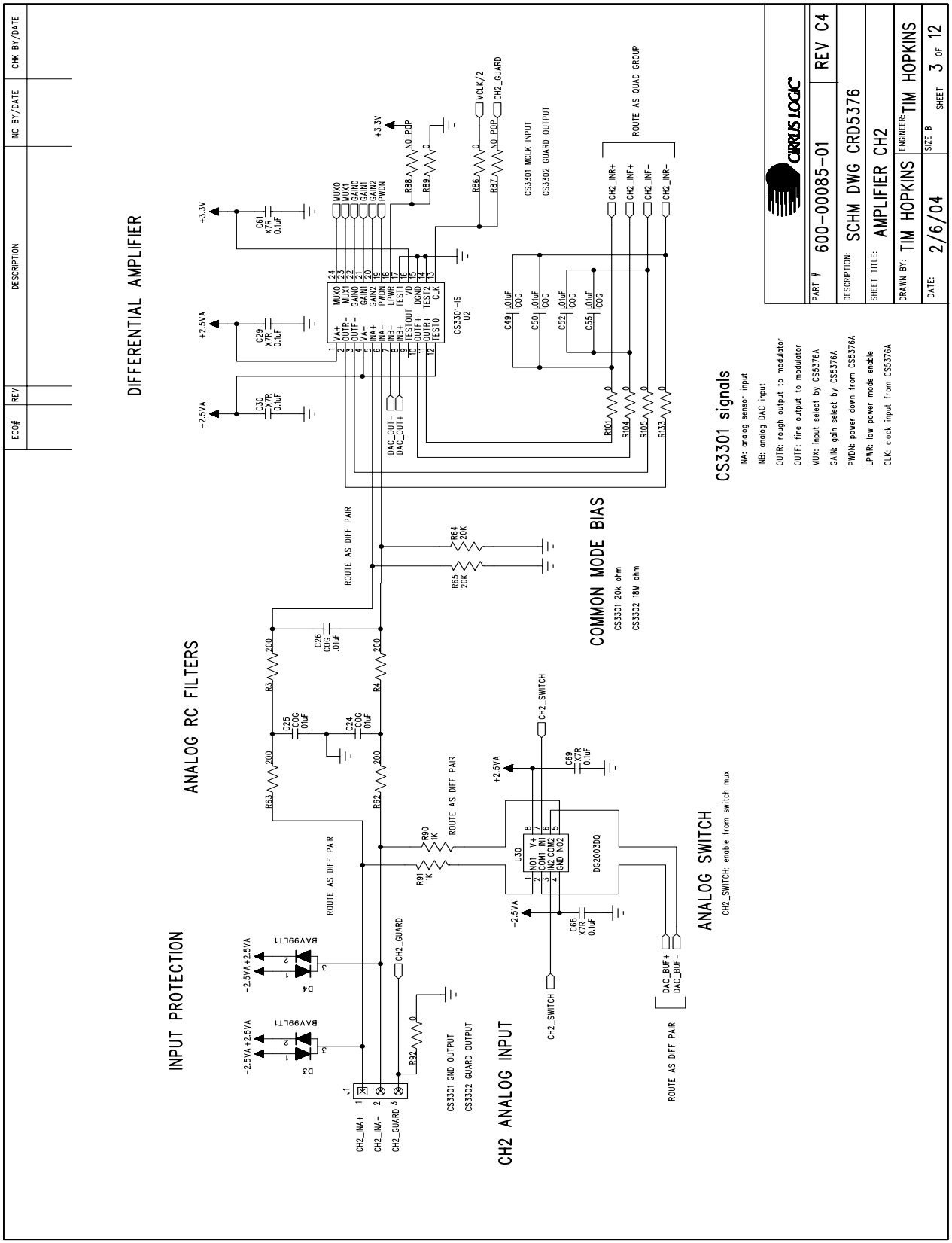
BOTTOM LAYER

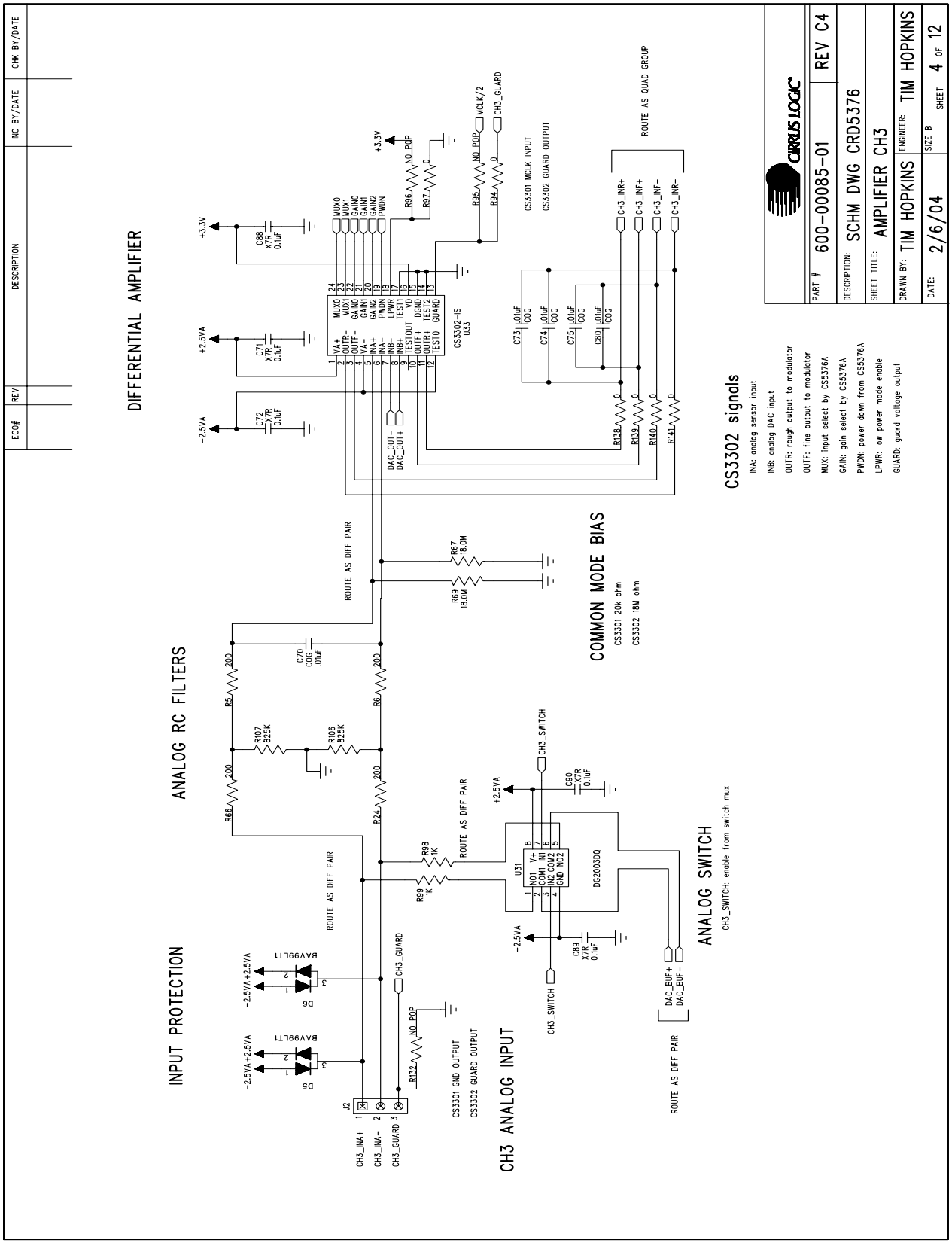
CRD5376 (240-00085-01 REV_C

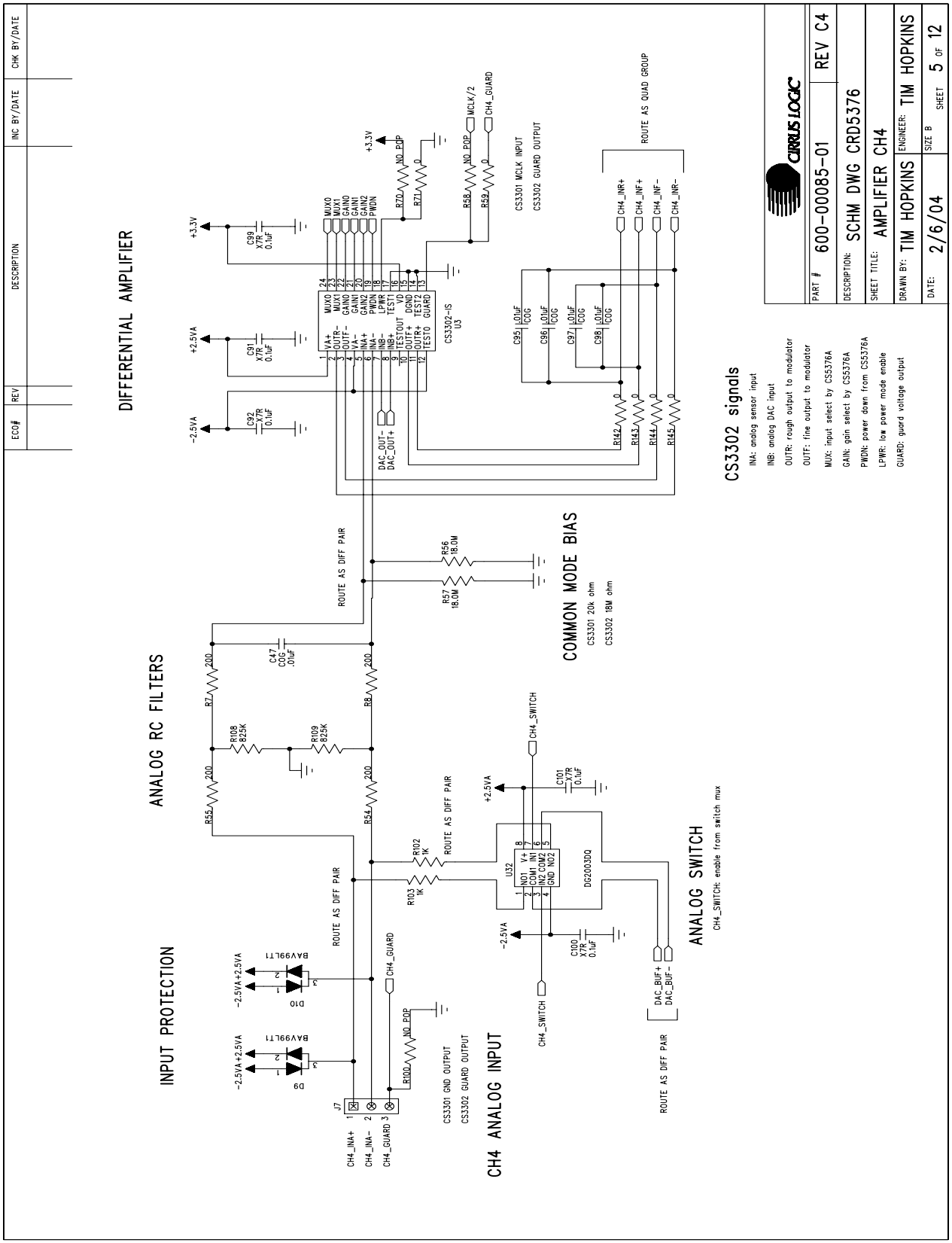
6. SCHEMATICS

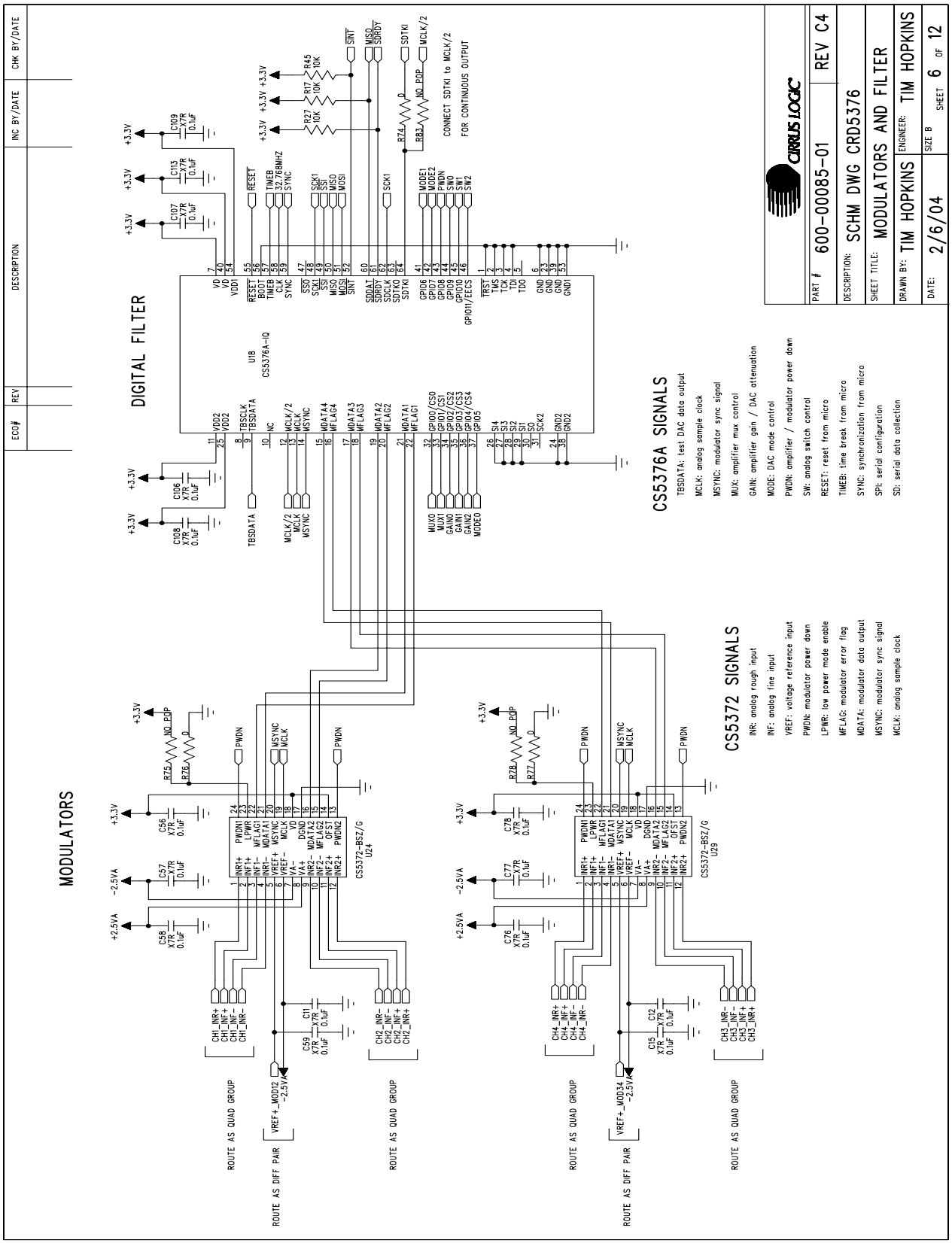


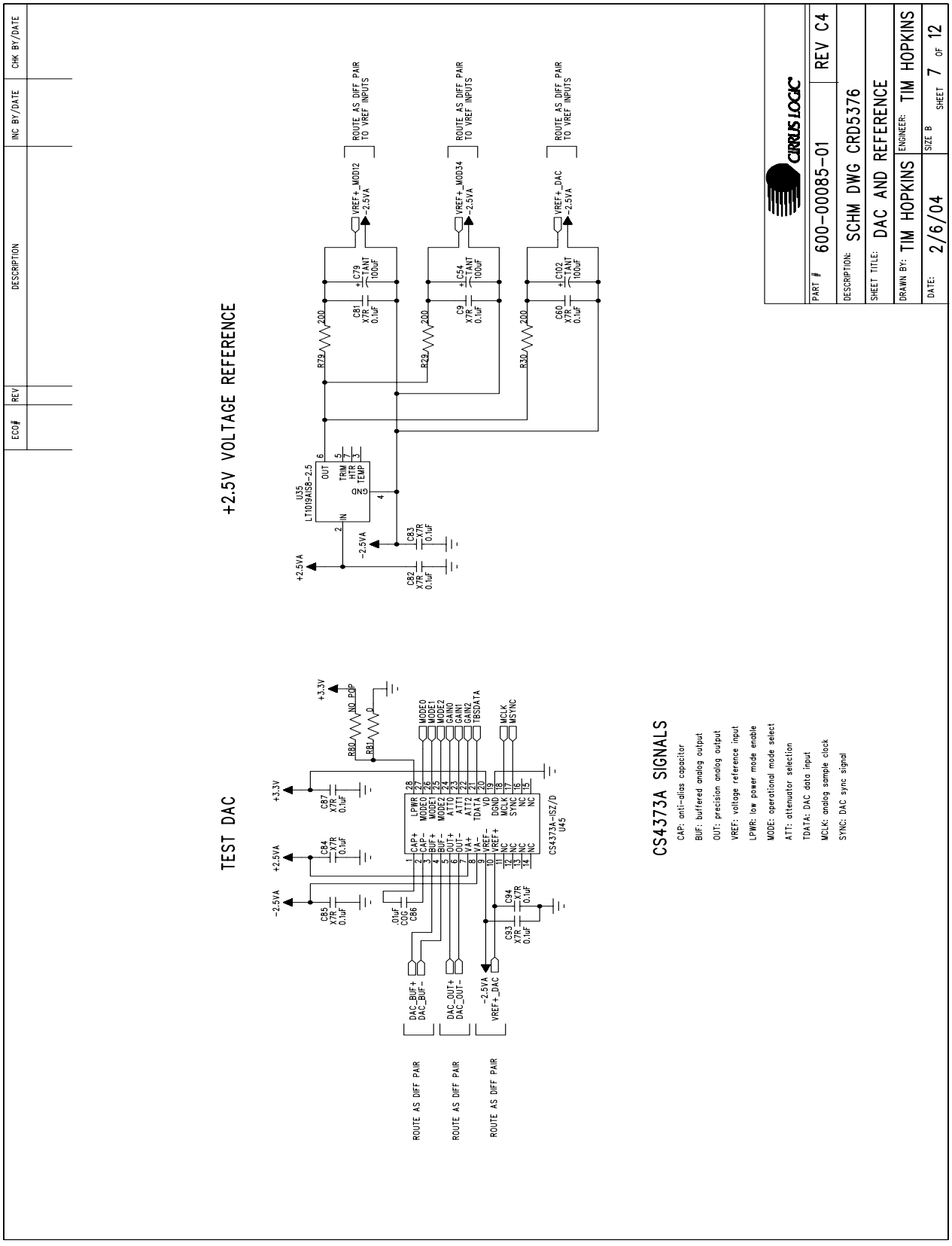

DIFFERENTIAL AMPLIFIER
ANALOG RC FILTERS
COMMON MODE BIAS
INPUT PROTECTION
CH1 ANALOG INPUT
ANALOG SWITCH
CS3301 signals
INA: analog sensor input
INB: analog DAC input
OUTR: rough output to modulator
OUTF: fine output to modulator
MUX: input select by CS5376A
GAIN: gain select by CS5376A
PWDN: power down from CS5376A
LPWR: low power mode enable
CLK: clock input from CS5376A
CH1_SWITCH: enable from switch mux
CS3301 20k ohm
CS3302 18W ohm
CS3301 MCLK INPUT
CS3302 GUARD OUTPUT
CS3301 GND OUTPUT
ROUTE AS DIFF PAIR
ROUTE AS QUAD GROUP
CS3301-HS
U16
DG2030Q
BAV99LT1
PART # 600-00085-01
REV C4
DESCRIPTION: SCHM DWG CRD5376
SHEET TITLE: AMPLIFIER CH1
DRAWN BY: TIM HOPKINS
ENGINEER: TIM HOPKINS
DATE: 2/6/04
SIZE B
SHEET 2 OF 12

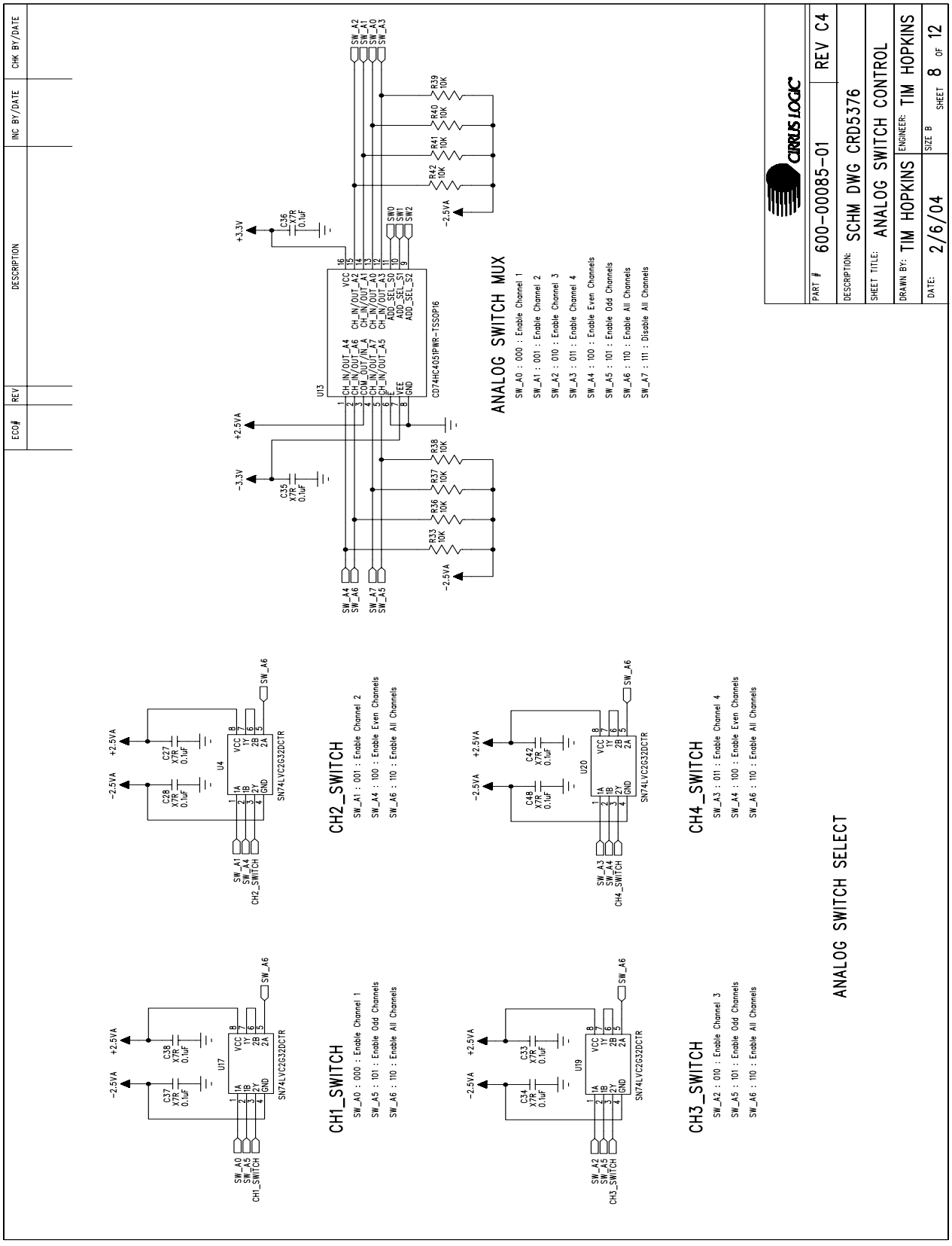

DIFFERENTIAL AMPLIFIER
ANALOG RC FILTERS
COMMON MODE BIAS
INPUT PROTECTION
CH2 ANALOG INPUT
ANALOG SWITCH
CS3301 signals
INA: analog sensor input
INB: analog DAC input
OUTR: rough output to modulator
OUTF: fine output to modulator
MUX: input select by CS5376A
GAIN: gain select by CS5376A
PWDN: power down from CS5376A
LPWR: low power mode enable
CLK: clock input from CS5376A
CS3301 20k ohm
CS3302 18M ohm
CH2_SWITCH: enable from switch mux
ROUTE AS DIFF PAIR
ROUTE AS QUAD GROUP
CS3301 MCLK INPUT
CS3302 GUARD OUTPUT
CS3301 GND OUTPUT
CS3302 GUARD OUTPUT
CS3301-IS
DG2003DQ
BAV99LT1
PART # 600-00085-01 REV C4
DESCRIPTION: SCHM DWG CRD5376
SHEET TITLE: AMPLIFIER CH2
DRAWN BY: TIM HOPKINS ENGINEER: TIM HOPKINS
DATE: 2/6/04 SIZE B SHEET 3 OF 12

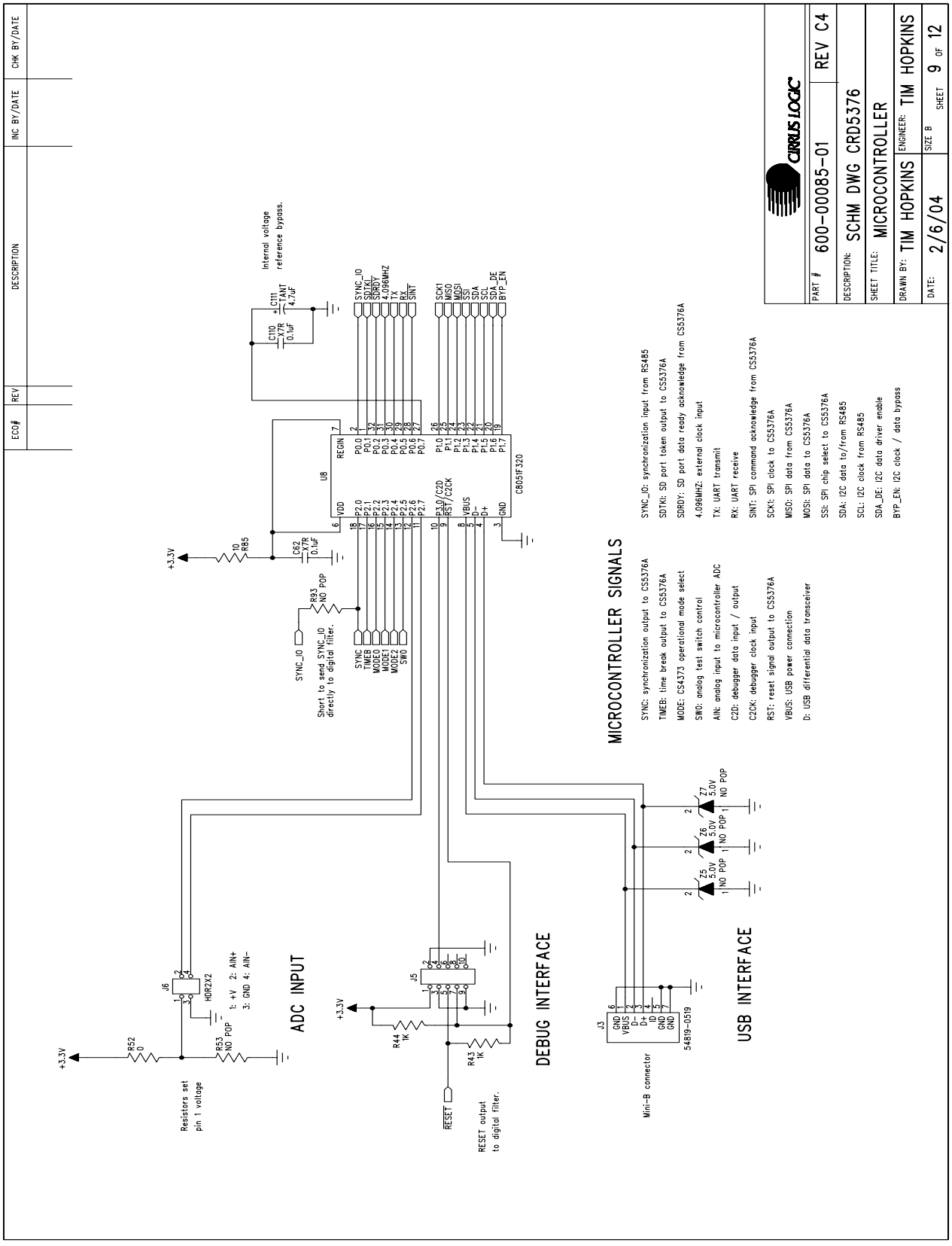

DIFFERENTIAL AMPLIFIER
ANALOG RC FILTERS
INPUT PROTECTION
CH3 ANALOG INPUT
COMMON MODE BIAS
ANALOG SWITCH
CS3302 signals
INA: analog sensor input
INB: analog DAC input
OUTR: rough output to modulator
OUTF: fine output to modulator
MUX: input select by CS5376A
GAIN: gain select by CS5376A
PWDN: power down from CS5376A
LPWR: low power mode enable
GUARD: guard voltage output
CS3301 MCLK INPUT
CS3302 GUARD OUTPUT
CS3301 GND OUTPUT
CS3302 GUARD OUTPUT
CS3301 20k ohm
CS3302 18M ohm
ROUTE AS QUAD GROUP
ROUTE AS DIFF PAIR
CH3_SWITCH: enable from switch mux
PART # 600-00085-01
REV C4
DESCRIPTION: SCHM DWG CRD5376
SHEET TITLE: AMPLIFIER CH3
DRAWN BY: TIM HOPKINS
ENGINEER: TIM HOPKINS
DATE: 2/6/04
SIZE B
SHEET 4 OF 12

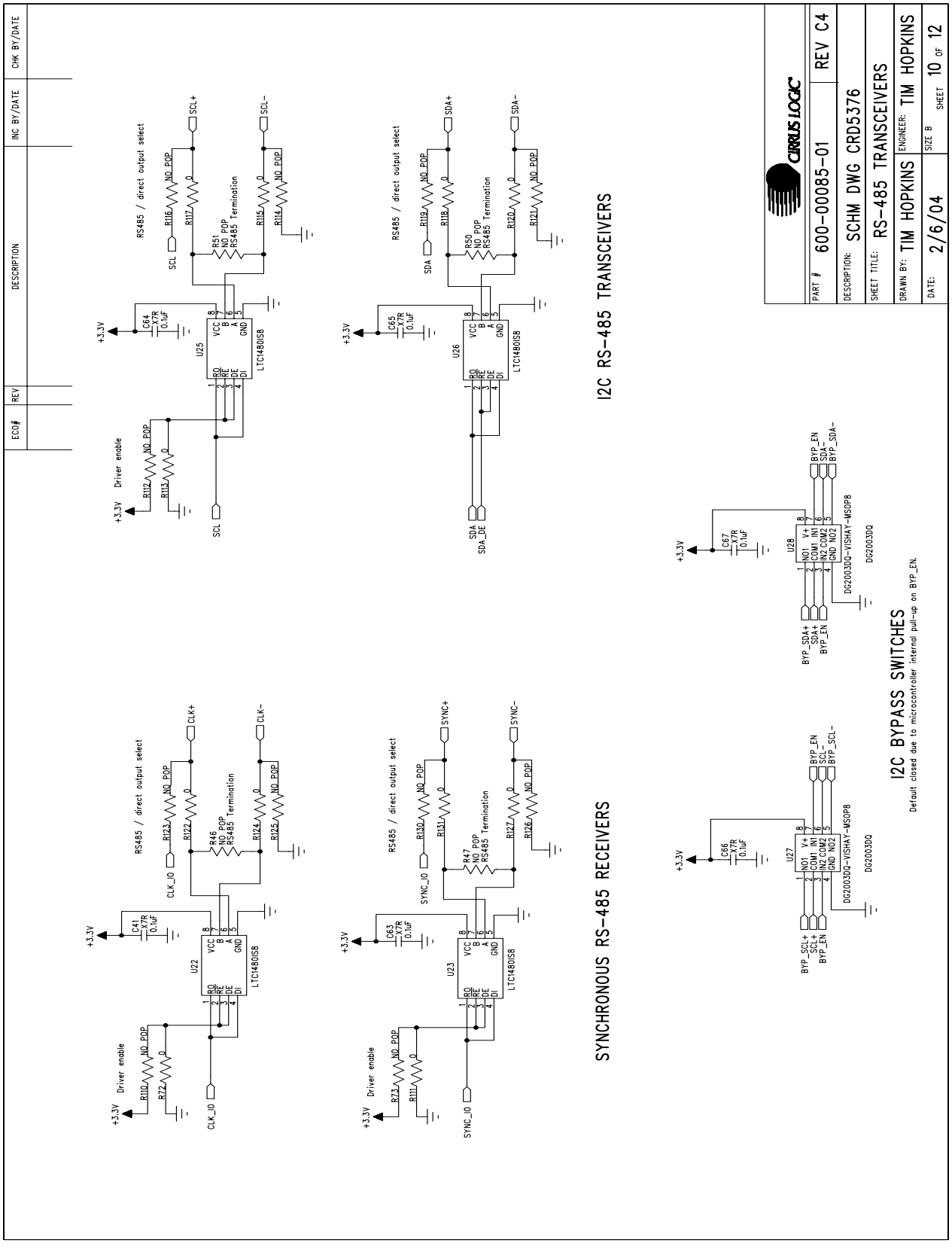

DIFFERENTIAL AMPLIFIER
ANALOG RC FILTERS
INPUT PROTECTION
CH4 ANALOG INPUT
COMMON MODE BIAS
ANALOG SWITCH
CS3302 signals
INA: analog sensor input
INB: analog DAC input
OUTR: rough output to modulator
OUTF: fine output to modulator
MUX: input select by CS5376A
GAIN: gain select by CS5376A
PWDN: power down from CS5376A
LPWR: low power mode enable
GUARD: guard voltage output
CS3301 MCLK INPUT
CS3302 GUARD OUTPUT
CS3301 GND OUTPUT
CS3302 GUARD OUTPUT
ROUTE AS DIFF PAIR
ROUTE AS QUAD GROUP
CH4_SWITCH: enable from switch mux
CS3302-IS
DG2003Q
BAV99LT1
PART # 600-00085-01 REV C4
DESCRIPTION: SCHM DWG CRD5376
SHEET TITLE: AMPLIFIER CH4
DRAWN BY: TIM HOPKINS ENGINEER: TIM HOPKINS
DATE: 2/6/04 SIZE B SHEET 5 OF 12

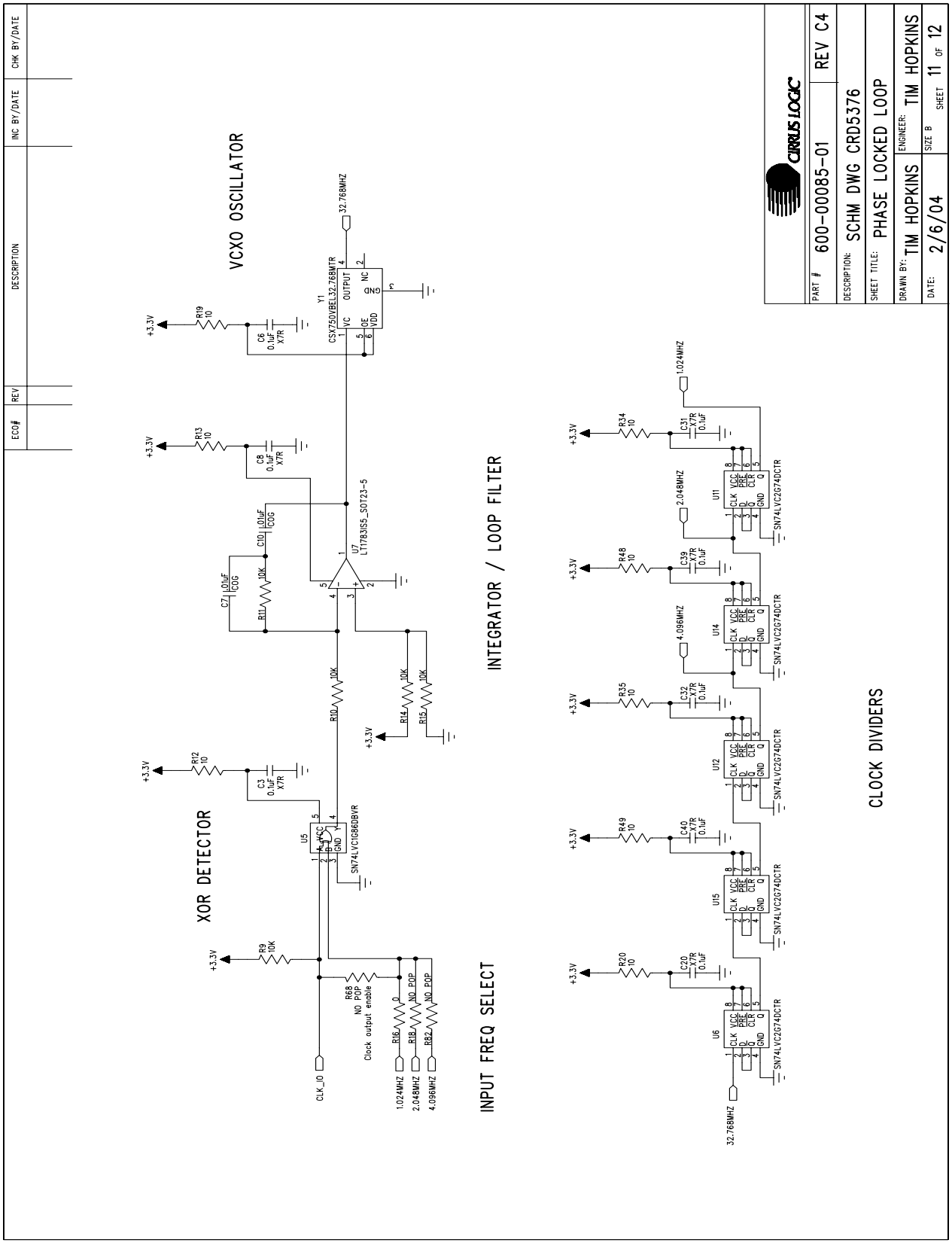

DIGITAL FILTER
MODULATORS
CS5376A SIGNALS
CS5372 SIGNALS
ROUTE AS QUAD GROUP
ROUTE AS DIFF PAIR
CONNECT SDTKI to MCLK/2
FOR CONTINUOUS OUTPUT
PART # 600-00085-01 REV C4
DESCRIPTION: SCHM DWG CRD5376
SHEET TITLE: MODULATORS AND FILTER
DRAWN BY: TIM HOPKINS
ENGINEER: TIM HOPKINS
DATE: 2/6/04
SIZE B
SHEET 6 OF 12

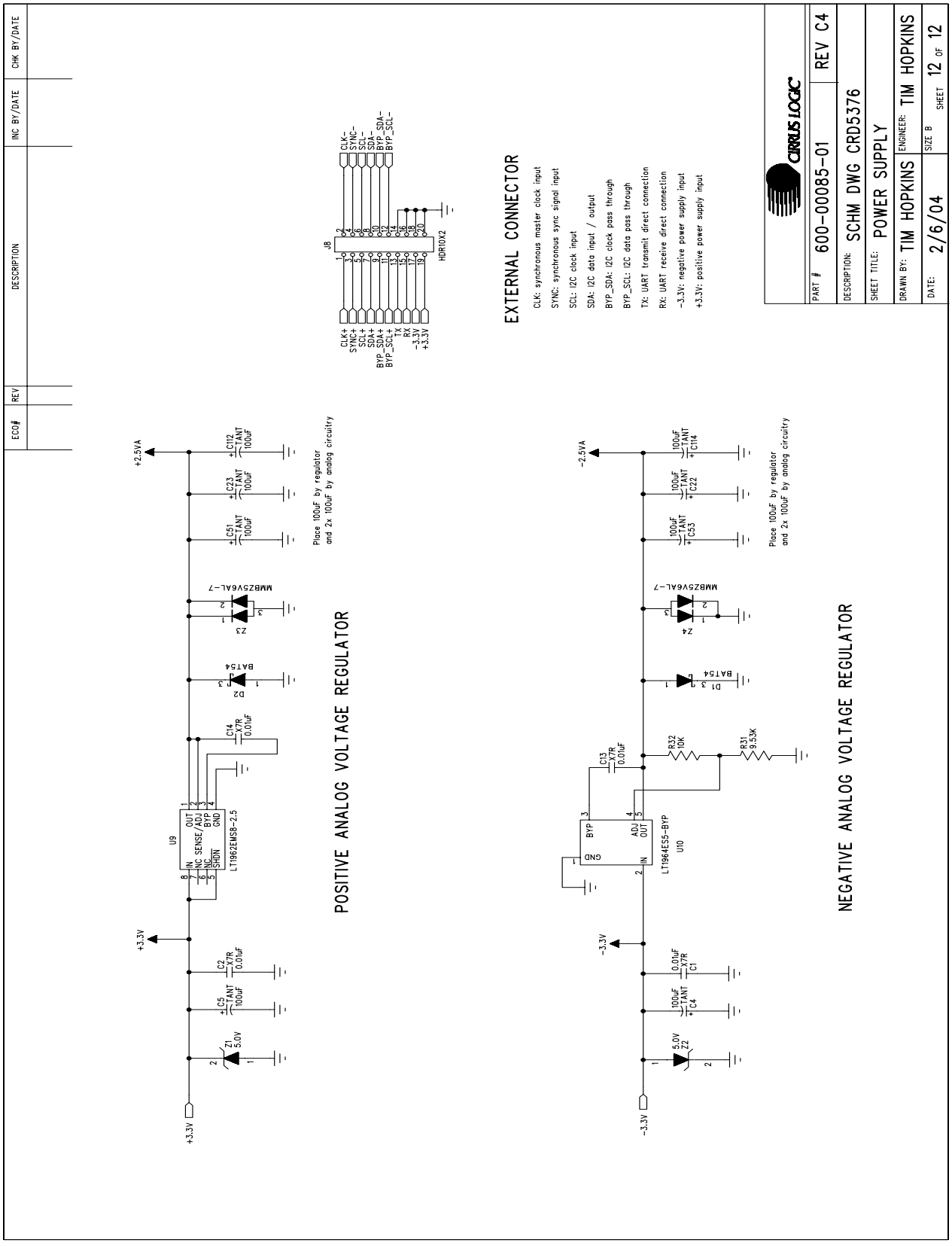

ECO#
REV
DESCRIPTION
INC BY/DATE
CHK BY/DATE
+2.5V VOLTAGE REFERENCE
ROUTE AS DIFF PAIR TO VREF INPUTS
VREF+_MOD12 -2.5VA
VREF+_MOD34 -2.5VA
VREF+_DAC -2.5VA
R29 200
R30 200
C79 +1ANT 100uF
C81 X7R 0.1uF
C54 +1ANT 100uF
C9 X7R 0.1uF
C102 +1ANT 100uF
C60 X7R 0.1uF
U35 LT1019AISB-2.5
OUT
TRIM HTR TEMP
GND
IN
+2.5VA
-2.5VA
C83 X7R 0.1uF
C82 X7R 0.1uF
TEST DAC
+3.3V
R82 NO_POP
R81 0
MODE0 MODE1 MODE2 GAIN0 GAIN1 GAIN2 TBSDATA
MCLK MSYNC
C87 X7R 0.1uF
C84 X7R 0.1uF
C85 X7R 0.1uF
.01uF C0G C86
C94 X7R 0.1uF
C93 X7R 0.1uF
LPWR MODE0 MODE1 MODE2 ATT0 ATT1 ATT2 TDATA DGND MCLK SYNC NC
CAP+ CAP- BUF+ BUF- OUT+ OUT- VA+ VA- VREF+ VREF- NC NC NC
CS4373A-ISZ/D U45
DAC_BUF+ DAC_BUF-
DAC_OUT+ DAC_OUT-
-2.5VA VREF+_DAC
ROUTE AS DIFF PAIR
CS4373A SIGNALS
CAP: anti-alias capacitor
BUF: buffered analog output
OUT: precision analog output
VREF: voltage reference input
LPWR: low power mode enable
MODE: operational mode select
ATT: attenuator selection
TDATA: DAC data input
MCLK: analog sample clock
SYNC: DAC sync signal
CIRRUS LOGIC
PART # 600-00085-01 REV C4
DESCRIPTION: SCHM DWG CRD5376
SHEET TITLE: DAC AND REFERENCE
DRAWN BY: TIM HOPKINS ENGINEER: TIM HOPKINS
DATE: 2/6/04 SIZE B SHEET 7 OF 12


ECO#
REV
DESCRIPTION
INC BY/DATE
CHK BY/DATE
ANALOG SWITCH MUX
SW_A0 : 000 : Enable Channel 1
SW_A1 : 001 : Enable Channel 2
SW_A2 : 010 : Enable Channel 3
SW_A3 : 011 : Enable Channel 4
SW_A4 : 100 : Enable Even Channels
SW_A5 : 101 : Enable Odd Channels
SW_A6 : 110 : Enable All Channels
SW_A7 : 111 : Disable All Channels
CD74HC4051PWR-TSSOP16
SN74LVC2G32DCTR
CH1_SWITCH
SW_A0 : 000 : Enable Channel 1
SW_A5 : 101 : Enable Odd Channels
SW_A6 : 110 : Enable All Channels
CH2_SWITCH
SW_A1 : 001 : Enable Channel 2
SW_A4 : 100 : Enable Even Channels
SW_A6 : 110 : Enable All Channels
CH3_SWITCH
SW_A2 : 010 : Enable Channel 3
SW_A5 : 101 : Enable Odd Channels
SW_A6 : 110 : Enable All Channels
CH4_SWITCH
SW_A3 : 011 : Enable Channel 4
SW_A4 : 100 : Enable Even Channels
SW_A6 : 110 : Enable All Channels
ANALOG SWITCH SELECT
CIRRUS LOGIC
PART # 600-00085-01
REV C4
DESCRIPTION: SCHM DWG CRD5376
SHEET TITLE: ANALOG SWITCH CONTROL
DRAWN BY: TIM HOPKINS
ENGINEER: TIM HOPKINS
DATE: 2/6/04
SIZE B
SHEET 8 OF 12


ECO# | REV | DESCRIPTION | INC BY/DATE | CHK BY/DATE
CIRRUS LOGIC
PART # 600-00085-01 REV C4
DESCRIPTION: SCHM DWG CRD5376
SHEET TITLE: MICROCONTROLLER
DRAWN BY: TIM HOPKINS ENGINEER: TIM HOPKINS
DATE: 2/6/04 SIZE B SHEET 9 OF 12
MICROCONTROLLER SIGNALS
SYNC: synchronization output to CS5376A
TIMEB: time break output to CS5376A
MODE: CS4373 operational mode select
SW0: analog test switch control
AIN: analog input to microcontroller ADC
C2D: debugger data input / output
C2CK: debugger clock input
RST: reset signal output to CS5376A
VBUS: USB power connection
D: USB differential data transceiver
SYNC_IO: synchronization input from RS485
SDTKI: SD port token output to CS5376A
SDRDY: SD port data ready acknowledge from CS5376A
4.096MHZ: external clock input
TX: UART transmit
RX: UART receive
SINT: SPI command acknowledge from CS5376A
SCKI: SPI clock to CS5376A
MISO: SPI data from CS5376A
MOSI: SPI data to CS5376A
SSI: SPI chip select to CS5376A
SDA: I2C data to/from RS485
SCL: I2C clock from RS485
SDA_DE: I2C data driver enable
BYP_EN: I2C clock / data bypass
ADC INPUT
DEBUG INTERFACE
USB INTERFACE
Internal voltage reference bypass.
Short to send SYNC_IO directly to digital filter.
Resistors set pin 1 voltage
RESET output to digital filter.
Mini-B connector
C805F320
HDR2X2
54819-0519
NO POP


I2C RS-485 TRANSCEIVERS
SYNCHRONOUS RS-485 RECEIVERS
I2C BYPASS SWITCHES
Default closed due to microcontroller internal pull-up on BYP_EN.
CIRRUS LOGIC
PART # 600-00085-01
REV C4
DESCRIPTION: SCHM DWG CRD5376
SHEET TITLE: RS-485 TRANSCEIVERS
DRAWN BY: TIM HOPKINS
ENGINEER: TIM HOPKINS
DATE: 2/6/04
SIZE B
SHEET 10 OF 12


ECO#
REV
DESCRIPTION
INC BY/DATE
CHK BY/DATE
VCXO OSCILLATOR
XOR DETECTOR
INTEGRATOR / LOOP FILTER
INPUT FREQ SELECT
CLOCK DIVIDERS
PART # 600-00085-01
REV C4
DESCRIPTION: SCHM DWG CRD5376
SHEET TITLE: PHASE LOCKED LOOP
DRAWN BY: TIM HOPKINS
ENGINEER: TIM HOPKINS
DATE: 2/6/04
SIZE B
SHEET 11 OF 12


ECO#
REV
DESCRIPTION
INC BY/DATE
CHK BY/DATE
EXTERNAL CONNECTOR
CLK: synchronous master clock input
SYNC: synchronous sync signal input
SCL: I2C clock input
SDA: I2C data input / output
BYP_SDA: I2C clock pass through
BYP_SCL: I2C data pass through
TX: UART transmit direct connection
RX: UART receive direct connection
-3.3V: negative power supply input
+3.3V: positive power supply input
J8
HDR10X2
CLK+
SYNC+
SCL+
SDA+
BYP_SDA+
BYP_SCL+
TX
RX
-3.3V
+3.3V
CLK-
SYNC-
SCL-
SDA-
BYP_SDA-
BYP_SCL-
POSITIVE ANALOG VOLTAGE REGULATOR
+2.5VA
+3.3V
+3.3V
U9
LT1962EMS8-2.5
OUT
SENSE/ADJ
BYP
GND
IN
NC
NC
SHDN
C14 X7R 0.01uF
C2 X7R 0.01uF
C5 TANT 100uF
C51 TANT 100uF
C23 TANT 100uF
C112 TANT 100uF
D2 BAT54
Z3 MMBZ5V6AL-7
Z1 5.0V
Place 100uF by regulator and 2x 100uF by analog circuitry
NEGATIVE ANALOG VOLTAGE REGULATOR
-2.5VA
-3.3V
-3.3V
U10
LT1964ES5-BYP
BYP
GND
IN
ADJ
OUT
C13 X7R 0.01uF
R32 10K
R31 9.53K
C1 X7R 0.01uF
C4 TANT 100uF
C53 TANT 100uF
C22 TANT 100uF
C114 TANT 100uF
D1 BAT54
Z4 MMBZ5V6AL-7
Z2 5.0V
Place 100uF by regulator and 2x 100uF by analog circuitry
CIRRUS LOGIC
PART # 600-00085-01
REV C4
DESCRIPTION: SCHM DWG CRD5376
SHEET TITLE: POWER SUPPLY
DRAWN BY: TIM HOPKINS
ENGINEER: TIM HOPKINS
DATE: 2/6/04
SIZE B
SHEET 12 OF 12