

## Description

### N-channel Enhancement Mode Power MOSFET

#### Features

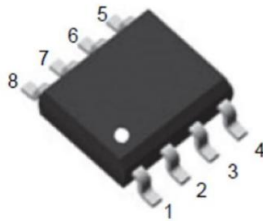
- 100V, 12A  
 $R_{DS(ON)}$  Typ = 10m $\Omega$  @  $V_{GS} = 10V$   
 $R_{DS(ON)}$  Typ = 13m $\Omega$  @  $V_{GS} = 4.5V$
- Advanced Split Gate Trench Technology
- Excellent  $R_{DS(ON)}$  and Low Gate Charge
- Lead Free

#### Applications

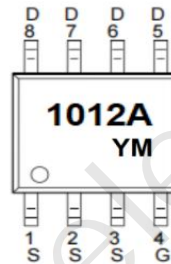
- Load Switch
- PWM Application
- Power Management



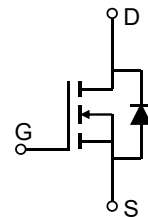
*100% UIS TESTED!*



SOP-8



Marking and Pin Assignment



Schematic Diagram

### Package Marking and Ordering Information

Device Marking	Device	Outline	Package	Reel Size	Reel(pcs)	Per Carton (pcs)
1012A	CRMPGL1012A	TAPING	SOP-8	13"	4000	40000

### Absolute Maximum Ratings (@ $T_j = 25^\circ C$ unless otherwise specified)

Symbol	Parameter	Value	Units
$V_{DS}$	Drain-to-Source Voltage	100	V
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current	$T_A = 25^\circ C$	12
		$T_A = 100^\circ C$	7.5
$I_{DM}$	Pulsed Drain Current <sup>(1)</sup>	48	A
$E_{AS}$	Single Pulsed Avalanche Energy <sup>(2)</sup>	72	mJ
$P_D$	Power Dissipation	$T_A = 25^\circ C$	3.1
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient <sup>(3)</sup>	40	$^\circ C/W$
$T_J, T_{STG}$	Junction & Storage Temperature Range	-55 to 150	$^\circ C$



## Electrical Characteristics (T<sub>J</sub> = 25°C unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>Off Characteristics</b>						
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> = 250μA, V <sub>GS</sub> = 0V	100	-	-	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 100V, V <sub>GS</sub> = 0V	-	-	1.0	μA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±20V	-	-	±100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	1.0	1.7	2.5	V
R <sub>DS(ON)</sub>	Static Drain-Source ON-Resistance <sup>(4)</sup>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 12A	-	10.0	13.0	mΩ
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 10A	-	13.0	17.0	mΩ
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 25V, f = 1MHz	-	1500	-	pF
C <sub>oss</sub>	Output Capacitance		-	840	-	pF
C <sub>riss</sub>	Reverse Transfer Capacitance		-	30	-	pF
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> = 0 to 10V V <sub>DS</sub> = 50V, I <sub>D</sub> = 12A	-	35	-	nC
Q <sub>gs</sub>	Gate Source Charge		-	4.5	-	nC
Q <sub>gd</sub>	Gate Drain("Miller") Charge		-	8	-	nC
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> = 10V, V <sub>DD</sub> = 50V I <sub>D</sub> = 12A, R <sub>GEN</sub> = 3Ω	-	16	-	ns
t <sub>r</sub>	Turn-On Rise Time		-	13	-	ns
t <sub>d(off)</sub>	Turn-Off DelayTime		-	37	-	ns
t <sub>f</sub>	Turn-Off Fall Time		-	17	-	ns
<b>Drain-Source Diode Characteristics and Max Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current		-	-	12	A
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current		-	-	48	A
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>S</sub> = 12A	-	-	1.2	V

- Notes:
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
  2. E<sub>AS</sub> condition: Starting T<sub>J</sub>=25C, V<sub>DD</sub>=30V, V<sub>e</sub>=10V, R<sub>G</sub>=25ohm, L=0.5mH, I<sub>AS</sub>=17A
  3. R<sub>θJA</sub> is measured with the device mounted on a 1inch<sup>2</sup> pad of 2oz copper FR4 PCB
  4. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 0.5%.

## Typical Performance Characteristics

Figure 1: Output Characteristics

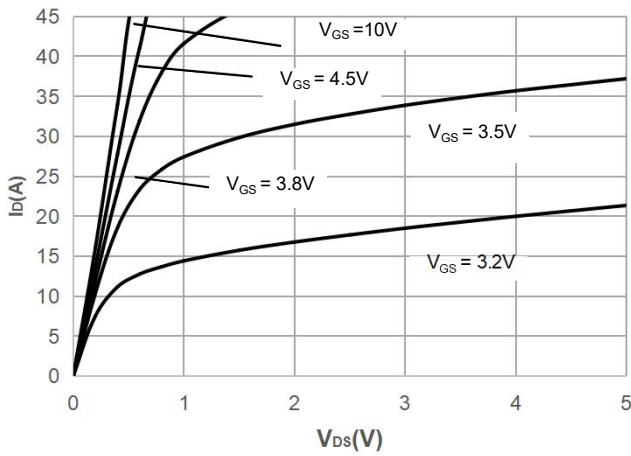


Figure 2: Typical Transfer Characteristics

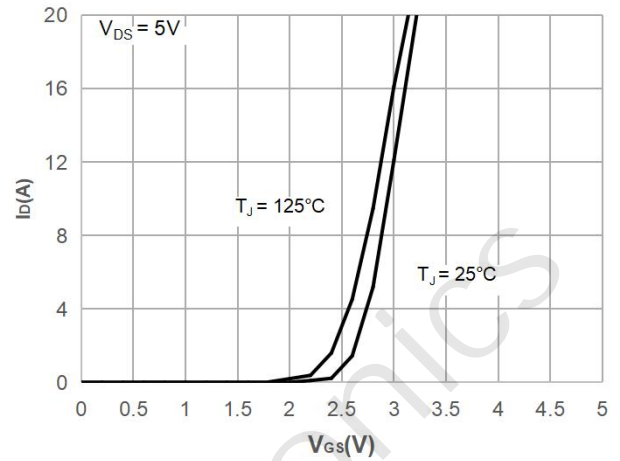


Figure 3: On-resistance vs. Drain Current

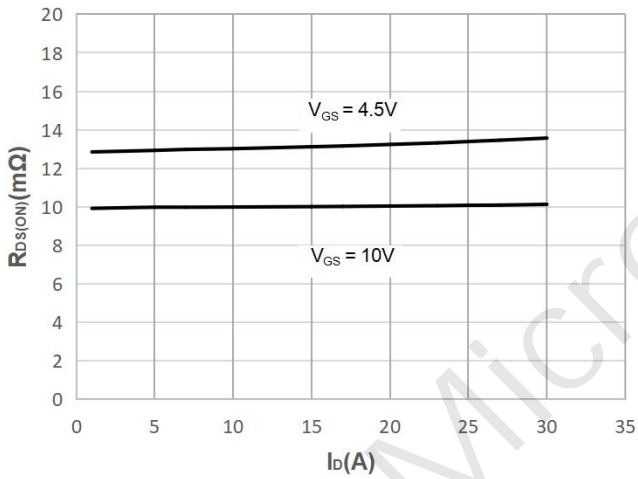


Figure 4: Body Diode Characteristics

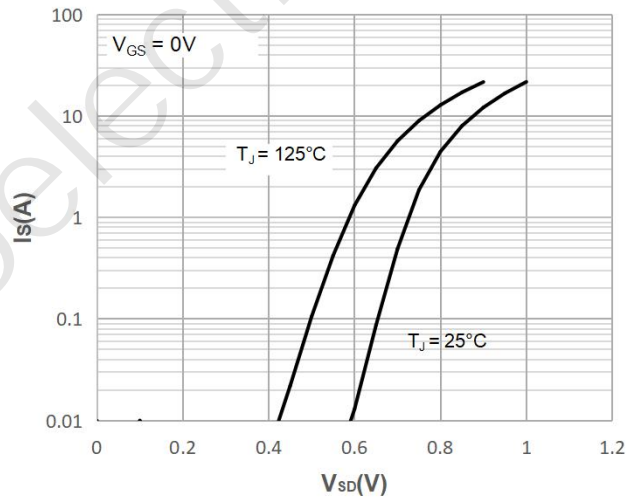


Figure 5: Gate Charge Characteristics

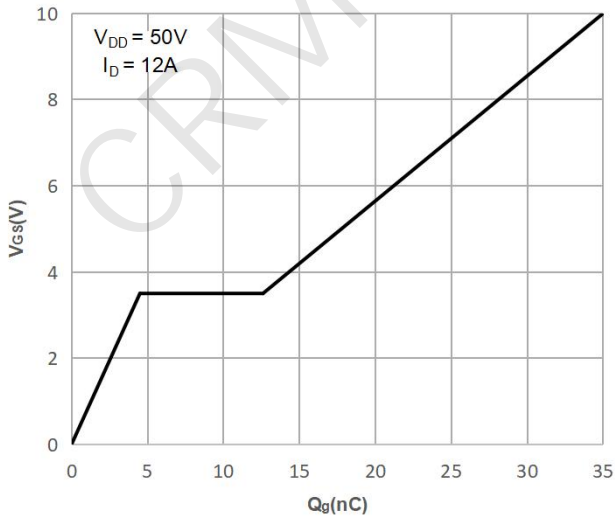
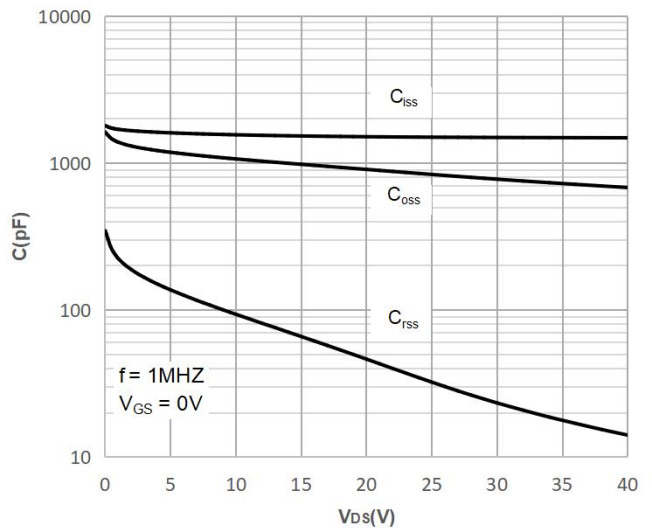


Figure 6: Capacitance Characteristics



## Typical Performance Characteristics

Figure 7: Normalized Breakdown voltage vs. Junction Temperature

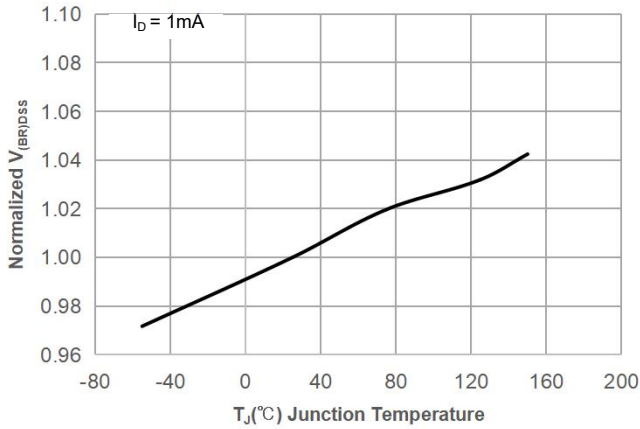


Figure 8: Normalized on Resistance vs. Junction Temperature

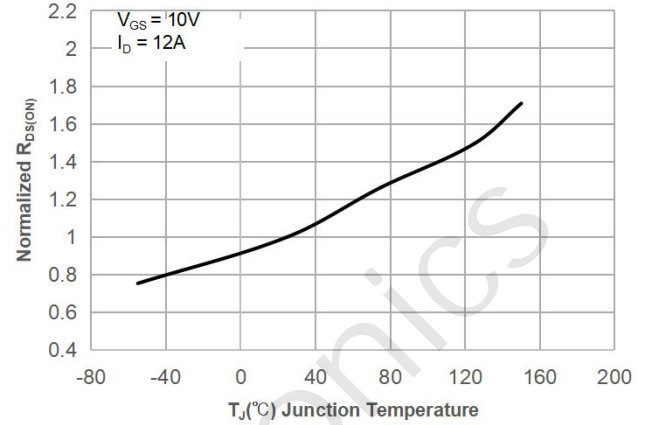


Figure 9: Maximum Safe Operating Area

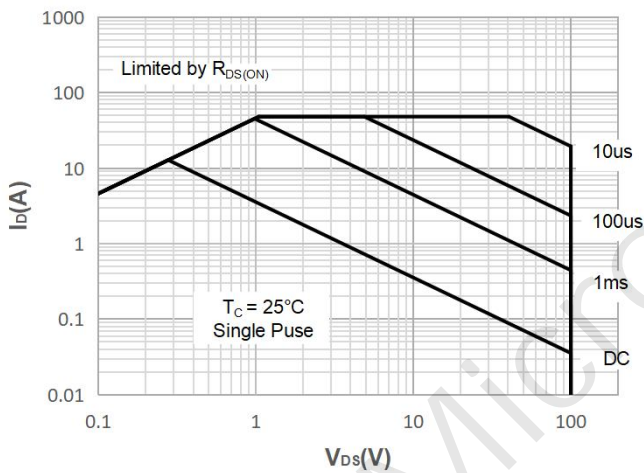


Figure 10: Maximum Continuous Driian Current vs. Case Temperature

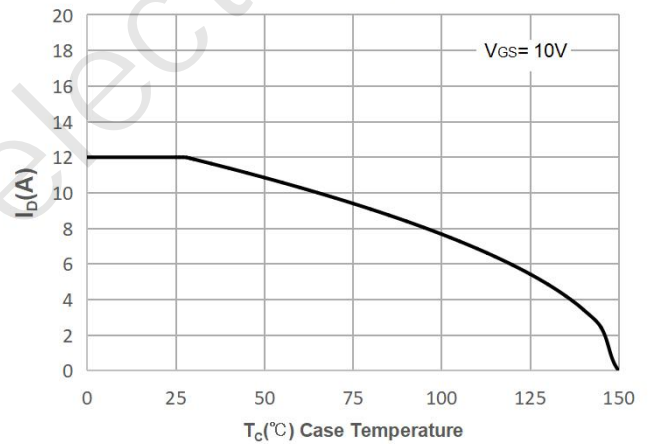


Figure 11: Normalized Maximum Transient Thermal Impedance

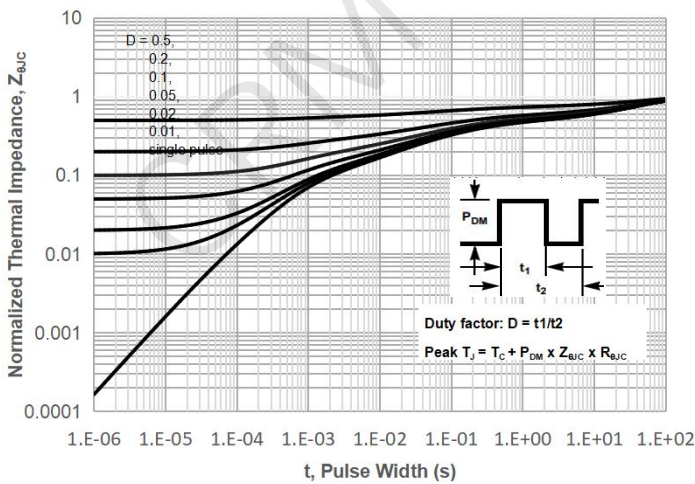
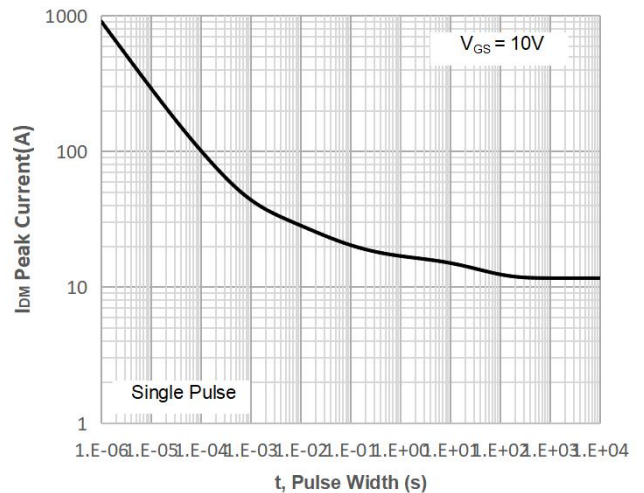
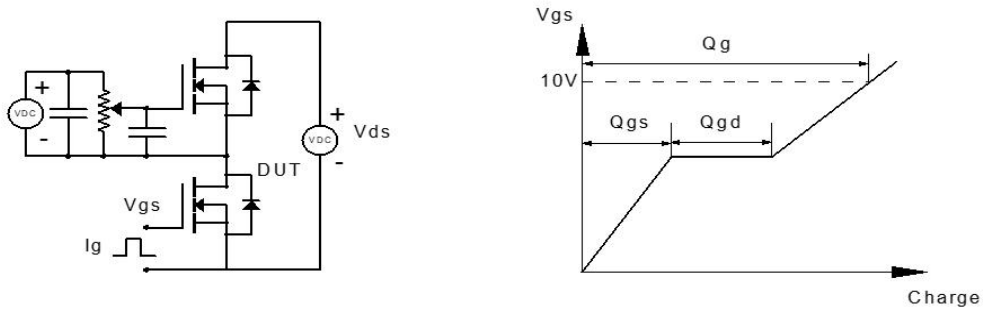


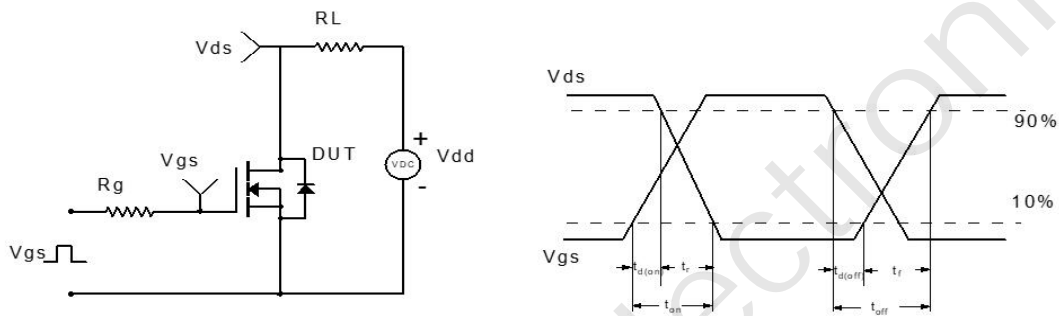
Figure 12: Peak Current Capacity



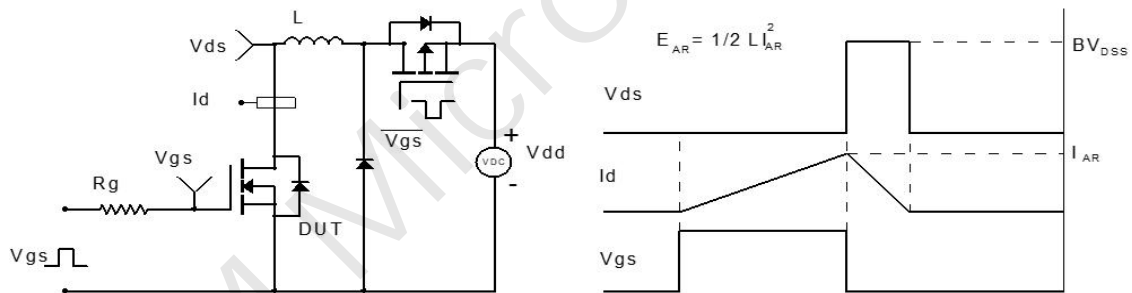
## Test Circuit



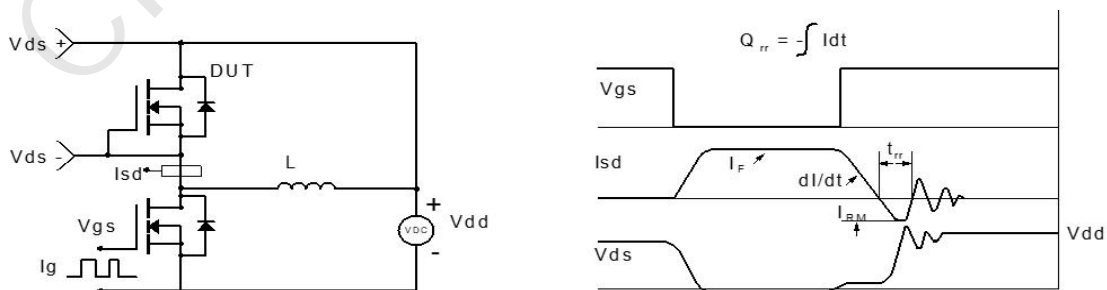
**Figure 1: Gate Charge Test Circuit & Waveform**



**Figure 2: Resistive Switching Test Circuit & Waveform**

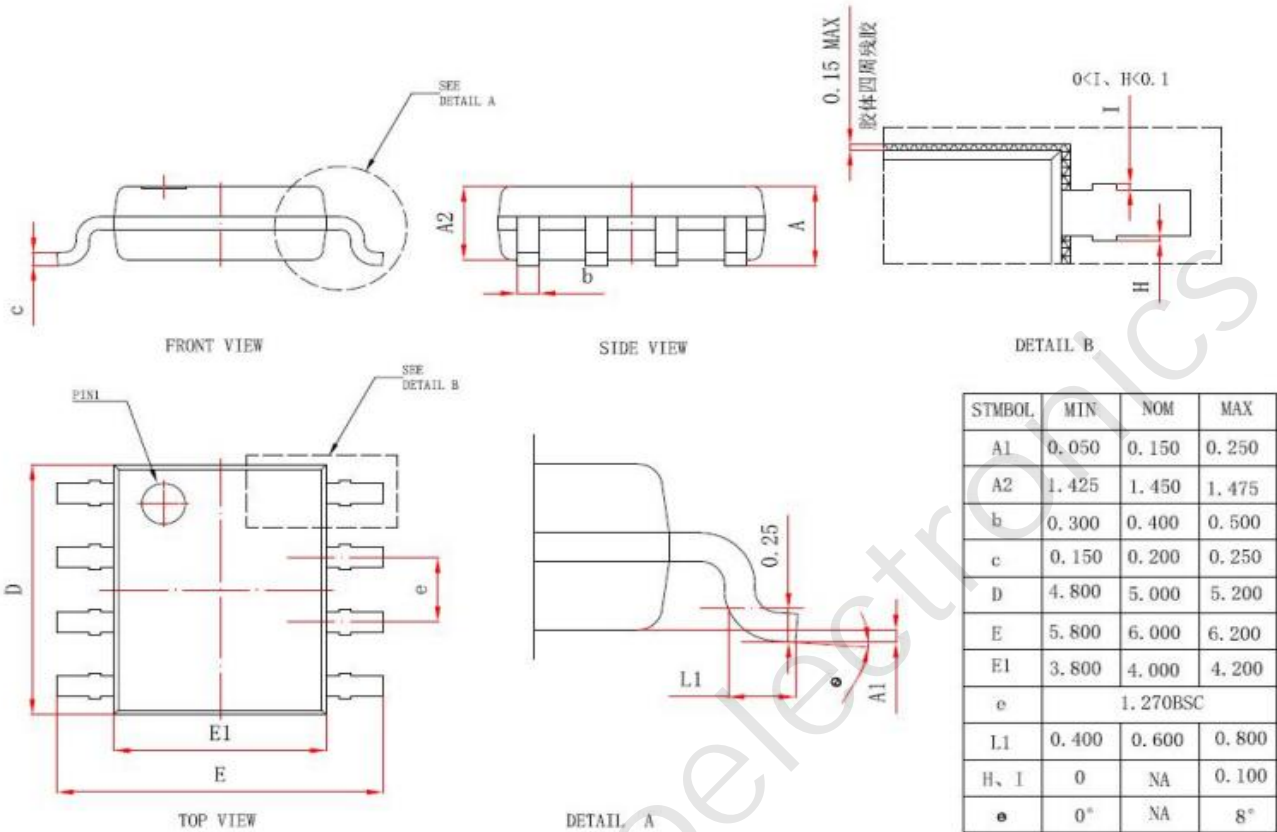


**Figure 3: Unclamped Inductive Switching Test Circuit & Waveform**



**Figure 4: Diode Recovery Test Circuit & Waveform**

## Package Mechanical Data(SOP-8)



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