

Description

N-channel Enhancement Mode Power MOSFET

Features

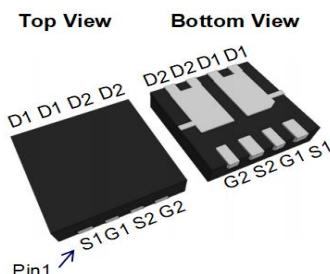
- 60V, 35A
- $R_{DS(ON)}$ Typ= 11.5mΩ @ V_{GS} = 10V
- $R_{DS(ON)}$ Typ= 14mΩ @ V_{GS} = 4.5V
- Advanced Split Gate Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge

Applications

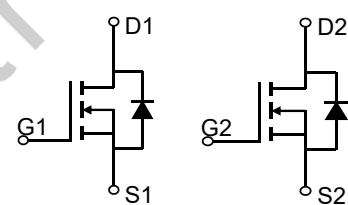
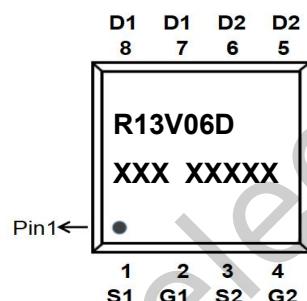
- Load Switch
- PWM Application
- Power Management



100% UIS TESTED!
100% ΔV_{ds} TESTED!



DFN3.3x3.3-8L-D



Package Marking and Ordering Information

Device Marking	Device	Outline	Package	Reel Size	Reel(pcs)	Per Carton (pcs)
R13V06D	CRMRGL0614AD	TAPING	DFN3.3x3.3-8L-D	13"	5000	50000

Absolute Maximum Ratings (@ T_J = 25°C unless otherwise specified)

Symbol	Parameter	Value	Units
V_{DS}	Drain-to-Source Voltage	60	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D	Continuous Drain Current $T_C = 25^\circ\text{C}$	35	A
		21	
I_{DM}	Pulsed Drain Current ⁽¹⁾	140	A
E_{AS}	Single Pulsed Avalanche Energy ⁽²⁾	49	mJ
P_D	Power Dissipation $T_C = 25^\circ\text{C}$	18	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ⁽³⁾	50	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	7	
T_J, T_{STG}	Junction & Storage Temperature Range	-55 to 150	$^\circ\text{C}$

**Electrical Characteristics** ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	60	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 60\text{V}, V_{GS} = 0\text{V}$	-	-	1.0	μA
I_{GSS}	Gate-Body Leakage Current	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1.0	1.6	2.5	V
$R_{\text{DS(ON)}}$	Static Drain-Source ON-Resistance ⁽⁴⁾	$V_{GS} = 10\text{V}, I_D = 20\text{A}$	-	11.5	14.0	$\text{m}\Omega$
		$V_{GS} = 4.5\text{V}, I_D = 10\text{A}$	-	14.0	19.0	$\text{m}\Omega$
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{GS} = 0\text{V}, V_{DS} = 30\text{V}, f = 1\text{MHz}$	-	930	-	pF
C_{oss}	Output Capacitance		-	230	-	pF
C_{rss}	Reverse Transfer Capacitance		-	8	-	pF
Q_g	Total Gate Charge	$V_{GS} = 0 \text{ to } 10\text{V}$ $V_{DS} = 30\text{V}, I_D = 10\text{A}$	-	32.8	-	nC
Q_{gs}	Gate Source Charge		-	5.3	-	nC
Q_{gd}	Gate Drain("Miller") Charge		-	6.4	-	nC
Switching Characteristics						
$t_{d(\text{on})}$	Turn-On Delay Time	$V_{GS} = 10\text{V}, V_{DD} = 30\text{V}$ $I_D = 10\text{A}, R_{\text{GEN}} = 4.7\Omega$	-	9	-	ns
t_r	Turn-On Rise Time		-	19.4	-	ns
$t_{d(\text{off})}$	Turn-Off Delay Time		-	31.5	-	ns
t_f	Turn-Off Fall Time		-	8.9	-	ns
Drain-Source Diode Characteristics and Max Ratings						
I_s	Maximum Continuous Drain to Source Diode Forward Current	-	-	35	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	140	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_s = 20\text{A}$	-	-	1.2	V

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.

2. E_{AS} condition: Starting $T_J = 25^\circ\text{C}$, $V_{DD} = 30\text{V}$, $V_G = 10\text{V}$, $R_G = 25\text{ohm}$, $L = 0.5\text{mH}$, $I_{AS} = 14\text{A}$

3. R_{\thetaJA} is measured with the device mounted on a 1inch² pad of 2oz copper FR4 PCB

4. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$.

Typical Performance Characteristics

Figure 1: Output Characteristics

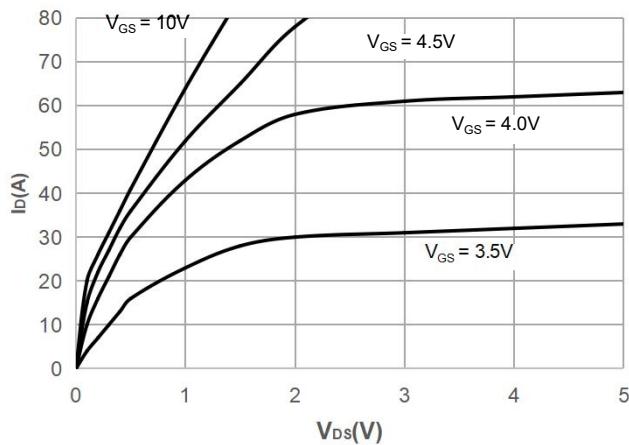


Figure 2: Typical Transfer Characteristics

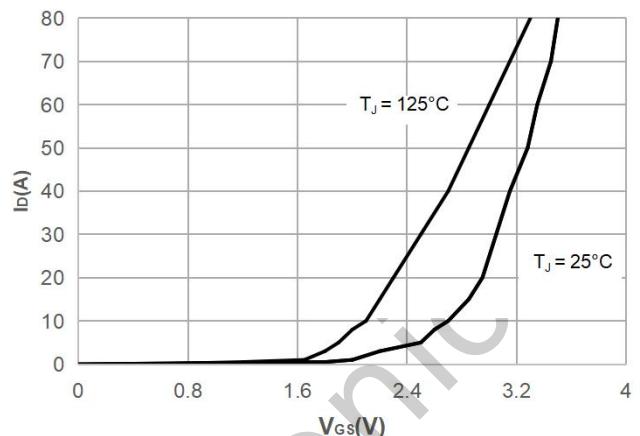


Figure 3: On-resistance vs. Drain Current

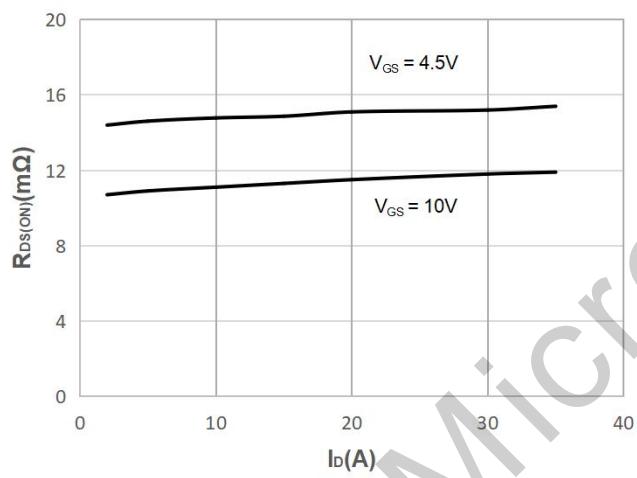


Figure 4: Body Diode Characteristics

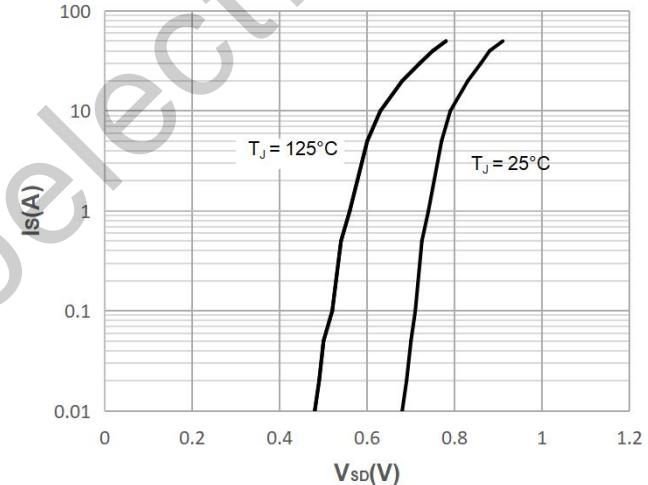


Figure 5: Gate Charge Characteristics

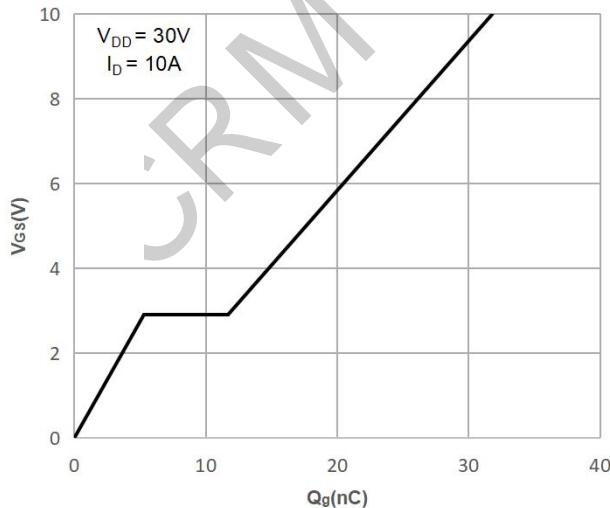
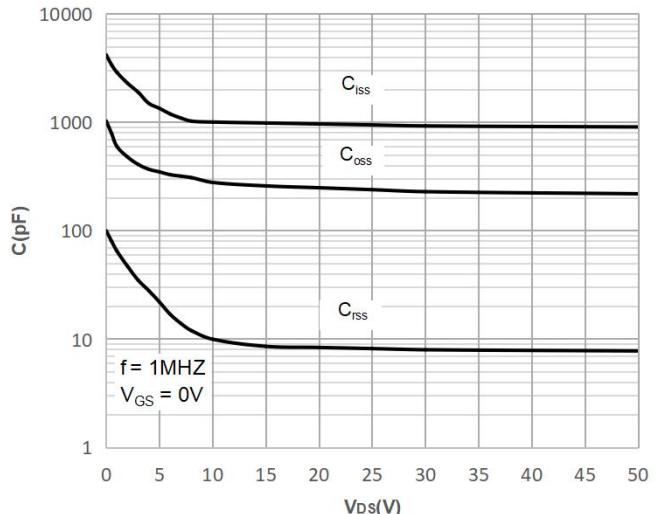


Figure 6: Capacitance Characteristics



Typical Performance Characteristics

Figure 7: Normalized Breakdown voltage vs. Junction Temperature

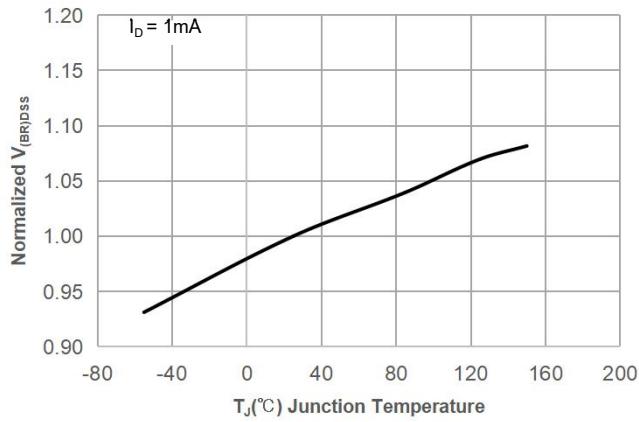


Figure 8: Normalized on Resistance vs. Junction Temperature

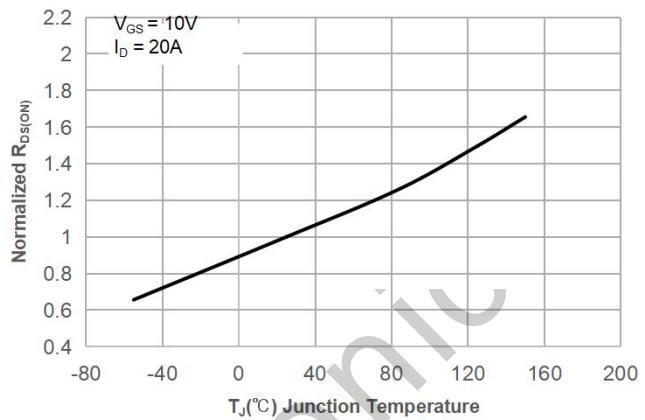


Figure 9: Maximum Safe Operating Area

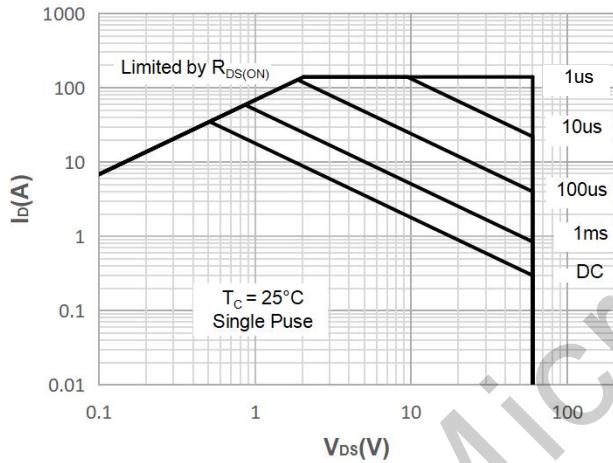


Figure 10: Maximum Continuous Drian Current vs. Case Temperature

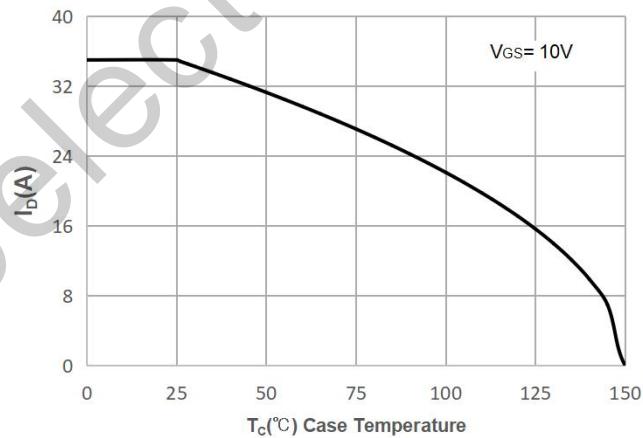


Figure 11: Normalized Maximum Transient Thermal Impedance

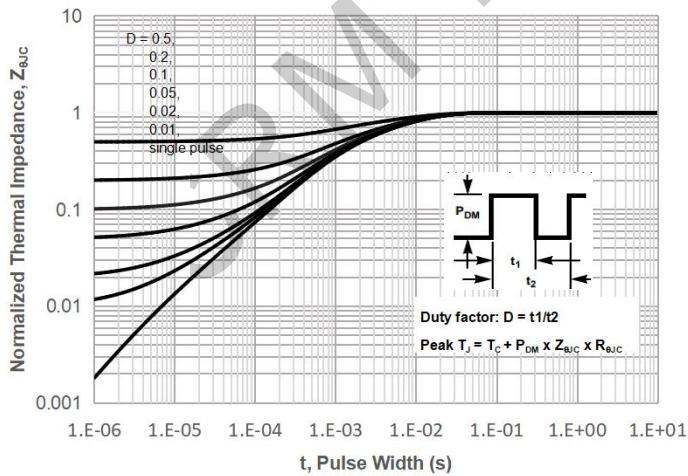
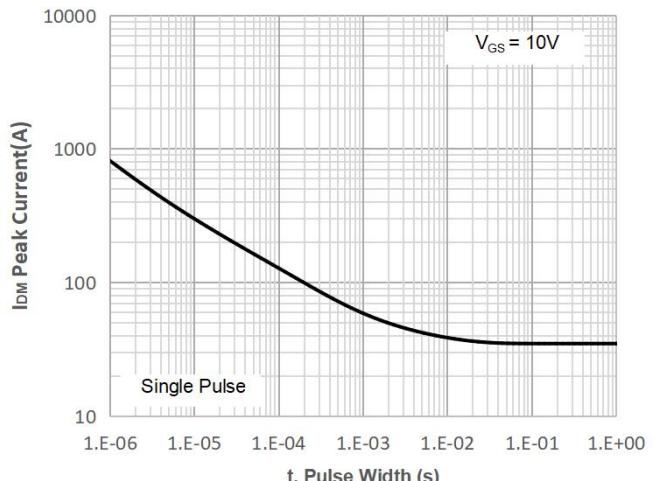


Figure 12: Peak Current Capacity



Test Circuit

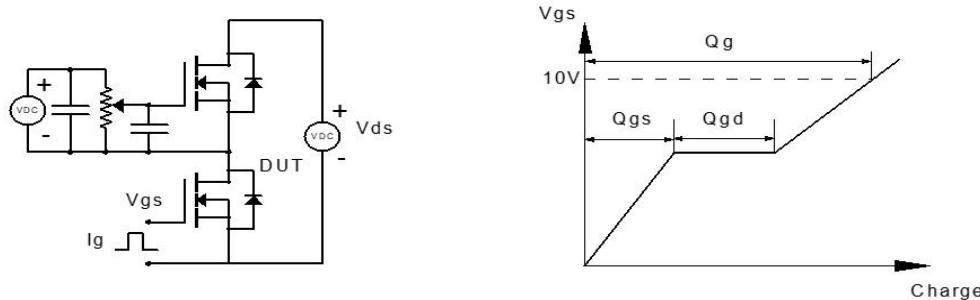


Figure 1: Gate Charge Test Circuit & Waveform

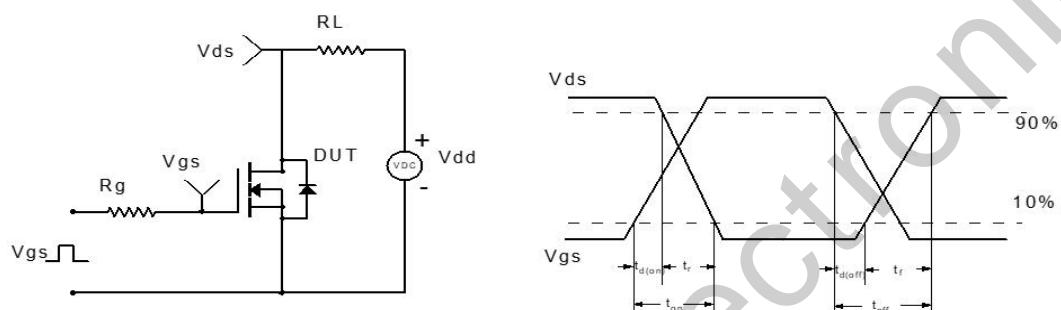


Figure 2: Resistive Switching Test Circuit & Waveform

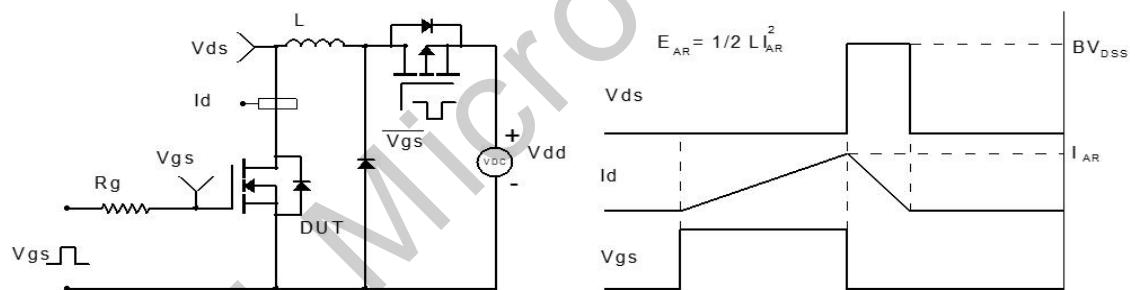


Figure 3: Unclamped Inductive Switching Test Circuit& Waveform

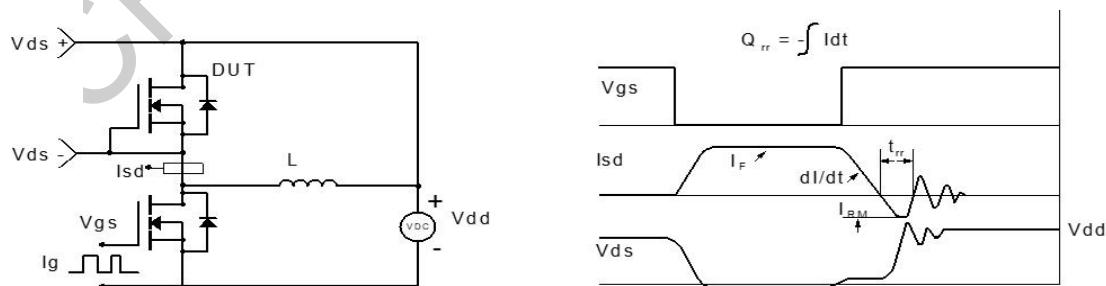
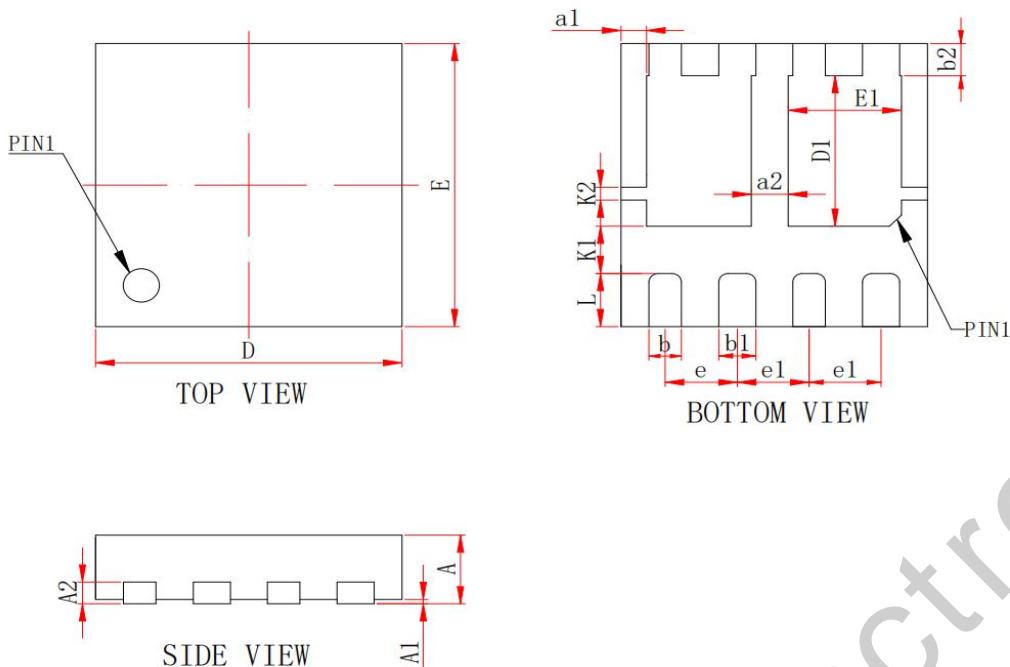


Figure 4: Diode Recovery Test Circuit & Waveform

Package Mechanical Data(DFN3.3x3.3-8L-D)



STMBOL	MIN	NOM	MAX
D	3.20	3.30	3.40
E	3.20	3.30	3.40
A	0.70	0.75	0.80
A1	0.00	-	0.05
A2	0.203REF		
L	0.50	0.60	0.70
b	0.30	0.35	0.40
b1	0.35	0.40	0.45
e	0.775BSC		
e1	0.725BSC		
K1	0.500BSC		
K2	0.200BSC		
b2	0.30	0.35	0.40
E1	0.10	1.15	1.20
D1	1.70	1.75	1.80
a1	0.30	0.35	0.40
a2	0.30	0.35	0.40

Information furnished in this document is believed to be accurate and reliable. However, CRM Microelectronics Co. , Ltd assumes no responsibility for the consequences of use without consideration for such information nor use beyond it.

Information mentioned in this document is subject to change without notice, apart from that when an agreement is signed, CRM complies with the agreement.

Products and information provided in this document have no infringement of patents. CRM assumes no responsibility for any infringement of other rights of third parties which may result from the use of such products and information.

 is a registered trademark of CRM Microelectronics Co. , Ltd.

Copyright ©2023 CRM Microelectronics Co. , Ltd. Printed All rights reserved.