### **Description**

#### N-channel Enhancement Mode Power MOSFET

#### **Features**

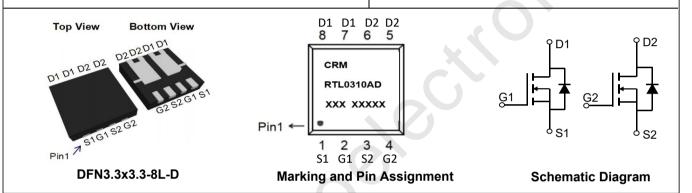
- 30V, 25A
  - $R_{DS(ON)}$  Typ=  $9m\Omega$  @  $V_{GS}$  = 10V  $R_{DS(ON)}$  Typ=  $13m\Omega$  @  $V_{GS}$  = 4.5V
- Advanced Trench Technology
- Excellent R<sub>DS(ON)</sub> and Low Gate Charge

#### **Applications**

- Load Switch
- PWM Application
- Power Management

100% UIS TESTED! 100% ΔVds TESTED!





#### Package Marking and Ordering Information

Device Marking	Device	Outline	Package	Reel Size	Reel(pcs)	Per Carton (pcs)
CRMRTL0310AD	CRMRTL0310AD	TAPING	DFN3.3x3.3-8L-D	13"	5000	50000

#### **Absolute Maximum Ratings** (@ T<sub>J</sub> = 25°C unless otherwise specified)

Symbol	Parameter		Value	Units
V <sub>DS</sub>	Drain-to-Source Voltage		30	V
$V_{GS}$	Gate-to-Source Voltage		±20	V
	Continuous Drain Current	T <sub>C</sub> = 25°C	25	
I <sub>D</sub>	Continuous Diain Current	T <sub>C</sub> = 100°C	15	А
I <sub>DM</sub>	Pulsed Drain Current <sup>(1)</sup>		100	Α
E <sub>AS</sub>	Single Pulsed Avalanche Energy (2)		36	mJ
$P_{D}$	Power Dissipation	T <sub>C</sub> = 25°C	34	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient <sup>(3)</sup>		59	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to	Case	3.7	C/VV
$T_{J}, T_{STG}$	Junction & Storage Temperature Range		-55 to 150	°C



#### **Electrical Characteristics** (T<sub>J</sub> = 25°C unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit	
Off Characteristics							
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	30	-	-	V	
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = 30V, V_{GS} = 0V$	-	-	1.0	μА	
$I_{GSS}$	Gate-Body Leakage Current	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	±100	nA	
On Cha	racteristics						
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1.0	1.5	2.2	V	
		V <sub>GS</sub> = 10V, I <sub>D</sub> = 15A	-	9 –	_11	mΩ	
$R_{DS(ON)}$	Static Drain-Source ON-Resistance <sup>(4)</sup>	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 10A	-	13	16	mΩ	
Dynamic Characteristics							
C <sub>iss</sub>	Input Capacitance		-	1060	-	pF	
C <sub>oss</sub>	Output Capacitance	$V_{GS} = 0V$ , $V_{DS} = 15V$ , f = 1MHz		122	-	pF	
$C_{rss}$	Reverse Transfer Capacitance	1 – 1101112	X- \	102	-	pF	
$Q_g$	Total Gate Charge	V 01 40V		21	-	nC	
$Q_{gs}$	Gate Source Charge	$V_{GS} = 0 \text{ to } 10V$ $V_{DS} = 15V, I_{D} = 30A$	)-	3	-	nC	
$Q_{gd}$	Gate Drain("Miller") Charge	V <sub>DS</sub> = 13V, 1 <sub>D</sub> = 30A	-	5	-	nC	
Switchi	ing Characteristics						
t <sub>d(on)</sub>	Turn-On DelayTime		-	4	-	ns	
t <sub>r</sub>	Turn-On Rise Time	$V_{GS} = 10V, V_{DD} = 15V$	-	2	-	ns	
$t_{d(off)}$	Turn-Off DelayTime	$I_D$ = 30A, $R_{GEN}$ = 3 $\Omega$	-	13	-	ns	
t <sub>f</sub>	Turn-Off Fall Time		-	7	-	ns	
Drain-S	Source Diode Characteristics and M	ax Ratings					
I <sub>s</sub>	Maximum Continuous Drain to Source Diode	Forward Current	-	-	25	Α	
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode For	ward Current	-	-	100	Α	
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	$V_{GS} = 0V, I_{S} = 15A$	-	-	1.2	V	

Notes:

- 1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
- 2.  $E_{AS}$  condition: Starting  $T_J$ =25C,  $V_{DD}$ =15V,  $V_G$ =10V,  $R_G$ =25ohm, L=0.5mH,  $I_{AS}$ =12A
- 3.  $R_{\text{\theta JA}}$  is measured with the device mounted on a 1inch  $^{\!2}$  pad of 2oz copper FR4 PCB
- 4. Pulse Test: Pulse Width $\leq$ 300µs, Duty Cycle $\leq$ 0.5%.

### **Typical Performance Characteristics**

Figure 1: Output Characteristics

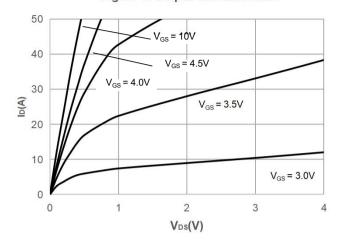


Figure 2: Typical Transfer Characteristics

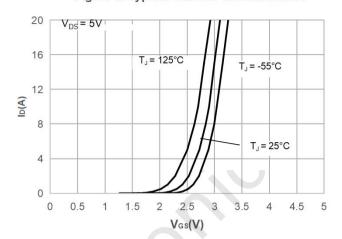


Figure 3: On-resistance vs. Drain Current

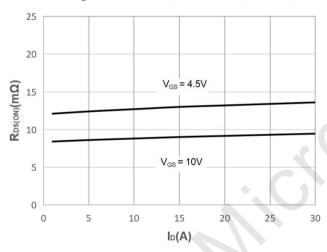


Figure 4: Body Diode Characteristics

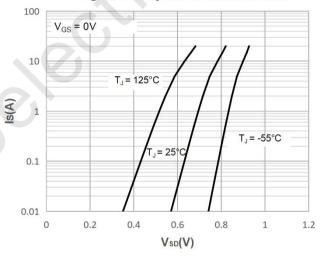


Figure 5: Gate Charge Characteristics

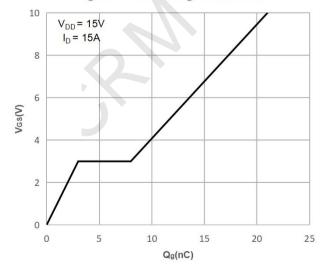
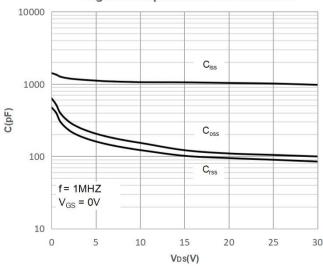


Figure 6: Capacitance Characteristics





### **Typical Performance Characteristics**

Figure 7: Normalized Breakdown voltage vs.
Junction Temperature

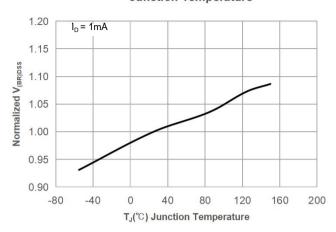


Figure 9: Maximum Safe Operating Area

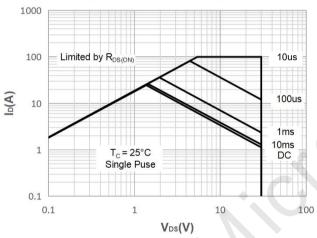


Figure 11: Normalized Maximum Transient
Thermal Impedance

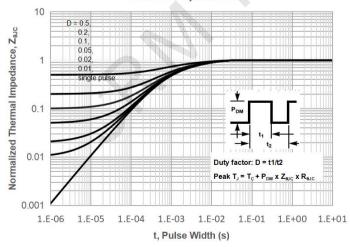


Figure 8: Normalized on Resistance vs. Junction Temperature

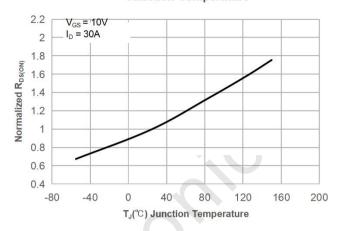


Figure 10: Maximum Continuous Drian Current vs. Case Temperature

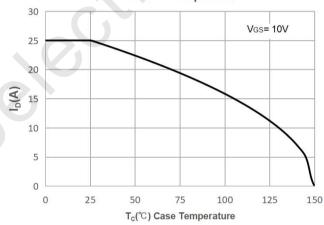
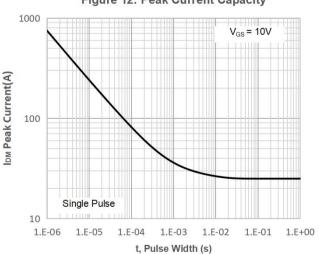


Figure 12: Peak Current Capacity





### **Test Circuit**

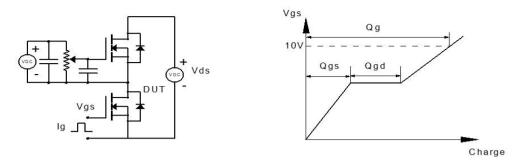


Figure 1: Gate Charge Test Circuit & Waveform

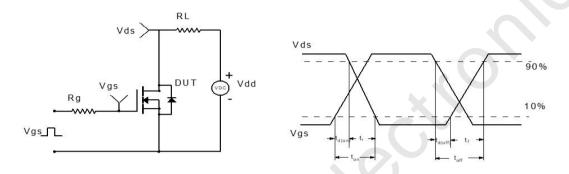


Figure 2: Resistive Switching Test Circuit & Waveform

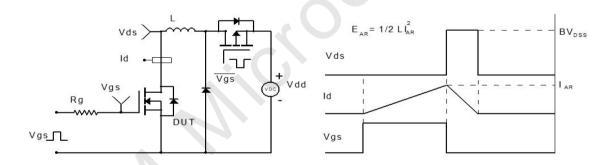


Figure 3: Unclamped Inductive Switching Test Circuit& Waveform

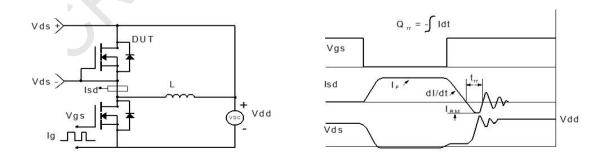
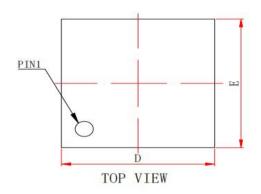
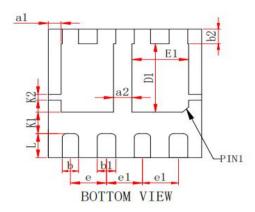


Figure 4: Diode Recovery Test Circuit & Waveform

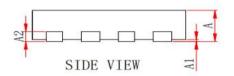


### Package Mechanical Data(DFN3.3x3.3-8L-D)





STMBOL	MIN	NOM	MAX	
D	3. 20	3.30	3. 40	
Е	3. 20	3. 30	3. 40	
A	0.70	0.75	0.80	
A1	0.00	323	0.05	
A2	0. 203REF			
L	0. 50	0.60	0. 70	
b	0.30	0. 35	0.40	
b1	0. 35	0.40	0. 45	
е	0. 775BSC			
e1	0. 725BSC			
K1	0. 500BSC			
K2	0. 200BSC			
b2	0.30	0.35	0.40	
E1	0.10	1. 15	1.20	
D1	1.70	1.75	1.80	
al	0.30	0.35	0. 40	
a2	0.30	0. 35	0.40	



Information furnished in this document is believed to be accurate and reliable. However, CRM Microelectronics Co., Ltd assumes no responsibility for the consequences of use without consideration for such information nor use beyond it.

Information mentioned in this document is subject to change without notice, apart from that when an agreement is signed, CRM complies with the agreement.

Products and information provided in this document have no infringement of patents. CRM assumes no responsibility for any infringement of other rights of third parties which may result from the use of such products and information.

is a registered trademark of CRM Microelectronics Co. , Ltd. Copyright ©2023 CRM Microelectronics Co. , Ltd. Printed All rights reserved.