

Features

- Dual N-channel Logic Level - Enhancement mode
- Uses CRM(CQ) advanced SkyMOS1 technology
- Extremely low on-resistance $R_{DS(on)}$
- Excellent $Q_g \times R_{DS(on)}$ product(FOM)
- AEC-Q101 Qualified

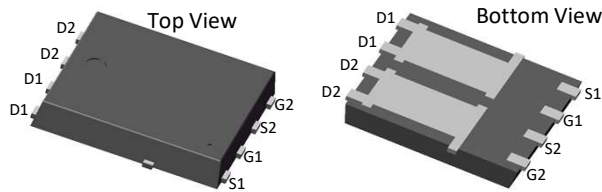
Applications

- DCDC Converter
- Switching applications
- UPS (Uninterruptible Power Supplies)

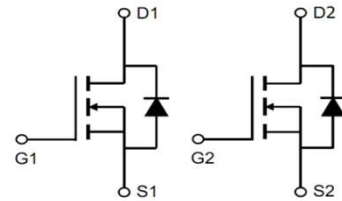
Product Summary

V_{DS}	60V
$R_{DS(on).typ}$	22mΩ
I_D	20A

100% DVDS Tested
100% Avalanche Tested



CRSM260N06LDQ


Package Marking and Ordering Information

Part #	Marking	Package	Packing	Reel Size	Tape Width	Qty
CRSM260N06LDQ	260N06LDQ	DFN5*6	Tape&reel	N/A	N/A	4000pcs

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	60	V
Continuous drain current $T_C = 25^\circ\text{C}$ (Silicon limit) $T_C = 25^\circ\text{C}$ (Package limit) $T_C = 100^\circ\text{C}$ (Silicon limit)	I_D	30 20 19	A
Pulsed drain current ($T_C = 25^\circ\text{C}$, t_p limited by T_{jmax})	$I_{D \text{ pulse}}$	80	A
Avalanche energy, single pulse ($I_{AS} = 11\text{A}$, $R_g = 25\Omega$) ^[1]	E_{AS}	30	mJ
Gate-Source voltage	V_{GS}	±20	V
Power dissipation ($T_C = 25^\circ\text{C}$)	P_{tot}	33	W
Operating junction and storage temperature	T_j, T_{stg}	-55...+175	°C
Soldering temperature, wave soldering only allowed at leads (1.6mm from case for 10s)	T_{sold}	260	°C

※. Notes:

EAS is tested at starting $T_j = 25^\circ\text{C}$, $L = 0.5\text{mH}$, $I_{AS} = 11\text{A}$, $V_{GS} = 10\text{V}$.

Thermal Resistance

Parameter	Symbol	Max	Unit
Thermal resistance, junction – case (junction-heat spreader)	R_{thJC}	4.5	°C/W
Thermal resistance, junction – ambient(min. footprint)	R_{thJA}	62	

Electrical Characteristic (at $T_j = 25^\circ\text{C}$, unless otherwise specified)

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Static Characteristic						
Drain-source breakdown voltage	BV _{DSS}	60	-	-	V	V _{GS} =0V, I _D =250uA
		60	-	-	V	V _{GS} =0V, I _D =1mA
Gate threshold voltage	V _{GS(th)}	1.5	2.0	2.5	V	V _{DS} =V _{GS} ,I _D =250uA
Zero gate voltage drain current	I _{DSS}	-	-	1	μA	V _{DS} =60V,V _{GS} =0V
		-	-	100		T _j =25°C
Gate-source leakage current	I _{GSS}	-	-	±100	nA	V _{GS} =±20V,V _{DS} =0V
Drain-source on-state resistance	R _{DS(on)}	-	22	26	mΩ	VGS=10V, ID=10A
		-	33	46		VGS=4.5V, ID=8A
Transconductance	g _{fs}	6	11	22	S	VDS=5V,ID=10A

Dynamic Characteristic

Input Capacitance	C_{iss}	330	660	1320	pF	$V_{GS}=0V, V_{DS}=30V, f=1MHz$
Output Capacitance	C_{oss}	80	160	320		
Reverse Transfer Capacitance	C_{rss}	-	7.5	38		
Gate Total Charge	Q_G	-	10	20	nC	$V_{GS}=10V, V_{DS}=30V, I_D=10A, f=1MHz$
Gate-Source charge	Q_{gs}	-	2.5	13		
Gate-Drain charge	Q_{gd}	-	2.0	10		
Turn-on delay time	$t_{d(on)}$	-	12.5	25	ns	$V_{GS}=10V, V_{DD}=30V, R_{G_ext}=3\Omega$
Rise time	t_r	-	4	20		
Turn-off delay time	$t_{d(off)}$	-	25	50		
Fall time	t_f	-	3.5	18		
Gate resistance	R_G	-	1.5	7.5	Ω	$V_{GS}=0V, V_{DS}=0V, f=1MHz$

Body Diode Characteristic

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Body Diode Forward Voltage	V_{SD}	-	0.9	1.4	V	$V_{GS}=0V, I_{SD}=10A$
Body Diode Reverse Recovery Time	t_{rr}	15	30	60	ns	$I_F=10A, dI/dt=100A/\mu s$
Body Diode Reverse Recovery Charge	Q_{rr}	15	29	60	nC	

Typical Performance Characteristics

Fig 1: Output Characteristics

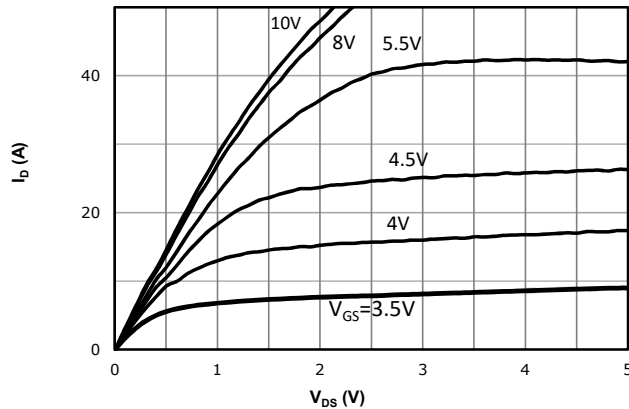


Fig 2: Transfer Characteristics

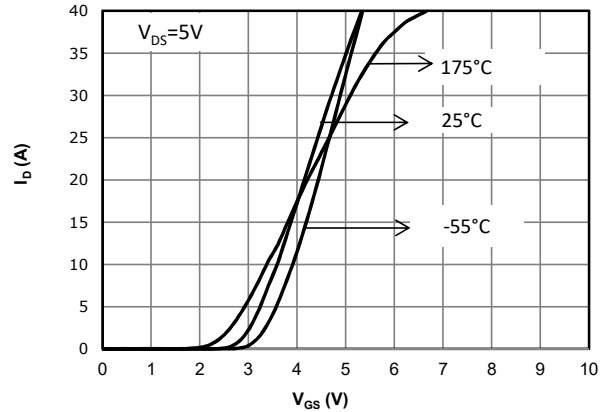


Fig 3: $R_{DS(on)}$ vs Drain Current and Gate Voltage

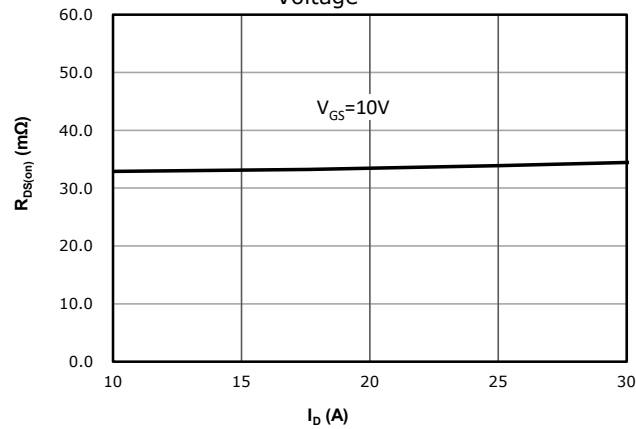


Fig 4: $R_{DS(on)}$ vs Gate Voltage

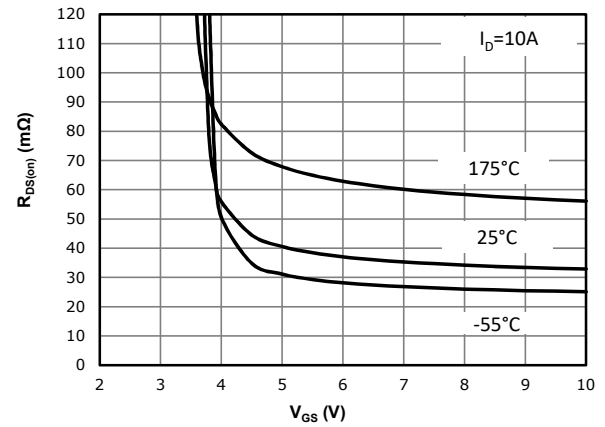


Fig 5: $R_{DS(on)}$ vs. Temperature

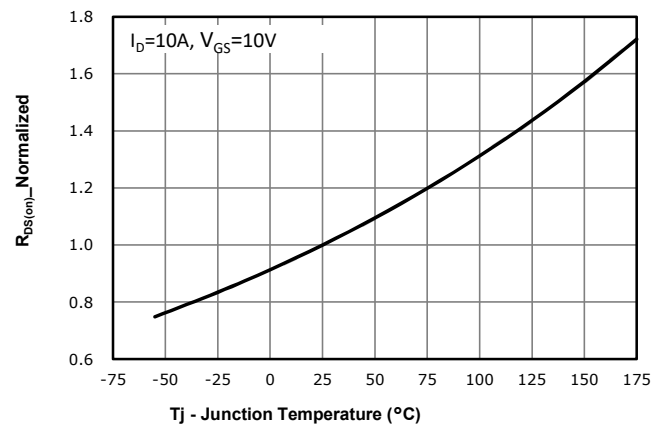


Fig 6: $V_{GS(th)}$ vs. Temperature

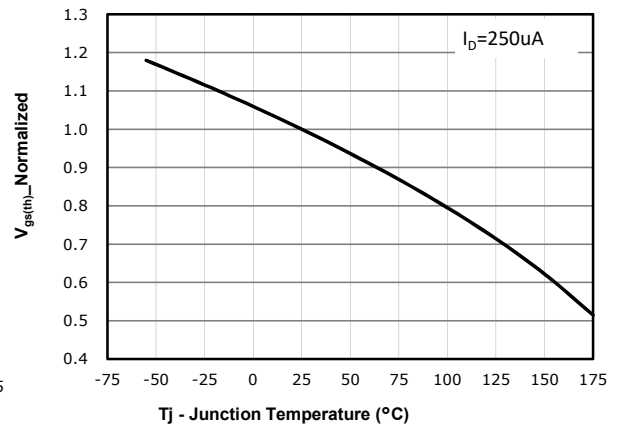


Fig 7: BVdss vs. Temperature

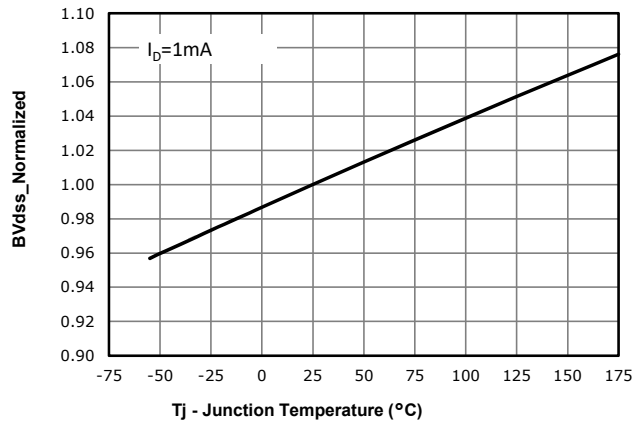


Fig 8: Capacitance Characteristics

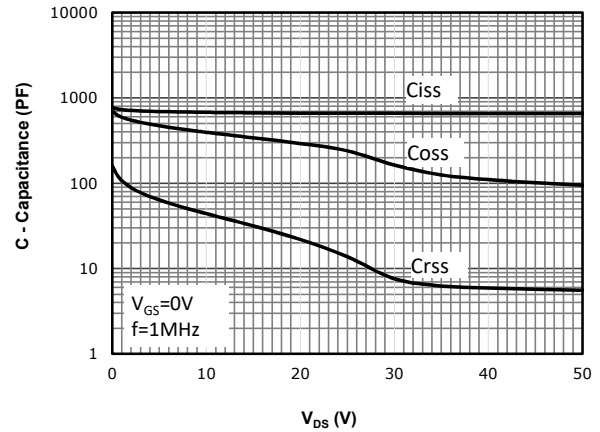


Fig 9: Gate Charge Characteristics

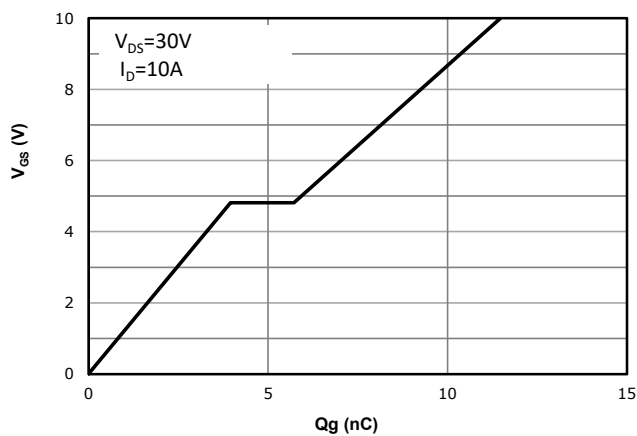


Fig 10: Body-diode Forward Characteristics

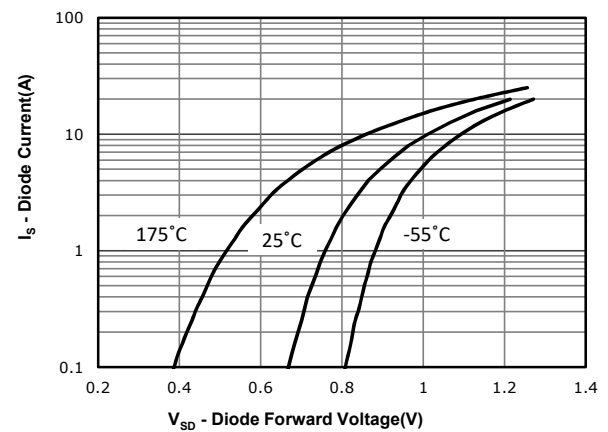


Fig 11: Power Dissipation

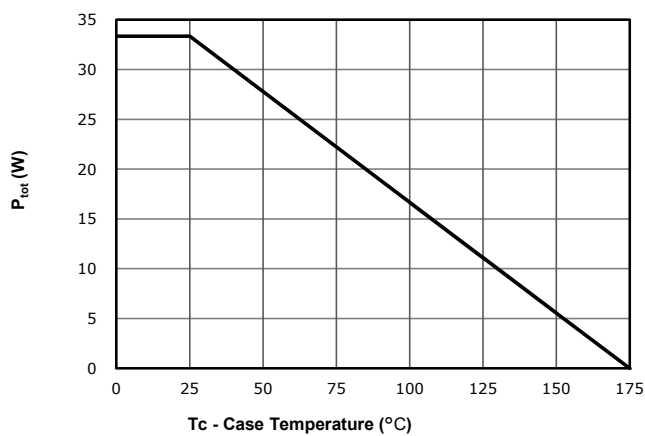


Fig 12: Drain Current Derating

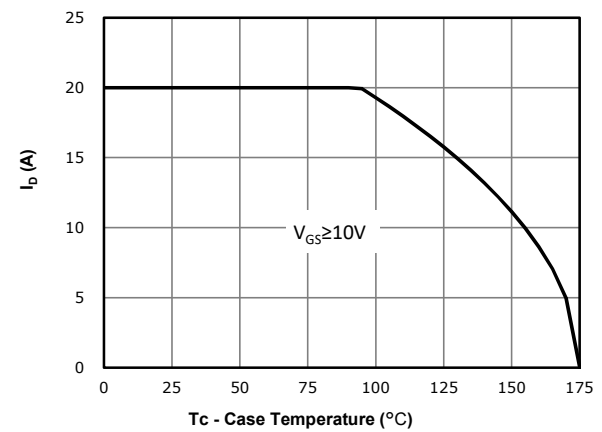


Fig 13: Safe Operating Area

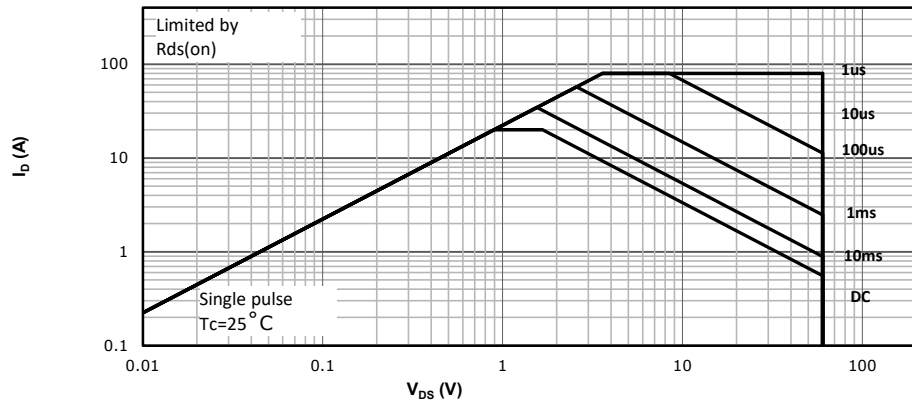
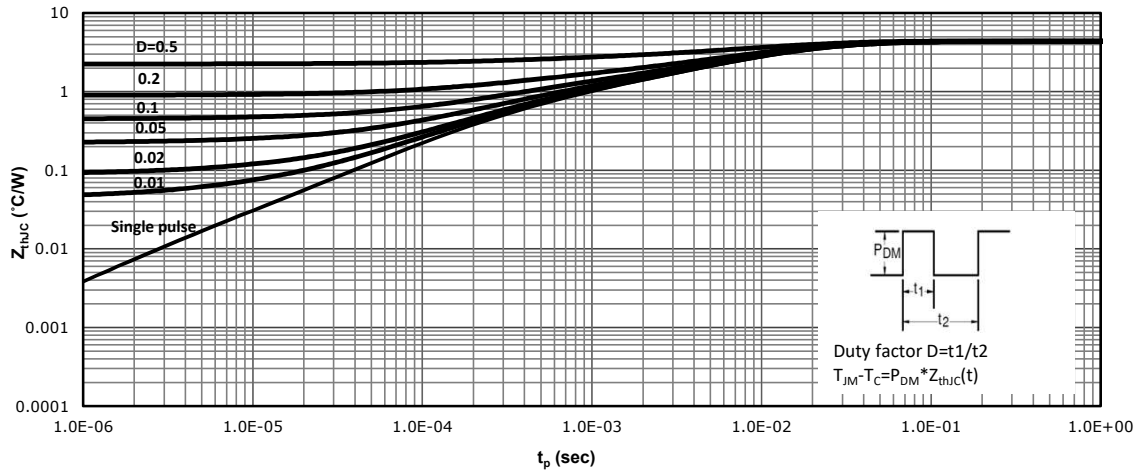
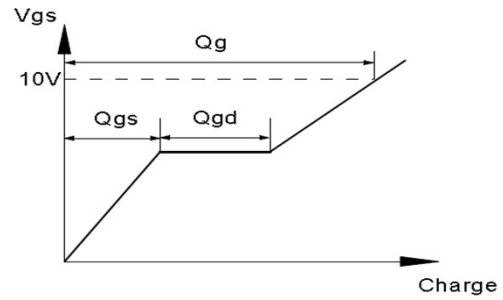
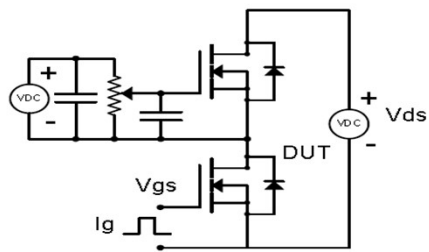


Fig 14: Max. Transient Thermal Impedance

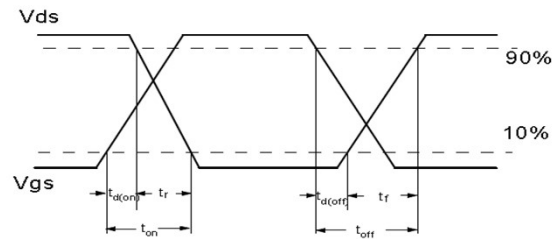
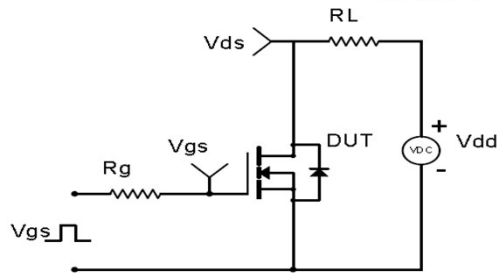


Test Circuit & Waveform

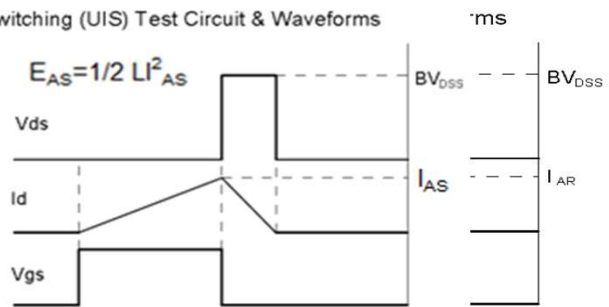
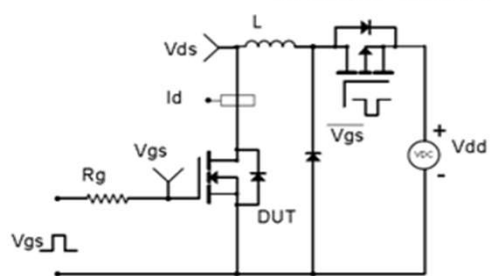
Gate Charge Test Circuit & Waveform



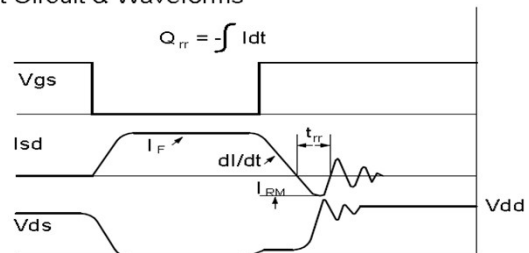
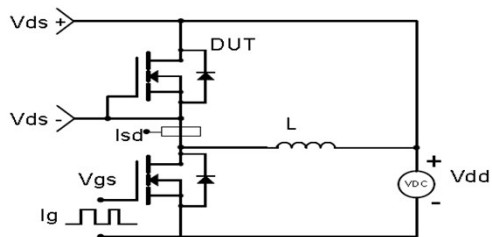
Resistive Switching Test Circuit & Waveforms



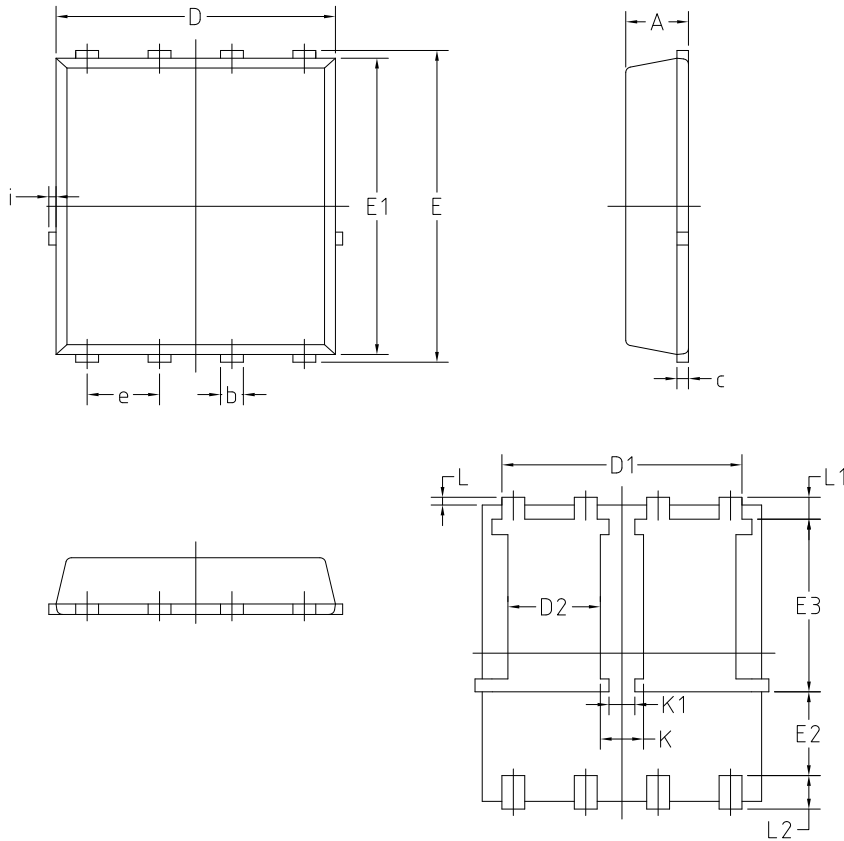
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Package Outline: PDFN5x6 Dual Pad Type 6



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.00	1.20	0.039	0.047
b	0.30	0.50	0.012	0.020
c	0.203 BSC		0.008 BSC	
D	4.80	5.00	0.189	0.197
D1	4.06	4.36	0.160	0.172
D2	1.47	1.77	0.058	0.070
E	5.90	6.20	0.232	0.244
E1	5.65	5.85	0.222	0.230
E2	1.45	-	0.057	-
E3	3.20	3.50	0.126	0.138
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.002	0.010
L1	0.325	0.525	0.013	0.021
L2	0.50	0.80	0.020	0.031
i	-	0.20	-	0.008
K	0.61	0.91	0.024	0.036
K1	0.31	0.60	0.012	0.024

Marking**NOTE:**

XAAAAAAAA-Y

X

—Assembly location code

AAAAAAA

—Assembly lot NO. last 7digits

Y

—Bin code

Revision History

Revision	Date	Major changes
1.0	2023/8/20	Release of preliminary version.

Disclaimer

CRM reserves the right to change any product or information in this Specification at any time without prior notice.

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