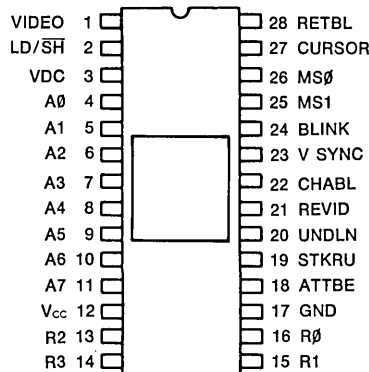


CRT Video Display Attributes Controller Video Generator VDAC™

FEATURES

- ☐ On chip character generator (mask programmable)
128 Characters (alphanumeric and graphic)
7 x 11 Dot matrix block
- ☐ On chip video shift register
Maximum shift register frequency 25 MHz
- ☐ ROM Access time 310 ns
- ☐ On chip horizontal and vertical retrace video blanking
- ☐ No descender circuitry required
- ☐ Four modes of operation (intermixable)
Internal character generator (ROM)
Wide graphics
Thin graphics
External inputs (fonts/dot graphics)
- ☐ On chip attribute logic—character, field
Reverse video
Character blank
Character blink
Underline
Strike-thru
- ☐ On chip cursor
- ☐ Programmable character blink rate
- ☐ Programmable cursor blink rate
- ☐ Subscriptable
- ☐ Expandable character set
External fonts
Alphanumeric and graphic
RAM, ROM, and PROM

PIN CONFIGURATION



- ☐ On chip address buffer
- ☐ On chip attribute buffer
- ☐ +5 volt operation
- ☐ TTL compatible
- ☐ N-channel COPLAMOS® Titanium
Disilicide Process
- ☐ Compatible with CRT 5027/37 VTAC®

General Description

The SMC CRT 8002H Video Display Attributes Controller (VDAC) is an n-channel COPLAMOS® MOS/LSI device. It contains a 7X11X128 character generator ROM, a wide graphics mode, a thin graphics mode, an external input mode, character address/data latch, field and/or character attribute logic, attribute latch, four cursor modes, two programmable blink rates, and a high speed video shift register. The CRT 8002H VDAC is a companion chip to SMC's CRT 5027/37 VTAC®. Together these two chips comprise the circuitry required for the display portion of a CRT video terminal.

The CRT 8002H video output may be connected directly to a CRT monitor video input. The CRT 5027/37 blanking output can be connected directly to the CRT 8002H retrace blank input to provide both horizontal and vertical retrace blanking of the video output.

The CRT 8002H attributes include: reverse video, character blank, blink, underline, and strike-thru. The character blink rate is mask programmable from 7.5 Hz to 1.0 Hz and has a duty cycle of 75/25. The underline

and strike-thru are similar but independently controlled functions and can be mask programmed to any number of raster lines at any position in the character block. These attributes are available in all modes.

In the wide graphic mode the CRT 8002H produces a graphic entity the size of the character block. The graphic entity contains 8 parts, each of which is associated with one bit of a graphic byte, thereby providing for 256 unique graphic symbols. Thus, the CRT 8002H can produce either an alphanumeric symbol or a graphic entity depending on the mode selected. The mode can be changed on a per character basis.

The thin graphic mode enables the user to create single line drawings and forms.

The external mode enables the user to extend the on-chip ROM character set and/or the on-chip graphics capabilities by inserting external symbols. These external symbols can come from either RAM, ROM or PROM.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range0°C to + 70°C
Storage Temperature Range–55°C to +150°C
Lead Temperature (soldering, 10 sec.)+325°C
Positive Voltage on any Pin, with respect to ground+8.0V
Negative Voltage on any Pin, with respect to ground–0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or “glitches” on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS ($T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=+5V\pm5\%$, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}	2.0		0.8	V	excluding VDC
High-level, V_{IH}				V	excluding VDC
INPUT VOLTAGE LEVELS-CLOCK					
Low-level, V_{iL}	4.3		0.8	V	See Figure 6
High-level, V_{iH}				V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}	2.4		0.4	V	$I_{OL} = 0.4\text{ mA}$, 74LSXX load $I_{OH} = -20\mu\text{A}$
High-level, V_{OH}				V	
INPUT CURRENT					
Leakage, I_L (Except CLOCK)			10	μA	$0 \leq V_{IN} \leq V_{CC}$
Leakage, I_L (CLOCK Only)			50	μA	$0 \leq V_{IN} \leq V_{CC}$
INPUT CAPACITANCE					
Data		10		pF	@ 1 MHz
LD/SH		20		pF	@ 1 MHz
CLOCK		25		pF	@ 1 MHz
POWER SUPPLY CURRENT					
I_{CC}		100		mA	
A.C. CHARACTERISTICS					
See Figure 6, 7					

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
VDC	Video Dot Clock Frequency	1.0	25	MHz
PW _H	VDC— High Time	11.0		ns
PW _L	VDC— Low Time	11.0		ns
t _{cy}	LD/SH cycle time	310		ns
t _r , t _f	Rise, fall time		9	ns
t _{SET-UP}	Input set-up time	≥0		ns
t _{HOLD}	Input hold time	15		ns
t _{PDI} , t _{PDO}	Output propagation delay	15	27	ns
t ₁	LD/SH set-up time	5		ns
t ₂	LD/SH hold time	5		ns

BLOCK DIAGRAM

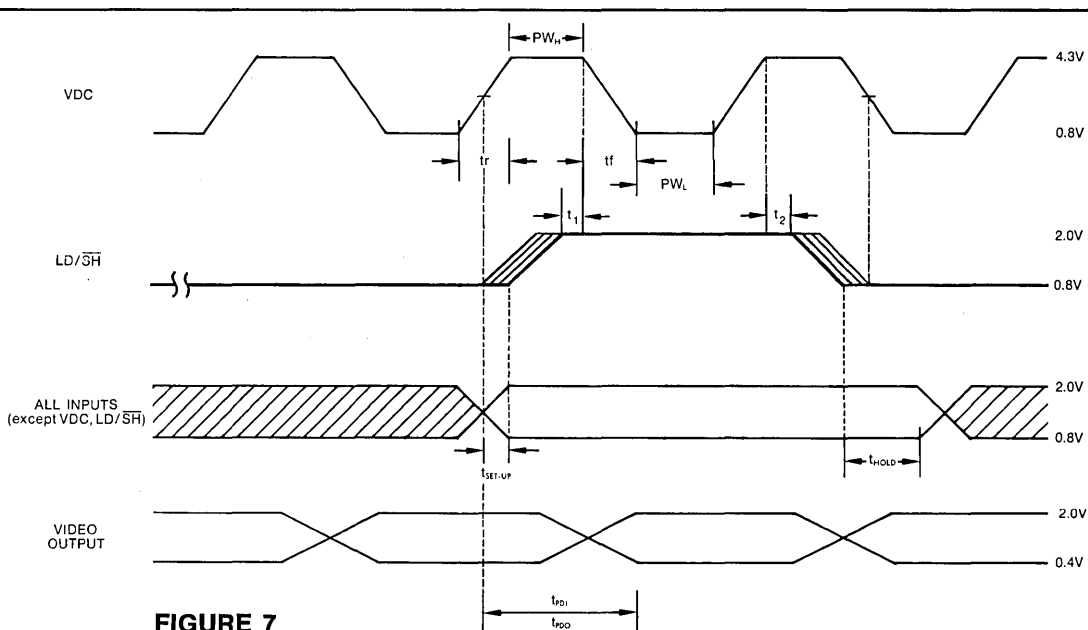
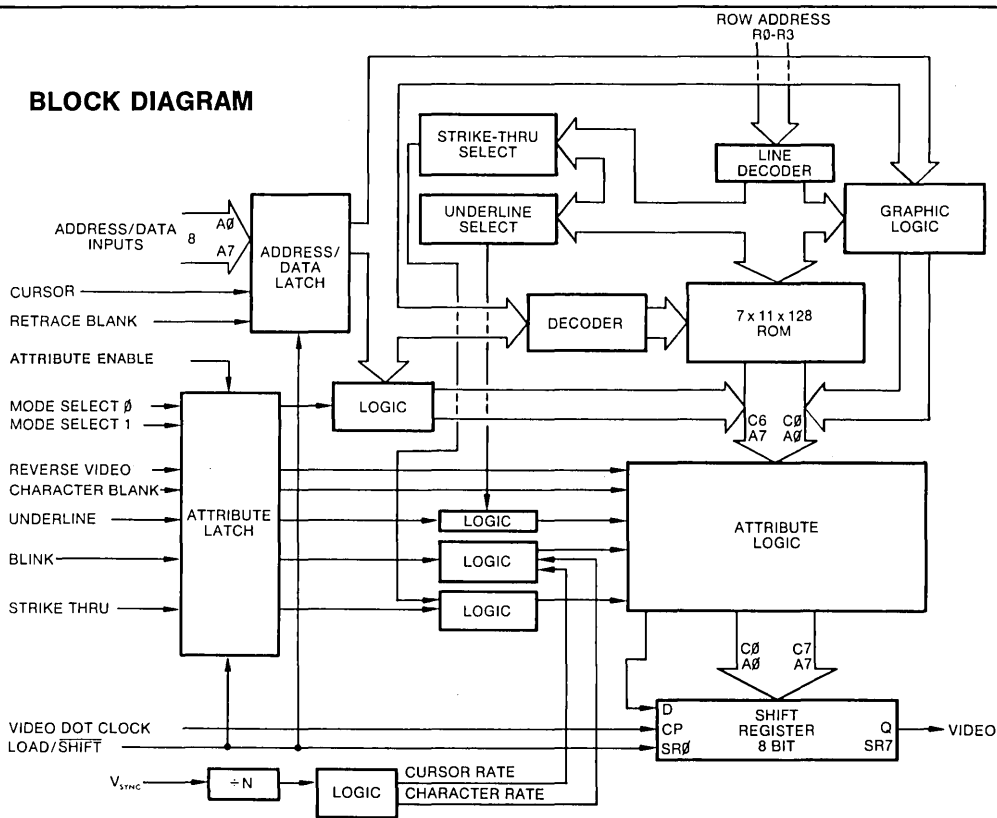


FIGURE 7
AC TIMING DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	INPUT/ OUTPUT	FUNCTION															
1	VIDEO	Video Output	0	<p>The video output contains the dot stream for the selected row of the alphanumeric, wide graphic, thin graphic, or external character after processing by the attribute logic, and the retrace blank and cursor inputs.</p> <p>In the alphanumeric mode, the characters are ROM programmed into the 77 dots, (7X11) allocated for each of the 128 characters. See figure 5. The top row (R0) and rows R12 to R15 are normally all zeros as is column C7. Thus, the character is defined in the box bounded by R1 to R11 and C0 to C6. When a row of the ROM, via the attribute logic, is parallel loaded into the 8-bit shift-register, the first bit serially shifted out is C7 (A zero; or a one in REVID). It is followed by C6, C5, through C0.</p> <p>The timing of the Load/Shift pulse will determine the number of additional (—, zero to N) backfill zeros (or ones if in REVID) shifted out. See figure 4.</p> <p>When the next Load/Shift pulse appears the next character's row of the ROM via the attribute logic, is parallel loaded into the shift register and the cycle repeats.</p>															
2	LD/SH	Load/Shift	I	<p>The 8 bit shift-register parallel-in load or serial-out shift modes are established by the Load/Shift input. When low, this input enables the shift register for serial shifting with each Video Dot Clock pulse. When high, the shift register parallel (broadside) data inputs are enabled and synchronous loading occurs on the next Video Dot Clock pulse. During parallel loading, serial data flow is inhibited. The Address/Data inputs (A0-A7) are latched on the negative transition of the Load/Shift input. See timing diagram, figure 7.</p>															
3	VDC	Video Dot Clock	I	<p>Frequency at which video is shifted.</p>															
4-11	A0-A7	Address/Data	I	<p>In the Alphanumeric Mode the 7 bits on inputs (A0-A6) are internally decoded to address one of the 128 available characters (A7 = X). In the External Mode, A0-A7 is used to insert an 8 bit word from a user defined external ROM, PROM or RAM into the on-chip Attribute logic. In the wide Graphic Modes A0-A7 is used to define one of 256 graphic entities. In the thin Graphic Mode A0-A2 is used to define the 3 line segments.</p>															
12	Vcc	Power Supply	PS	<p>+ 5 volt power supply</p>															
13,14,15,16	R2,R3,R1,R0	Row Address	I	<p>These 4 binary inputs define the row address in the current character block.</p>															
17	GND	Ground	GND	<p>Ground</p>															
18	ATTBE	Attribute Enable	I	<p>A positive level on this input enables data from the Reverse Video, Character Blank, Underline, Strike-Thru, Blink, Mode Select 0, and Mode Select 1 inputs to be strobed into the on-chip attribute latch at the negative transition of the Load/Shift pulse. The latch loading is disabled when this input is low. The latched attributes will remain fixed until this input becomes high again. To facilitate attribute latching on a character by character basis, tie ATTBE high. See timing diagram, figure 7.</p>															
19	STKRU	Strike-Thru	I	<p>When this input is high and RETBL = 0, the parallel inputs to the shift register are forced high (SR0-SR7), providing a solid line segment throughout the character block. The operation of strike-thru is modified by Reverse Video (see table 1). In addition, an on-chip ROM programmable decoder is available to decode the line count on which strike-thru is to be placed as well as to program the strike-thru to be 1 to N raster lines high. Actually, the strike-thru decoder (mask programmable) logic allows the strike-thru to be any number or arrangement of horizontal lines in the character block. The standard strike-thru will be a double line on rows R5 and R6.</p>															
20	UNDLN	Underline	I	<p>When this input is high and RETBL = 0, the parallel inputs to the shift register are forced high (SR0-SR7), providing a solid line segment throughout the character block. The operation of underline is modified by Reverse Video (see table 1). In addition, an on-chip ROM programmable decoder is available to decode the line count on which underline is to be placed as well as to program the underline to be 1 to N raster lines high. Actually, the underline decoder (mask programmable) logic allows the underline to be any number or arrangement of horizontal lines in the character block. The standard underline will be a single line on R11.</p>															
21	REVID	Reverse Video	I	<p>When this input is low and RETBL = 0, data into the Attribute Logic is presented directly to the shift register parallel inputs. When reverse video is high data into the Attribute Logic is inverted and then presented to the shift register parallel inputs. This operation reverses the data and field video. See table 1.</p>															
22	CHABL	Character Blank	I	<p>When this input is high, the parallel inputs to the shift register are all set low, providing a blank character line segment. Character blank will override blink. The operation of Character Blank is modified by the Reverse Video input. See table 1.</p>															
23	V SYNC	V SYNC	I	<p>This input is used as the clock input for the two on-chip mask programmable blink rate dividers. The cursor blink rate (50/50 duty cycle) will be twice the character blink rate (75/25 duty cycle). The divisors can be programmed from ÷ 4 to ÷ 30 for the cursor (÷ 8 to ÷ 60 for the character).</p>															
24	BLINK	Blink	I	<p>When this input is high and RETBL = 0 and CHABL = 0, the character will blink at the programmed character blink rate. Blinking is accomplished by blanking the character block with the internal Character Blink clock. The standard character blink rate is 1.875 Hz.</p>															
25 26	MS1 MS0	Mode Select 1 Mode Select 0	I I	<p>These 2 inputs define the four modes of operation of the CRT 8002 as follows:</p> <p>Alphanumeric Mode— In this mode addresses A0-A6 (A7=X) are internally decoded to address 1 of the 128 available ROM characters. The addressed character along with the decoded row will define a 7 bit output from the ROM to be loaded into the shift register via the attribute logic.</p> <p>Thin Graphics Mode— In this mode A0-A2 (A3-A7=X) will be loaded into the thin graphic logic along with the row addresses. This logic will define the segments of a graphic entity as defined in figure 2. The top of the entity will begin on row 0000 and will end on a mask programmable row.</p>															
<table><tr><th>MS1</th><th>MS0</th><th>MODE</th></tr><tr><td>1</td><td>1</td><td>Alphanumeric</td></tr><tr><td>1</td><td>0</td><td>Thin Graphics</td></tr><tr><td>0</td><td>1</td><td>External Mode</td></tr><tr><td>0</td><td>0</td><td>Wide Graphics</td></tr></table>				MS1	MS0	MODE	1	1	Alphanumeric	1	0	Thin Graphics	0	1	External Mode	0	0	Wide Graphics	
MS1	MS0	MODE																	
1	1	Alphanumeric																	
1	0	Thin Graphics																	
0	1	External Mode																	
0	0	Wide Graphics																	

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	INPUT/OUTPUT	FUNCTION
25 26 (cont.)				<p>External Mode—In this mode the inputs A0-A7 go directly from the character latch into the shift register via the attribute logic. Thus the user may define external character fonts or graphic entities in an external PROM, ROM or RAM. See figure 3.</p> <p>Wide Graphics Mode—In this mode the inputs A0-A7 will define a graphic entity as described in figure 1. Each line of the graphic entity is determined by the wide graphic logic in conjunction with the row inputs R0 to R3. In this mode each segment of the entity is defined by one of the bits of the 8 bit word. Therefore, the 8 bits can define any 1 of the 256 possible graphic entities. These entities can butt up against each other to form a contiguous pattern or can be interspaced with alphanumeric characters. Each of the entities occupies the space of 1 character block and thus requires 1 byte of memory.</p> <p>These 4 modes can be intermixed on a per character basis.</p>
27	CURSOR	Cursor	I	<p>When this input is enabled 1 of the 4 pre-programmed cursor modes will be activated. The cursor mode is on-chip mask programmable. The standard cursor will be a blinking (at 3.75Hz) reverse video block. The 4 cursor modes are:</p> <p>Underline—In this mode an underline (1 to N raster lines) at the programmed underline position occurs.</p> <p>Blinking Underline—In this mode the underline blinks at the cursor rate.</p> <p>Reverse Video Block—In this mode the Character Block is set to reverse video.</p> <p>Blinking Reverse Video Block—In this mode the Character Block is set to reverse video at the cursor blink rate. The Character Block will alternate between normal video and reverse video.</p> <p>The cursor functions are listed in table 1.</p>
28	RETBL	Retrace Blank	I	<p>When this input is latched high, the shift register parallel inputs are unconditionally cleared to all zeros and loaded into the shift register on the next Load/Shift pulse. This blanks the video, independent of all attributes, during horizontal and vertical retrace time.</p>

TABLE 1

CURSOR	RETBL	REVID	CHABL	UNDLN*	FUNCTION
X	1	X	X	X	"0" (S.R.) All
0	0	0	0	0	D (S.R.) All
0	0	0	0	1	"1" (S.R.)*
0	0	0	1	X	D (S.R.) All others
0	0	1	0	0	D (S.R.) All
0	0	1	0	1	"0" (S.R.)*
0	0	1	1	X	D (S.R.) All others
0	0	1	1	X	"1" (S.R.) All
Underline*	0	0	0	X	"1" (S.R.)*
Underline*	0	0	1	X	D (S.R.) All others
Underline*	0	1	0	X	"1" (S.R.)*
Underline*	0	1	0	X	"0" (S.R.) All others
Underline*	0	1	1	X	D (S.R.) All others
Underline*	0	1	1	X	"0" (S.R.)*
Underline*	0	1	1	X	"1" (S.R.) All others
Blinking** Underline*	0	0	0	X	"1" (S.R.)* Blinking
Blinking** Underline*	0	0	1	X	D (S.R.) All others
Blinking** Underline*	0	1	0	X	"1" (S.R.)* Blinking
Blinking** Underline*	0	1	0	X	"0" (S.R.) All others
Blinking** Underline*	0	1	1	X	D (S.R.) All others
Blinking** Underline*	0	1	1	X	"0" (S.R.)* Blinking
Blinking** Underline*	0	1	1	X	"1" (S.R.) All others
REVID Bldck	0	0	0	0	D (S.R.) All
REVID Bldck	0	0	0	1	"0" (S.R.)*
REVID Bldck	0	0	1	X	D (S.R.) All others
REVID Bldck	0	0	0	1	"1" (S.R.) All
REVID Bldck	0	0	0	1	"0" (S.R.)*
REVID Bldck	0	1	0	0	D (S.R.) All others
REVID Bldck	0	1	0	1	D (S.R.) All
REVID Bldck	0	1	0	1	"1" (S.R.)*
REVID Bldck	0	1	1	X	D (S.R.) All others
REVID Bldck	0	1	1	X	"0" (S.R.) All
Blink** REVID Block	0	0	0	0	D (S.R.) All
Blink** REVID Block	0	0	0	1	"0" (S.R.)*
Blink** REVID Block	0	0	1	X	D (S.R.) All others
Blink** REVID Block	0	1	0	0	"1" (S.R.) All
Blink** REVID Block	0	1	0	1	"0" (S.R.)*
Blink** REVID Block	0	1	1	X	D (S.R.) All others
Blink** REVID Block	0	1	1	X	"0" (S.R.) All

*At Selected Row Decode **At Cursor Blink Rate

Note: If Character is Blinking at Character Rate, Cursor will change it to Cursor Blink Rate.

ROM CHARACTER BLOCK FORMAT

											ROWS	R3	R2	R1	R0
(ALL ZEROS) →											R0	0	0	0	0
77 BITS (7 x 11 ROM)	0	0	0	0	0	0	0	0	0	0	R1	0	0	0	1
	0	0	0	0	0	0	0	0	0	0	R2	0	0	1	0
	0	0	0	0	0	0	0	0	0	0	R3	0	0	1	1
	0	0	0	0	0	0	0	0	0	0	R4	0	1	0	0
	0	0	0	0	0	0	0	0	0	0	R5	0	1	0	1
	0	0	0	0	0	0	0	0	0	0	R6	0	1	1	0
	0	0	0	0	0	0	0	0	0	0	R7	0	1	1	1
	0	0	0	0	0	0	0	0	0	0	R8	1	0	0	0
	0	0	0	0	0	0	0	0	0	0	R9	1	0	0	1
	0	0	0	0	0	0	0	0	0	0	R10	1	0	1	0
(ALL ZEROS)	0	0	0	0	0	0	0	0	0	0	R11	1	0	1	1
	0	0	0	0	0	0	0	0	0	0	R12	1	1	0	0
	0	0	0	0	0	0	0	0	0	0	R13	1	1	0	1
	0	0	0	0	0	0	0	0	0	0	R14	1	1	1	0
	0	0	0	0	0	0	0	0	0	0	R15	1	1	1	1

*C7 C6 C5 C4 C3 C2 C1 C0

*COLUMN 7 IS ALL ZEROS (REVID = 0)
COLUMN 7 IS SHIFTED OUT FIRST

EXTENDED ZEROS (BACK FILL)
FOR INTERCHARACTER SPACING
(NUMBER CONTROLLED
BY LD/SH, VDC TIMING)

A3..A0		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
A6..A4		C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0
000	R1																
	R11																
001	R1																
	R11																
010	R1																
	R11																
011	R1																
	R11																
100	R1																
	R11																
101	R1																
	R11																
110	R1																
	R11																
111	R1																
	R11																

CONSULT FACTORY FOR CUSTOM FONT AND OPTION PROGRAMMING FORMS.

FIGURE 1
WIDE GRAPHICS MODE
 $MS0=0 \quad MS1=0$

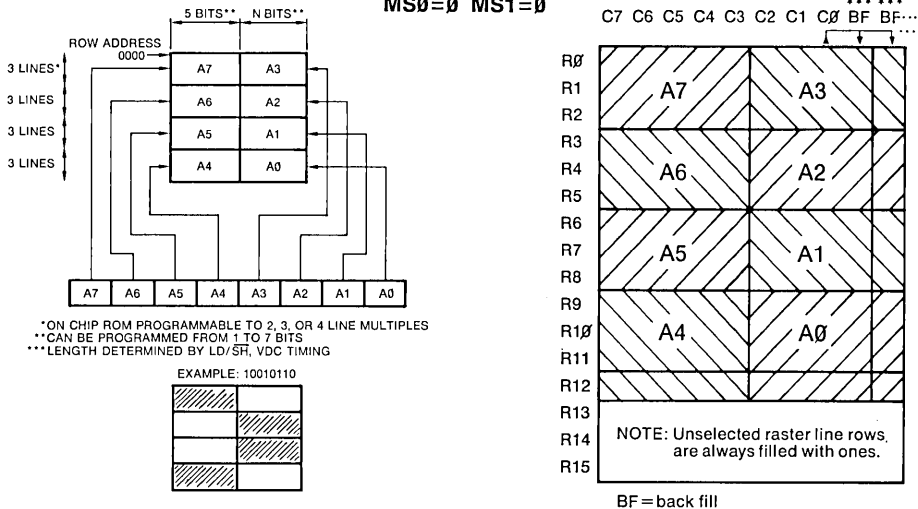


FIGURE 2
THIN GRAPHICS MODE
 $MS0=0 \quad MS1=1$

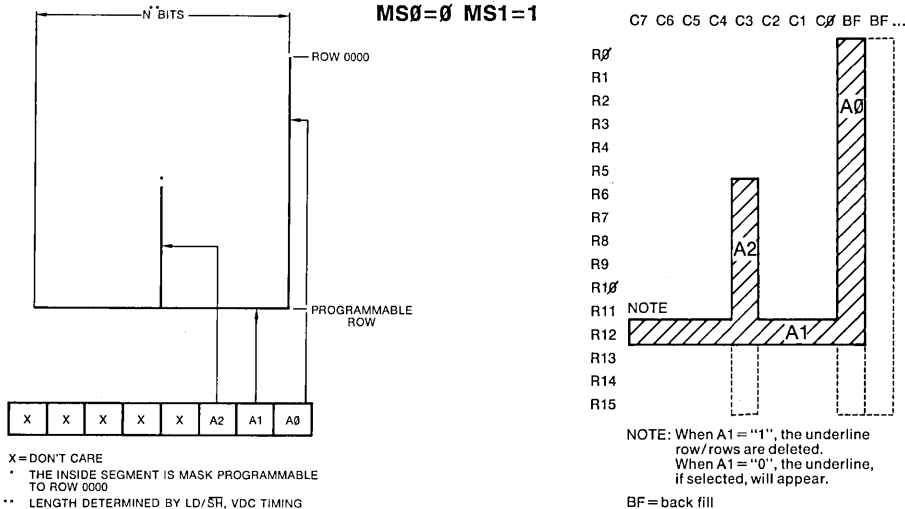


FIGURE 3
EXTERNAL MODE
 $MS0=1 \quad MS1=0$

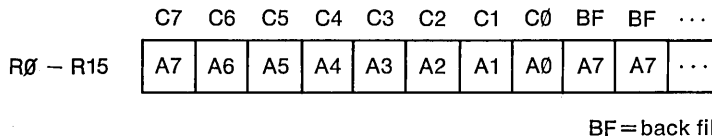


FIGURE 4 TYPICAL VIDEO OUTPUT

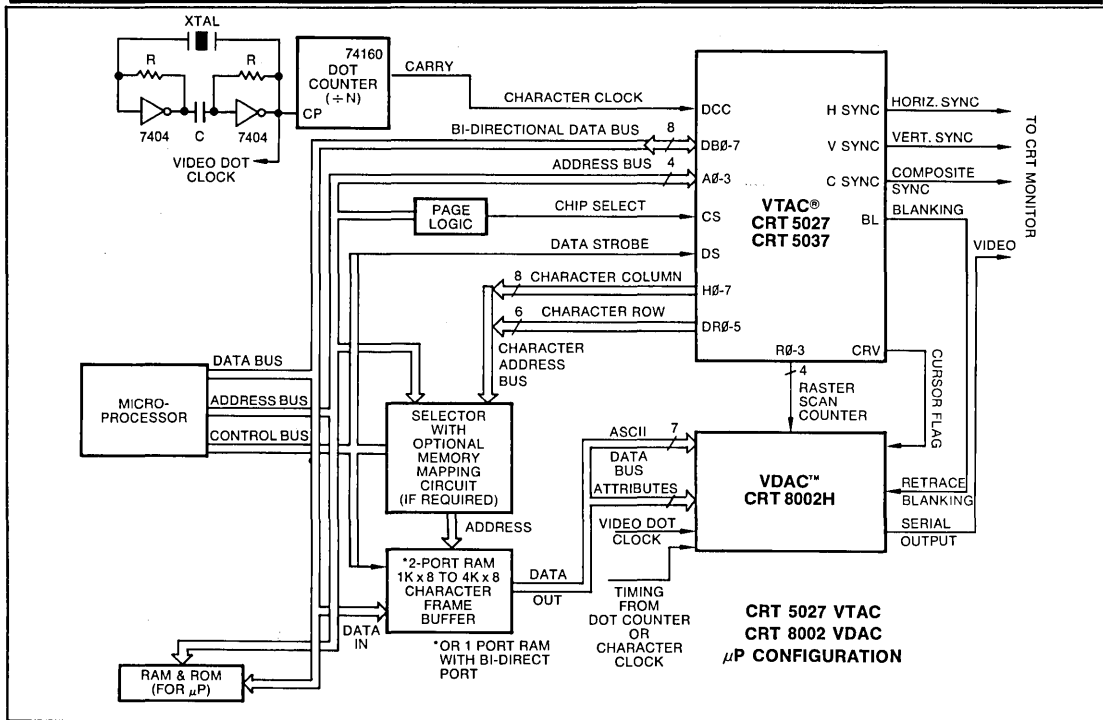
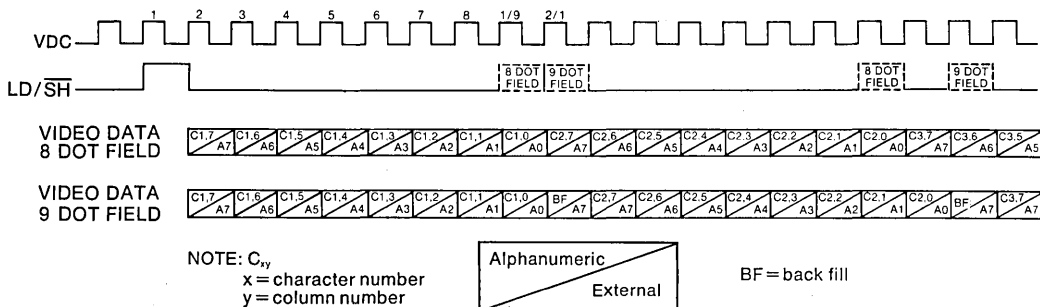
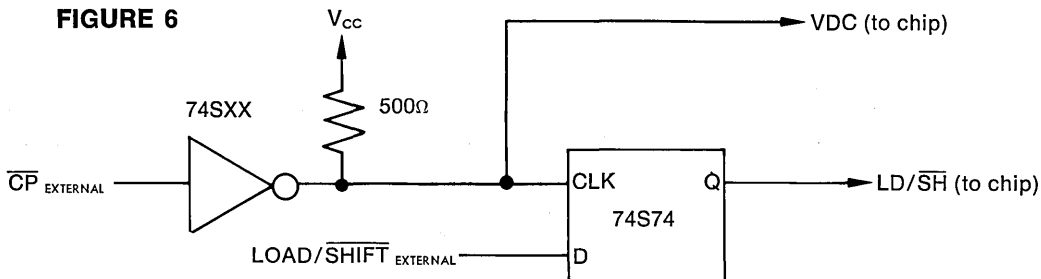


FIGURE 6



STANDARD MICROSYSTEMS CORPORATION

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We keep ahead of our competition so you can keep ahead of yours.

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