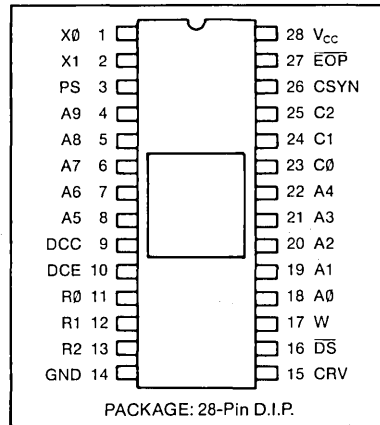


CRT Controller

FEATURES

- Single +5v power supply
- 16 line x 64 character display
- On chip sync oscillator
- Complete cursor control
- Automatic scrolling
- Erase functions built in
- Performs character entry during horizontal sync
- Internal blinking cursor
- Page linking logic built in
- LS-TTL compatible
- Compatible with CRT 8002, CRT 7004

PIN CONFIGURATION



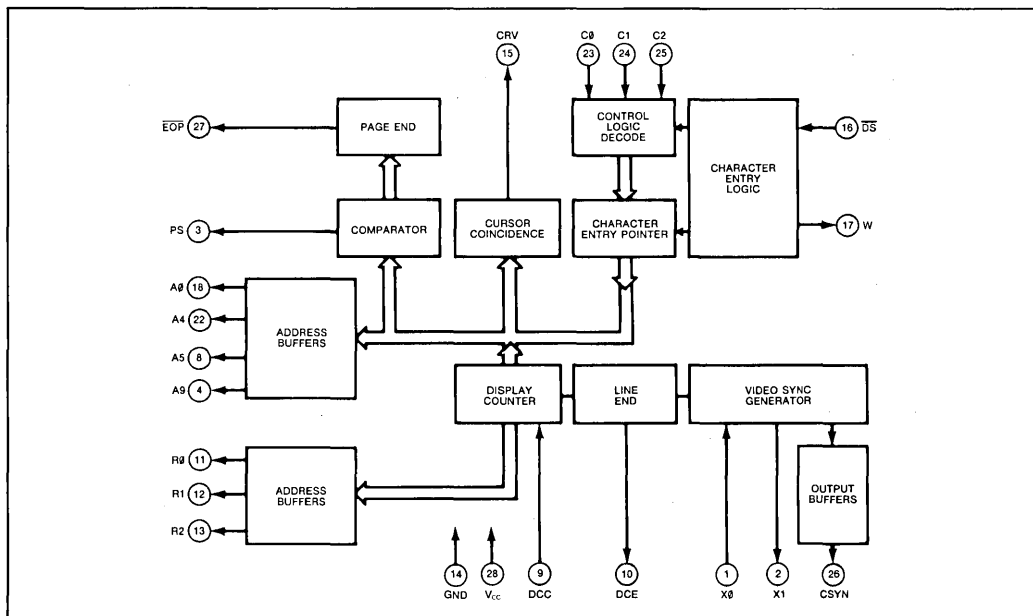
GENERAL DESCRIPTION

The CRT 96364A/B is a CRT Controller which controls all of the functions associated with a 16 line x 64 character video display. Functions include CRT refresh, character entry, and cursor management.

The CRT 96364A/B contains an internal oscillator which produces the composite sync output. The CRT 96364 B generates a 60 Hz vertical sync while the CRT 96364 A generates a 50 Hz vertical sync.

Standard functions such as ERASE PAGE, ERASE LINE, and ERASE TO END OF LINE make the CRT 96364A/B easy to interface to any computer or microprocessor, or to use as a stand-alone video processor.

The CRT 96364A/B requires only +5v power at less than 100 mA. It is manufactured in COPLAMOS® N channel silicon gate technology.



SECTION V

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION																																				
1 2	Crystal in Crystal out	X \emptyset X1	Pin one is the sync clock input. It may be driven directly from a TTL gate or from a parallel mode crystal connected between pins one and two. When a crystal is used, a 10 M Ω resistor should be connected in parallel. For standard 60 Hz line operation, a 1.018 MHz frequency source or crystal is required (with the CRT 96364 B). For 50 Hz line operation, the CRT 96364 A requires a 1.008 MHz crystal.																																				
3	Page Select	PS	PS provides automatic page selection when two pages of memory are used. A "zero" output indicates selection of page 1; a logic "one" indicates page 2.																																				
4-8	Memory Address	A9-A5	Upper order memory address lines; A6-A9 determine which lines of text are being refreshed or written. A5 along with A \emptyset -A4 determine the character position.																																				
9	Character Clock	DCC	Character clock input. Addresses are changed on the trailing edge of DCC.																																				
10	Dot Clock Enable	DCE	A logic zero from DCE is used to inhibit oscillation of the dot clock for retrace blanking.																																				
11-13	Row Address	R \emptyset -R2	Character Generator row addresses. Blanks are generated by forcing R \emptyset -R2 to "000". During character entry, R2 gates data into memory to control the erase function. Row addressing follows the sequence 0-1-2-3-4-5-6-7-0-0-0-0-increment text line-0-1-2-etc.																																				
14	Ground	GND	Ground																																				
15	Cursor	CRV	Cursor video output. Indicates cursor location by a 2 Hz blinking underline.																																				
16	Data Strobe	\overline{DS}	The rising edge of \overline{DS} strobes the appropriate C \emptyset -C2 control word into the CRT 96364 A/B.																																				
17	Write	W	A positive going signal which indicates that the CRT 96364 A/B is allowing a memory write. W is approximately 4 μ s, and occurs during H sync. Memory address lines are latched at the cursor address during W.																																				
18-22	Memory Address	A \emptyset -A4	Lower order memory addresses. A \emptyset -A4 plus A5 (pin 8) determine the character position.																																				
23-25	Command Inputs	C \emptyset -C2	<p>Command inputs are strobed into the CRT 96364 A/B by \overline{DS}. Functions are as follows:</p> <table style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: left;">Function</th> <th style="text-align: center;">C₂</th> <th style="text-align: center;">C₁</th> <th style="text-align: center;">C₀</th> </tr> </thead> <tbody> <tr> <td>Page erase and cursor home (top-left)</td> <td style="text-align: center;">0</td> <td style="text-align: center;">0</td> <td style="text-align: center;">0</td> </tr> <tr> <td>Erase to end of line and return cursor (to left)</td> <td style="text-align: center;">0</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> <tr> <td>Line feed (cursor down)</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> </tr> <tr> <td>No operation*</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> </tr> <tr> <td>Cursor left (one position)</td> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td style="text-align: center;">0</td> </tr> <tr> <td>Erasure of cursor-line</td> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> <tr> <td>Cursor up (one position)</td> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> </tr> <tr> <td>Normal character. Write signal is generated and cursor position is incremented</td> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> </tr> </tbody> </table> <p>* In order to suppress non-displayed characters</p>	Function	C ₂	C ₁	C ₀	Page erase and cursor home (top-left)	0	0	0	Erase to end of line and return cursor (to left)	0	0	1	Line feed (cursor down)	0	1	0	No operation*	0	1	1	Cursor left (one position)	1	0	0	Erasure of cursor-line	1	0	1	Cursor up (one position)	1	1	0	Normal character. Write signal is generated and cursor position is incremented	1	1	1
Function	C ₂	C ₁	C ₀																																				
Page erase and cursor home (top-left)	0	0	0																																				
Erase to end of line and return cursor (to left)	0	0	1																																				
Line feed (cursor down)	0	1	0																																				
No operation*	0	1	1																																				
Cursor left (one position)	1	0	0																																				
Erasure of cursor-line	1	0	1																																				
Cursor up (one position)	1	1	0																																				
Normal character. Write signal is generated and cursor position is incremented	1	1	1																																				
26	Composite Sync	CSYN	Positive logic composite sync output. Horizontal sync is generated during VSYNC and \overline{VSYNC} time. A vertical sync output may be generated by logically "ANDing" CSYN and DCE.																																				
27	End of Page	\overline{EOP}	This output is used to increment an external page counter when using more than one page of memory.																																				
28	Power Supply	V _{CC}	+ 5 volt supply.																																				

OPERATION

The CRT 96364A/B provides all of the control functions required by a CRT display with a minimum of external circuitry.

The cursor and erase commands may be decoded from the data bus by a low cost 256 x 4 PROM. The CRT 96364A/B then provides the necessary cursor movement and gates the memory for writing or erasing. Erase is controlled by providing a write signal to RAM, and

gating "zeros" to the RAM input bus. Use of an external PROM allows user selection of control words.

The RAM write command, "W", is generated during horizontal retrace. At this time, the RAM address is set to the cursor address. Immediately following the write command, the RAM addresses revert to refresh addressing and the cursor is shifted one character.

CURSOR

The cursor location is indicated by an alternating high on pin 15 (CRV) at row 7, and a low on pin 15 with R0-R2 forced low at rows 0-6. These alternate at a 2 Hz rate. If CRV is used to

force the display on, the result will be a blink of the cursor character position alternating with an underline at a 2 Hz rate.

CHARACTER ENTRY

When a Normal Character code (C2, C1, C0 = 1, 1, 1) and a Data Strobe are received, the write command will be generated during horizontal retrace. If, at the end of the horizontal retrace, the cursor is at the last position on a line, a carriage return and line feed will automatically occur. When the cursor is at the last position of the last line, a carriage return and up-scroll will automatically occur.

riage return and line feed will automatically occur. When the cursor is at the last position of the last line, a carriage return and up-scroll will automatically occur.

EXTRA FUNCTIONS

By using the fourth bit of the decoder PROM as a write enable signal, and properly programming the PROM, the additional commands of Home Cursor, Return Cursor, and Roll Screen may be generated. This is done by inhibiting the

W signal to the page memory and inputting the control codes, respectively, of Page Erase and Home Cursor, Erase to end of line and Return Cursor, and Line Feed.

SCROLLING

Scrolling of the screen text will occur under any of the following characteristics:

1. Inputting a line feed command when the cursor is at the bottom line of the screen.
 2. Inputting a character when the cursor is at the bottom right hand side of the screen.
- Scrolling will result in the entire top line of the

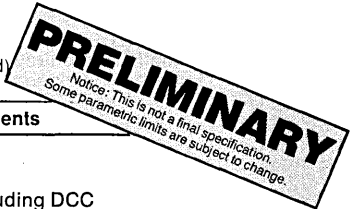
screen being erased and all of the remaining lines shifting up. Alternatively, a Roll (defined as all of the lines shifting up with the previous top line reappearing at the bottom of the screen) may be performed by inhibiting the write signal to the page memory as described in "Extra Functions."

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range 0°C to + 70°C
Storage Temperature Range -55°C to +150°C
Lead Temperature (soldering, 10 sec.) +325°C
Positive Voltage on any Pin, with respect to ground - 7.0V
Negative Voltage on any Pin, with respect to ground -0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C, V_{CC}= - 5V±5%, unless otherwise noted)

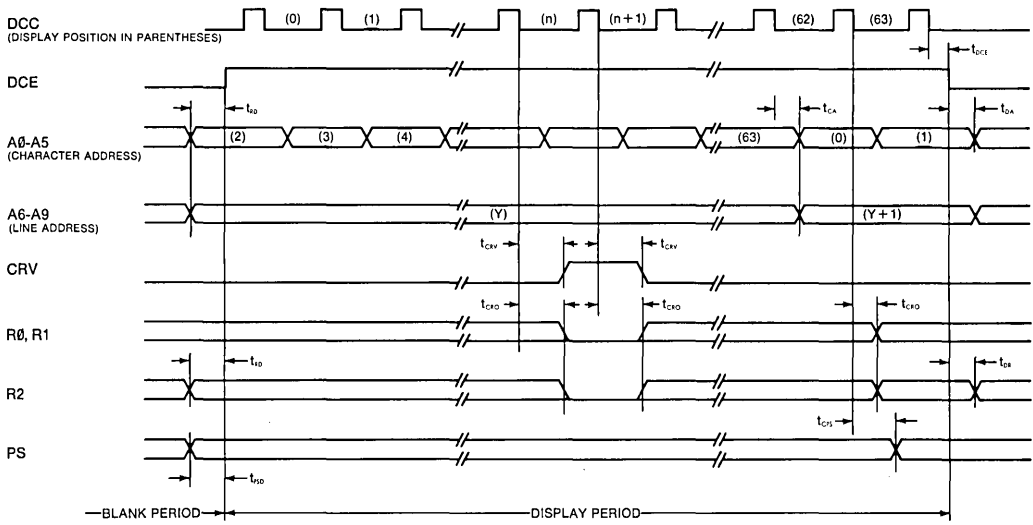


Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS (except DCC)					
Low-level, V _{IL}	2.2		0.65	V	excluding DCC
High-level, V _{IH}				V	excluding DCC
INPUT VOLTAGE LEVELS—DCC					
Low-level, V _{IL}	3.5		0.65	V	
High-level, V _{IH}				V	
OUTPUT VOLTAGE LEVELS (DCE Only)					
Low-level, V _{OL}	2.2		0.4	V	I _{OL} = 1.9 mA
High-level, V _{OH}				V	I _{OH} = -100 μA
OUTPUT VOLTAGE LEVELS (except DCE)					
Low-level, V _{OL}	2.2		0.4	V	I _{OL} = 0.36 mA
High-level, V _{OH}				V	I _{OH} = -100 μA
INPUT CURRENT					
Low-level, I _{IL}			10	μA	0 ≤ V _{IN} ≤ +5V
INPUT CAPACITANCE					
All inputs, C _{IN} (except DCE)		5		pF	V _{IN} = GND
C _{IN} (DCC Only)		25		pF	V _{IN} = GND
POWER SUPPLY CURRENT					
I _{CC}		100	120	mA	

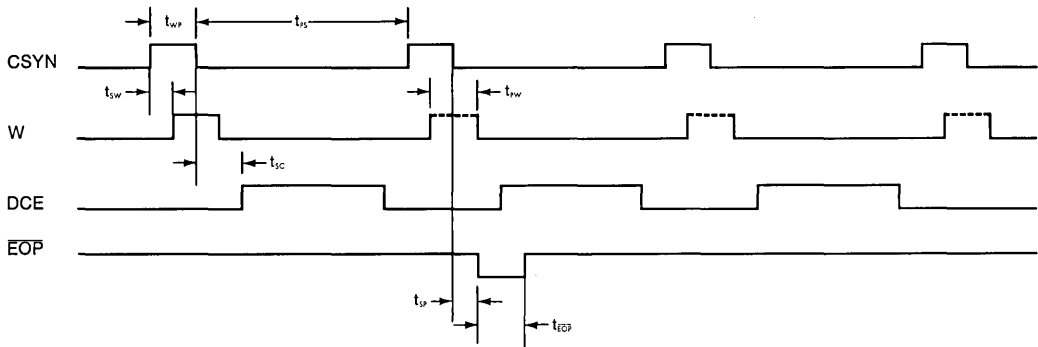
AC CHARACTERISTICS

PARAMETERS	SYMBOL	VALUES			UNIT
		MIN.	TYP.	MAX.	
Frequency of control clock DCC	f _{DCC}		1.6		MHz
Crystal Frequency CRT 96364 A	f _X		1.008		MHz
	f _X		1.018		MHz
DCC pulse width	t _{DCC}	200			ns
Rise and fall times	t _r t _f		20	40	ns
Refresh memory address access time	t _{CA}		200	250	ns
Character memory address access time	t _{CRO}		200	250	ns
PS access time (read)	t _{CPS}		300	1000	ns
CRV access time	t _{CRV}		200	250	ns
DCE access time (high to low)	t _{DCE}		100		ns
SYNC period	t _{PS}		64		μs
SYNC pulse width	t _{WP}		4		μs
DCE access time (low to high level)	t _{SC}		11		μs
EOP access time (high to low level)	t _{SP}		1	1.5	μs
W access time (low to high)	t _{SW}		500	1000	ns
W pulse width	t _{PW}		4		μs
EOP pulse width	t _{EOP}		10		μs
Address to rising edge of DCE delay	t _{AD}	0		2.1	μs
Falling edge of DCE to Address delay	t _{DA}	0		1	μs
Row to rising edge of DCE delay	t _{RD}	0		2.1	μs
Falling edge of DCE to row delay	t _{DR}	0		1	μs
PS to rising edge of DCE delay	t _{PSD}	0			μs

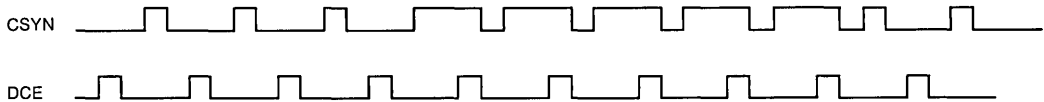
LINE TIMING



SYNC TIMING



FRAME TIMING



DATA INPUT TIMING

Asynchronous Operation

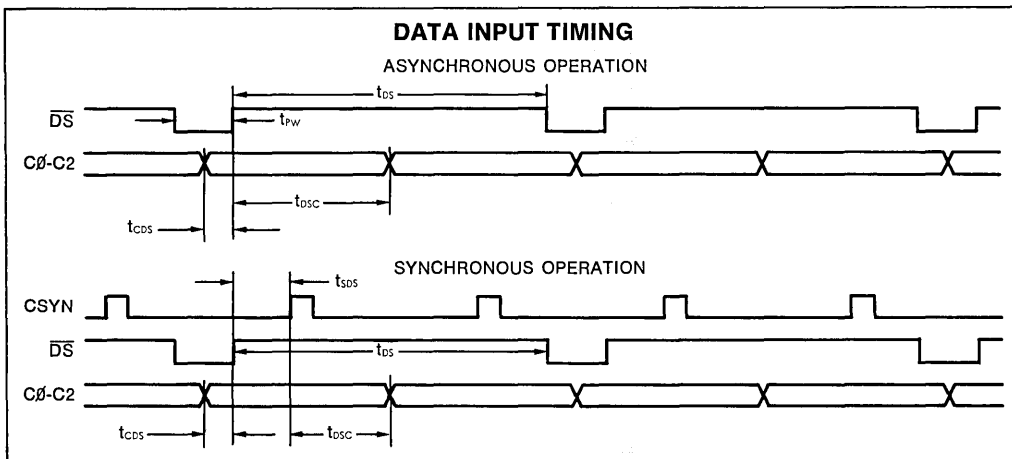
PARAMETER	SYMBOL	Value			UNIT
		MIN	TYP	MAX	
DS Pulse Width	t_{PW}	0.5			μS
C0-C2 Set Up Time	t_{CDS}	1			μS
C0-C2 Hold Time	t_{DSC}	90			μS
Minimum Strobe Period (Operation Execution Time)	t_{DS}				
FUNCTION					
		C2	C1	C0	
Page Erase & Cursor Home		0	0	0	132 ms
Erase to End of Line & Return Cursor		0	0	1	4.2 ms
Line Feed (Cursor Down)		0	1	0	130* μS
No Operation		0	1	1	80 μS
Cursor Left		1	0	0	80 μS
Erasure of Cursor Line		1	0	1	8.3 ms
Cursor Up		1	1	0	80 μS
Normal Character		1	1	1	130* μS

*Will increase to 8.3 ms when text scroll occurs. See "Scrolling" for conditions.

Synchronous Operation

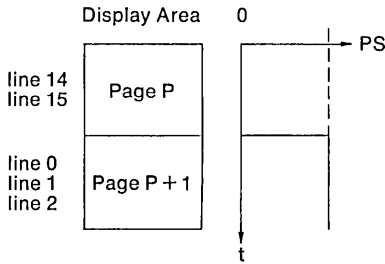
PARAMETER	SYMBOL	Value			UNIT
		MIN	TYP	MAX	
DS Pulse Width	t_{PW}	0.5			μS
C0-C2 Set-Up Time	t_{CDS}	1			μS
C0-C2 Hold Time	t_{DSC}	16			μS
DS Set Up Time	t_{SDS}	1			μS
Minimum Strobe Period (Operation Execution Time)	t_{DS}				
FUNCTION					
		C2	C1	C0	
Page Erase & Cursor Home		0	0	0	132 ms
Erase to End of Line & Return Cursor		0	0	1	4.2 ms
Line Feed (Cursor Down)		0	1	0	64* μS
No Operation		0	1	1	64 μS
Cursor Left		1	0	0	64 μS
Erasure of Cursor Line		1	0	1	8.3 ms
Cursor Up		1	1	0	64 μS
Normal Character		1	1	1	64* μS

*Will increase to 8.3 ms when text scroll occurs. See "Scrolling" for conditions.



MULTIPLE PAGE DISPLAY

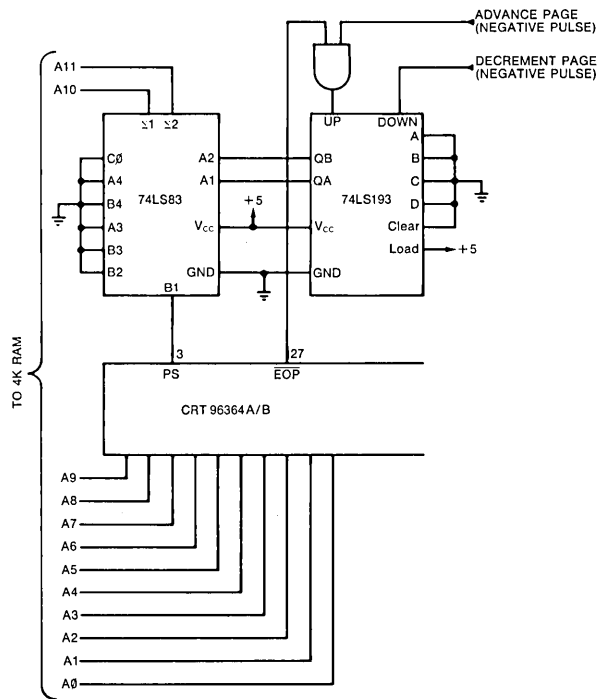
When linking two or more pages, the EOP and PS signals may be used to allow a "moving window" text display. PS (Page Select) indicates the end of page location. If a scroll has occurred, PS will show the transition from the end of line 15 of page P and the beginning of line 0 of page P + 1.



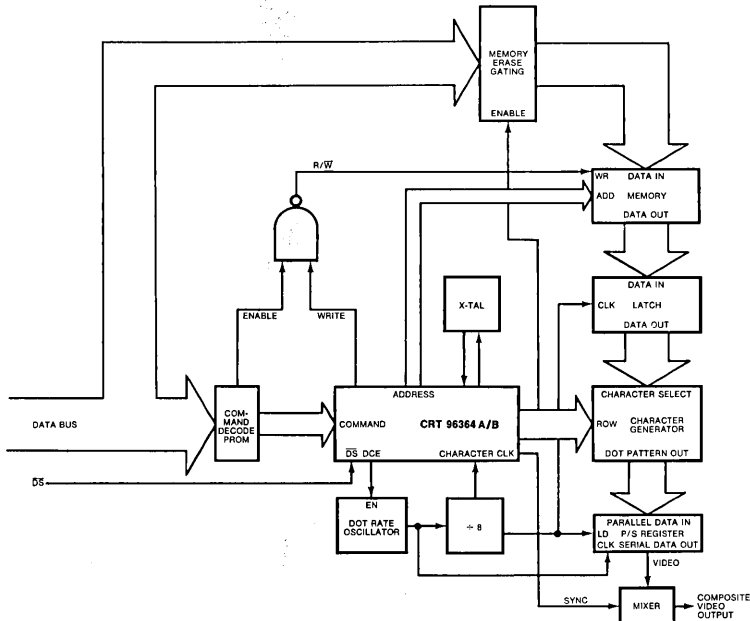
To properly maintain the memory address when displaying more than two pages, EOP pulses low at the point in time when page P is scrolled completely off the screen. At this time, PS will remain low for the entire frame since page P + 1 is now the only displayed page.

The circuit at the right will allow scrolling through 4 pages of memory.

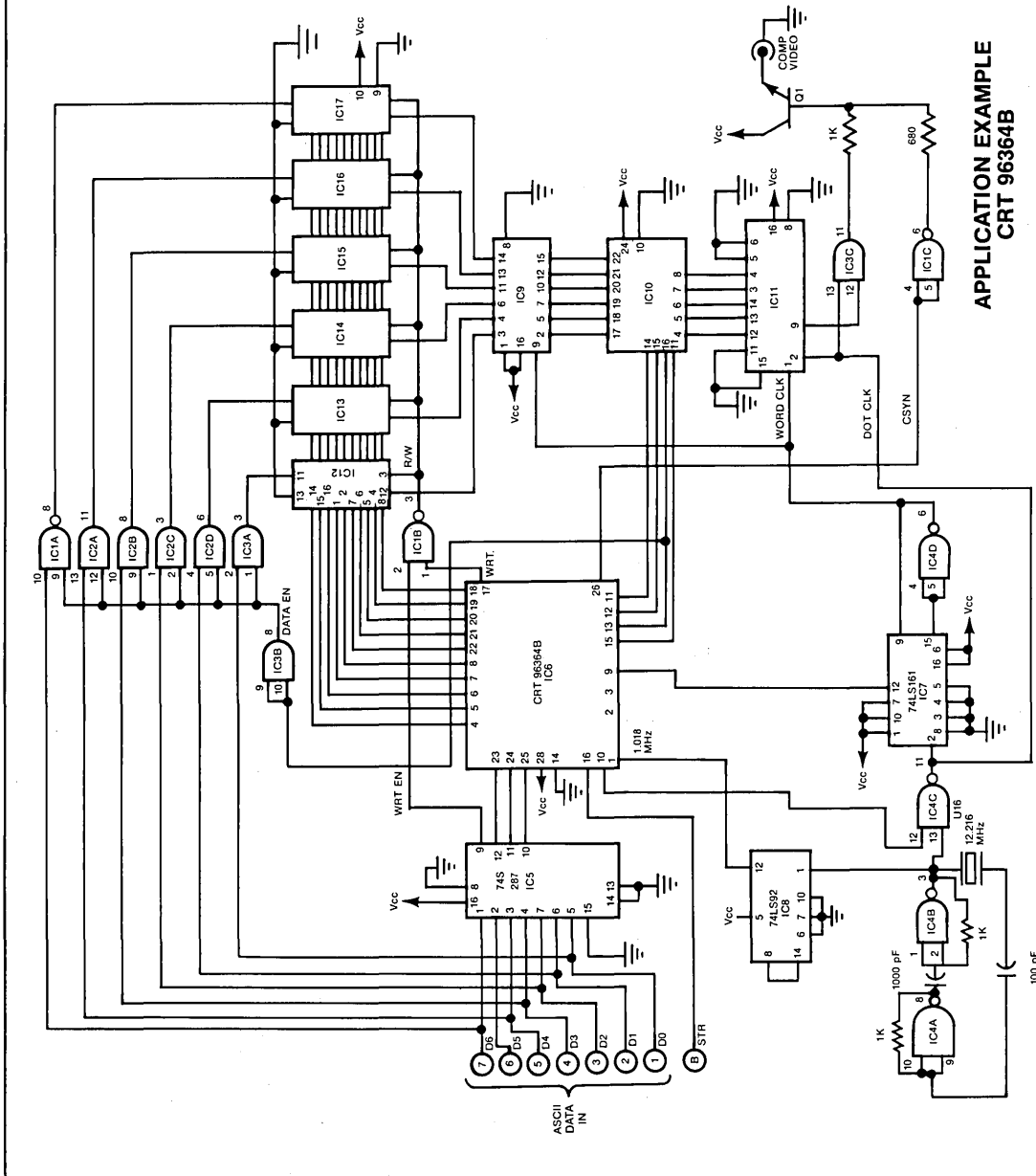
4 PAGE DISPLAY



TYPICAL SYSTEM APPLICATION



- IC1 74LS00
- IC2 74LS08
- IC3 74LS08
- IC4 74LS00
- IC5 74LS00
- IC6 CRT96364B
- IC7 74LS161
- IC8 74LS92
- IC9 74LS161
- IC10 RO.3.2513
- IC11 74LS165
- IC12 74LS165
- IC13 74LS165
- IC14 2102AL-4
- IC15 74LS165
- IC16 74LS165
- IC17 74LS165
- Q1 2N4400



**APPLICATION EXAMPLE
CRT 96364B**

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