CS1237

July 13, 2018

1 Chip Function Description

The CS1237 is a high-precision, low-power analog-to-digital conversion chip with one differential input channel, built-in temperature sensor and high-precision oscillator.

The CS1237 PGA is optional: 1, 2, 64, 128. The default is 128.

CS1237 ADC data output rate in normal mode is optional: 10Hz, 40Hz, 640Hz, 1.28kHz, default is 10Hz;

The MCU can communicate with the CS1237 through the 2-wire SPI interface SCLK, $\overline{DRDY}$/DOUT to configure it, such as channel selection, PGA selection, output rate selection, and so on.

1.1 The main function of the chip

- Built-in crystal
- Integrated temperature sensor
- With Power down function
- 2-wire SPI interface with a maximum speed of 1.1MHz
- 24 bits without missing code

ADC functional characteristics:

- 24 bits without missing code
- PGA gain options: 1, 2, 64, 128
- One 24-bit differential input with no missing codes. When PGA=128 ENOB is 20 bits (5V),19.5 bits (3.3V)
- P-P noise: PGA=128, 10Hz: 180nV;
- INL less than 0.0015%
- Output rate options: 10Hz, 40Hz, 640Hz, 1.28kHz
- In-band short function

1.2 Chip applications

- Industrial process control
- Electronic scale
- Liquid/gas chemical analysis
- Blood meter
- Smart converter
- Portable equipment

1.3 Chip basic structure function description

The CS1237 is a high-precision, low-power Sigma-Delta analog-to-digital converter with one Sigma-Delta ADC, one differential input channel, and one temperature sensor. The ADC uses a two-stage sigma delta modulator through a low-noise instrumentation amplifier. To achieve PGA amplification, magnification options: 1, 2, 64, 128. At PGA=128, the effective resolution is up to 20 bits (working at 5V).

The CS1237 has an internal RC oscillator and does not require an external crystal.

The CS1237 can be configured for multiple functional modes via $\overline{DRDY}$/DOUT and SCLK, such as temperature detection, PGA selection, ADC data output rate selection, and more.

The CS1237 has Power down mode.

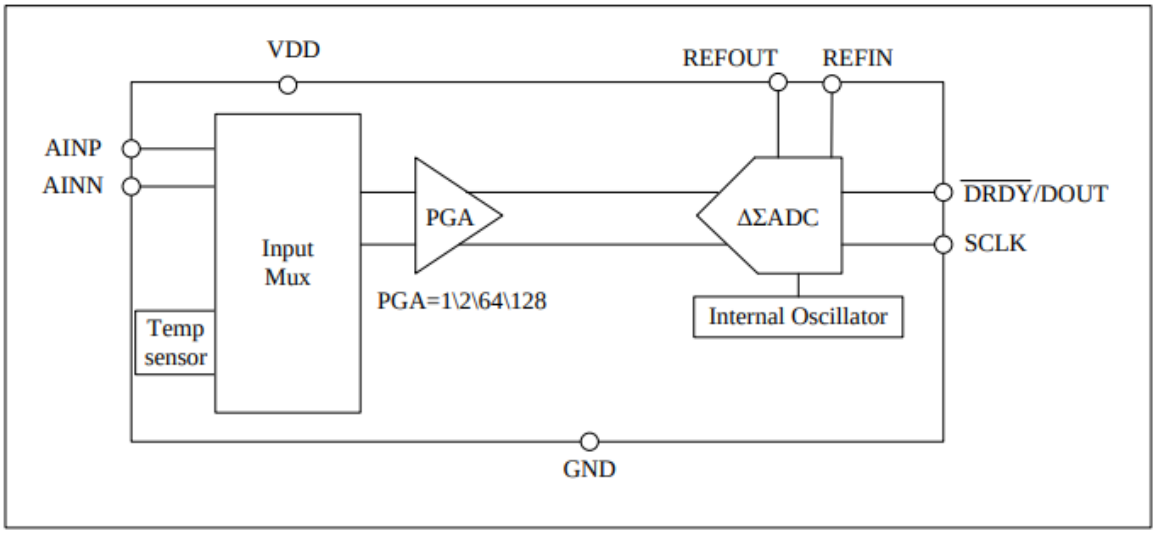

Figure 1: CS1237 Functional Block Diagram

1.4 Absolute maximum limit of the chip

Name	Symbol	Minimal	Maximum	Unit
Voltage	VDD	-0.3	6	V
Power instantaneous current			100	mA
Power supply constant current			10	mA
Digital pin input voltage		-0.3	DVDD+0.3	V
Digital output pin voltage		-0.3	DVDD+0.3	V
Temperature			150	℃
Operating temperature		-40	85	℃
Storage temperature		-60	150	℃
Chip pin soldering temperature			240	℃

Table 1: CS1237 Limits

1.5 CS1237 Digital Logic Features

Parameter	Minimal	Typical	Maximum	Unit	Condition Description
VIH	0.7xDVDD		DVDD+0.1	V	
VIL	DGND		0.3xDVDD	V	
VOH	DVDD-0.4		DVDD	V	Ioh=1mA
VOL	DGND		0.2xDVDD	V	IoL=1mA
IIH			10	μA	VI=DVDD
IIL	-10			μA	VI=DVDD
Serial clock SCLK operating frequency			1.1	MHz	

Table 2: CS1237 Digital Logic Features

1.6 CS1237 Electrical Characteristics

All parameter tests are tested at ambient temperature -40 to 85°C with built-in reference conditions, unless otherwise noted.

Parameter	Condition	Min	Typical	Max	Unit
Analog input					
Full-scale input voltage (AINP-AINN)			±0.5VREF/PGA		V
Common-mode input voltage	PGA=1,2	AGND-0.1		AVDD+0.1	V
	PGA=64,128	AGND+0.75		AVDD-0.75	V
Differential input impedance	PGA=1,2		190		MΩ
	PGA=64,128		28		MΩ
System performance					
Resolution	No missing code		24		Bits
AD rate			10	1280	Hz
System performance	Full establishment	3: ADC output rate is 10-40Hz, 4: ADC output rate is 640-1280Hz			Conversion Cycle
P-P noise	PGA=128,10Hz		180		nV
Effective accuracy	PGA=128,10Hz		20(5V) 19.5(3.3V)		Bit
Integral linearity	PGA=128		±15		pmm
Offset error	PGA=128		±1.4		μV
Offset error drift	PGA=128		20		nV/°C
Gain error	PGA=128		±0.5		%
Gain error drift	PGA=128		8		ppm/°C
Reference voltage input					
Reference voltage input	REFIN	1.5	VDD	VDD+0.1	V
Reference voltage output					
Reference voltage output	REFOUT		VDD		V
Clock					
Internal oscillator frequency			5.2		MHz
Built-in clock drift			250		ppm/°C
Temperature Sensor					
Temperature measurement error	TempError		±3		°C

Table 3: CS1237 Electrical Characteristics (VDD = 5V, 3.3V)

Parameter	Condition		Min	Typical	Max	Unit
Voltage	VDD		4.5	5	5.5	V
Working current	Normal Mode	PGA=1,2		1.57		mA
		PGA=64,128		2.34		mA
	Power Down			0.1	0.1	μA

Table 4: CS1237 Power Supply Electrical Characteristics (VDD=5V)

Parameter	Condition		Min	Typical	Max	Unit
Voltage	VDD		3	3.3	3.6	V
Working current	Normal Mode	PGA=1,2		1.26		mA
		PGA=64,128		2.11		mA
	Power Down			0.1		μA

Table 5: CS1237 Power Supply Electrical Characteristics (VDD=3.3V)

1.7 Chip pin

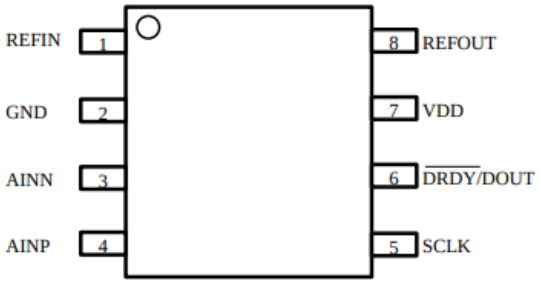

Figure 2: CS1237 Chip Pinout

No.	Pin Name	Input/Output	Instructions
1	REFIN	AI	Reference source input
2	GND	P	Chip ground
3	AINN	AI	Channel negative input
4	AINP	AI	Channel positive input
5	SCLK	DI	SPI input interface
6	$\overline{DRDY}$/DOUT	DI/DO	SPI data input-output interface
7	VDD	P	power supply
8	REFOUT	AO	Reference output

Table 6: Note: REFOUT is the sensor excitation source output (output value is VDD).

2 Chip Function Module Description

2.1 Analog input front end

There is one ADC in CS1237, one differential input is integrated. The signal input can be differential input signal AINP, AINN, or the output signal of temperature sensor. The switching of input signal is controlled by register (ch_sel[1:0]). The basic structure is shown below:

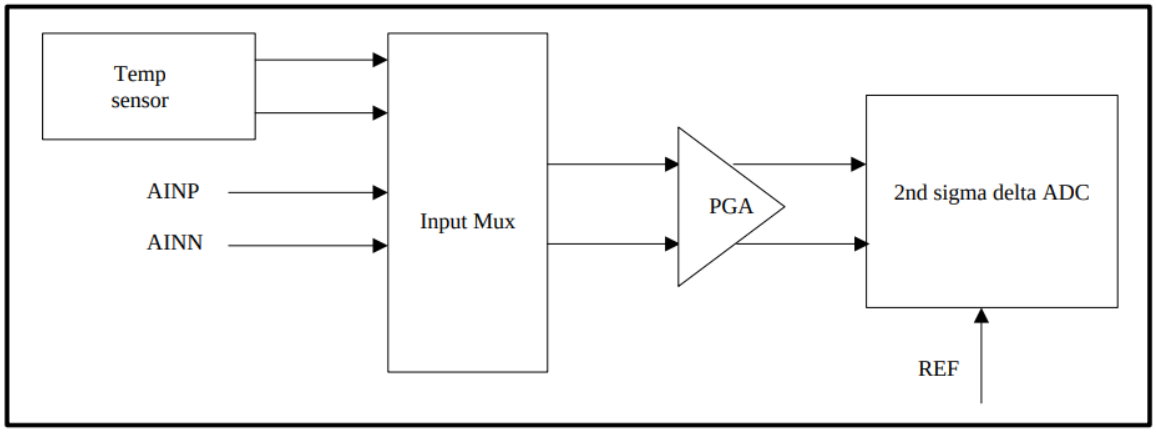

Figure 3: Analog input structure diagram

The CS1237 PGA can be configured with: 1, 2, 64, 128, controlled by registers (pga_sel[1:0]);

The reference voltage can be either external or internal. If an external reference voltage is to be used, the internal reference must be turned off first and the internal reference control is controlled by a register (refo_off).

2.2 Temperature Sensor

The chip provides temperature measurement inside. When ch_sel[1:0]=2'b10, the ADC analog signal input is connected to the internal temperature sensor, and other analog input signals are invalid. The ADC derives the actual temperature value by measuring the voltage difference at the output of the internal temperature sensor. When ch_sel[1:0]=2'b10, ADC only supports PGA=1. **The temperature sensor requires a single point of correction. Correction method: At a certain temperature point A, a temperature sensor is used to measure the code value Ya.**

Then the temperature of other temperature point:

$$B = \frac{Yb * (273.15 + A)}{Ya - 273.15} \tag{1}$$

A is the temperature unit is Celsius. Ya is the A-point corresponding temperature code value. Yb is the temperature code value corresponding to point B.

2.3 Low noise PGA amplifier

CS1237 provides a low-noise, low-drift PGA amplifier and bridge sensor differential output connection, the basic structure of the diagram as shown below, front anti-EMI filter circuit R = 450Ω, C = 18pF 20M high-frequency filtering. The low-noise PGA amplifier achieves 64-fold amplification with RF1, R1, RF2, and PGA amplification with 64- and 128-point PGA. Different PGAs such as 1, 2, 64, and 128 are configured through pga_sel[1:0]. When using PGA = 1,2, the 64-times low-noise PGA amplifier is turned off to save power. When using a low-noise PGA amplifier, the input range is between GND + 0.75V and VDD - 0.75V. Exceeding this range results in a decrease in actual performance. Connect a built-in 45pF capacitor at the CAP port, and make a low-pass filter with the built-in 2k resistor RINT to use as a high-frequency filter for the output signal of the low-noise PGA amplifier. The low-pass filter can also be used as an anti-alias filter for the ADC.

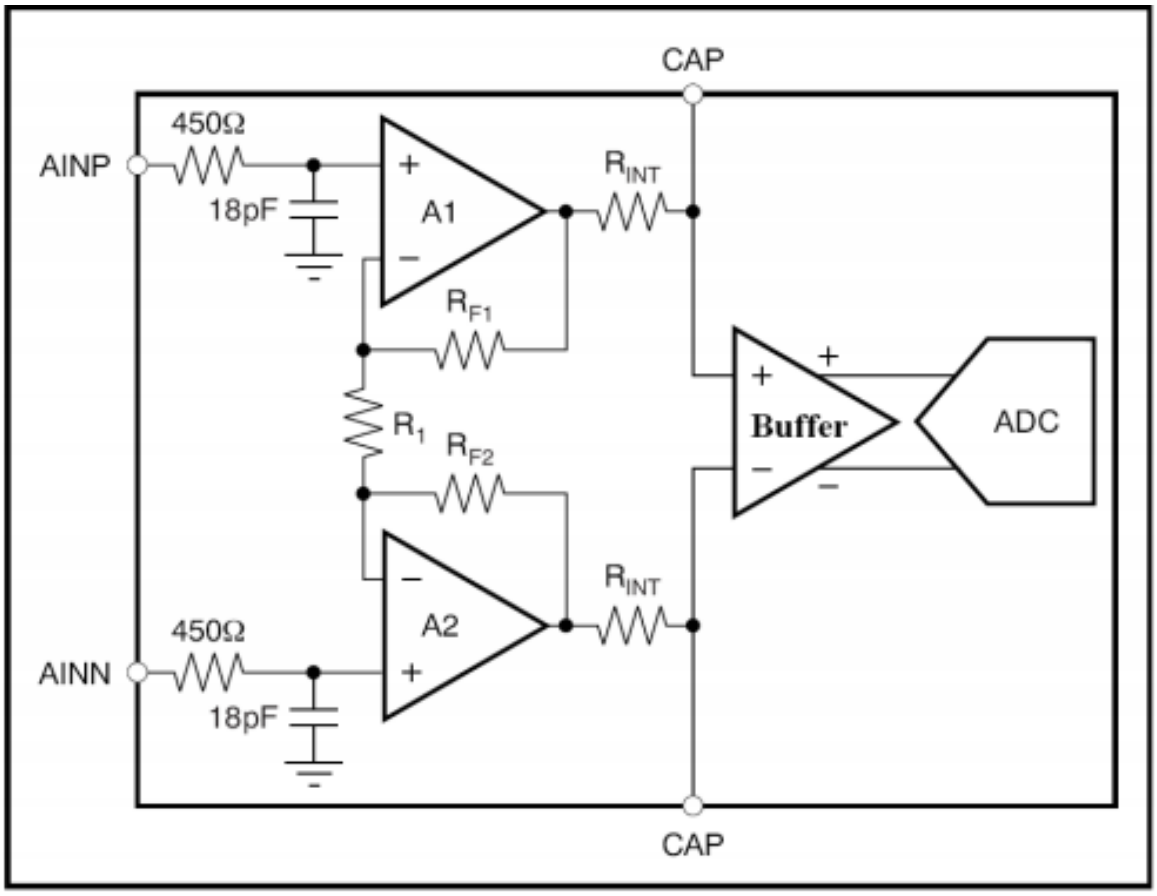

Figure 4: PGA structure diagram

CS1237 has built-in buffer. When PGA=1,2, CS1237 uses Buffer to reduce problems caused by low ADC differential input impedance, such as insufficient settling time and large gain error. When PGA=64,128, CS1237 also Use Buffer to reduce setup error, gain error, and inner code drift caused by the low-pass filtering of low noise PGA with RINT=2K, CINT=0.1μF.

2.4 Clock source

The CS1237 uses a built-in crystal to provide the system's desired clock frequency, typically 5.2MHz.

2.5 Reset and power off(POR & power down)

When the chip is powered on, the built-in power-on reset circuit will generate a reset signal to automatically reset the chip.

When SCLK goes from low to high and stays high for more than 100μs, the CS1237 enters PowerDown mode, which consumes less than 0.1μA. When SCLK goes back low, the chip will resume normal operation.

When the system is re-entered into normal working mode by Power down, all functions are configured to be in the state before Power Down, and no functional configuration is required.

2.6 SPI serial communication

2-wire SPI serial communication is used in the CS1237, and data reception and function configuration can be realized through SCLK and $\overline{DRDY}$/DOUT.

2.6.1 Setup time

When the ADC data output rate is 10Hz or 40Hz, the digital part needs to have 3 data conversion periods to meet the establishment of the analog input signal and the filter settling time requirement; When the ADC data output rate is 640Hz or 1280Hz, the digital part needs to have 4 data conversion cycles to meet the setup of the analog input signal and the settling time of the filter. The entire setup process of CS1237 is shown in the following figure:

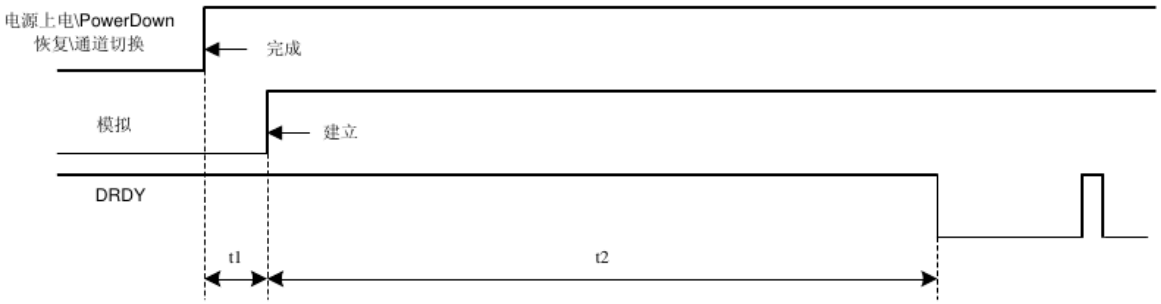

Figure 5: Data Creation Process 1

Figure 6: Data Creation Process 2

Parameter	Description (1)		Minimum value	Typical value	Maximum	Unit
t1	Power On/Power Down Recovery/Setting time required for simulation after channel switching			2		ms
t3	Settling time required for simulation after PGA switch/rate switching			0.8		μs
t2	Setting time ($\overline{DRDY}$/DOUT remains high)	10/40Hz		300/75		ms
		640/1280Hz		6.25/3.125		ms

2.6.2 ADC data output rate

The CS1237 data output rate can be configured via the registers speed_sel[1:0].

SPEED_SEL[1:0]	ADC output rate (Hz)
00	10
01	40
10	640
11	1280

Table 7: Output Rate Settings

2.6.3 Data Format

The data output by CS1237 is 24-bit 2's complement, and the highest bit (MSB) is the first output. The least significant bit (LSB) is (0.5VREF/Gain)/(2^{23}-1). The positive full-size output code is 7FFFFFH, and the negative full-size output code is 800000H. The table below shows the ideal output codes for the different analog input signals.

Input signal VIN (AINP-AINN)	Ideal output
≥+0.5VREF/Gain	7FFFFFH
(+0.5VREF/Gain)/(2^{23} -1)	000001H
0	000000H
(-0.5VREF/Gain)/(2^{23} -1)	FFFFFFH
≤+0.5VREF/Gain	800000H

Table 8: Ideal output code and input signal (1)

(1) Regardless of noise, INL, offset error and gain error

2.6.4 Data preparation, data input and output ($\overline{DRDY}$/DOUT)

The $\overline{DRDY}$/DOUT pin has 4 uses. First, when the output is low, it means that the new data has been converted; Second, as the data output pin, when the data is ready, after the rising edge of the first SCLK, $\overline{DRDY}$/DOUT outputs the highest bit (MSB) of the converted data. On each rising edge of SCLK, the data is automatically shifted by one bit. Reads all 24-bit data after 24 SCLKs. If SCLK is paused at this time, $\overline{DRDY}$/DOUT will hold the last bit of data until the next data is ready to be pulled high, after which $\overline{DRDY}$/DOUT is Pulling low again, indicating that the new data has been converted, and the next data can be read; Fourth, as the register data write or read pin, when the configuration register or read register value is needed, the SPI needs to send 46 SCLKs. According to the command word input by $\overline{DRDY}$/DOUT, it is judged whether it is a write register operation or a read register operation. .

2.6.5 Serial clock input (SCLK)

Serial Clock Input SCLK is a digital pin. This signal should be guaranteed to be a clean signal, and glitch or slow rising edges can cause errors or errors to be read. Therefore, it should be ensured that the rise and fall times of SCLK are less than 50ns.

2.6.6 Data transmission

The CS1237 can continuously convert the analog input signal. When $\overline{DRDY}$ /DOUT is pulled low, it indicates that the data is ready to be accepted. The first SCLK input can read the highest bit of the output. After 24 SCLKs, all the signals will be read. 24-bit data read. If SCLK is suspended, $\overline{DRDY}$/DOUT will hold the last bit of data until it is pulled high. Whether the 25th and 26th SCLK output configuration registers have a write flag, the $\overline{DRDY}$/DOUT corresponding to the 25th SCLK is 1 indicating that the configuration register Config has been written with a new value. The $\overline{DRDY}$/DOUT corresponding to the 26th SCLK is the chip extension reserved bit, and the current output is always 0. $\overline{DRDY}$/DOUT can be pulled high by the 27th SCLK, and then $\overline{DRDY}$/DOUT is pulled low again, indicating that the new data is ready to be accepted and the next data is converted. The basic timing is shown in the figure:

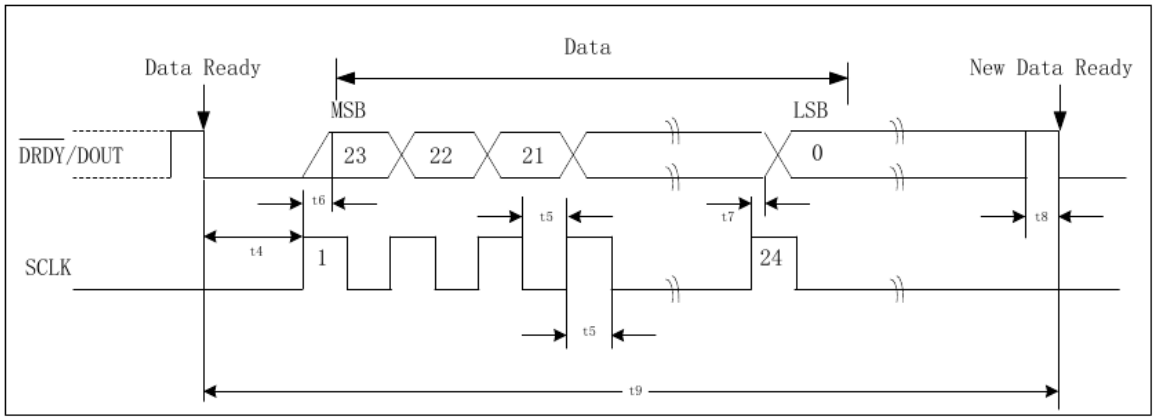

Figure 7: Read data timing diagram 1

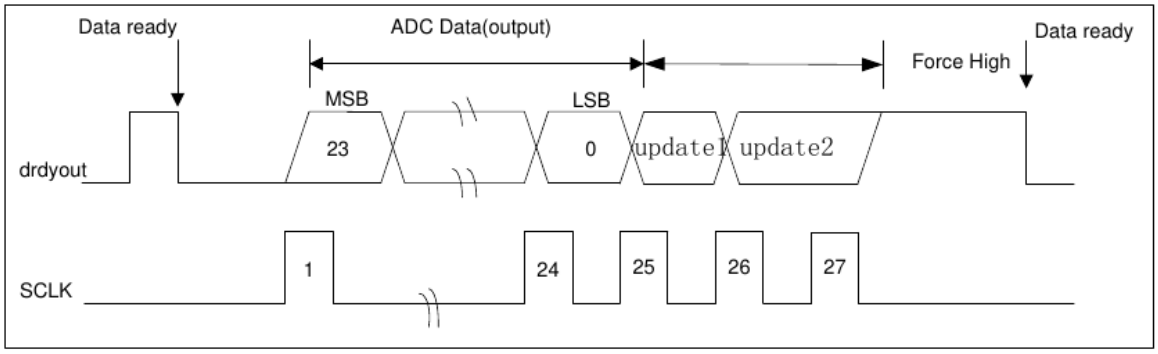

Figure 8: Read data timing diagram 2

2.6.7 Functional configuration

The CS1237 can be configured with different functions through SCLK and $\overline{DRDY}$/DOUT. The function configuration timing diagram is shown below:

SYMBOL	DESCRIPTION		MIN	TYP	MAX	UNITS
t4	$\overline{DRDY}$/DOUT goes low to the first SCLK rising edge		0			ns
t5	SCLK high or low pulse width		455			ns
t6	SCLK rising edge to new data bit valid (transmission delay)		455			ns
t7	SCLK rising edge to old data bit valid (hold time)		227.5		455	ns
t8	Data update, not allowed to read previous data			26.13		μs
t9	Conversion time (1/data rate)	10Hz		100		ms
		40Hz		25		ms
		640Hz		1.5625		ms
		1280Hz		0.78125		ms

Table 9: Read data timing table

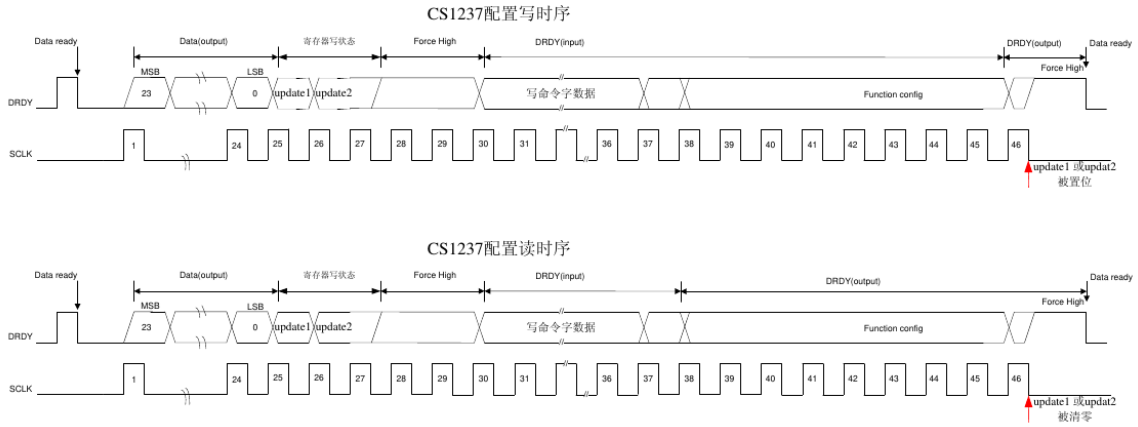

Figure 9: Function configuration timing diagram

A brief description of the functional configuration process, after $\overline{DRDY}$/DOUT goes from high to low:

1. The 1st to 24th SCLKs read the ADC data. If you do not need to configure registers or read registers, you can omit the following steps.
2. The 25th to 26th SCLKs read the register write operation status.
3. The 27th SCLK pulls the $\overline{DRDY}$/DOUT output high.
4. From the 28th to the 29th SCLK, switch $\overline{DRDY}$/DOUT to the input.
5. The 30th to 36th SCLK, the input register writes or reads the command word data (the high order first input).
6. The 37th SCLK, the direction of $\overline{DRDY}$/DOUT is switched (if it is a write register, $\overline{DRDY}$/DOUT is the input; if it is a read register, $\overline{DRDY}$/DOUT is the output).
7. The 38th to 45th SCLK, input register configuration data or output register configuration data (high order first input/output).

8. For the 46th SCLK, switch $\overline{DRDY}$/DOUT to the output and pull $\overline{DRDY}$/DOUT high. Update1/update2 is set or cleared.

2.6.7.1 SPI command word

CS1237 has 2 command words, the length of the command word is 7bits, and the command words are described as follows:

Command name	Command byte	Description
Write configuration register	0x65	Write configuration register Config
Read configuration register	0x56	Read configuration register Config

Table 10: Command word description table

2.6.7.2 SPI register

The CS1237 has a set of Config registers.

Register	R/W	Description	Reset value
Description	Reserved bit	Configuration register	0x0C

Configuration bit	B7	B6	B5	B4
Description	Reserved bit	REF output switch	ADC output rate selection	
Configuration bit	**B3**	**B2**	**B1**	**B0**
Description	PGA selection		Channel selection	

Bits	Description		
[7]	-	The chip retains the use bits. **The default is 0, write 0 when writing, do not write 1**	
[6]	REFO_OFF	**REF output switch:** Default REF output is on 1 = Turn off REF output. 0 = REF Normal output.	
[5:4]	SPEED_SEL	**ADC output rate selection:**The default is 10Hz	
		SPEED_SEL[1:0]	**Description**
		00	ADC output rate is 10Hz
		01	ADC output rate is 40Hz
		10	ADC output rate is 640Hz
		11	ADC output rate is 1280Hz
[3:2]	PGA_SEL	**PGA selection:**The default PGA is 128, in the temperature mode PGA_SEL=00	
		PGA_SEL[1:0]	**Description**
		00	1
		01	2
		10	64
		11	128
[1:0]	CH_SEL	**Channel selection:**The default channel is channel A	
		CH_SEL[1:0]	**Description**
		00	Channel A
		01	Chip retention
		10	Temperature
		11	Internal short

Table 11: Config register description table

2.6.8 Power down mode

When SCLK goes from low to high and stays high for more than 100μs, CS1237 enters PowerDown mode, which will turn off all circuits of the chip, and the power consumption is close to 0. When SCLK returns to low level, the chip will re-enter normal operation.

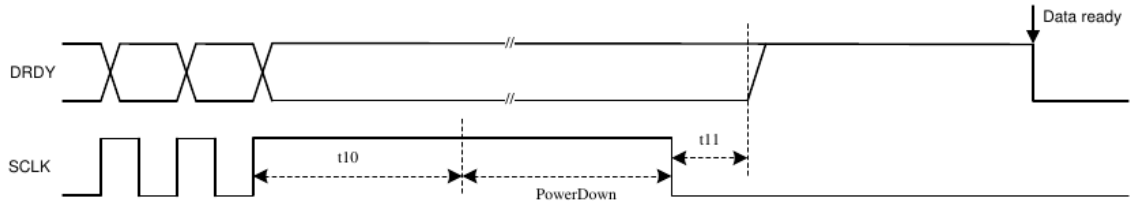

Figure 10: PowerDown mode diagram

Symbol	Description	Minimum value	Typical value	Maximum
t10	SCLK high hold time	100μs		
t11	Low hold time after SCLK falls	10μs		

3 Chip package

CS1237 is available in SOP8 package.

尺寸 / 标注	最小（mm）	最大（mm）	尺寸 / 标注	最小（mm）	最大（mm）
A	4.95	5.15	C3	0.05	0.20
A1	0.37	0.47	C4	0.20TYP	
A2	1.27TYP		D	1.05TYP	
A3	0.41TYP		D1	0.40	0.60
B	5.80	6.20	R1	0.07TYP	
B1	3.80	4.00	R2	0.07TYP	
B2	5.0TYP		θ1	17°TYP	
C	1.30	1.50	θ2	13°TYP	
C1	0.55	0.65	θ3	4°TYP	
C2	0.55	0.65	θ4	12°TYP	

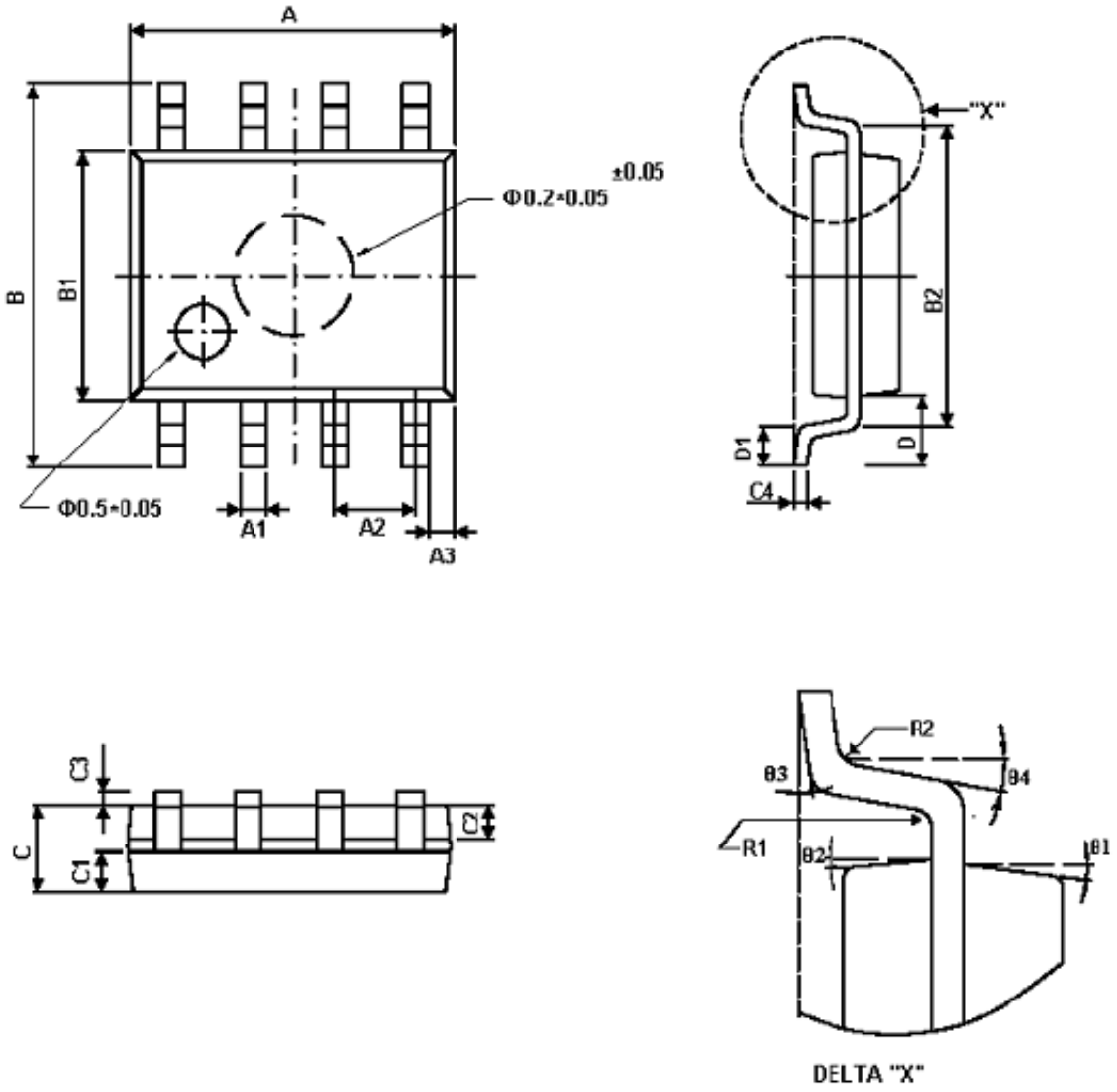

Figure 11: Chip SOP8 Package Size Information