Revision History

Rev. No.	History	Issue Date	Remark
1.3	Add green code in part no.	Jul. 22, 2005	
1.4	Add in 28L TSOP 1-8x13.4mm	Mar. 10,2006	
1.5	Remove 28L TSOP 1-8x13.4mm	Jun. 12,2006	
1.6	Revise speed option and DC/AC Characteristics.	Mar. 05,2007	
1.7	Remove 28L PDIP 300mil	Apr. 24,2007	
1.8	Increase version description in Order Information	Sep, 05, 2008	

■ DESCRIPTION

The CS18HS02565 series products are 32,768-words by 8-bits static RAMs fabricated with advanced 8" wafer submicron CMOS technology. Using unique CMOS peripheral circuits and special poly-load 4-transistor memory cells, the CS18HS02565 series products exhibit very high-speed performance with single +5-volt power supply while requiring low power and no clock or refreshing to operate. The CS18HS02565 is packed in 28-pin SOP-330mil and 28-pin SOJ-300mil.

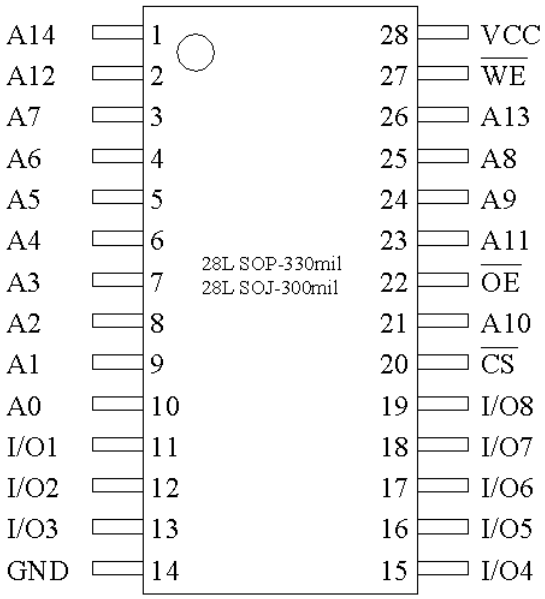
■ FEATURES

1. 32,768-word x 8-bit organization
2. Operation voltage: 4.5 ~ 5.5V
3. Fully static operation: no clock or refreshing required
4. LVTTL-compatible inputs and outputs
5. Common I/O capability
6. Low power consumption
   - Active: 45/35 mA（Max.）
   - Standby: 350 μA
7. Very high speed access: 10/12 ns
8. Output Enable ($\overline{OE}$) available for very fast access

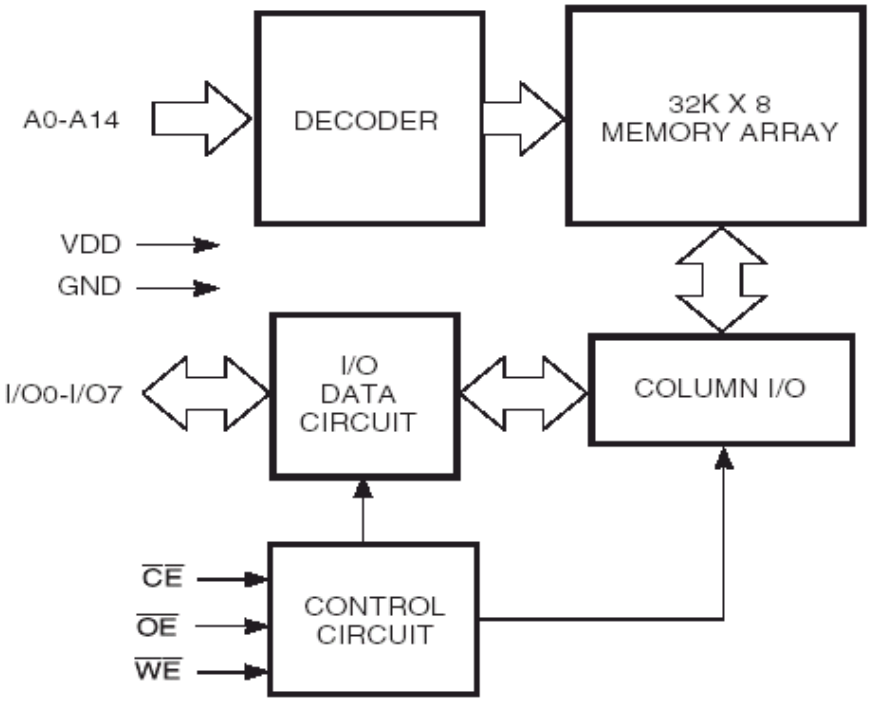
■ Product Family

Part No.	Operating Temp	Vcc. Range	Speed (ns)	Supply Current mA (Max.)	Package Type
CS18HS02565	0~70°C	4.5~5.5V	10	45	28 SOP-330mil 28 SOJ-300mil
			12	35	

■ PIN CONFIGURATIONS



■ BLOCK DIAGRAM



■ PIN DESCRIPTIONS

Symbols	Functions
A0～A14	Address Inputs
I/O1～I/O8	Data Inputs / Outputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{CC}	Power Supply
Vss	Ground

■ TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O1～I/O8	V_{CC} Current
H	X	X	Not Selected	High Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High Z	I_{DD}
L	L	H	Read	Data Out	I_{DD}
L	X	L	Write	Data In	I_{DD}

■ ABSOLUTE MAXIMUM RATINGS

Parameters	Rating	Unit
Supply Voltage to Vss	-0.5 to +7.0	V
Input/Output to Vss	-0.5 to V_{CC} +0.5	V
Allowable Power Dissipation	1.5	W
Storage Temperature	-65 to +150	℃
Operating Temperature	0 to +70	℃

■ OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0~70°C	5.0V±5%

■ DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, Vss = 0V, Ta = 0 to 70℃)

Parameters	Symbols	Test Conditions		Min.	Typ.	Max	Unit
Input Low Voltage	V_{IL}	-		-0.3	-	0.8	V
Input High Voltage	V_{IH}	-		2.2	-	V_{CC}+0.5	V
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{CC}		-1	-	+1	μA
Output Leakage Current	I_{LO}	$V_{I/O}$ = V_{SS} to V_{CC}, $\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}		-1	-	+1	μA
Output Low Voltage	V_{OL}	I_{OL} = +8.0mA		-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA		2.4	-	-	V
Operating Power Supply Current	I_{DD}	$\overline{CS}$ = V_{IL}, I/O = 0 mA Cycle = MIN Duty = 100%	10	-	-	45	mA
			12	-	-	35	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}, Cycle = MIN Duty = 100%		-	-	1	mA
	I_{SB1}	$\overline{CS} \geqq$ V_{CC} -0.2V		-	-	350	μA

Note: Typical characteristics are measured at V_{CC} = 5 V, Ta = 25℃

■ AC Characteristics:

Capacitances

(V_{CC} = 5V, Ta = 25℃, f = 1 MHz)

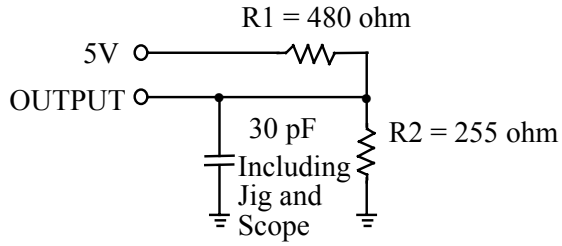
Parameters	Symbols	Conditions	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	8	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT} = 0V	10	pF

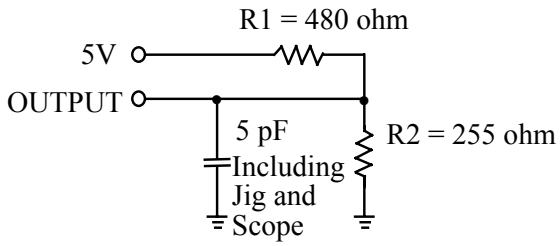
Note: These parameters are sampled but not 100% tested.

AC Test Conditions

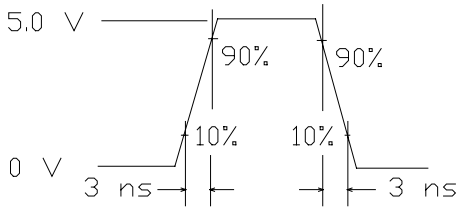
Parameters	Conditions
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3 ns
Input and Output Timing Reference Level	1.5V
Output Load	C_L = 30 pF, I_{OH}/I_{OL} = -4 mA / 8 mA

■ AC Test Loads and Waveforms





(For T_{CLZ}, T_{OLZ}, T_{CHZ}, T_{OHZ}, T_{WHZ}, T_{OW})



■ AC Performances:

(VCC = 5V, VSS = 0V, Ta = 0 to 70℃)

(1) Read Cycle

Parameters	Symbols	CS18HS02565-10		CS18HS02565-12		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	TRC	10	-	12	-	ns
Address Access Time	TAA	-	10	-	12	ns
Chip Select Access Time	TACS	-	10	-	12	ns
Output Enable to Output Valid	TAOE	-	6	-	6	ns
Chip Selection to Output in Low Z	TCLZ*	2	-	3	-	ns
Output Enable to Output in Low Z	TOLZ*	0	-	0	-	ns
Chip Deselection to Output in High Z	TCHZ*	-	5	-	6	ns
Output Disable to Output in High Z	TOHZ*	-	5	-	7	ns
Output Hold from Address Change	TOH	2	-	2	-	ns

■ These parameters are sampled but not 100% tested

(2) Write Cycle

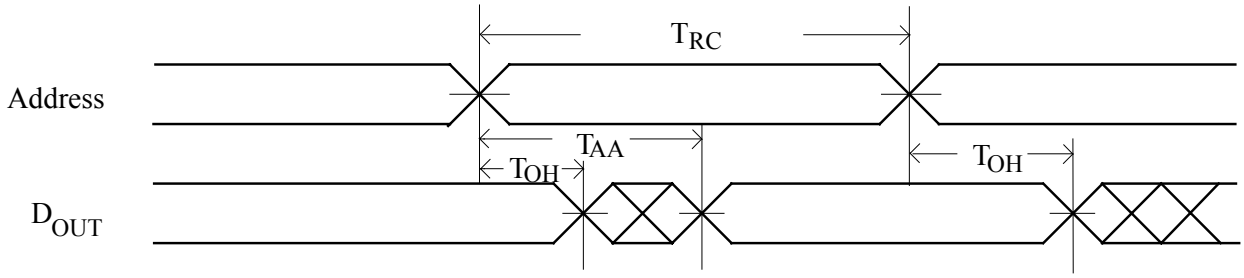
Parameters	Symbols	CS18HS02565-10		CS18HS02565-12		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	TWC	10	-	12	-	ns
Chip Selection to End of Write	TCW	9	-	10	-	ns
Address Valid to End of Write	TAW	9	-	10	-	ns
Address Setup Time	TAS	0	-	0	-	ns
Write Pulse Width	TWP	9	-	9	-	ns
Write Recovery Time	TWR	0	-	0	-	ns
Data Valid to End of Write	TDW	7	-	7	-	ns
Data Hold from End of Write	TDH	0	-	0	-	ns
Write to Output in High Z	TWHZ*	-	6	-	6	ns
Output Disable to Output in High Z	TOHZ*	-	6	-	6	ns
Output Active from End of Write	TOW	0	-	0	-	ns

■ These parameters are sampled but not 100% tested

■ Timing Waveforms

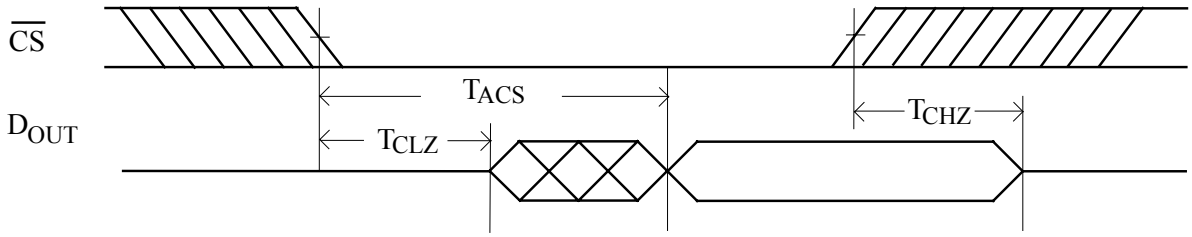
Read Cycle 1

(Address Controlled)



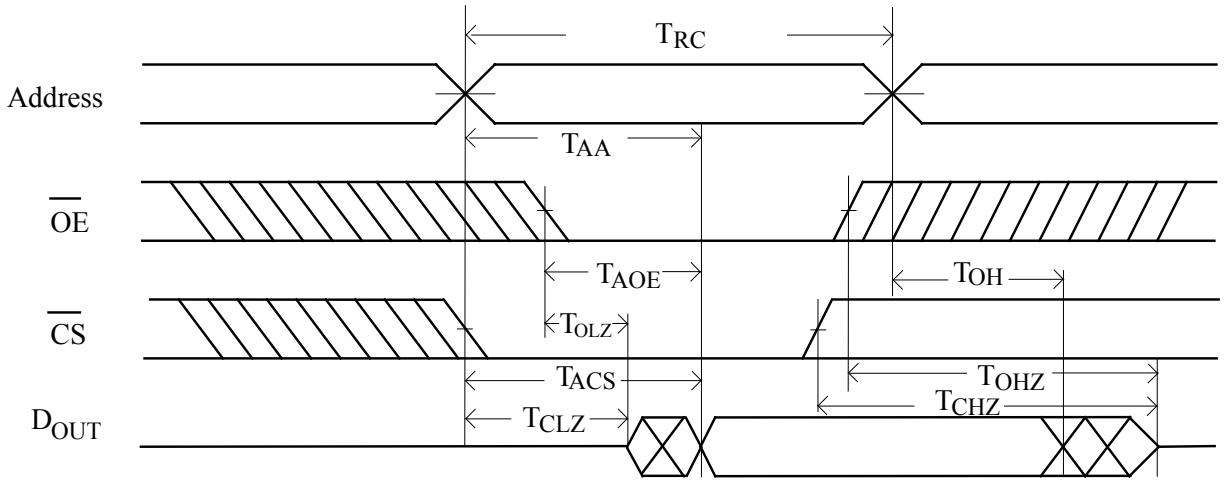
Read Cycle 2

(Chip Select Controlled)



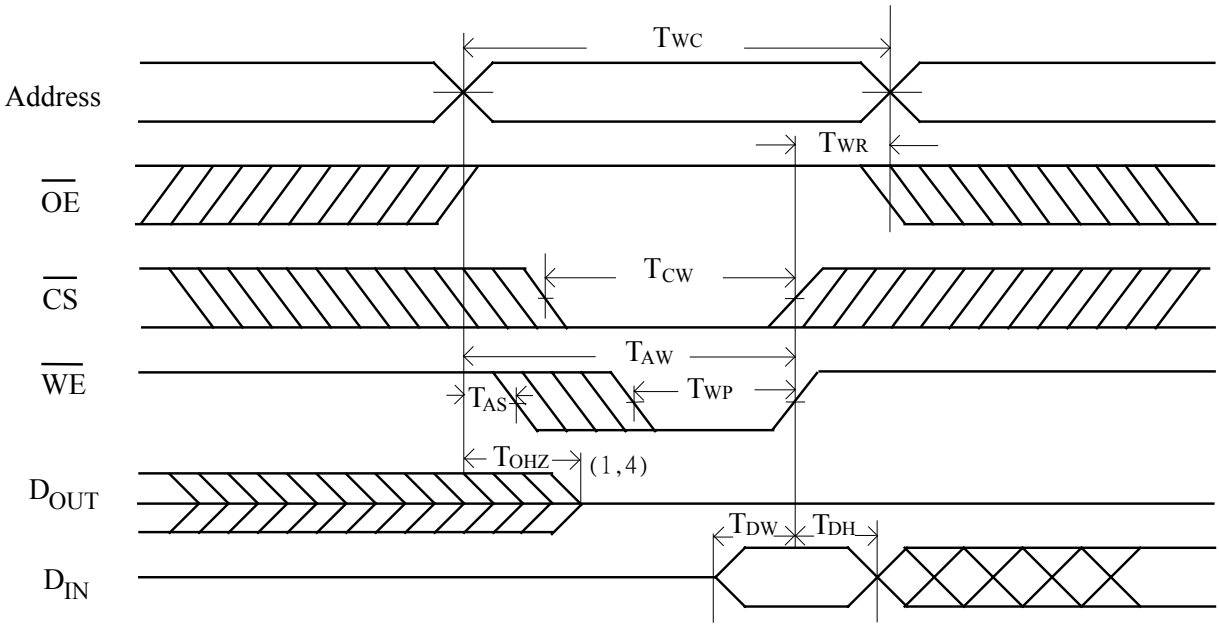
Read Cycle 3

(Output Enable Controlled)



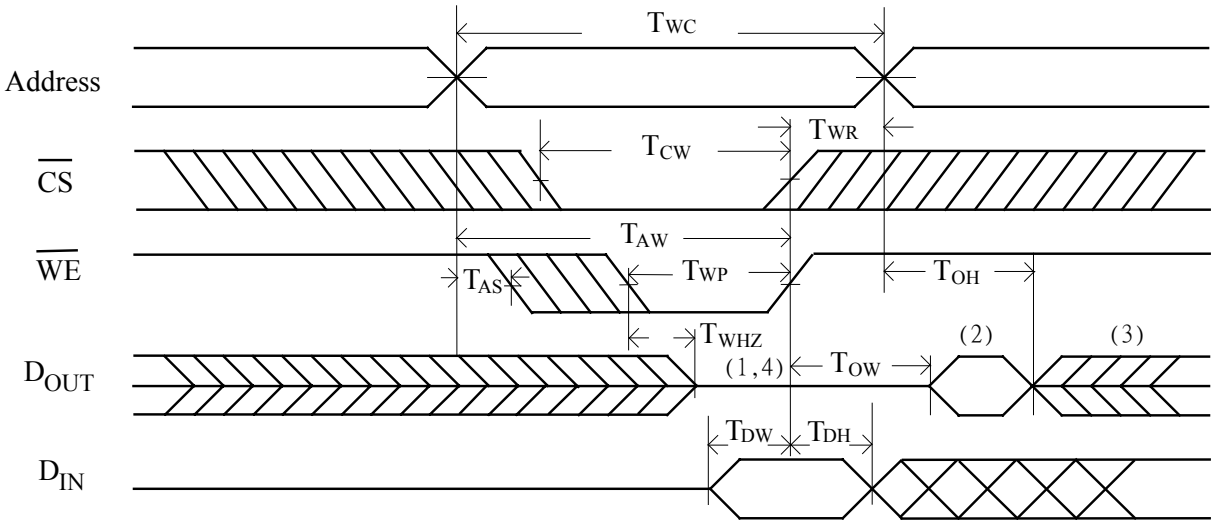
Write Cycle 1

($\overline{OE}$ Clock)



Write Cycle 2

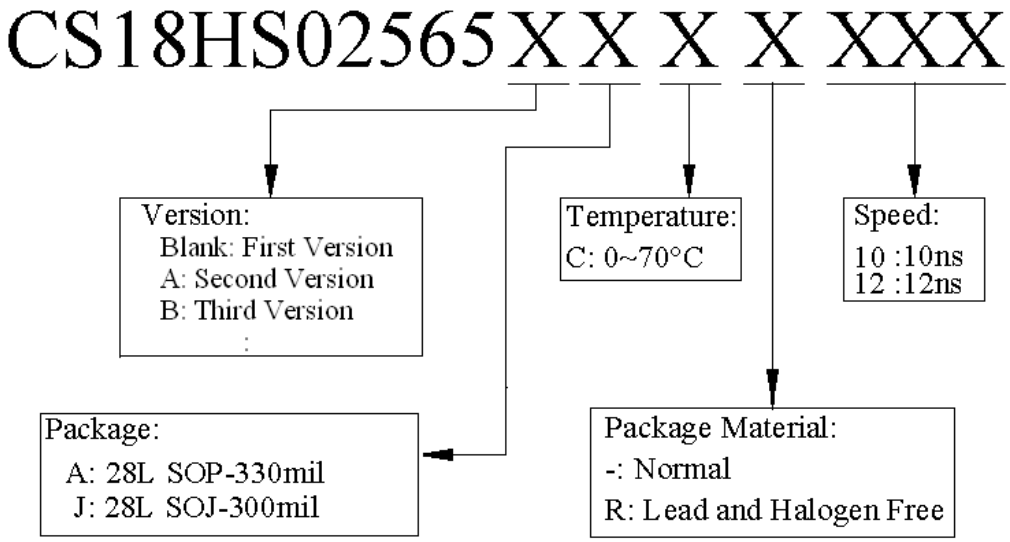
($\overline{OE}$ = VIL Fixed)



Notes:

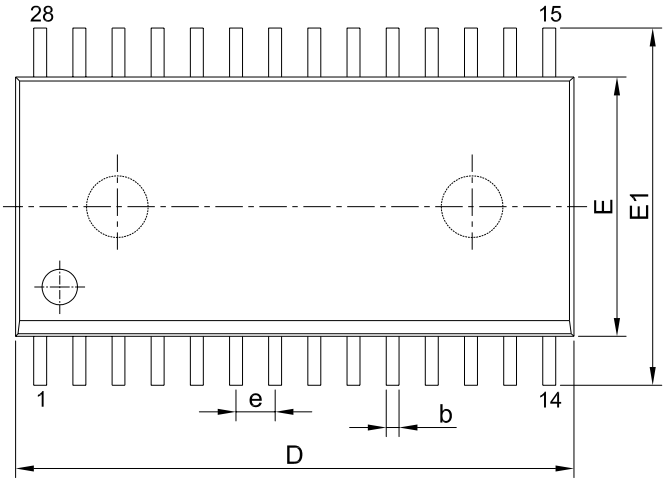
1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from D_{OUT} are the same as the data written to D_{IN} during the write cycle.
3. D_{OUT} provides the read data for the next address.
4. Transition is measured ±500mV from steady state with CL = 5pF. This parameter is guaranteed but not 100% tested.

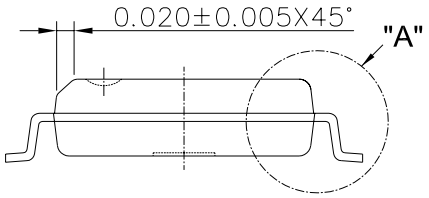
■ ORDER INFORMATION

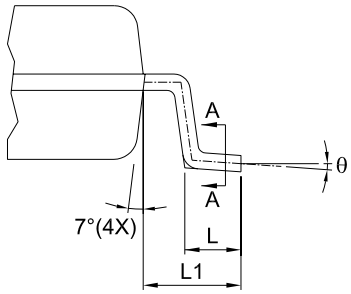


Note: Package material code “R” meets ROHS

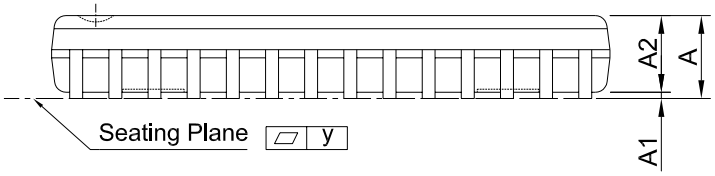
■ PACKAGE DIMENSIONS - 28L SOP -330mil

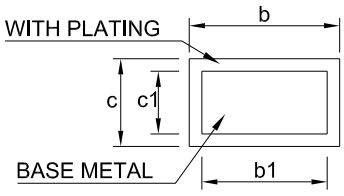






DETAIL "A" (2:1)

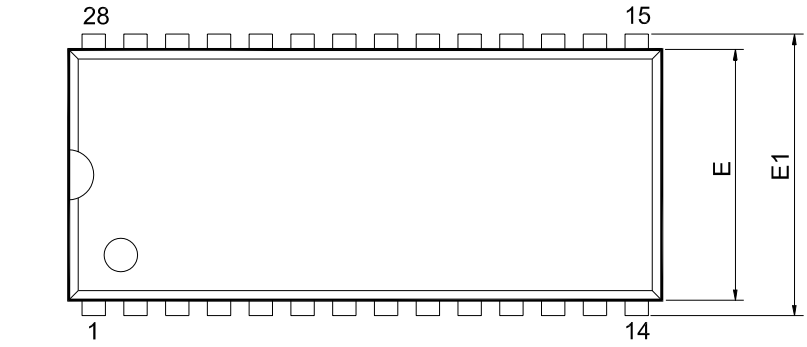


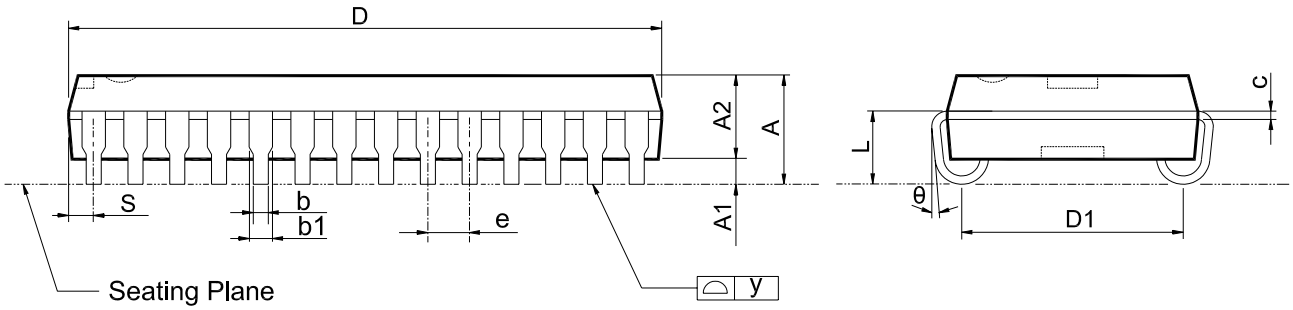


SECTION A-A

SYMBOL / UNIT		A	A1	A2	b	b1	c	c1	D	E	E1	e	L	L1	y	⊙
mm	Min.	2.540	0.102	2.362	0.35	0.35	0.20	0.20	17.983	8.280	11.506	1.118	0.700	1.520	–	0°
	Nom.	2.692	0.226	2.489	–	–	–	–	18.110	8.407	11.811	1.270	0.964	1.720	–	–
	Max.	2.844	0.350	2.616	0.50	0.45	0.32	0.28	18.237	8.534	12.116	1.422	1.228	1.920	0.1	10°
inch	Min.	0.100	0.004	0.093	0.014	0.014	0.008	0.008	0.708	0.326	0.453	0.044	0.0276	0.0598	–	0°
	Nom.	0.106	0.009	0.098	–	–	–	–	0.713	0.331	0.465	0.050	0.0380	0.0677	–	–
	Max.	0.112	0.014	0.103	0.020	0.018	0.012	0.011	0.718	0.336	0.477	0.056	0.0484	0.0756	0.004	10°

■ PACKAGE DIMENSIONS - 28L SOJ -300mil





SYMBOL / UNIT		A	A1	A2	b1	b	c	D	E	e	D1	E1	L	S	y	⊖
mm	Min.	–	0.69	2.41	0.66	0.41	0.20	–	7.49	1.12	6.22	8.31	1.96	–	–	0°
	Nom.	–	–	2.54	0.71	0.46	0.25	18.03	7.62	1.27	6.73	8.56	2.21	–	–	–
	Max.	3.56	–	2.67	0.81	0.56	0.36	18.54	7.75	1.42	7.24	8.81	2.46	1.14	0.10	10°
inch	Min.	–	0.027	0.095	0.026	0.016	0.008	–	0.295	0.044	0.245	0.327	0.077	–	–	0°
	Nom.	–	–	0.100	0.028	0.018	0.010	0.710	0.300	0.050	0.265	0.337	0.087	–	–	–
	Max.	0.140	–	0.105	0.032	0.022	0.014	0.730	0.305	0.056	0.285	0.347	0.097	0.045	0.004	10°