CS2500

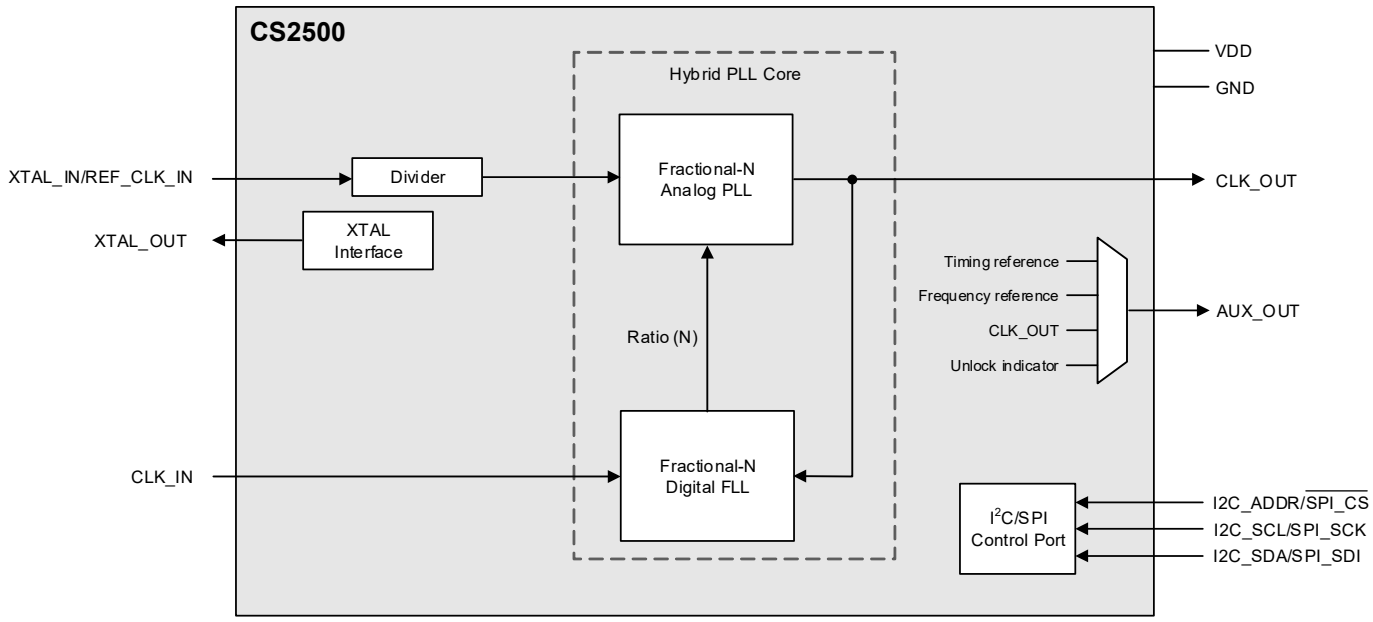
Fractional-N Clock Synthesizer and Multiplier

Features

- Clock frequency synthesizer incorporating delta-sigma fractional-N analog PLL
  - — Generates low-jitter 6–75 MHz clock (CLK_OUT) from 8–75 MHz timing reference (REF_CLK_IN)
- Fractional clock multiplier and jitter reduction using hybrid analog/digital PLL
  - — Generates low-jitter 6–75 MHz clock (CLK_OUT), synchronized to a 50 Hz–30 MHz low-quality or intermittent frequency reference (CLK_IN)
- Flexible timing reference source
  - — External clock or external crystal
- High resolution PLL ratio (1 PPM)
- 40 ps_{RMS} period jitter
- Glitchless clock output generated from intermittent input
- I²C/SPI control port
- Configurable auxiliary clock/status output
- Minimal board space required
  - — No external analog loop-filter components
- Pin-to-pin, register map, and control compatible with CS2000 and CS2200
- Single-supply operation at 1.8 V or 3.3 V

Applications

- Automotive audio systems
- Digital audio systems
- Network and USB audio interfaces
- IoT sensor and transducer systems
- Embedded systems



Advanced Product Information

This document contains information for a product under development. Cirrus Logic reserves the right to modify this product.

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General Description

The CS2500 is a system-clocking device incorporating a programmable phase-locked loop (PLL). The hybrid analog/digital PLL architecture comprises a delta-sigma fractional-N analog PLL and a digital frequency-locked loop (FLL). The CS2500 enables frequency synthesis and clock generation from a stable timing reference clock. The device can generate low-jitter clocks from a noisy clock reference at frequencies as low as 50 Hz. The CS2500 can be configured using a control interface supporting I²C and SPI modes of operation.

The CS2500 can be powered from a single 1.8 V or 3.3 V supply. The device combines high performance with low power consumption.

The CS2500 is available in commercial-grade 10-pin TSSOP package for operation from –40°C to +85°C. The device is also available in the AEC-Q100-qualified grade-2 package for operation from –40°C to +105°C.

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1 Pin Assignments and Descriptions

These sections show pin assignments and describe pin functions.

1.1 TSSOP Pin Assignments (Top View, Through Package)

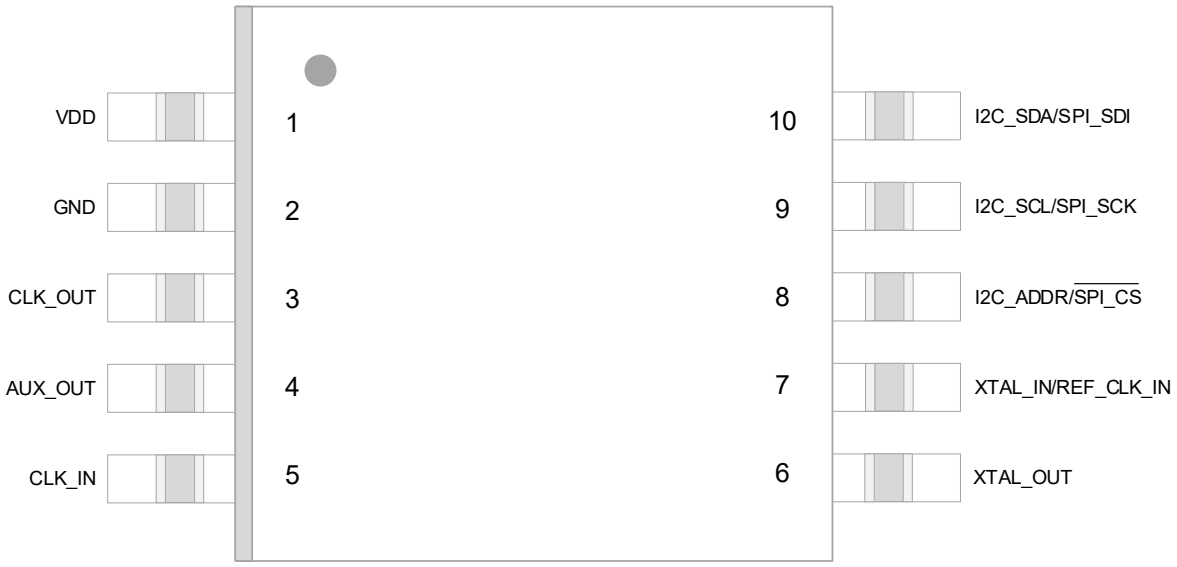


Figure 1-1. TSSOP 10-Pin Diagram (Top View, Through-Package)

Note the CS2500 is pin-to-pin compatible with CS2000 and CS2200.

1.2 Pin Descriptions

Table 1-1. Pin Descriptions

Pin Name	Pin #	Power Supply	I/O	Description
VDD	1	—	—	**Power Supply.** 3.3 V/1.8 V supply for the digital and analog blocks.
GND	2	—	—	**Ground**.
CLK_OUT	3	VDD	O	**Clock Output.** PLL clock output.
AUX_OUT	4	VDD	O	**Auxiliary Output.** Configurable clock output or status output.
CLK_IN	5	VDD	I	**Clock Input.** Frequency reference input for the digital FLL.
XTAL_OUT	6	VDD	O	**Crystal Connection.** Output for an external crystal.
XTAL_IN/REF_CLK_IN	7	VDD	I	**Crystal Connection.** Input for an external crystal. **Reference Clock.** External low-jitter timing reference clock input.
I2C_ADDR/$\overline{\text{SPI\_CS}}$	8	VDD	I	**I²C Control-Port Address.** Chip address input for the I²C interface. **SPI Control-Port Chip Select.** Active-low chip select input for the SPI interface.
I2C_SCL/SPI_SCK	9	VDD	I	**I²C Control-Port Clock.** Clock input for the I²C interface. **SPI Control-Port Clock.** Clock input for the SPI interface.
I2C_SDA/SPI_SDI	10	VDD	I/O	**I²C Control-Port Data.** Data input/output for the I²C interface. **SPI Control-Port Serial Data In.** SPI data input.

1.3 Electrostatic Discharge (ESD) Protection Circuitry

ESD-sensitive device. The CS2500 is manufactured on a CMOS process. Therefore, it is generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken while handling and storing this device. This device is qualified to current JEDEC ESD standards.

2 Typical Connections

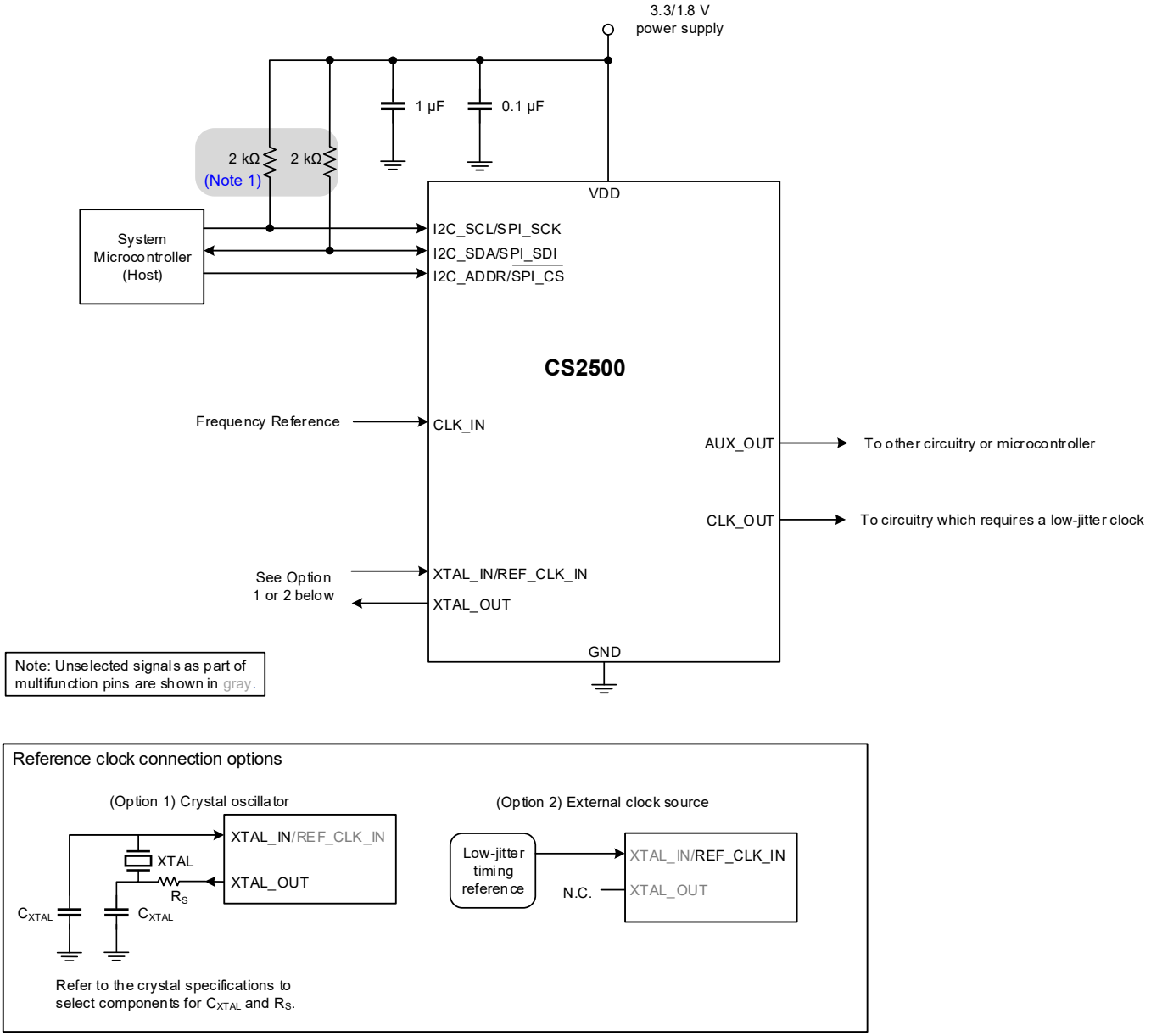


Figure 2-1. Typical Connection Diagram

Note referenced in the typical connection diagram:

1. The pull-up resistors are required only for I²C operation. The diagram shows 2 kΩ pull-up, but higher impedance can be supported depending on clock speed and bus capacitance.

3 Characteristics and Specifications

Table 3-1. Recommended Operating Conditions

Test Conditions (unless specified otherwise): Ground = GND = 0 V; voltages are with respect to ground.

Parameters	Symbol	Min	Typ	Max	Units
DC power supply	VDD	3.1	3.3	3.5	V
		1.71	1.8	1.89	V
Supply ramp up/down	t_{PWR_UD}	0.01	—	10	ms
Ambient temperature — Commercial Grade	T_A	–40	—	85	°C
Ambient temperature — AEC-Q100 Grade 2	T_A	–40	—	105	°C

Table 3-2. Absolute Maximum Ratings

Test Conditions (unless specified otherwise): Ground = GND = 0 V; voltages are with respect to ground.

Parameters	Symbol	Min	Max	Units
DC power supply	VDD	–0.3	4.32	V
External voltage applied to digital input/output	V_{INDI}	–0.3	VDD + 0.3	V
Input current	I_{in}	—	±10	mA
Ambient temperature	T_A	–55	125	°C
Storage temperature	T_{STG}	–65	150	°C

Table 3-3. DC Electrical Characteristics

Test Conditions (unless specified otherwise): T_A = 25°C; timing reference = 12 MHz (external clock or crystal).

Parameters	Symbol	Min	Typ	Max	Units
Power supply current—unloaded [1]	I_{VDD}	—	4	—	mA
Input leakage current (per pin)	I_{IN}	—	—	±10	µA
Input capacitance (per pin)	I_C	—	—	5	pF
High-level input voltage	V_{IH}	0.70 × VDD	—	—	V
Low-level input voltage	V_{IL}	—	—	0.30 × VDD	V
High-level output voltage	V_{OH}	0.90 × VDD	—	—	V
Low-level output voltage	V_{OL}	—	—	0.10 × VDD	V

1. To calculate the additional current consumption due to loading (per output pin), multiply clock output frequency by load capacitance (C_L) and power supply voltage (VDD).

Table 3-4. AC Electrical Characteristics

Test Conditions (unless specified otherwise): T_A = –40°C to 85°C (commercial grade); T_A = –40°C to 105°C (AEC-Q100 grade-2); Load capacitance (C_L) = 15 pF.

Parameters		Symbol	Min	Typ	Max	Units
Crystal frequency	REF_CLK_IN_DIV = 10 REF_CLK_IN_DIV = 01 REF_CLK_IN_DIV = 00	f_{XTAL}	8 16 32	— — —	18.75 37.50 50	MHz MHz MHz
Reference clock input frequency	REF_CLK_IN_DIV = 10 REF_CLK_IN_DIV = 01 REF_CLK_IN_DIV = 00	$f_{REF\_CLK\_IN}$	8 16 32	— — —	18.75 37.50 75	MHz MHz MHz
Reference clock input duty cycle		$D_{REF\_CLK\_IN}$	45	—	55	%
Clock input frequency		f_{CLK_IN}	50	—	30×10^6	Hz
Clock input pulse width	$f_{CLK\_IN} < f_{SYSCLK} / 96$ [1] $f_{CLK\_IN} > f_{SYSCLK} / 96$ [1]	pw_{CLK_IN}	2 10	— —	— —	UI [2] ns
Clock skipping timeout		t_{CS}	20	—	—	ms
Clock skipping input frequency		f_{CLK_SKIP}	50	—	80×10^3	Hz
CLK_OUT frequency range		f_{CLK_OUT}	6	—	75	MHz
Clock output duty cycle	measured at VDD / 2	t_{OD}	45	50	55	%
Clock output rise time	10% to 90% of VDD	t_{OR}	—	2.5	—	ns
Clock output fall time	90% to 10% of VDD	t_{OF}	—	2.5	—	ns
CLK_OUT period jitter [3,4]		t_{JIT}	—	40	TBD	ps_{RMS}
CLK_OUT baseband TIE jitter [3,5]		—	—	50	TBD	ps_{RMS}
CLK_OUT wideband TIE jitter [3,6]		—	—	165	TBD	ps_{RMS}
PLL lock time—Multiplier Mode	f_{CLK_IN} < 200 kHz f_{CLK_IN} > 200 kHz	t_{LC}	— —	100 1	200 3	UI [7] ms
PLL lock time—Synthesizer Mode	$f_{REF\_CLK\_IN}$ = 8 to 75 MHz	t_{LR}	—	1	3	ms
CLK_OUT frequency resolution [3,8]	high resolution high multiplication	—	— —	1 224	— —	ppm ppm
Clock output frequency deviation	CLK_IN stopped, holdover enabled	—	—	—	0.1	%

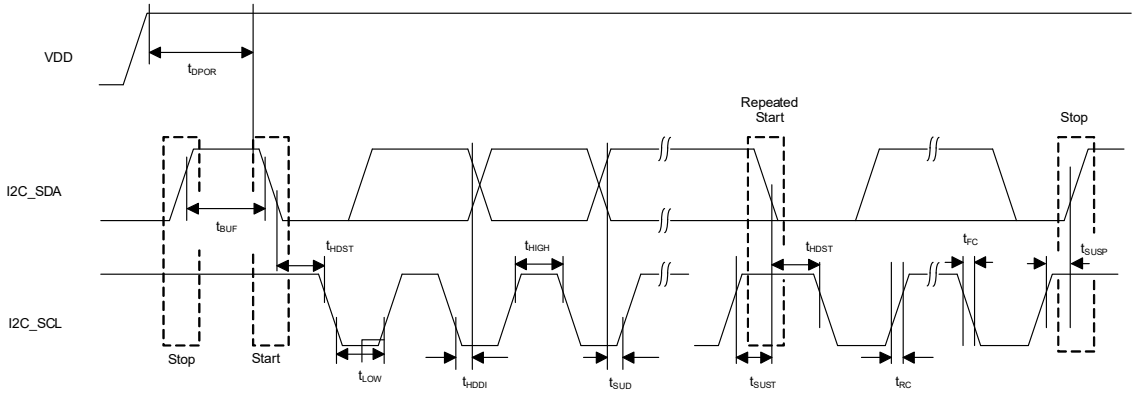
1. The internal timing reference clock (SYSCLK) is derived from REF_CLK_IN.
2. UI (unit interval) corresponds to t_{SYSCLK} or 1 / f_{SYSCLK}.
3. REF_CLK_IN is a 12 MHz timing reference clock, with phase noise 20 dB lower than the output clock noise. The clock output frequency (f_{CLK_OUT}) is 24.576 MHz.
4. Sample size is 10000.
5. Using 3rd order 100 Hz–40 kHz bandpass filter as defined in AES-12id-2020 Section 3.4.2.
6. Using 3rd order 100 Hz high pass filter as defined in AES-12id-2020 Section 3.4.1.
7. UI (unit interval) corresponds to t_{CLK_IN} or 1 / f_{CLK_IN}.
8. The frequency accuracy of the PLL clock output is directly proportional to the accuracy of the clock input.

Table 3-5. Switching Specifications—I²C Control Port

Test conditions (unless specified otherwise): Ground = GND = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds; T_A = 25°C.

Parameters [1,2]	Symbol	Min	Max	Units
SCL clock frequency	f_{SCL}	—	400	kHz
Clock low time	t_{LOW}	4.7	—	µs
Clock high time	t_{HIGH}	4.0	—	µs
Start condition hold time (before first pulse clock)	t_{HDST}	4.0	—	µs
Setup time for repeated start	t_{SUST}	4.7	—	µs
Rise time of SCL and SDA $f_{SCL} \le 100$ kHz 100 kHz < $f_{SCL} \le 400$ kHz	t_{RC}	— —	1000 300	ns ns
Fall time SCL and SDA $f_{SCL} \le 100$ kHz 100 kHz < $f_{SCL} \le 400$ kHz	t_{FC}	— —	300 300	ns ns
Setup time for stop condition	t_{SUSP}	4.7	—	µs
SDA setup time to SCL rising	t_{SUD}	250	—	ns
SDA input hold time from SCL falling	t_{HDDI}	0	—	ns
Bus free time between transmissions	t_{BUF}	4.7	—	µs
Start-up time from power-up/software reset to control port ready [3]	t_{DPOR}	—	200	µs

1. The I²C control port uses a 8-bit register address and 8-bit data words.
2. I²C control-port timing.



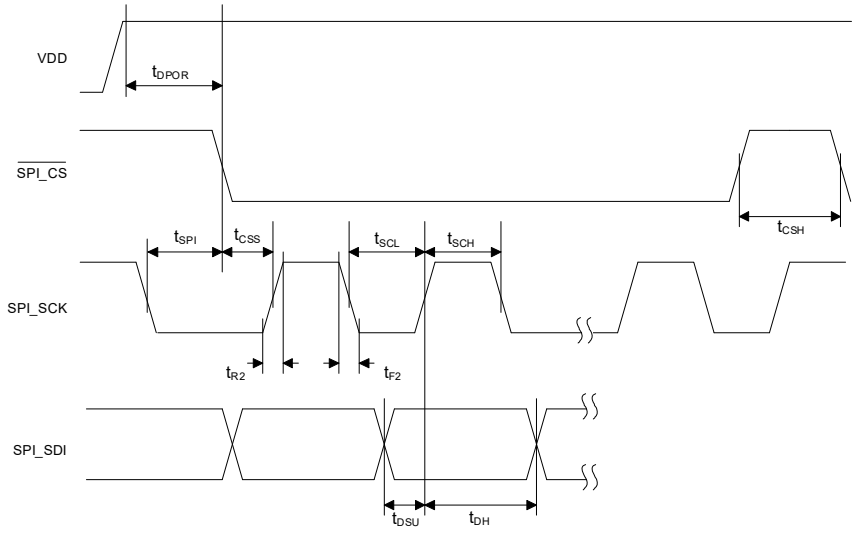
3. Time from power-up measured from when VDD is within the recommended operating conditions (see Table 3-1).

Table 3-6. Switching Specifications—SPI Control Port

Test conditions (unless specified otherwise): Ground = GND = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds; T_A = 25°C.

Parameters [1,2]	Symbol	Min	Max	Units
SCK clock frequency	f_{SCL}	—	6	MHz
SCK edge to $\overline{CS}$ falling [3]	t_{SPI}	500	—	ns
$\overline{CS}$ high time between transmissions	t_{CSH}	1	—	µs
$\overline{CS}$ falling to SCK rising edge	t_{CSS}	20	—	ns
SCK pulse width low	t_{SCL}	66	—	ns
SCK pulse width high	t_{SCH}	66	—	ns
SDI to SCK rising setup time	t_{DSU}	40	—	ns
SCK rising to SDI hold time [4]	t_{DH}	15	—	ns
Rise time of SCK and SDI [5]	t_{R2}	—	100	ns
Fall time of SCK and SDI [5]	t_{F2}	—	100	ns
Delay from supply voltage stable to control port ready [6]	t_{DPOR}	—	200	µs

1. The SPI control port uses a 7-bit register address and 8-bit data words.
2. SPI control-port timing.



3. t_{SPI} is only needed before first falling edge of $\overline{CS}$ after power is applied; t_{SPI} is 0 all other times.
4. Data must be held for sufficient time to bridge the transition time of SCK.
5. For f_{SCK} < 1 MHz.
6. The supply voltage is considered stable when VDD is within the recommended operating conditions (see Table 3-1).

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com.