

## Fractional-N Clock Multiplier

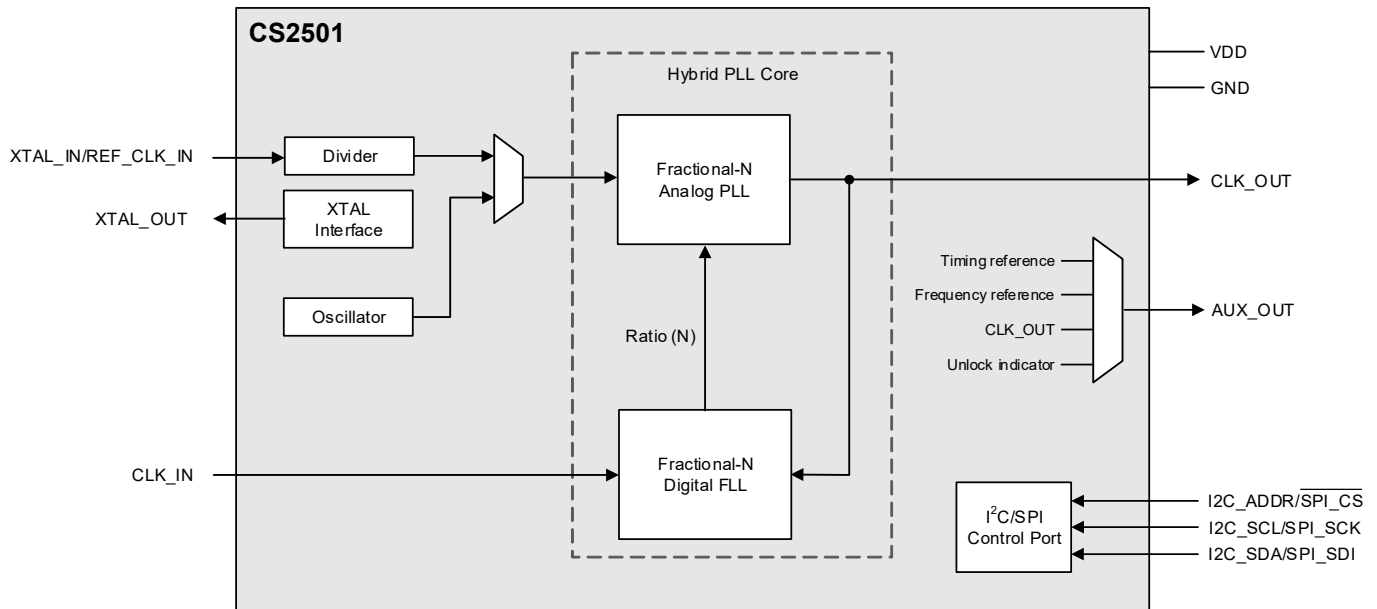
### Features

- Fractional clock multiplier and jitter reduction using hybrid analog/digital PLL
  - Generates low-jitter 6–75 MHz clock (CLK\_OUT), synchronized to a 50 Hz–30 MHz low-quality or intermittent frequency reference (CLK\_IN)
- Flexible timing reference source
  - External clock, external crystal, or built-in oscillator
- High resolution PLL ratio (1 PPM)
- 40 ps<sub>RMS</sub> period jitter (external timing reference), 35 ps<sub>RMS</sub> period jitter (oscillator reference)
- Glitchless clock output generated from intermittent input

- I<sup>2</sup>C/SPI control port
- Configurable auxiliary clock/status output
- Minimal board space required
  - No external analog loop-filter components
- Pin-to-pin, register map, and control compatible with CS2100 and CS2300
- Single-supply operation at 1.8 V or 3.3 V

### Applications

- Automotive audio systems
- Digital audio systems
- Network and USB audio interfaces
- IoT sensor and transducer systems
- Embedded systems



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## General Description

The CS2501 is a system-clocking device incorporating a programmable phase-locked loop (PLL). The hybrid analog/digital PLL architecture comprises a delta-sigma fractional-N analog PLL and a digital frequency-locked loop (FLL). The CS2501 enables clock generation from a stable timing reference clock. The device can generate low-jitter clocks from a noisy clock reference at frequencies as low as 50 Hz. An internal oscillator can provide the timing reference clock, enabling a reduction in external component requirements. The CS2501 can be configured using a control interface supporting I<sup>2</sup>C and SPI modes of operation.

The CS2501 can be powered from a single 1.8 V or 3.3 V supply. The device combines high performance with low power consumption.

The CS2501 is available in commercial-grade 10-pin TSSOP package for operation from –40°C to +85°C. The device is also available in the AEC-Q100-qualified grade-2 package for operation from –40°C to +105°C.

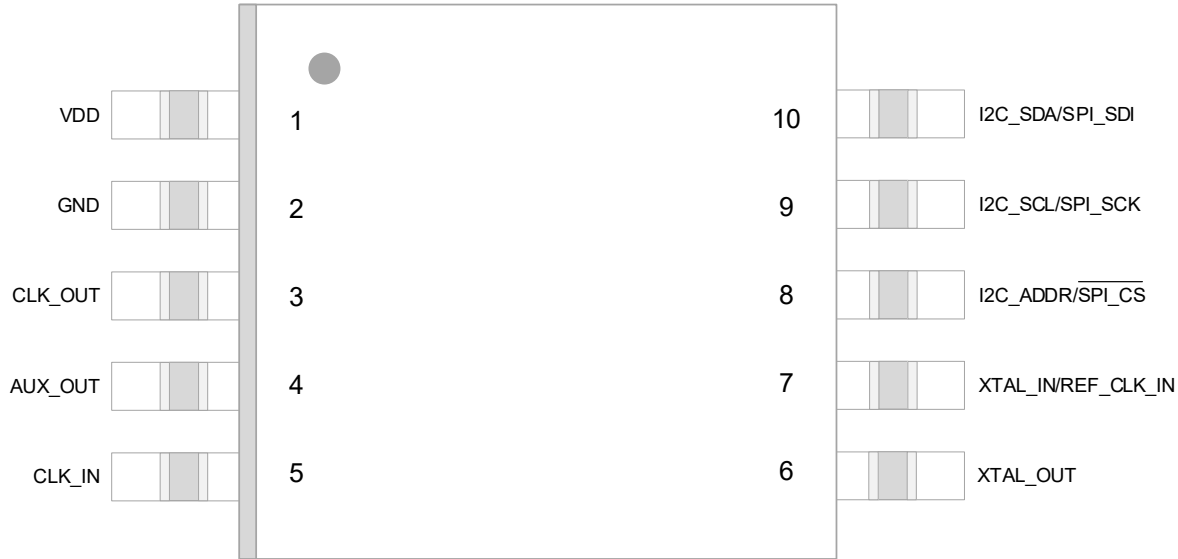
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# 1 Pin Assignments and Descriptions

These sections show pin assignments and describe pin functions.

## 1.1 TSSOP Pin Assignments (Top View, Through Package)



**Figure 1-1. TSSOP 10-Pin Diagram (Top View, Through-Package)**

Note the CS2501 is pin-to-pin compatible with CS2100 and CS2300.

## 1.2 Pin Descriptions

**Table 1-1. Pin Descriptions**

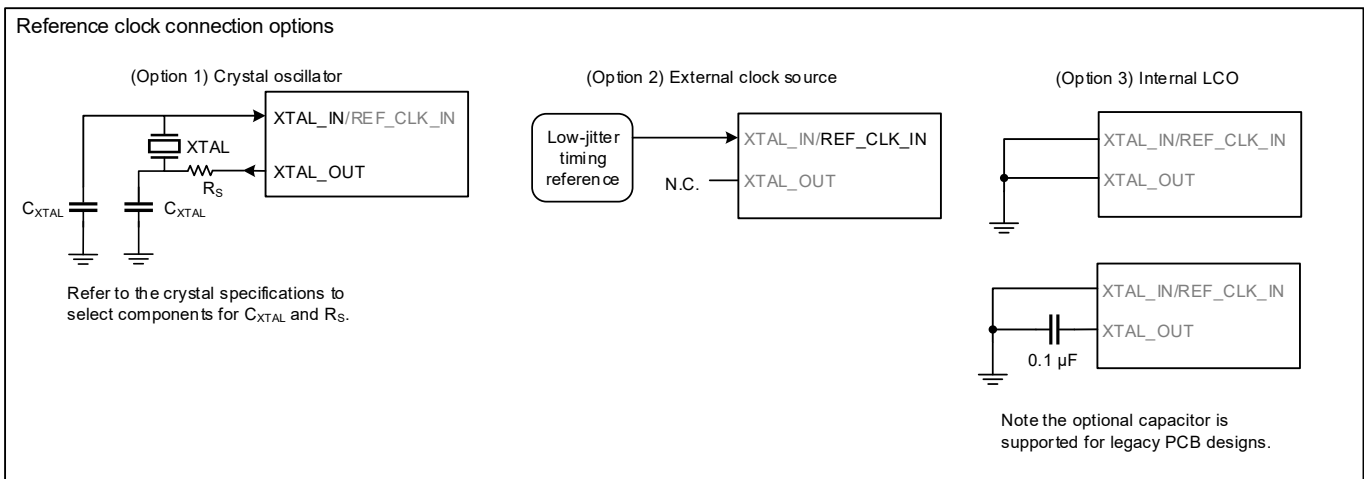
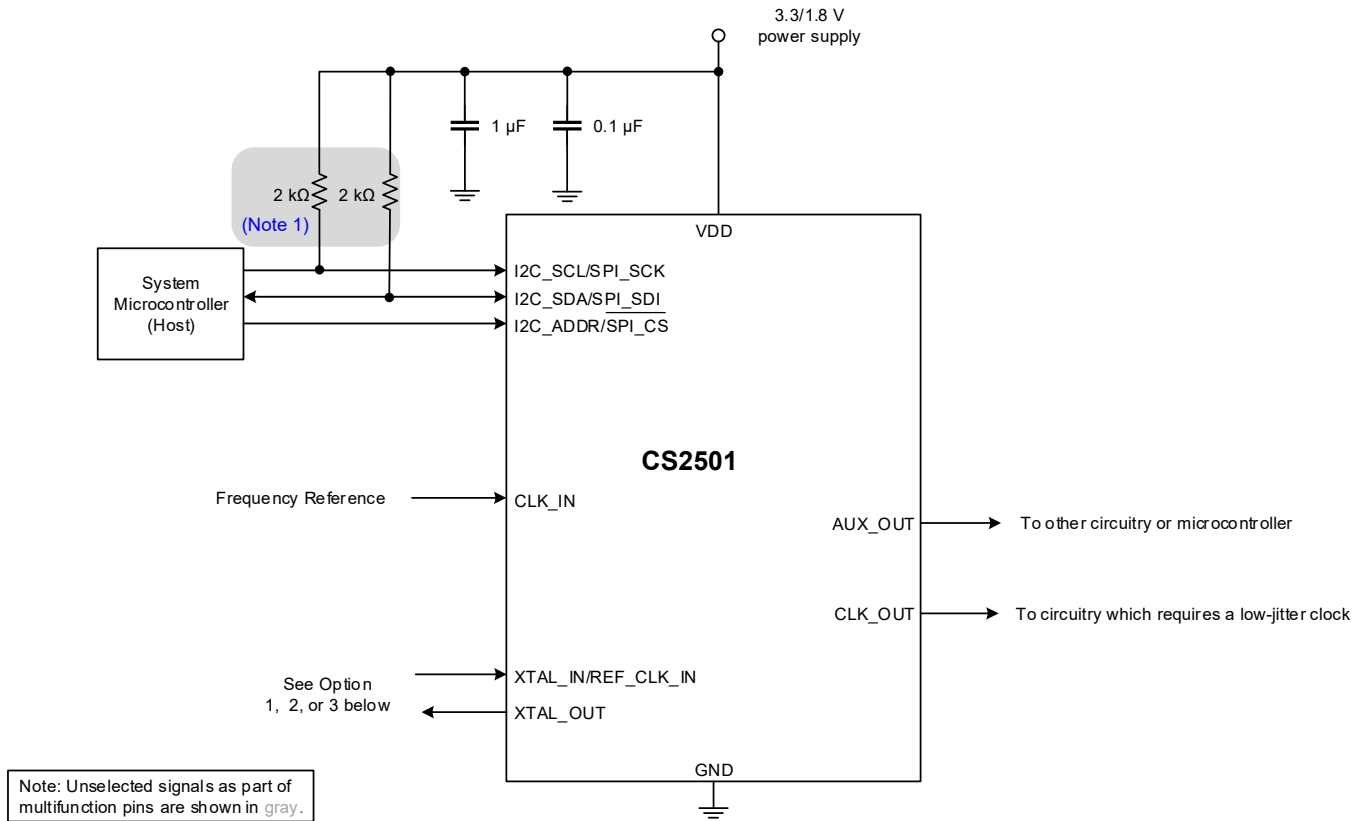
Pin Name	Pin #	Power Supply	I/O	Description
VDD	1	—	—	<b>Power Supply.</b> 3.3 V/1.8 V supply for the digital and analog blocks.
GND	2	—	—	<b>Ground.</b>
CLK_OUT	3	VDD	O	<b>Clock Output.</b> PLL clock output.
AUX_OUT	4	VDD	O	<b>Auxiliary Output.</b> Configurable clock output or status output.
CLK_IN	5	VDD	I	<b>Clock Input.</b> Frequency reference input for the digital FLL.
XTAL_OUT	6	VDD	O	<b>Crystal Connection.</b> Output for an external crystal. Connect to GND for internal oscillator reference clock. (A capacitor connection is also supported for legacy PCB designs, as shown in <a href="#">Section 2.</a> )
XTAL_IN/REF_CLK_IN	7	VDD	I	<b>Crystal Connection.</b> Input for an external crystal. <b>Reference Clock.</b> External low-jitter timing reference clock input. Connect to GND for internal oscillator reference clock.
I2C_ADDR/SPI_CS	8	VDD	I	<b>I2C Control-Port Address.</b> Chip address input for the I2C interface. <b>SPI Control-Port Chip Select.</b> Active-low chip select input for the SPI interface.
I2C_SCL/SPI_SCK	9	VDD	I	<b>I2C Control-Port Clock.</b> Clock input for the I2C interface. <b>SPI Control-Port Clock.</b> Clock input for the SPI interface.
I2C_SDA/SPI_SDI	10	VDD	I/O	<b>I2C Control-Port Data.</b> Data input/output for the I2C interface. <b>SPI Control-Port Serial Data In.</b> SPI data input.

### 1.3 Electrostatic Discharge (ESD) Protection Circuitry



ESD-sensitive device. The CS2501 is manufactured on a CMOS process. Therefore, it is generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken while handling and storing this device. This device is qualified to current JEDEC ESD standards.

## 2 Typical Connections



**Figure 2-1. Typical Connection Diagram**

Note referenced in the typical connection diagram:

1. The pull-up resistors are required only for I<sup>2</sup>C operation. The diagram shows 2 kΩ pull-up, but higher impedance can be supported depending on clock speed and bus capacitance.

### 3 Characteristics and Specifications

**Table 3-1. Recommended Operating Conditions**

Test Conditions (unless specified otherwise): Ground = GND = 0 V; voltages are with respect to ground.

Parameters	Symbol	Min	Typ	Max	Units
DC power supply	VDD	3.1	3.3	3.5	V
		1.71	1.8	1.89	V
Supply ramp up/down	$t_{PWR\_UD}$	0.01	—	10	ms
Ambient temperature	$T_A$	Commercial Grade	—	85	°C
		AEC-Q100 Grade 2	—40	—	105

**Table 3-2. Absolute Maximum Ratings**

Test Conditions (unless specified otherwise): Ground = GND = 0 V; voltages are with respect to ground.

Parameters	Symbol	Min	Max	Units
DC power supply	VDD	−0.3	4.32	V
External voltage applied to digital input/output	$V_{INDI}$	−0.3	VDD + 0.3	V
Input current	$I_{in}$	—	±10	mA
Ambient temperature	$T_A$	−55	125	°C
Storage temperature	$T_{STG}$	−65	150	°C

**Table 3-3. DC Electrical Characteristics**

Test Conditions (unless specified otherwise):  $T_A = 25^\circ\text{C}$ ; timing reference = 12 MHz (external clock or crystal).

Parameters	Symbol	Min	Typ	Max	Units
Power supply current—unloaded <sup>1</sup>	$I_{VDD}$	—	4	—	mA
Input leakage current (per pin)	$I_{IN}$	—	—	±10	µA
Input capacitance (per pin)	$I_C$	—	—	5	pF
High-level input voltage	$V_{IH}$	$0.70 \times VDD$	—	—	V
Low-level input voltage	$V_{IL}$	—	—	$0.30 \times VDD$	V
High-level output voltage	$V_{OH}$	$0.90 \times VDD$	—	—	V
Low-level output voltage	$V_{OL}$	—	—	$0.10 \times VDD$	V

1. To calculate the additional current consumption due to loading (per output pin), multiply clock output frequency by load capacitance ( $C_L$ ) and power supply voltage (VDD).

**Table 3-4. AC Electrical Characteristics**

Test Conditions (unless specified otherwise):  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  (commercial grade);  $T_A = -40^\circ\text{C}$  to  $105^\circ\text{C}$  (AEC-Q100 grade-2); Load capacitance ( $C_L$ ) = 15 pF.

Parameters	Symbol	Min	Typ	Max	Units	
Crystal frequency	$f_{\text{XTAL}}$	REF_CLK_IN_DIV = 10	8	—	18.75	MHz
		REF_CLK_IN_DIV = 01	16	—	37.50	MHz
		REF_CLK_IN_DIV = 00	32	—	50	MHz
Reference clock input frequency	$f_{\text{REF\_CLK\_IN}}$	REF_CLK_IN_DIV = 10	8	—	18.75	MHz
		REF_CLK_IN_DIV = 01	16	—	37.50	MHz
		REF_CLK_IN_DIV = 00	32	—	75	MHz
Reference clock input duty cycle	$D_{\text{REF\_CLK\_IN}}$	45	—	55	%	
Clock input frequency	$f_{\text{CLK\_IN}}$	50	—	$30 \times 10^6$	Hz	
Clock input pulse width	$p_{\text{W\_CLK\_IN}}$	$f_{\text{CLK\_IN}} < f_{\text{SYSCLK}} / 96$ [1]	2	—	—	UI <sup>2</sup>
		$f_{\text{CLK\_IN}} > f_{\text{SYSCLK}} / 96$ [1]	10	—	—	ns
Clock skipping timeout	$t_{\text{CS}}$	20	—	—	ms	
Clock skipping input frequency	$f_{\text{CLK\_SKIP}}$	50	—	$80 \times 10^3$	Hz	
CLK_OUT frequency range	$f_{\text{CLK\_OUT}}$	6	—	75	MHz	
Clock output duty cycle	$t_{\text{OD}}$	45	50	55	%	
Clock output rise time	$t_{\text{OR}}$	—	2.5	—	ns	
Clock output fall time	$t_{\text{OF}}$	—	2.5	—	ns	
CLK_OUT period jitter <sup>3,4</sup>	$t_{\text{JIT}}$	external timing reference	—	40	TBD	pSRMS
		internal oscillator reference	—	35	TBD	pSRMS
CLK_OUT baseband TIE jitter <sup>3,5</sup>	—	external timing reference	—	50	TBD	pSRMS
		internal oscillator reference	—	300	TBD	pSRMS
CLK_OUT wideband TIE jitter <sup>3,6</sup>	—	external timing reference	—	165	TBD	pSRMS
		internal oscillator reference	—	300	TBD	pSRMS
PLL lock time	$t_{\text{LC}}$	$f_{\text{CLK\_IN}} < 200$ kHz	—	100	200	UI <sup>7</sup>
		$f_{\text{CLK\_IN}} > 200$ kHz	—	1	3	ms
CLK_OUT frequency resolution <sup>3,8</sup>	—	high resolution	—	1	—	ppm
		high multiplication	—	224	—	ppm
Oscillator frequency	—	11.76	12.0	12.24	MHz	
Oscillator frequency thermal sensitivity	—	—	50	—	ppm/ $^\circ\text{C}$	
Oscillator frequency stability (relative to $25^\circ\text{C}$ )	—	$-40$ to $85^\circ\text{C}$	—0.2	—	0.4	%
		$-40$ to $105^\circ\text{C}$	—0.2	—	0.6	%
Clock output frequency deviation	—	—	—	0.1	%	

1. The internal timing reference clock (SYSCLK) is derived from REF\_CLK\_IN.

2. UI (unit interval) corresponds to  $t_{\text{SYSCLK}}$  or  $1 / f_{\text{SYSCLK}}$ .

3. REF\_CLK\_IN is a 12 MHz timing reference clock, with phase noise 20 dB lower than the output clock noise. The clock output frequency ( $f_{\text{CLK\_OUT}}$ ) is 24.576 MHz.

4. Sample size is 10000.

5. Using 3rd order 100 Hz–40 kHz bandpass filter as defined in AES-12id-2020 Section 3.4.2.

6. Using 3rd order 100 Hz high pass filter as defined in AES-12id-2020 Section 3.4.1.

7. UI (unit interval) corresponds to  $t_{\text{CLK\_IN}}$  or  $1 / f_{\text{CLK\_IN}}$ .

8. The frequency accuracy of the PLL clock output is directly proportional to the accuracy of the clock input.

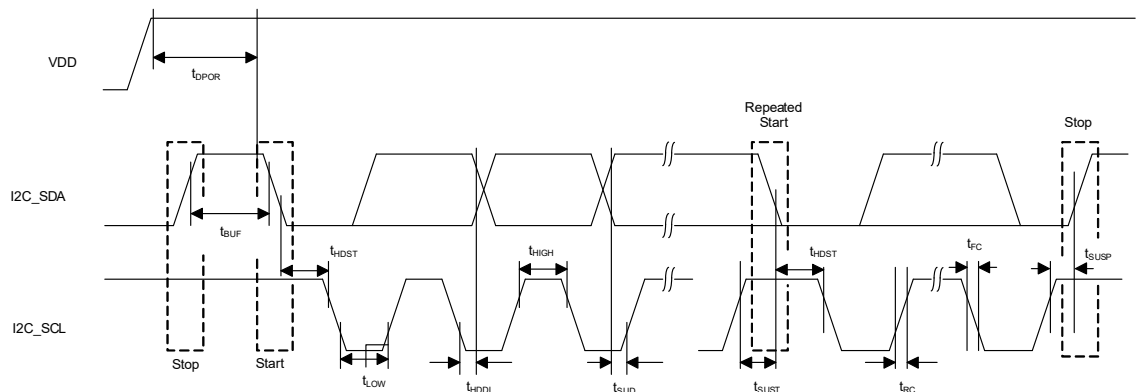
**Table 3-5. Switching Specifications—I2C Control Port**

Test conditions (unless specified otherwise): Ground = GND = 0 V; voltages are with respect to ground; input timings are measured at  $V_{IL}$  and  $V_{IH}$  thresholds, output timings are measured at  $V_{OL}$  and  $V_{OH}$  thresholds;  $T_A = 25^\circ\text{C}$ .

Parameters <sup>1,2</sup>	Symbol	Min	Max	Units
SCL clock frequency	$f_{SCL}$	—	400	kHz
Clock low time	$t_{LOW}$	4.7	—	$\mu\text{s}$
Clock high time	$t_{HIGH}$	4.0	—	$\mu\text{s}$
Start condition hold time (before first pulse clock)	$t_{HDST}$	4.0	—	$\mu\text{s}$
Setup time for repeated start	$t_{SUST}$	4.7	—	$\mu\text{s}$
Rise time of SCL and SDA	$f_{SCL} \leq 100 \text{ kHz}$	—	1000	ns
	$100 \text{ kHz} < f_{SCL} \leq 400 \text{ kHz}$	—	300	ns
Fall time SCL and SDA	$f_{SCL} \leq 100 \text{ kHz}$	—	300	ns
	$100 \text{ kHz} < f_{SCL} \leq 400 \text{ kHz}$	—	300	ns
Setup time for stop condition	$t_{SUSP}$	4.7	—	$\mu\text{s}$
SDA setup time to SCL rising	$t_{SUD}$	250	—	ns
SDA input hold time from SCL falling	$t_{HDDI}$	0	—	ns
Bus free time between transmissions	$t_{BUF}$	4.7	—	$\mu\text{s}$
Start-up time from power-up/software reset to control port ready <sup>3</sup>	$t_{DPOR}$	—	200	$\mu\text{s}$

1. The I2C control port uses a 8-bit register address and 8-bit data words.

2. I2C control-port timing.



3. Time from power-up measured from when VDD is within the recommended operating conditions (see Table 3-1).

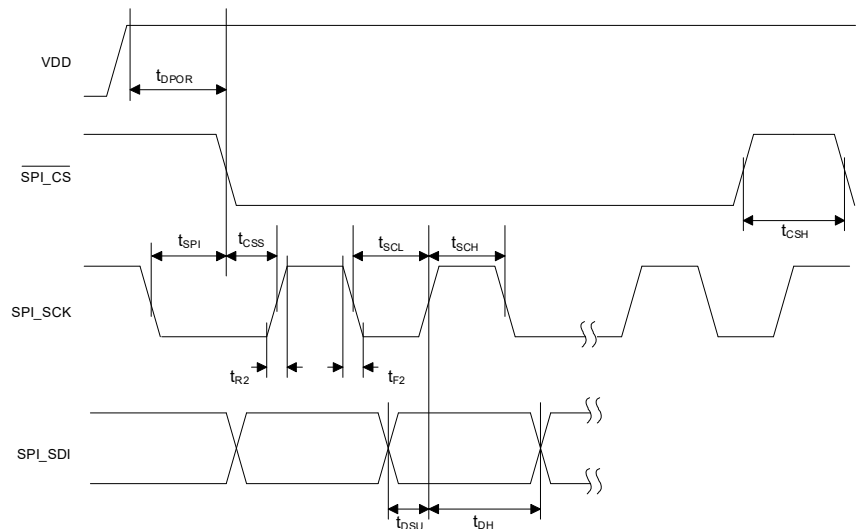


**Table 3-6. Switching Specifications—SPI Control Port**

Test conditions (unless specified otherwise): Ground = GND = 0 V; voltages are with respect to ground; input timings are measured at  $V_{IL}$  and  $V_{IH}$  thresholds, output timings are measured at  $V_{OL}$  and  $V_{OH}$  thresholds;  $T_A = 25^\circ\text{C}$ .

Parameters <sup>1,2</sup>	Symbol	Min	Max	Units
SCK clock frequency	$f_{SCL}$	—	6	MHz
SCK edge to $\overline{CS}$ falling <sup>3</sup>	$t_{SPI}$	500	—	ns
$\overline{CS}$ high time between transmissions	$t_{CSH}$	1	—	$\mu\text{s}$
$\overline{CS}$ falling to SCK rising edge	$t_{CSS}$	20	—	ns
SCK pulse width low	$t_{SCL}$	66	—	ns
SCK pulse width high	$t_{SCH}$	66	—	ns
SDI to SCK rising setup time	$t_{DSU}$	40	—	ns
SCK rising to SDI hold time <sup>4</sup>	$t_{DH}$	15	—	ns
Rise time of SCK and SDI <sup>5</sup>	$t_{R2}$	—	100	ns
Fall time of SCK and SDI <sup>5</sup>	$t_{F2}$	—	100	ns
Delay from supply voltage stable to control port ready <sup>6</sup>	$t_{DPOR}$	—	200	$\mu\text{s}$

1. The SPI control port uses a 7-bit register address and 8-bit data words.
2. SPI control-port timing.



3.  $t_{SPI}$  is only needed before first falling edge of  $\overline{CS}$  after power is applied;  $t_{SPI}$  is 0 all other times.
4. Data must be held for sufficient time to bridge the transition time of SCK.
5. For  $f_{SCK} < 1$  MHz.
6. The supply voltage is considered stable when VDD is within the recommended operating conditions (see [Table 3-1](#)).

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