



# CS2N65 A3

## General Description:

CS2N65 A3, the silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-251, which accords with the RoHS standard..

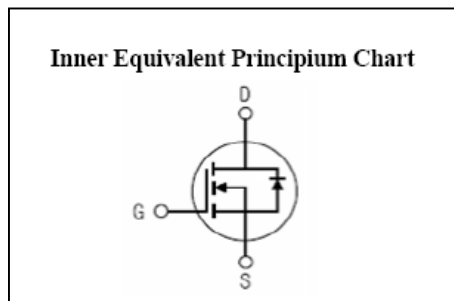
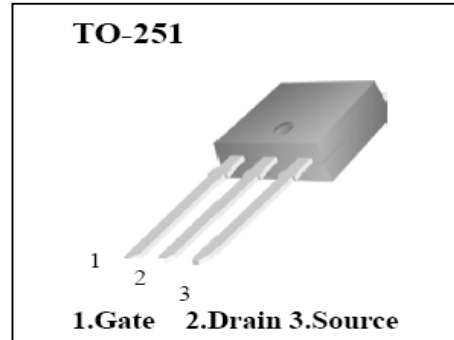
## Features:

- I **Fast Switching**
- I **Low ON Resistance**( $R_{dson} \leq 5\Omega$ )
- I **Low Gate Charge** (Typical Data:9nC)
- I **Low Reverse transfer capacitances**(Typical:6pF)
- I **100% Single Pulse avalanche energy Test**

## Applications:

Power switch circuit of adaptor and charger.

$V_{DSS}$	650	V
$I_D$	2	A
$P_D$ ( $T_C=25^\circ\text{C}$ )	35	W
$R_{DS(ON)Typ}$	3.9	$\Omega$



**Absolute** ( $T_c = 25^\circ\text{C}$  unless otherwise specified)

Symbol	Parameter	Rating	Units
$V_{DSS}$	Drain-to-Source Voltage	650	V
$I_D$	Continuous Drain Current	2.0	A
	Continuous Drain Current $T_C = 100^\circ\text{C}$	1.45	A
$I_{DM}^{a1}$	Pulsed Drain Current	8	A
$V_{GS}$	Gate-to-Source Voltage	$\pm 30$	V
$E_{AS}^{a2}$	Single Pulse Avalanche Energy	68	mJ
$E_{AR}^{a1}$	Avalanche Energy ,Repetitive	6.4	mJ
$I_{AR}^{a1}$	Avalanche Current	1.1	A
$dv/dt^{a3}$	Peak Diode Recovery dv/dt	5	V/ns
$P_D$	Power Dissipation	35	W
	Derating Factor above $25^\circ\text{C}$	0.28	W/ $^\circ\text{C}$
$T_J, T_{stg}$	Operating Junction and Storage Temperature Range	150, $-55$ to 150	$^\circ\text{C}$
$T_L$	Maximum Temperature for Soldering	300	$^\circ\text{C}$



# CS2N65 A3



## Electrical Characteristics (Tc= 25°C unless otherwise specified):

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V <sub>DSS</sub>	Drain to Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	650	--	--	V
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Bvdss Temperature Coefficient	ID=250uA, Reference 25°C	--	0.6	--	V/°C
I <sub>DSS</sub>	Drain to Source Leakage Current	V <sub>DS</sub> = 650V, V <sub>GS</sub> = 0V, T <sub>a</sub> = 25°C	--	--	1	μA
		V <sub>DS</sub> =520V, V <sub>GS</sub> = 0V, T <sub>a</sub> = 125°C			100	
I <sub>GSS(F)</sub>	Gate to Source Forward Leakage	V <sub>GS</sub> = 30V	--	--	100	nA
I <sub>GSS(R)</sub>	Gate to Source Reverse Leakage	V <sub>GS</sub> =-30V	--	--	-100	nA

ON Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
R <sub>DS(ON)</sub>	Drain-to-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =1.0A	--	3.9	4.5	Ω
V <sub>GS(TH)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	2.0		4.0	V
Pulse width tp ≤ 300μs, δ ≤ 2%						

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g <sub>fs</sub>	Forward Trans conductance	V <sub>DS</sub> =15V, I <sub>D</sub> =2A		2.6	--	S
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> = 0V V <sub>DS</sub> = 25V f = 1.0MHz	--	290		pF
C <sub>oss</sub>	Output Capacitance		--	31		
C <sub>rss</sub>	Reverse Transfer Capacitance		--	6		

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
t <sub>d(ON)</sub>	Turn-on Delay Time	I <sub>D</sub> =2.0A V <sub>DD</sub> = 325V V <sub>GS</sub> = 10V R <sub>G</sub> = 9.1Ω	--	8	--	ns
t <sub>r</sub>	Rise Time		--	6	--	
t <sub>d(OFF)</sub>	Turn-Off Delay Time		--	30	--	
t <sub>f</sub>	Fall Time		--	11	--	
Q <sub>g</sub>	Total Gate Charge	I <sub>D</sub> =2.0A V <sub>DD</sub> =325V V <sub>GS</sub> = 10V	--	9		nC
Q <sub>gs</sub>	Gate to Source Charge		--	1.5		
Q <sub>gd</sub>	Gate to Drain ("Miller") Charge		--	4		



Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$I_S$	Continuous Source Current (Body Diode)		--	--	2	A
$I_{SM}$	Maximum Pulsed Current (Body Diode)		--	--	8	A
$V_{SD}$	Diode Forward Voltage	$I_S=2.0A, V_{GS}=0V$	--	--	1.5	V
$t_{rr}$	Reverse Recovery Time	$I_S=2.0A, T_j = 25^\circ C$	--	425	--	ns
$Q_{rr}$	Reverse Recovery Charge	$dI_f/dt=100A/us, V_{GS}=0V$	--	1140	--	nC
Pulse width $t_p \leq 300\mu s, \delta \leq 2\%$						

Symbol	Parameter	Typ.	Units
$R_{\theta JC}$	Junction-to-Case	3.57	$^\circ C/W$
$R_{\theta JA}$	Junction-to-Ambient	62	$^\circ C/W$

<sup>a1</sup>: Repetitive rating; pulse width limited by maximum junction temperature

<sup>a2</sup>:  $L=10.0mH, I_D=3.7A, Start T_j=25^\circ C$

<sup>a3</sup>:  $I_{SD}=2A, di/dt \leq 100A/us, V_{DD} \leq BV_{DS}, Start T_j=25^\circ C$

## Characteristics Curve:

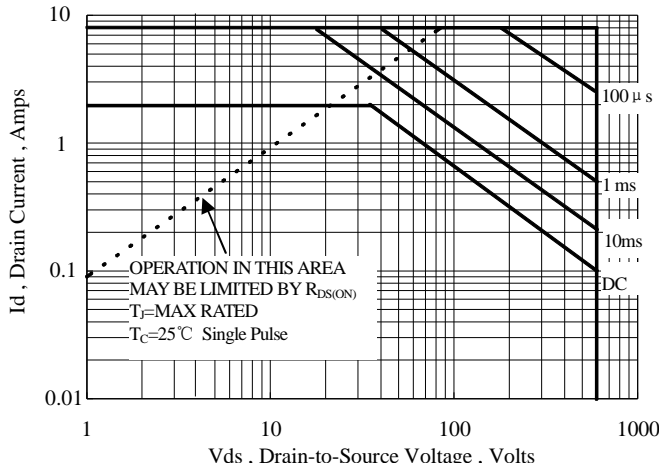


Figure 1 Maximum Forward Bias Safe Operating Area

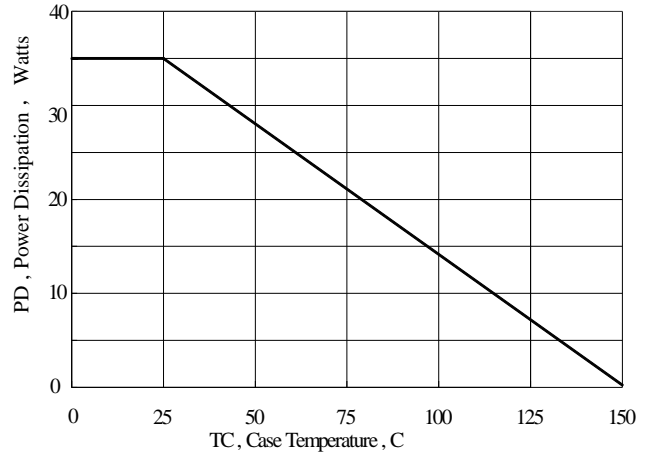


Figure 2 Maximum Power Dissipation vs Case Temperature

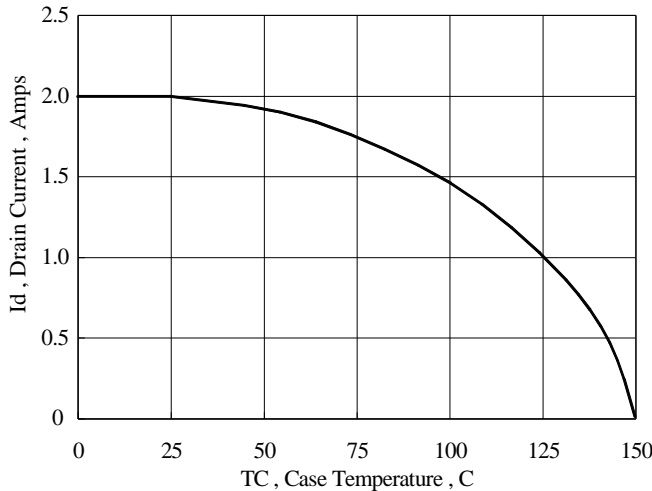


Figure 3 Maximum Continuous Drain Current vs Case Temperature

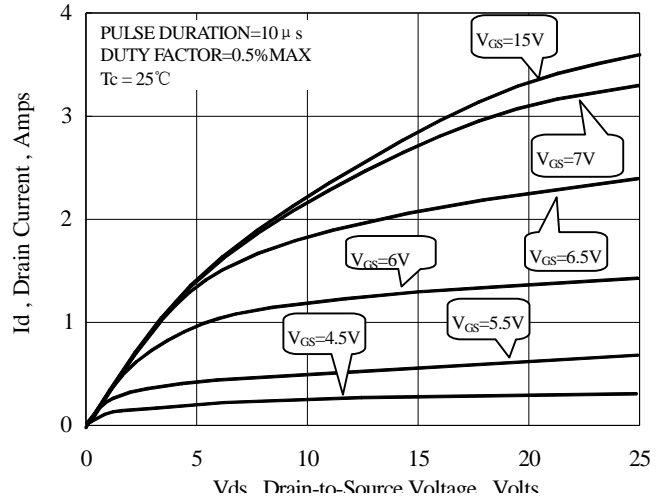


Figure 4 Typical Output Characteristics

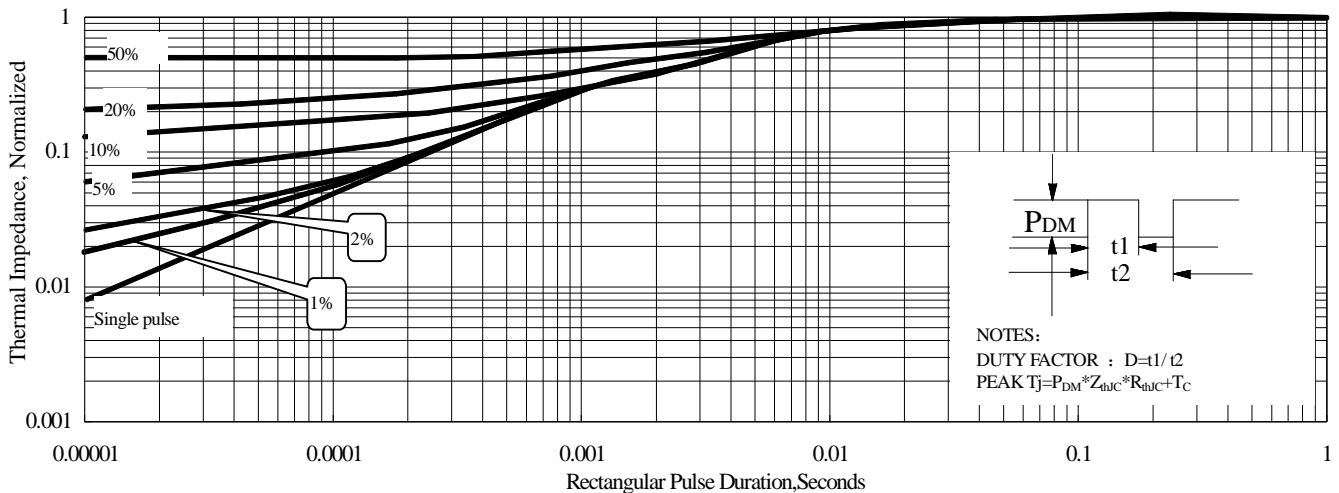


Figure 5 Maximum Effective Thermal Impedance, Junction to Case

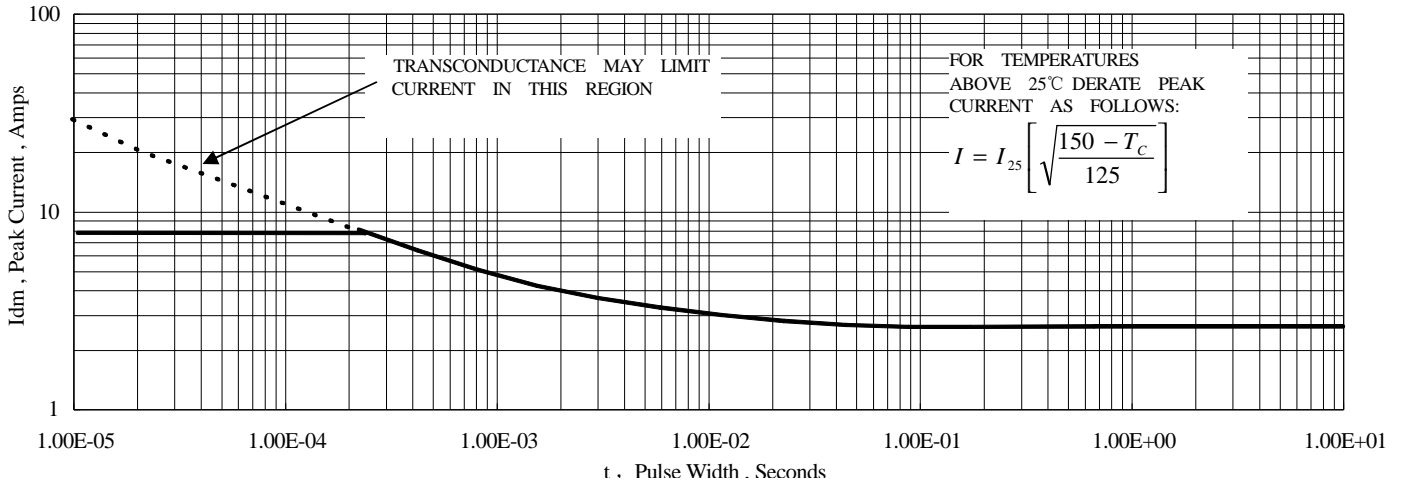


Figure 6 Maximum Peak Current Capability

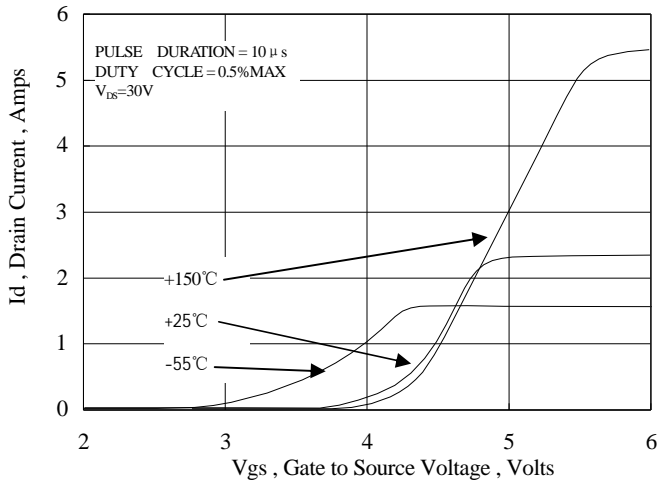


Figure 7 Typical Transfer Characteristics

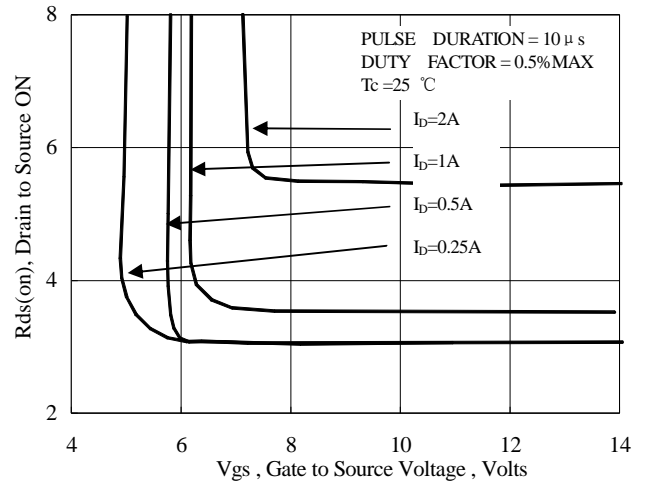


Figure 8 Typical Drain to Source ON Resistance vs Gate Voltage and Drain Current

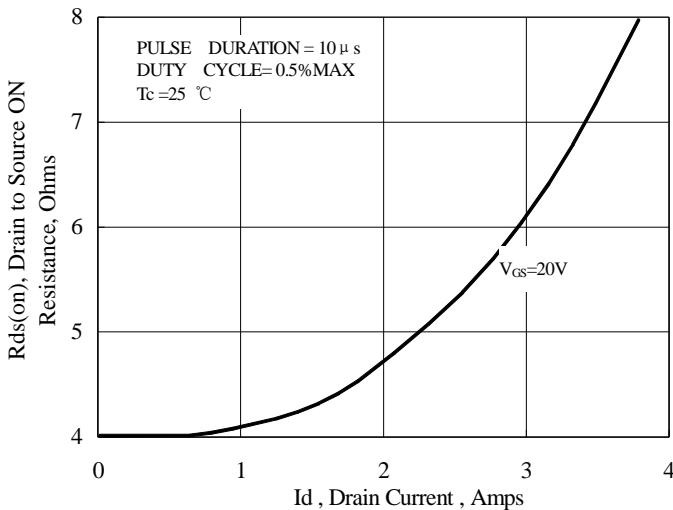


Figure 9 Typical Drain to Source ON Resistance vs Drain Current

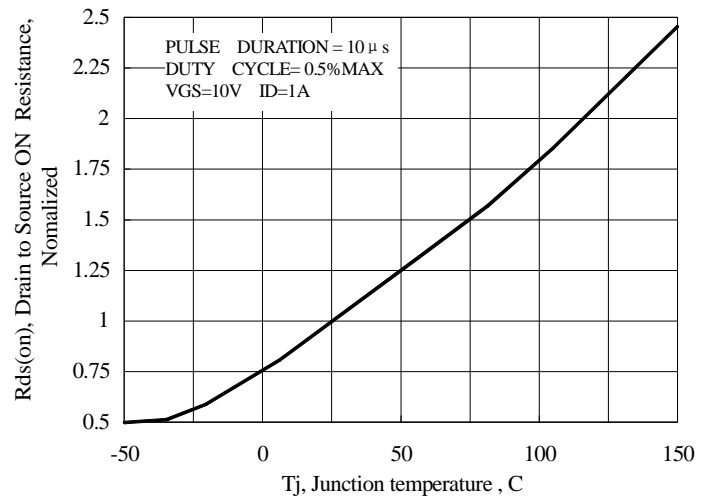


Figure 10 Typical Drain to Source on Resistance vs Junction Temperature



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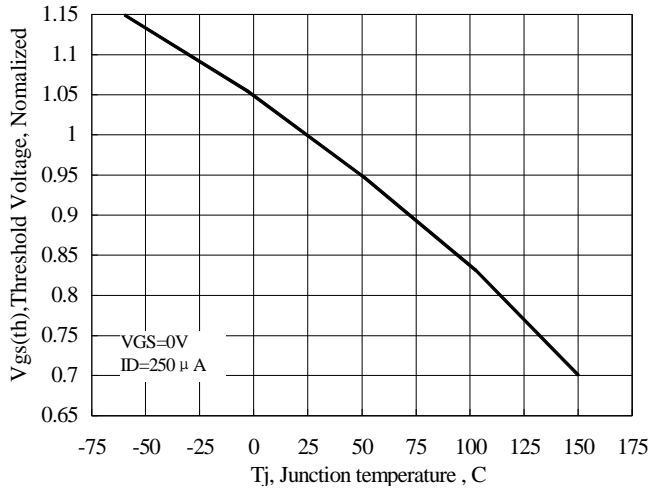


Figure 11 Typical Theshold Voltage vs Junction Temperature

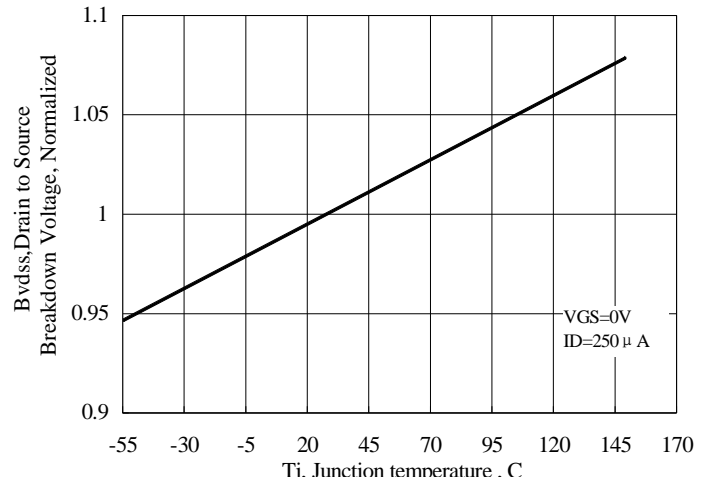


Figure 12 Typical Breakdown Voltage vs Junction Temperature

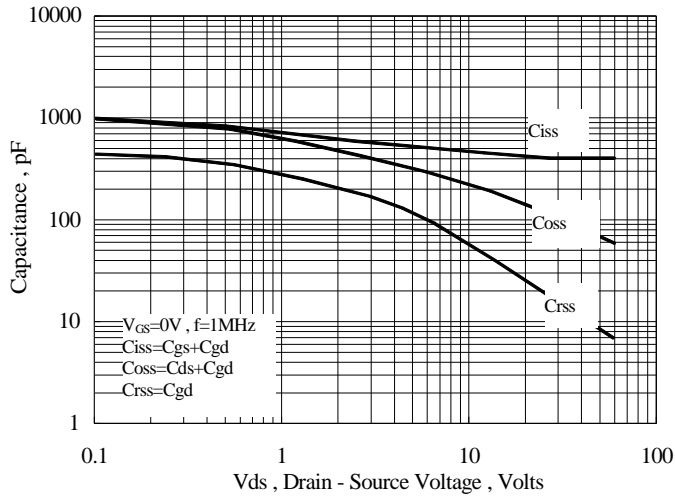


Figure 13 Typical Capacitance vs Drain to Source Voltage

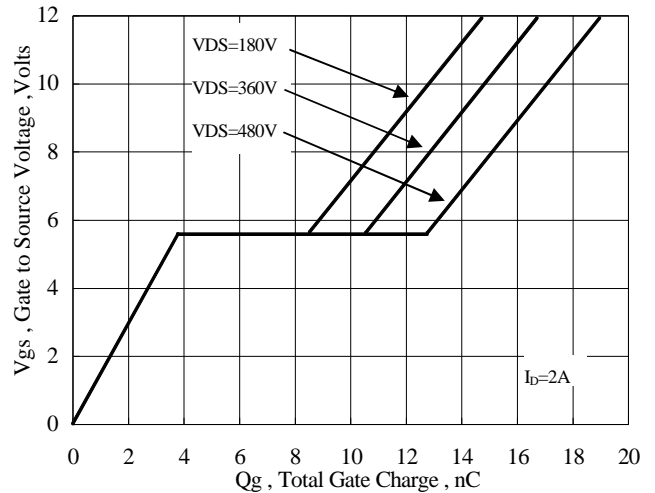


Figure 14 Typical Gate Charge vs Gate to Source Voltage

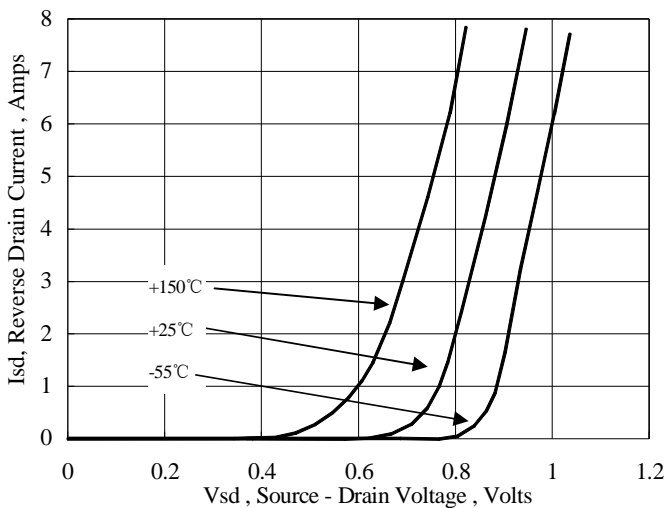


Figure 15 Typical Body Diode Transfer Characteristics

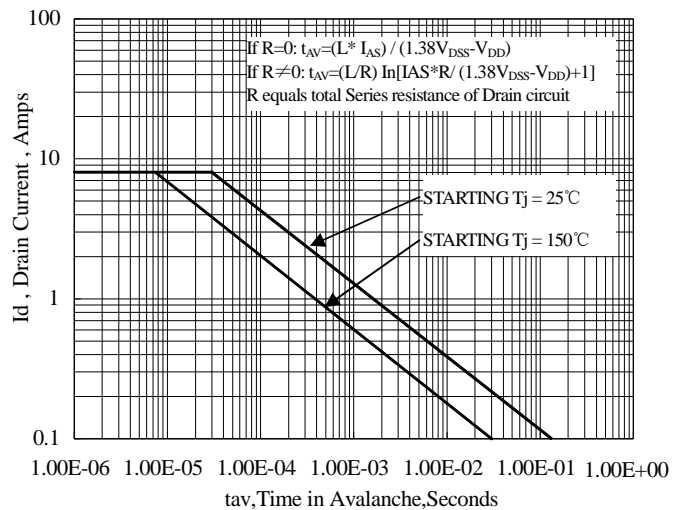


Figure 16 Unclamped Inductive Switching Capability

## Test Circuit and Waveform

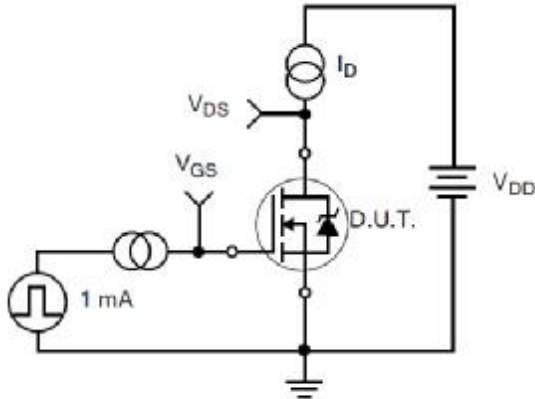


Figure 17. Gate Charge Test Circuit

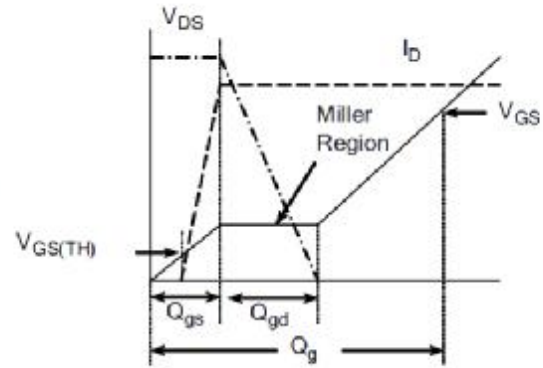


Figure 18. Gate Charge Waveform

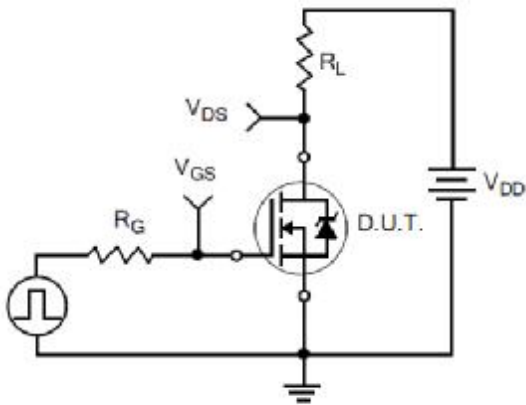


Figure 19. Resistive Switching Test Circuit

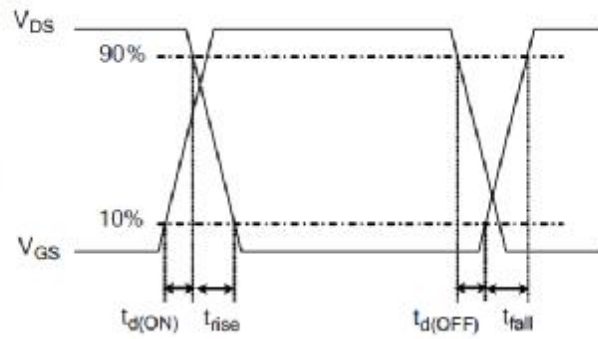


Figure 20. Resistive Switching Waveforms

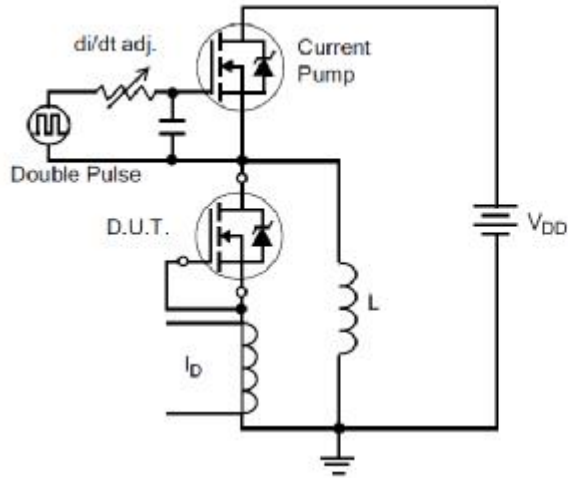


Figure 21. Diode Reverse Recovery Test Circuit

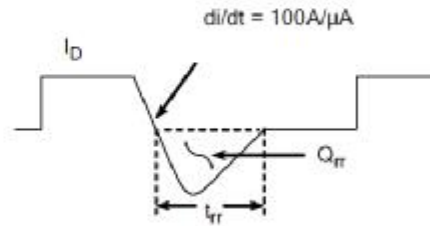


Figure 22. Diode Reverse Recovery Waveform

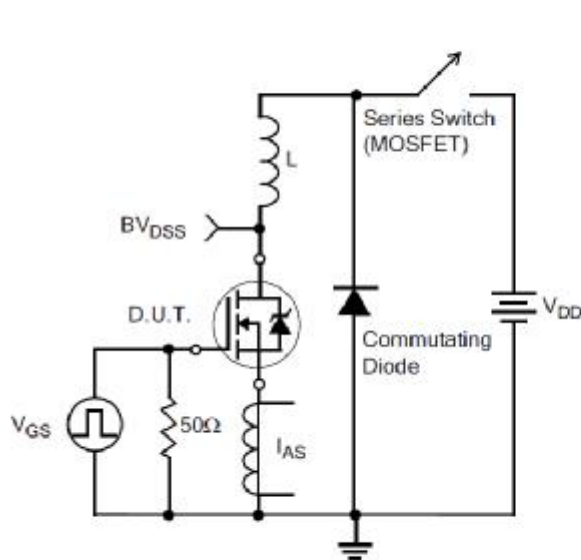


Figure 23. Unclamped Inductive Switching Test Circuit

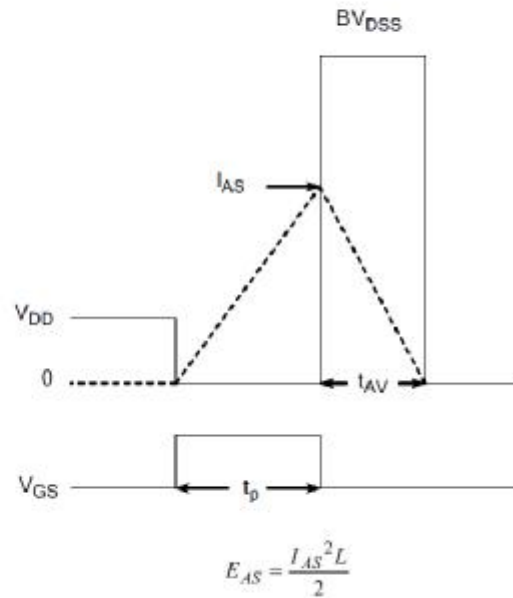
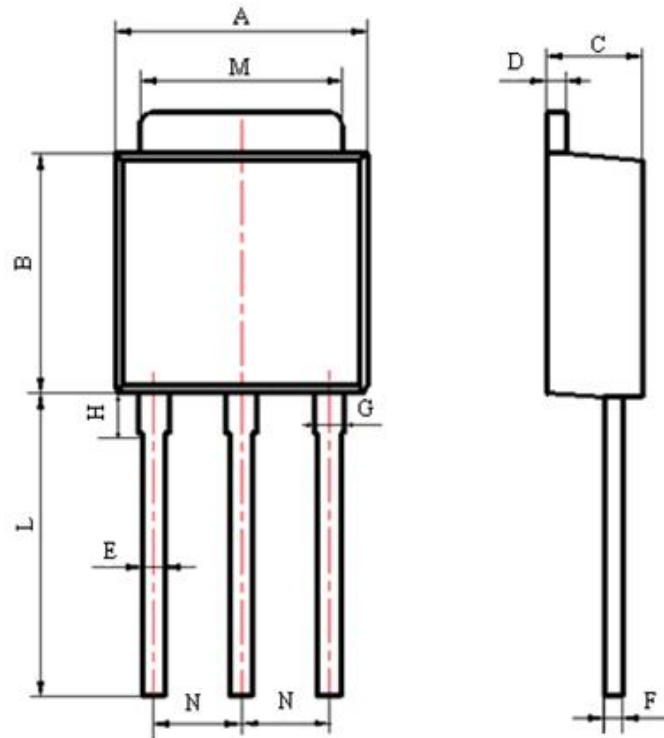


Figure 24. Unclamped Inductive Switching Waveforms



**Package Information:**


Items	Values(mm)	
	MIN	MAX
A	6.30	6.90
B	5.70	6.30
C	2.10	2.50
D	0.30	0.60
E	0.50	0.70
F	0.30	0.60
G	0.70	1.00
H	1.60	2.40
L	7.70	9.80
	6.00	6.30
	4.50	5.80
	2.10	3.70
M	5.10	5.50
N	2.09	2.49

**TO-251 Package**

**The name and content of poisonous and harmful material in products**

Part's Name	Hazardous Substance					
	Pb	Hg	Cd	Cr(VI)	PBB	PBDE
Limit	≤0.1%	≤0.1%	≤0.01%	≤0.1%	≤0.1%	≤0.1%
Lead Frame	○	○	○	○	○	○
Molding Compound	○	○	○	○	○	○
Chip	○	○	○	○	○	○
Wire Bonding	○	○	○	○	○	○
Solder	×	○	○	○	○	○
Note	○: means the hazardous material is under the criterion of SJ/T11363-2006. ×: means the hazardous material exceeds the criterion of SJ/T11363-2006. The plumbum element of solder exist in products presently, but within the allowed range of Eurogroup's RoHS.					

**Warnings**

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. It is suggested to be used under 80 percent of the maximum ratings of the device.
2. When installing the heatsink, please pay attention to the torsional moment and the smoothness of the heatsink.
3. VDMOSFETs is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
4. This publication is made by Huajing Microelectronics and subject to regular change without notice.

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