1. Product Overview

1.1. Functional Features

Type-C and USB PD supports

- Supporting USB PD3.1 and PPS.
- Certified by USBIF, TID：1047
- Configurable RP and RD at CC port.
- Supporting 2 Type-C ports, and allowing independent PD communication.
- The CC port supports 21V voltage resistance.
- Integrated with 2 high-voltage control ports.
- Supporting fast role swap (FRS).

Other protocols

- Supporting QC4.0+, SCP, FCP and AFC protocols.
- Supporting VOOC protocol.
- Supporting BC1.2 and Apple 2.4A.
- Supporting all configuration on DP and DM.
- Supporting multiple quick charge protocol input such as FCP and AFC.

Peripherals

- Max. 27 universal (GPIO) pins
- 3 × 16-bit timers, 8-bit prescaler
- 1 set of UART
- 1 set of SPI
- 1 set of I^2C (supporting master/slave mode)
- 2 analog comparators
- 12 bit Analog-to-digital convertor (ADC)
- 11-bit digital-to-analog convertor (DAC)
- Undervoltage detection (BOD)

32-bit MCU

- An ARM®Cortex™-M0 core, with max. clock rate of 48 MHz
- 60K Flash memory for storing applications (APROM)
- Configurable data Flash (Data Flash)
- 4KB startup code space (LDROM)
- Built-in 8KB SRAM
- System startup section configurable from APROM, LDROM or SRAM

Clock and crystal oscillator

- 24/8 MHz built-in oscillator (HSI) (25°C, 5V, 1% error)
- 10 KHz built-in low power oscillator (LSI)

Operating modes (low power mode, multi-clock low power strategy)

- Normal mode, operating current is 10 mA@5V, 25°C
- Sleep mode, operating current is 2 mA@5V, 25°C
- Deep-Sleep1 mode, operating current is 100 μA@5V, 25°C
- Deep-Sleep2 mode, operating current is 12 μA@5V, 25°C
- Deep Power-Down mode, operating current is 2.5 μA@5V, 25°C

Chip safety

- Providing multilevel confidential policies for Flash memory.
- Providing CRC-32 computing element with polynomial as 0x4C11DB7 (same as Ethernet standard).
- Integrating SRAM to support odd/even parity.
- Operating conditions:
  --Operating temperature: -40°C~85°C
  --Operating voltage: 2.5 V~5.5 V

Package

- QFN24
- QFN32

Application scope

- Adapter
- Power banks
- Car chargers
- HUB
- Display

1.2. Product description

The CS32G020/1 Series are USB Type-C and USB PD controllers suitable for device or power supply applications. The series integrate two-channel independent Type-C CC and USB PD features, Load Switch Driver and USB BC1.2. Moreover, the series support fast charging protocols of multiple cell phone models to strengthen the charging compatibility of end devices. The series are applicable to adapters, power banks, car chargers, HUB and displays. One chip can easily provide a solution with two Type-C ports.

1.3. Model selection table

Table 1 CS32G020/1 series

Model	Flash	SRAM	IO	CC port	PD Module	Dead batteries function	QC PHY	Timer	ADC	DAC	Package
CS32G020K8U6	64K	8K	27	2 groups	2	Support	2 channels	3*16bit	24-channel	11bit	QFN32
CS32G020E8U6	64K	8K	19	2 groups	2	Not supported	2 channels	3*16bit	20-channel	11bit	QFN24
CS32G021K8U6	64K	8K	27	2 groups	2	Support	2 channels	3*16bit	24-channel	11bit	QFN32
CS32G021E8U6	64K	8K	19	2 groups	2	Not supported	2 channels	3*16bit	20-channel	11bit	QFN24

1.4. Block diagram

1.4.1. Block diagram of function modules

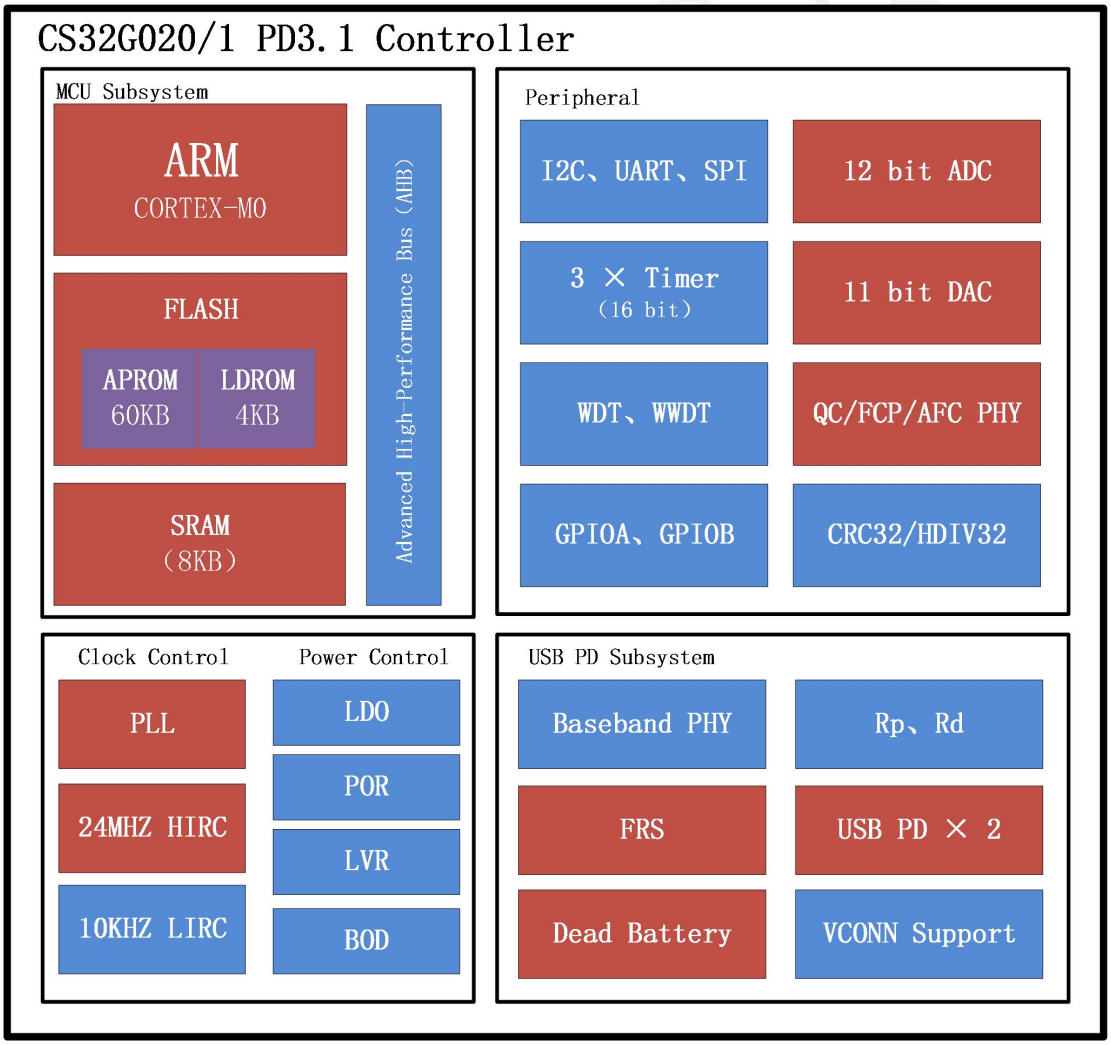


Figure 1 Block diagram of CS32G020/1 system

1.4.2. Block diagram of internal circuit

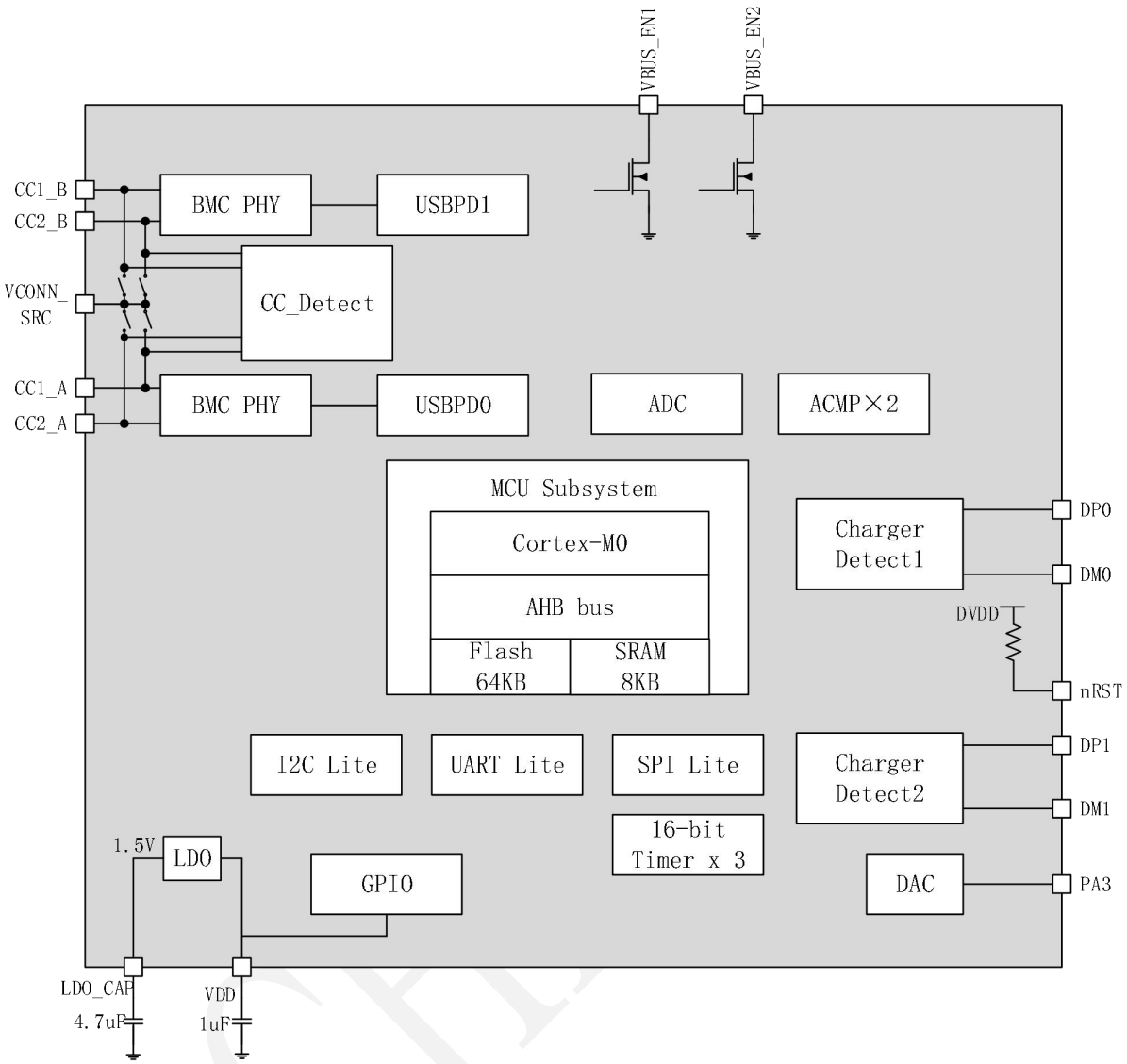


Figure 2 Block diagram of internal circuit

Table of Contents

Version History

History version	Revised contents	Date
V 1.0	Initial version	2018-05-05
V 1.1	1. Add the user configuration zone, P15 - P18 2. Add the description on encrypted zones, P18 - P19	2018-09-03
V 1.2	1. Delete external crystal oscillators	2018-10-24
V 1.3	1. Add Chapter 9: Naming conventions of products 2. Update the descriptions in Chapter 5 3. Update resistance of RDM pull-down resistor in Characteristics of QC3.0	2019-02-13
V 1.4	1. Modify DAC DNL, INL feature, P36 2. Modify errors, P5, P15 3. Modify QFN24 package information, P40 4. Modify Encrypted zone for program mode, P20	2019-04-02
V 1.5	1. Modify QFN24 package information, P40 2. Modify QFN32 package information, P41 3. Add comparator response time, P37 4. Modify typical application, P30	2019-08-08
V 1.6	1. Modify QFN24 package L value, P40	2020-05-15
V 1.7	1. Modify descriptions of pins of VCONN_SRC in chapter 3.3	2021-02-19
V 1.8	1. Update thermal characteristics of package QFN32	2021-09-29
V 1.9	1. Update template and PD3.1	2022-09-07

2. Definitions of pins

2.1. QFN24

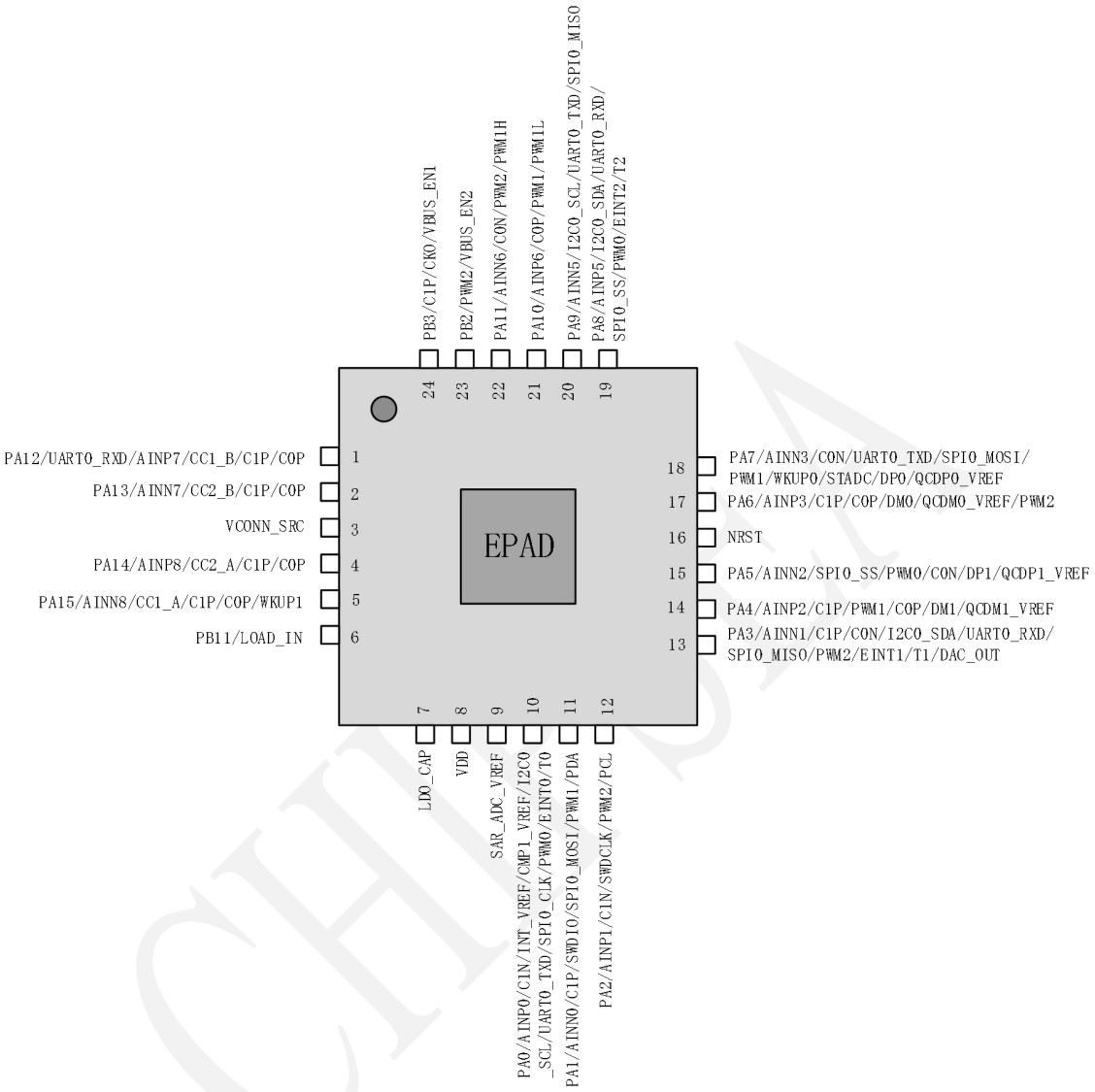


Figure 3 Diagram of pins: QFN24 (Top View)

2.2. QFN32

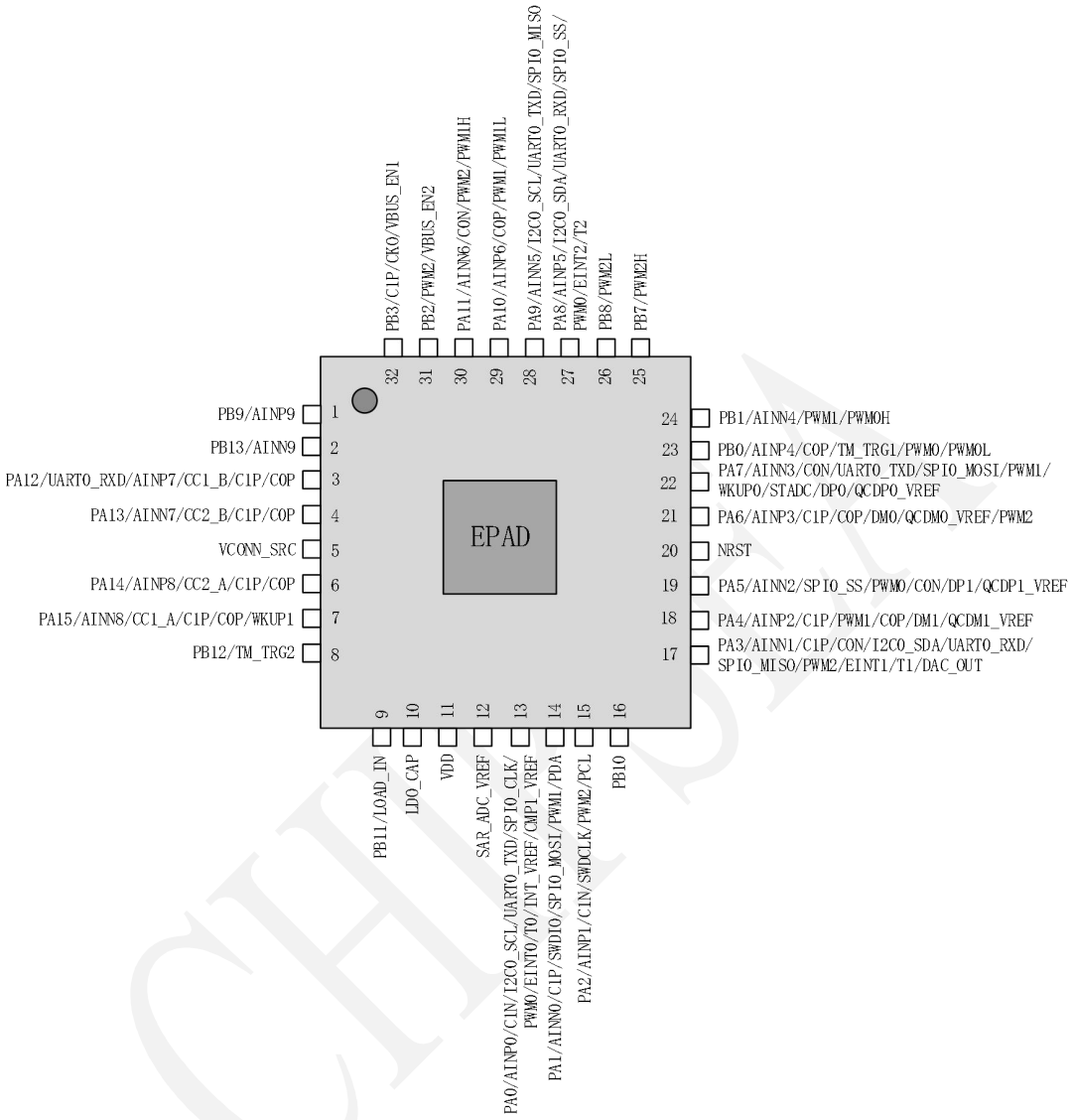


Figure 4 Diagram of pins: QFN32 (Top View)

2.3. Descriptions of pins

Abbreviation of pin types
I: Digital input port
O: Digital output port
I/O: Digital input/output port
AI: Analog input port
AO: Analog output port
P: Power supply

Table 2 Pin description

QFN32 -PIN	QFN24 -PIN	Name of pin	Type	Description
1		PB9	I/O	Universal input/output pin
		AINP9	AI	AINP9 input
2		PB13	I/O	Universal input/output pin
		AINN9	AI	AINN9 input
3	1	PA12	I/O	Universal input/output pin
		UART0_RXD	I	UART0 receipt signal
		AINP7	AI	AINP7 input
		CC1_B	I/O	End of USB PD1 CC1
		C1P	AI	Plus-end input of Comparator 1
		C0P	AI	Plus-end input of Comparator 0
4	2	PA13	I/O	Universal input/output pin
		AINN7	AI	AINN7 input
		CC2_B	I/O	End of USB PD1 CC2
		C1P	AI	Plus-end input of Comparator 1
		C0P	AI	Plus-end input of Comparator 0
5	3	VCONN_SRC	P	VCONN power input end, requiring input voltage of 2.5 V~5.5 V, VCONN voltage cannot be higher than VDD+0.3V
6	4	PA14	I/O	Universal input/output pin
		AINP8	AI	AINP8 input
		CC2_A	I/O	End of USB PD0 CC2
		C1P	AI	Plus-end input of Comparator 1
		C0P	AI	Plus-end input of Comparator 0
7	5	PA15	I/O	Universal input/output pin
		AINN8	AI	AINN8 input
		CC1_A	I/O	End of USB PD0 CC1
		C1P	AI	Plus-end input of Comparator 1
		C0P	AI	Plus-end input of Comparator 0
		WKUP1	I	Waking up pins under power down mode. Effective under high level.
8		PB12	I/O	Universal input/output pin
		TM_TRG2	I	Timer External Trigger Input 2
9	6	PB11	I/O	Universal input/output pin
		LOAD_IN	I	Universal input/ output pins, supporting 800K pull-down resistors
10	7	LDO_CAP	AO	LDO output pin, requiring connection to a 4.7 μF capacitor
11	8	VDD	P	IO power (1.8 V~5.5 V)
12	9	SAR_ADC_VREF	AO	SAR_ADC voltage reference output, requiring connection to a 1 μF capacitor
13	10	PA0	I/O	Universal input/output pin
		AINP0	AI	AINP0 input

		C1N	AI	Minus-end input of Comparator 1
		I2C0_SCL	I/O	I²C0 clock signal
		UART0_TXD	O	UART0 clock signal
		SPI0_CLK	I/O	SPI0 clock signal
		PWM0	O	PWM0 output
		EINT0	I	EINT0 input
		T0	I	Timer 0 input
		INT_VREF	AO	Internal reference voltage output
		CMP1_VREF	AI	Voltage reference output of Comparator 1
14	11	PA1	I/O	Universal input/output pin
		AINN0	AI	AINN0 input
		C1P	AI	Plus-end input of Comparator 1
		SWDIO	I/O	SWD data signals
		SPI0_MOSI	I/O	SPI0 master output/slave input signals
		PWM1	O	PWM1 output
		PDA	I/O	Data port for programming
15	12	PA2	I/O	Universal input/output pin
		AINP1	AI	AINP1 input
		C1N	AI	Minus-end input of Comparator 1
		SWDCLK	I	SWD clock signal
		PWM2	O	PWM2 output
		PCL	I	Clock port for programming
16		PB10	I/O	Universal input/output pin
17	13	PA3	I/O	Universal input/output pin
		AINN1	AI	AINN1 input
		C1P	AI	Plus-end input of Comparator 1
		C0N	AI	Minus-end input of Comparator 0
		I2C0_SDA	I/O	I²C0 data signals
		UART0_RXD	I	UART0 receipt signal
		SPI0_MISO	I/O	SPI0 master input/slave output signals
		PWM2	O	PWM2 output
		EINT1	I	EINT1 input
		T1	I	Timer 1 input
		DAC_OUT	AO	DAC output
18	14	PA4	I/O	Universal input/output pin
		AINP2	AI	AINP2 input
		C1P	AI	Plus-end input of Comparator 1
		C0P	AI	Plus-end input of Comparator 0
		PWM1	O	PWM1 output
		DM1	AI	QC Port Group 1: minus-end input
		QCDM1_VREF	AO	QCDM1_VREF voltage output
19	15	PA5	I/O	Universal input/output pin
		AINN2	AI	AINN2 input
		C0N	AI	Minus-end input of Comparator 0
		SPI0_SS	I/O	SPI0 chip select signals
		PWM0	O	PWM0 output
		DP1	AI	QC Port Group 1: plus-end input
		QCDP1_VREF	AO	QCDP1_VREF voltage output
20	16	NRST	I	Reset pin input, with a 40K pull-up resistor by default
21	17	PA6	I/O	Universal input/output pin
		AINP3	AI	AINP3 input
		C1P	AI	Plus-end input of Comparator 1
		C0P	AI	Plus-end input of Comparator 0
		PWM2	O	PWM2 output

		DM0	AI	QC Port Group 0: minus-end input
		QCDM0_VREF	AO	QCDM0_VREF voltage output
22	18	PA7	I/O	Universal input/output pin
		AINN3	AI	AINN3 input
		UART0_TXD	O	UART0 clock signal
		SPI0_MOSI	I/O	SPI0 master output/slave input signals
		PWM1	O	PWM1 output
		WKUP0	I	Waking up pins under power down mode. Effective under high level.
		STADC	I	ADC Trigger Input Pin
		C0N	AI	Minus-end input of Comparator 0
		DP0	AI	QC Port Group 0: plus-end input
		QCDP0_VREF	AO	QCDP0_VREF voltage output
23		PB0	I/O	Universal input/output pin
		AINP4	AI	AINP4 input
		COP	AI	Plus-end input of Comparator 0
		TM_TRG1	I	Timer External Trigger Input 1
		PWM0	O	PWM0 output
		PWM0L	O	Complementary PWM0L output
24		PB1	I/O	Universal input/output pin
		AINN4	AI	AINN4 input
		PWM1	O	PWM1 output
		PWM0H	O	Complementary PWM0H output
25		PB7	I/O	Universal input/output pin
		PWM2H	O	Complementary PWM2H output
26		PB8	I/O	Universal input/output pin
		PWM2L	O	Complementary PWM2L output
27	19	PA8	I/O	Universal input/output pin
		AINP5	AI	AINP5 input
		I2C0_SDA	I/O	I^2C0 data signals
		UART0_RXD	I	UART0 receipt signal
		SPI0_SS	I/O	SPI0 chip select signals
		PWM0	O	PWM0 output
		EINT2	I	EINT2 input
		T2	I	Timer 2 input
28	20	PA9	I/O	Universal input/output pin
		AINN5	AI	AINN5 input
		I2C0_SCL	I/O	I^2C0 clock signal
		UART0_TXD	O	UART0 clock signal
		SPI0_MISO	I/O	SPI0 master input/slave output signals
29	21	PA10	I/O	Universal input/output pin
		AINP6	AI	AINP6 input
		C0P	AI	Plus-end input of Comparator 0
		PWM1	O	PWM1 output
		PWM1L	O	Complementary PWM1L output
30	22	PA11	I/O	Universal input/output pin
		AINN6	AI	AINN6 input
		C0N	AI	Minus-end input of Comparator 0
		PWM2	O	PWM2 output
		PWM1H	O	Complementary PWM1H output
31	23	PB2	I/O	Universal input/open drain output pin
		PWM2	O	PWM2 output
		VBUS_EN2	O	High voltage control switch, open drain output
32	24	PB3	I/O	Universal input/open drain output pin

		VBUS_EN1	I/O	High voltage control switch, open drain output
		C1P	AI	Plus-end input of Comparator 1
		CKO	O	Frequency divider output
-	-	EPAD	GND	Ground

3. Functional Description

3.1. MCU subsystem

The MCU subsystem features are stated in the following:

- The CS32G020/1 series are 32-bit microprocessors integrated with an ARM® Cortex™-M0 core.
- Applicable to industrial control and occasions requiring high performance and low power consumption.
- The core contains a serial debugging interface (SWD) that can be used for development debugging and application programming.
- Supporting 4 breakpoints and 2 viewpoints.

3.2. Flash

The CS32G020/1 is integrated with 60K on-chip Flash as application memory (APROM). The characteristics of the Flash controller are as follows:

- Zero latency continuation Flash read access of up to 24 MHz
- 60KB application memory space (APROM)
- 4KB BootLoader space (LDROM)
- Configurable data Flash, 512-byte page erase unit
- All built-in Flash page erase unit is 512 bytes
- Supporting in-system programming (ISP)/in-application programming (IAP) to update on-chip Flash EPROM

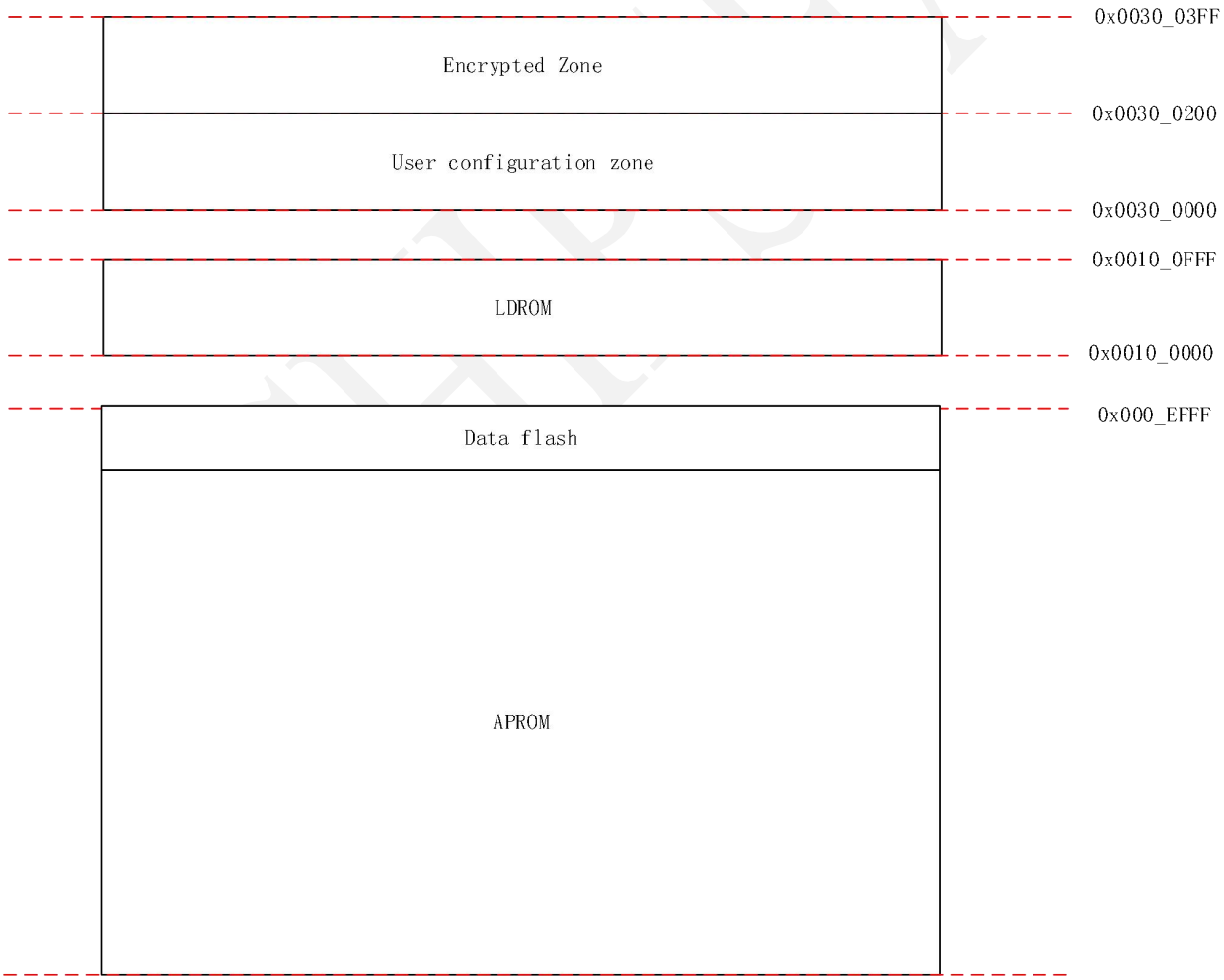


Figure 5 Block diagram of flash memory controller

3.2.1. LDROM

LDROM is used to store BootLoader. The space for BootLoader in CS32G020/1 is 4K bytes. Users can't modify any program in LDROM.

3.3. User configuration zone

User configuration zone is an internally programmable configuration zone. There are a total of 4 addresses for user configuration zone in flash memory, i.e. 0x0030_0000, 0x0030_0004, 0x0030_0008 and 0x0030_000C. Its content is used to configure certain external registers during system startup. The lower half-word is user configuration bits, while the higher one is the negation of the user configuration bits.

Table 3 CONFIG0 (address = 0x0030_0000)

31	30	29	28	27	26	25	24
~CWDTEN	~CLIRC_EN	Reserve		~CDELAY[1:0]		~XT_SEL	~HIRC_SEL
23	22	21	20	19	18	17	16
~CBODEN	~CBOV[2:0]			~CBORST	~CHVRST	Reserve	Reserve
15	14	13	12	11	10	9	8
CWDTEN	CLIRC_EN	Reserve		CDELAY[1:0]		XT_SEL	HIRC_SEL
7	6	5	4	3	2	1	0
CBODEN	CBOV[2:0]			CBORST	CHVRST	Reserve	Reserve

Bits	Description	
31:16	Reserve	Inverse code of the lower 16 bits
15	CWDTEN	**Watchdog enable control** 0 = Enabling watchdog timer when the chip is powered on. 1 = The watchdog is disabled by default when powered on.
14	CLIRC_EN	**LIRC enable control** 0 = Forcing the 10K clock source of LIRC to be constantly enabled and cannot be disabled by software. 1 = The 10K clock source of LIRC is controlled by LIRC_EN (CLKCON[3]).
13:12	Reserve	Reserve
11:10	CDELAY[1:0]	**Selection of reset delay** 00 = 20ms 01 = 40ms 10 = 60ms 11 = 98ms CDELAY[1:0] is the bit for delay selection, and valid when the delay selection bit is opposite to parity bit. For other conditions, the max. delay of 98 ms is always selected.
9	Reserve	Reserve
8	HIRC_SEL	**Frequency selection of built-in high-speed oscillator** 1 = 24MHz 0 = 8MHz
7	CBODEN	**Undervoltage detection enablement** 0 = Enabling undervoltage detection when powered on 1 = Disabling undervoltage detection when powered on Note: Enabling/disabling undervoltage detection will enable/disable 6.5 V high voltage detection simultaneously.
6:4	CBOV[2:0]	**Selection of undervoltage value** 000 = 1.8V 001 = 2.0V 010 = 2.4V 011 = 2.7V

		100 = 3.0V 101 = 3.6V 110 = 4.0V 111 = 4.0V
3	CBORST	**Enablement of undervoltage reset** 0 = Enabling undervoltage reset when powered on 1 = Disabling undervoltage reset when powered on
2	CHVRST	**Enablement of 6.5 V high voltage reset** 0 = Enabling 6.5 V high voltage reset when powered on 1 = Disabling 6.5 V high voltage reset when powered on
1:0	Reserve	Reserve

Table 4 CONFIG1 (address = 0x0030_0004)

31	30	29	28	27	26	25	24
~CWDTSEN	Reserve	~CWDTSIS[2:0]			~FRD_CFG[2:0]		
23	22	21	20	19	18	17	16
~CBS[1:0]		Reserve					~DFEN
15	14	13	12	11	10	9	8
CWDTSEN	Reserve	CWDTSIS[2:0]			FRD_CFG[2:0]		
7	6	5	4	3	2	1	0
CBS[1:0]		Reserve					DFEN

Bits	Description	
31:16	Reserve	Inverse code of the lower 16 bits
15	CWDTSEN	**Simplified watchdog enable control** 0 = Enabling watchdog timer when the chip is powered on. 1 = The watchdog is disabled by default when powered on.
14	Reserve	Reserve
13:11	CWDTSIS[2:0]	**Selecting timeout interval of simplified watchdog timer.** Reset delay CDELAY[1:0]=00 or 01 000 = 2^{13} *T_{LIRC} 001 = 2^{14} * T_{LIRC} 010 = 2^{15} * T_{LIRC} 011 = 2^{16} * T_{LIRC} 100 = 2^{12} * T_{LIRC} 101 = 2^{11} * T_{LIRC} 110 = 2^{10} * T_{LIRC} 111 = 2^{9} * T_{LIRC} Reset delay CDELAY[1:0]=10 or 11 000 = 2^{13} *T_{LIRC} 001 = 2^{14} * T_{LIRC} 010 = 2^{15} * T_{LIRC} 011 = 2^{16} * T_{LIRC} 100 = 2^{13} *T_{LIRC} 101 = 2^{14} * T_{LIRC} 110 = 2^{15} * T_{LIRC} 111 = 2^{16} * T_{LIRC}
10:8	FRD_CFG[2:0]	Instruction fetch of flash under normal operation These 3 bits must be configured as 000.
7:6	CBS[1:0]	**Selection of chip startup** CBS[1] = 1 : The chip starts from APROM. CBS[1] = 0 : LDROM startup

		CBS[0]	Note
		1	IAP not available
		0	Enabling IAP
5:1	Reserve	Reserve	
0	DFEN	**Data flash enablement** 0 = Enabling data flash 1 = Enabling data flash	

Table 5 CONFIG2 (address = 0x0030_0008)

31	30	29	28	27	26	25	24
~DFBADR[15:8]							
23	22	21	20	19	18	17	16
~DFBADR[7:0]							
15	14	13	12	11	10	9	8
DFBADR[15:8]							
7	6	5	4	3	2	1	0
DFBADR[7:0]							

Bits	Description	
31:16	~DFBADR[15:0]	Inverse code of the lower 16 bits
15:0	DFBADR[15:0]	**Data Flash base address** The data flash base address is subject to the definition of users. Since the erase unit of on-chip flash occupies 512 bytes, bit 8-0 is maintained 0 mandatorily. The min. of DFBA [15:0] is 200h. Where the value is lower than 200h, it is equivalent to 200h, i.e. the space of APROM is 0.5KB at minimum.

Table 6 CONFIG3 (address = 0x0030_000C)

31	30	29	28	27	26	25	24
~SWD_EN[7:0]							
23	22	21	20	19	18	17	16
Reserve							
15	14	13	12	11	10	9	8
SWD_EN[7:0]							
7	6	5	4	3	2	1	0
Reserve							

Bits	Description	
31:24	~SWD_EN[7:0]	Negating SWD_EN [7:0]
23:16	Reserve	Has to be 0xFF.
15:8	SWD_EN[7:0]	SWD debugging enablement bit 0x55: Disabling SWD debugging Others: Enabling SWD debugging
7:0	Reserve	Has to be 0x00.

3.4. Encrypted zone

Table 7 Encrypted zone

S/N	Address	Note
1	0x0030_0200	Read enable configuration for the first 32 KB of Flash under User Mode Bit 31~16: negation of the lower 16 bits, used for verification. It is assumed encrypted in case of verification failure. Bit15: 1 represents Read Enable of 2KB (0x0000_7800~0x0000_7FFF). 0 represents Read Disable of 2KB (0x0000_7800~0x0000_7FFF). … bit 1: 1 represents Read Enable of 2KB (0x0000_0800~0x0000_0FFF). 0 represents Read Disable of 2KB (0x0000_0800~0x0000_0FFF). bit 0: 1 represents Read Enable of 2KB (0x0000_0000~0x0000_07FF). 0 represents Read Disable of 2KB (0x0000_0000~0x0000_07FF).
2	0x0030_0204	Read enable configuration for the last 32 KB of Flash under User Mode Bit 31~16: negation of the lower 16 bits, used for verification. It is assumed encrypted in case of verification failure. Bit15: 1 represents Read Enable of 2KB (0x0000_F800~0x0000_FFFF). 0 represents Read Disable of 2KB (0x0000_F800~0x0000_FFFF). … bit 1: 1 represents Read Enable of 2KB (0x0000_8800~0x0000_8FFF). 0 represents Read Disable of 2KB (0x0000_8800~0x0000_8FFF). bit 0: 1 represents Read Enable of 2KB (0x0000_8000~0x0000_87FF). 0 represents Read Disable of 2KB (0x0000_8000~0x0000_87FF).
3	0x0030_0208	Write enable configuration for the first 32 KB of Flash under User Mode Bit 31~16: negation of the lower 16 bits, used for verification. It is assumed encrypted in case of verification failure. Bit15: 1 represents Write Enable of 2KB (0x0000_7800~0x0000_7FFF). 0 represents Write Disable of 2KB (0x0000_7800~0x0000_7FFF). … bit 1: 1 represents Write Enable of 2KB (0x0000_0800~0x0000_0FFF). 0 represents Write Disable of 2KB (0x0000_0800~0x0000_0FFF). bit 0: 1 represents Write Enable of 2KB (0x0000_0000~0x0000_07FF). 0 represents Write Disable of 2KB (0x0000_0000~0x0000_07FF).
4	0x0030_020C	Write enable configuration for the last 32 KB of Flash under User Mode Bit 31~16: negation of the lower 16 bits, used for verification. It is assumed encrypted in case of verification failure. Bit15: 1 represents Write Enable of 2KB (0x0000_F800~0x0000_FFFF). 0 represents Write Disable of 2KB (0x0000_F800~0x0000_FFFF). … bit 1: 1 represents Write Enable of 2KB (0x0000_8800~0x0000_8FFF). 0 represents Write Disable of 2KB (0x0000_8800~0x0000_8FFF). bit 0: 1 represents Write Enable of 2KB (0x0000_8000~0x0000_87FF). 0 represents Write Disable of 2KB (0x0000_8000~0x0000_87FF).
5	0x0030_0210	Erase enable configuration for the first 32 KB of Flash under User Mode Bit 31~16: negation of the lower 16 bits, used for verification. It is assumed encrypted in case of verification failure. bit 15: 1 represents Erase Enable of 2KB (0x0000_7800~0x0000_7FFF). 0 represents Erase Disable of 2KB (0x0000_7800~0x0000_7FFF). … bit 1: 1 represents Erase Enable of 2KB (0x0000_0800~0x0000_0FFF). 0 represents Erase Disable of 2KB (0x0000_0800~0x0000_0FFF). bit 0: 1 represents Erase Enable of 2KB (0x0000_0000~0x0000_07FF). 0 represents Erase Disable of 2KB (0x0000_0000~0x0000_07FF).
6	0x0030_0214	Erase enable configuration for the last 32 KB of Flash under User Mode

S/N	Address	Note
		Bit 31~16: negation of the lower 16 bits, used for verification. It is assumed encrypted in case of verification failure. bit 15: 1 represents Erase Enable of 2KB (0x0000_7800~0x0000_7FFF). 0 represents Erase Disable of 2KB (0x0000_7800~0x0000_7FFF). … bit 1: 1 represents Erase Enable of 2KB (0x0000_8800~0x0000_8FFF). 0 represents Erase Disable of 2KB (0x0000_8800~0x0000_8FFF). bit 0: 1 represents Erase Enable of 2KB (0x0000_8000~0x0000_87FF). 0 represents Erase Disable of 2KB (0x0000_8000~0x0000_87FF).
7	0x0030_0214~ 0x0030_021C	Reserve
8	0x0030_0220	Read enable configuration for the 64 KB of Flash under Program Mode Bit 31: 1 represents Read Enable of 2KB(0x0000_F800~0x0000_FFFF). 0 represents Read Disable of 2KB(0x0000_F800~0x0000_FFFF). Bit30: 1 represents Read Enable of 2KB (0x0000_F000~0x0000_F7FF). 0 represents Read Disable of 2KB (0x0000_F000~0x0000_F7FF). … bit 1: 1 represents Read Enable of 2KB (0x0000_0800~0x0000_0FFF). 0 represents Read Disable of 2KB (0x0000_0800~0x0000_0FFF). bit 0: 1 represents Read Enable of 2KB (0x0000_0000~0x0000_07FF). 0 represents Read Disable of 2KB (0x0000_0000~0x0000_07FF).

3.5. USB PD

3.5.1. Type-C port

The CS32G020/1 supports 2 groups of Type-C ports, whose characteristics are as follows:

- Each group of CC ports is configured with an independent, configurable 5.1 K pull-down resistor and an 80/180/330 μA current source.
- Supporting detection of dead batteries.
- Automatic detection of device connection at CC port, and the users have direct access to the detection results.
- Supporting FRS detection.
- Supporting automatic wakeup upon device access under low power mode.

The USB PD module supports USB PD3.1 protocol, and the 2 groups of CC ports may perform independent communication without interference to the other.

3.5.2. USB PD physical layer

The USB PD physical layer contains a transmitter and a receiver, performing communication with BMC-coded data through CC ports on the basis of PD3.1 protocol. All communication is half-duplex. The physical layer, or the PHY layer, is integrated with a conflict avoidance mechanism to minimize communication errors on the channel. The USB-PD module comprises of the R_P and R_D that are used for connection detection, port initialization and USB DFP/UFP identification. The resistor R_P is realized with a pull-up current source.

In accordance with the USB Type-C protocol specifications, a fixed resistor must be connected to the CC port based on its power role when a Type-C controller is not powered on. When a power bank is used as Sink, the R_D must be connected to the CC port; but if it is used as an power adapter, both CC ports must be suspended. To accommodate such application, the CC port may be configured with the dead battery resistor R_D when the CS32G020/1 is not powered on. CC ports of QFN32 package will be provided with the function of dead battery detection, while the ones of QFN24 package won't.

3.6. VBUS PFE control port

The CS32G020/1 is integrated with 2 PFET control output ports to drive the VBUS control switch, i.e. Port VBUS_EN1 (PB3) and VBUS_EN2 (PB2). These two ports are of open drain output, and support low level output or high resistance input only. Where high output is required, an external pull-up resistor shall be connected.

3.7. ADC

The CS32G020/1 contains a 12-bit SAR analog-digital converter with 20+4 channels (SAR A/D Converter). Main characteristics are as shown below:

- Analog input voltage range: 0 - VDD
- 12-bit resolution
- 10 pairs of differential input channels at maximum.
- 20+4 ways of single-ended analog input channels at maximum.
- SPS sampling rate of up to 200 KHz.
- 5 operation modes.
  - Single Conversion Mode: A/D conversion is carried out once on the specified channel.
  - Burst Mode: A/D conversion is carried out continuously on a specified single channel, and the results are stored in the data register sequentially.
  - Single-Cycle Scanning Mode: A/D conversion is carried out once on all specified channels (from low serial number to high).
  - Limited-Cycle Scanning Mode: The next channel will be toggled to when one has performed the specified number of conversion. Computation configuration of discarding the previous conversion result of the specified times and discarding the maximum and minimum are supported.
  - Continuous Sweeping Mode: The A/D conversion is carried out continuously under single-cycle scanning mode until such conversion is ceased by the software.
- Conversion results of each channel are stored in the corresponding data register with validity and overflow flags.

The SAR_ADC VREF port is of internal voltage reference output, which requires the connection of an external 1 μF capacitor. The CS32G020/1 supports 10 pairs of differential input channels at maximum, and may be configured as single-ended mode as well.

3.8. DAC

The CS32G020/1 has a built-in 11-bit voltage-output digital-to-analog converter, whose max conversion speed is 200KHz SPS and voltage reference optional among internal voltage references of 2 V, 3 V and 4 V.

3.9. Analog comparator

The CS32G020/1 may be provided with up to 2 comparators for use under various configuration. When the plus-end input is greater than the minus-end one, the comparator will output logic “1”, otherwise “0”. Where the output value of comparators varies, each comparator may be configured to interrupt. The primary characteristics of analog comparators are:

- Analog input voltage range: 0~V_{DD}
- Supporting hysteresis function.
- Supporting 8-gear output filter.
- Supporting output inversion.
- The internal voltage reference may be input for the plus/minus end of each analog comparator.
- Supporting calibration of offset voltage.
- Each comparator supports one interrupt vector.

3.10. GPIO

The CS32G020/1 has up to 27 universal I/O pins that are shared with other functions. The 27 pins are divided into to 2 ports named PA and PB, each of which has 16 pins at maximum. Each pin is independent and provided with corresponding register for operating mode and data control.

The I/O model of each pin may be individually configured as input, output and open drain by software. Main characteristics are as shown below:

- 3 I/O modes:
  - Input mode with high resistance
  - Push-pull output
  - open-drain output
- The Schmitt Trigger Input mode is enabled or disabled by Px_TYPEn[15:0].
- Each I/O pin may act as the interrupt source and edge/level trigger is supported.
- When the interrupt function is enabled for a pin, its wakeup function is enabled as well.

- Each I/O may be configured as pull-up or -down.

3.11. Communication interface

The CS32G020/1 supports 3 universal communication interfaces, i.e. I²C, SPI and UART.

3.11.1.I²C

The I²C is a 2-line bidirectional serial bus, allowing simple, effective data communication between equipment. A standard I²C is a multiple-mainframe bus, incorporating conflict detection and arbitration mechanism to prevent data collision arising out of simultaneous control on the bus by two or more mainframes.

The I²C bus transmits data between equipment connected to it through two lines (SDA and SCL). Its main characteristics include:

- Supporting master and slave modes.
- Bidirectional data transmission between master and slave.
- Multiple-mainframe bus (without central mainframe).
- The serial data on the bus is free from damage when multiple mainframes are transmitting data arbitration at the same time.
- Supporting 7-bit addressing mode.
- Supporting fast and standard modes.
- The clock is programmable and applicable to control of varying speeds.
- Independent transmission and receipt cache, 8 levels for each.

3.11.2.SPI

The CS32G020/1 supports 1 simplified SPI interface, including the master and slave modes.

The SPI interface allows full-duplex, synchronized and serial communication between MCU and other SPI interfaces. It has two modes: the master mode and the slave mode. Generally, the SPI employs 4-line communication, i.e. the 4 signal lines of SPICLK, MOSI, MISO and SPISS. And 3-line communication, i.e. the 3 signal lines of SPICLK, MOSI and MISO only, is used to save an interface under certain circumstances. When two SPI devices communicate, one will be the master and the other, the slave. All communication between SPI interfaces is initiated by the master. The master controls data exchange by transmitting clock (SPICLK) and slave selection signals (SPISS). The mater and the slave may transmit and receive data simultaneously.

3.11.3.UART

The CS32G020/1 mainly offers 1 programmable full-duplex serial communication interface that allows to transmit and receive data at the same time. The primary characteristics of UART are:

- 1 set of UART.
- Supporting simultaneous transmission and receipt of data.
- Configurable baud rate.
- Supporting automatic baud rate.
- Both the receipt and transmission contains 8 levels of FIFO, RX_FIFO (8*9Bit) and TX_FIFO (8*9Bit).
- Receives interrupts, supports non-blank interrupts, and receives flow line interrupts.
- Transmits interrupts, supports transmission of non-blank interrupts, and transmits flow line interrupts.
- Supporting 8/9-bit data transmission and receipt.

3.12. Timer

The timer controller comprises of 3 groups of 16-bit timers from TIMER0 to TIMER2, allowing users to realize real-time control applications. The timer module supports functions such as time counting, external hardware trigger, clock generation, PWM output and complementary PWM output, etc.

The primary characteristics of the timers are described below:

- 3 groups of 16-bit timers, with 16-bit up counter and one 4-bit prescale counter.
- Supporting counting.
- Supporting PWM.
- Supporting complementary PWM with an adjustable dead zone.
- Supporting clock counting of up to 96MHz.

3.13. Watch dog timer

A watchdog timer resets the system when the software runs to an unknown state, prevents the system from hanging forever, and wakes up the CPU from Idle/Sleep Mode. The CS32G020/1 is integrated with 3 watchdogs, i.e. the watchdog timer (WDT), window watchdog timer (WWDT), and watchdog timer lite (WDT Lite).

3.13.1.WDT

Enablement of WDT module is subject to the control of code options only. Once enabled, software can't close the watch dog timer, but it can clear the counter. The WDT has the following main characteristics:

- A 18-bit free-running counter for timeout interval of the watchdog.
- The ($2^4 \sim 2^{18}$) WDT_CLK cycle may be used as the timeout interval, making it range from 104 ms - 26.3168 s (if WDT_CLK = 10 KHz).
- Supporting delay reset by the watchdog, for which the time may be 3/18/130/1026 * WDT_CLK.
- Where the bit CWDTEN (CONFIG[31], bit of watchdog enablement) is 0, enablement of watchdog upon powering on is supported.
- Where the clock source of the watchdog is defined as 10 kHz, the function of watchdog timeout wakeup is supported.
- Where a 32.768 kHz external low-speed crystal oscillator is selected as the watchdog clock source, the function of watchdog timeout wakeup is supported.

3.13.2.WWDT

The WWDT resets the system in a specified window cycle to prevent the software from entering an uncontrollable state permanently. Main characteristics are as shown below

- The 6-bit down counter current value (WWDTCVAL) and the 6-bit comparison window value (WINCMP) allows flexibility of the WWDT in timeout window cycle.
- Supporting 4-bit values, and up to 11-bit prescale counter cycle for programmable WWDT counter.

3.13.3.WDT Lite

This kind of WDT is mainly used for wakeup of Powerdown Mode, and is invalid under other modes. Main characteristics are as shown below

- Operating under 5 V power domain, and remaining operational under the power down mode.
- With the clock source of LIRC 10 KHz.
- Supporting CPU wakeup under power down mode only.

3.14. Arithmetic unit

The hardware of CS32G020/1 supports 3 common kinds of arithmetic, i.e. single-cycle multiplier, hardware divider and CRC32 computing element.

3.14.1.Single-cycle multiplier

This is a 32-bit single-cycle multiplier that allows direct 32-bit data multiplication without any register, making it quite convenient for use.

3.14.2.Hardware divider

The hardware divider (HDIV) helps increase the efficiency of applications. This is a signed integer divider that outputs quotients and remainders. The primary characteristics of the divider are described below:

- Signed (2's complement) integer calculation.
- Computing power for 32-bit dividends and 16-bit divisors.
- Output of 32-bit quotients and 32-bit remainders (16-bit remainders are extended to 32 bits with signs).
- Warning marks for 0 division.
- Each computation requires 16 HCLK clock cycles.
- Computation of write divisor trigger.
- Awaiting completing computation automatically when reading quotients and remainders.

3.14.3.CRC32 computing element

The CRC computing element may be used for fast computation of result codes of cyclic redundancy check (CRC) based on the data input, in accordance with the defined polynomial algorithm. The CRC technology is generally used to check the intactness of data transmission or storage in many applications. This provides a technical mean to check the storage reliability of Flash within the scope of functional safety standard. The CRC computing element may compute software signatures at any time, which allows completing signature comparison during communication and storage.

Main characteristics of CRC32 computing element:

- The employed CRC-32 (same as Ethernet standard) polynomial 0x4C11DB7
  $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$.
- Operating 8, 16 and 32-bit data.
- The CRC initial value may be preset.
- Single input/output 32-bit data register.
- Configured with input cache, protecting real-time computation from any effect by a bus pause.
- Each CRC computation is completed within 4 AHB clock cycles (HCLK).
- Configured with an 8-bit register for general purposes (usable for temporary storage).
- Used to provide reversibility options for I/O data.

3.15. Power management

The CS32G020/1 provides 5 operating modes to fulfill the requirements on clocks and power consumption by different applications, including Normal Operation Mode, Sleep Mode, Deep-Sleep Mode 1, Deep-Sleep Mode 2 and Power-Down Mode. See the table below for entering and wakeup methods of the abovementioned modes.

Table 8 Ways of entering and waking up operating modes

Mode	Enter	Wakeup	Effects on clocks	Effects on voltage	Wakeup delay
Sleep mode (sleep)	(LPMODE=000)+WFI	Any interruption	The CPU clock is closed. No effect on other clocks and simulation clocks.	None (primary and secondary LDO for digital circuit power supply are on.)	Inherent delay of M0 core
	(LPMODE=000)+WFE	Wakeup time			Inherent delay of M0 core
Deep-Sleep Mode 1 (deepsleep1)	(LPMODE = 001) + WFI or WFE	Any external interruption, supporting interruptions of LSE or LSI (WDT/WWDT), BOD and comparators.	HSE and HSI are off.	Primary and secondary LDO for digital circuit power supply are on.	HSE or HSI oscillation start-up stabilization delay + inherent delay of M0 core.
Deep-Sleep Mode 2 (deepsleep2)	(LPMODE = 011) + WFI or WFE			Primary and secondary LDO for digital circuit power supply are off and on respectively.	Primary LDO start-up delay + LDO toggle + HSE or HSI oscillation start-up stabilization delay + inherent delay of M0 core.
Power failure mode	(LPMODE = 1 × 1) + WFI or WFE	Wakeup pin, NRST reset,	HSE, HSI, LSE and LSI	Primary and secondary	Reset delay

Mode	Enter	Wakeup	Effects on clocks	Effects on voltage	Wakeup delay
(Powerdown)		POR reset.	are off.	LDO for digital circuit power supply are off.	

3.15.1.Normal Operation Mode

In Normal Operation Mode, the ARM®Cortex™-M0 core runs commands in a normal method. Different peripheral clocks may be configured separately, or disabled or enabled individually. Each analog module may be disabled or enabled through the enablement bit. The Normal Operation Mode consumes great power.

3.15.2.Sleep mode

In Sleep Mode, the clock of ARM Cortex- M0 core and execution of commands cease, while the clock oscillators remain working. Any interruption wakes up the Sleep Mode and resumes command execution by the core.

In Sleep Mode, the values of processor state register, external register and internal register remain the same, the logic level of pins static, and RESET valid.

Peripheral functions are free from any interference. Any enabled module will continue to work under the Sleep Mode.

The state of analog module is determined by the module enablement bit.

3.15.3.Deep-Sleep 1 Mode

In Deep-Sleep 1 Mode, the system clock of ARM Cortex- M0 core and execution of commands cease. The internal high-speed oscillator HSI stops as well, while the LSI remains working if enabled. The Deep-Sleep 1 Mode may be woken up through external interruptions or WDT interruption or reset.

In the Deep-Sleep Mode, the values of processor state register, external register and internal register remain the same, the logic level of pins static, and RESET valid.

Since the clock and peripherals stop, it is recommended to shut down analog modules such as SAR_ADC, comparators and operational amplifiers, reducing and power consumption under the Deep-Sleep Mode.

In the Deep-Sleep Mode, FLASH is under power-down state to reduce the static leakage power consumption, and requires a long time to resume operation when woken up.

3.15.4.Deep-Sleep 2 Mode

In Deep-Sleep 2 Mode, the system clock of ARM Cortex- M0 core and execution of commands cease. The internal high-speed oscillator HSI stops as well, while the LSI remains working if enabled. The Deep-Sleep 2 Mode may be woken up through external interruptions or WDT interruption or reset.

The Deep-Sleep 2 Mode has lower power consumption than Deep-Sleep 1, but requires longer wakeup time.

In the Deep-Sleep Mode, the values of processor state register, external register and internal register remain the same, the logic level of pins static, and RESET valid.

Since the clock and peripherals stop, it is recommended to shut down analog modules such as SAR_ADC, comparators and operational amplifiers, reducing and power consumption under the Deep-Sleep Mode.

In the Deep-Sleep Mode, FLASH is under power-down state to reduce the static leakage power consumption, and requires a long time to resume operation when woken up.

3.15.5.Deep Power-Down Mode

In the Deep Power-Down Mode, the power of the entire chip (with built-in LDO shut down) and the clock are off except for pins WKUP0 and WKUP1, which may wake up the chip from the Deep Power-Down Mode when inputting a rising edge. When WKUP0 and WKUP1 are enabled, they will turn on a pull-down resistor mandatorily and, in case of detecting the rising edge input, reset the chip.

In the Deep Power-Down Mode, the values of processor state register, external register and internal register will no longer remain the same, nor will the validity of the RESET pin.

Where the chip is woken up from the Deep Power-Down Mode, the built-in LDO is turned on, and the chip resumes working.

4. Application programming

The CS32G020/1 supports three ways of updating applications:

1. Programming applications through the serial programming interface.
2. Updating applications by firmware upgrade at Type-C port.
3. Programming through the SWD interface, which is used for debugging only.

Generally, the CS32G020/1 performs programming through the serial programming interface. When a product is completed and requires application update, such purpose may be fulfilled through the serial programming interface or by BootLoader calling a Type-C port.

4.1. Flash programming through serial programming interface

In case of mass production, CHIPSEA will supply a special tool for programming.

The programming files are in the format of hex, produced by the compiler, and may be downloaded and written into the FLASH to complete programming.

The connection for programming through serial interface is shown below. The chip is powered by the source for programming hardware, and match the programming clock, data port and NRST port with each other.

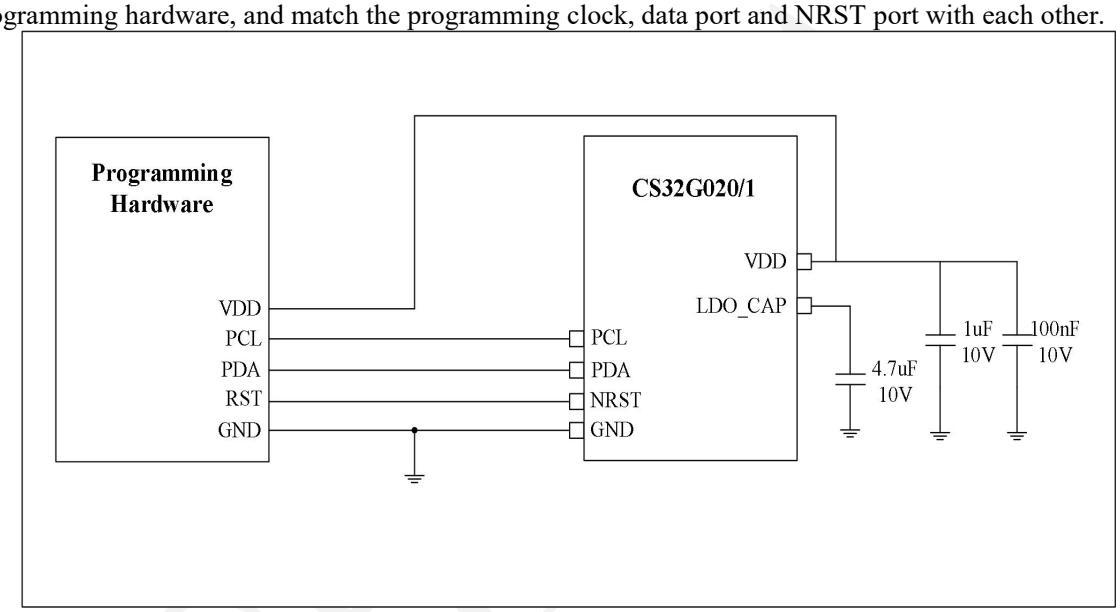


Figure 6 CS32G020/1 programming through serial interface

4.2. Updating applications through Type-C interface

All CS32G020/1 chips, when leaving the factory, are provided with the BoostLoader upgrade program that supports PD3.1 firmware upgrades. Software upgrades may be completed by simply connecting the CC data cable to the accompanied firmware upgrade tool.

The programming files are in the format of hex, produced by the compiler, and may be downloaded and programmed to the FLASH by configuring the host computer and firmware upgrade tool through the CS32G020/1 and using the non-block transmission PD3.1.

The programming connection of firmware upgrade tool is shown below:

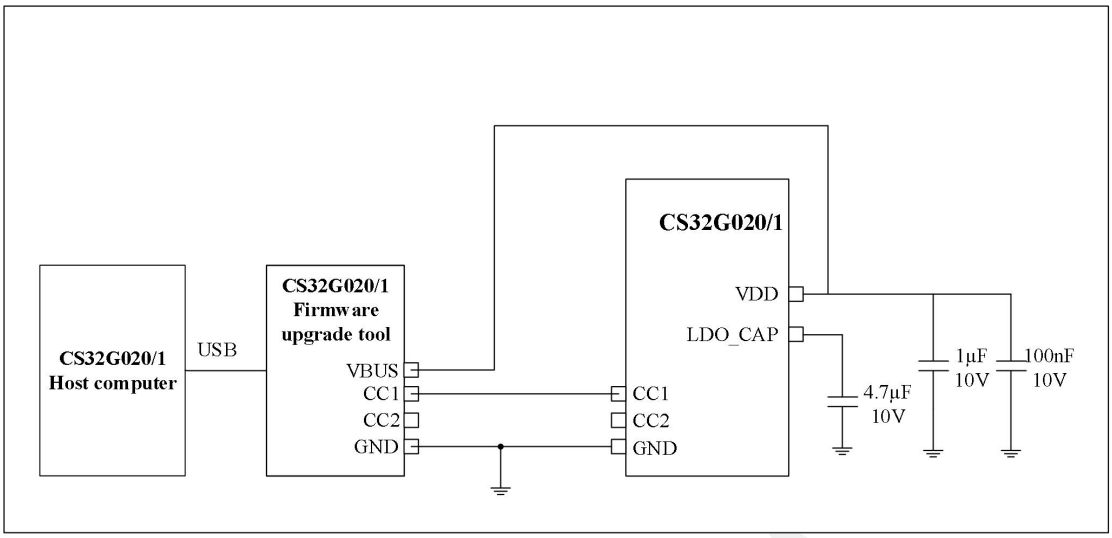


Figure 7 CS32G020/1 programming through Type-C interface

4.3. Programming through SWD interface

The CS32G020/1 supports programming and debugging through the SWD interface. In case of debugging or light programming, the SWD interface may be used, provided that it is not shared with other functions.

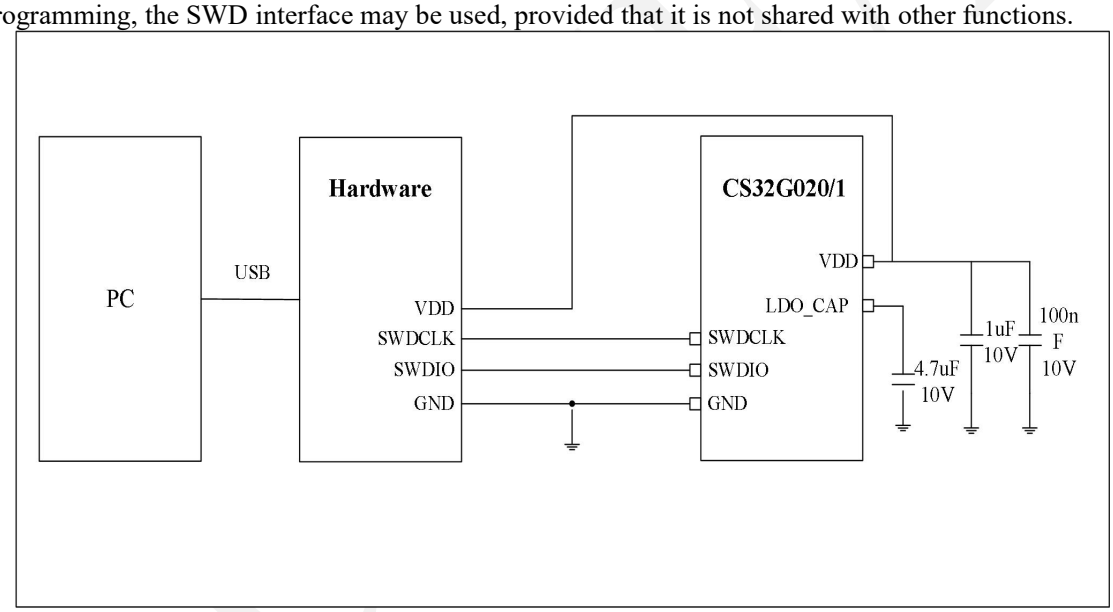


Figure 8 CS32G020/1 programming through SWD interface

4.4. Selection of programming method

Programming method for the chip may vary with the particular circumstances.

- In case of a bare chip, programming may be carried out with a special programmer or through the SWD interface.
- If the chip is already mounted on a board with a programming interface and a SWD interface reserved, the work may be performed with a special programmer or through the SWD interface.
- If the chip is already mounted on a board and uses a Type-C port and supports upgrade by bootloader, the bootloader may be employed for programming purpose.
- During solution development, programming by SWD is simple and easy for debugging.
- During mass production, a special programmer is recommended. We supply two programmers: the One-driving-four programmer and the programmer lite. The programmer lite is for development purpose only. For mass production, the one-driving-four programmer shall be used as long as practicable instead of the programmer lite, which is not suggested.

5. Typical application

5.1. Power banks

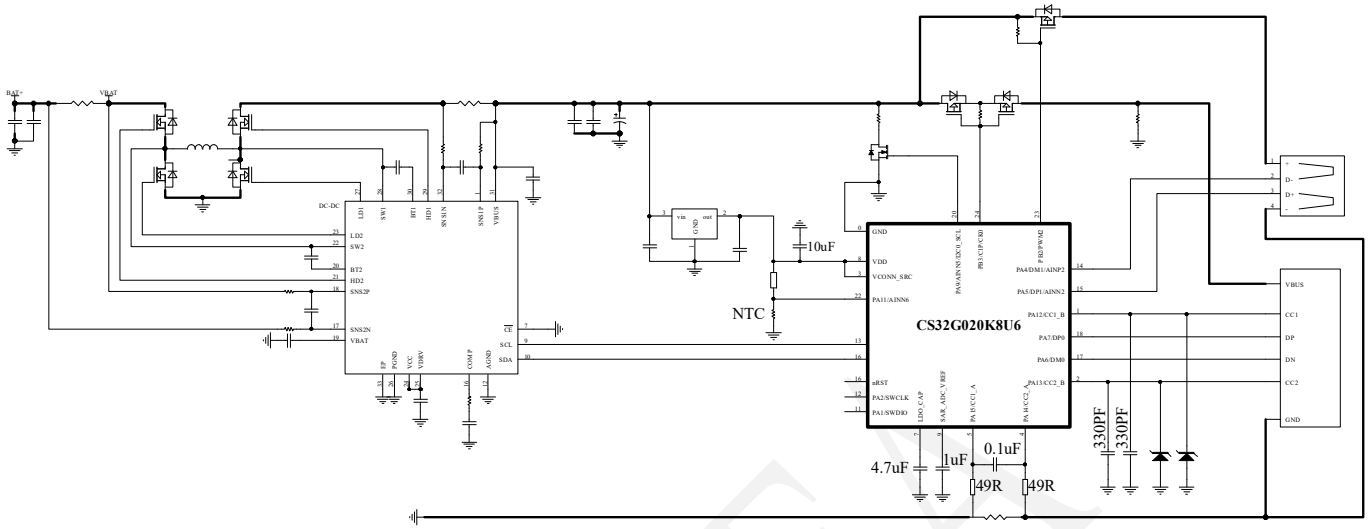


Figure 9 Typical application diagram of power banks

5.2. Car chargers

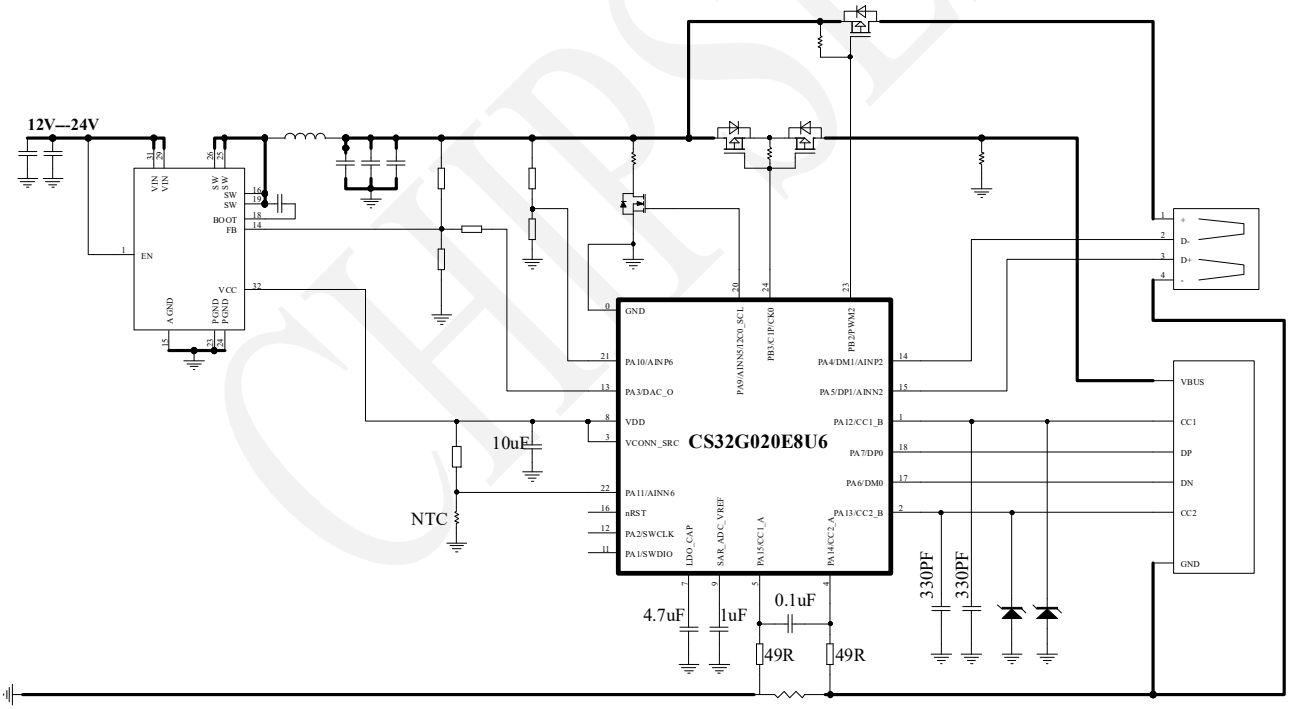


Figure 10 Typical application diagram of car chargers

5.3. AC adapters

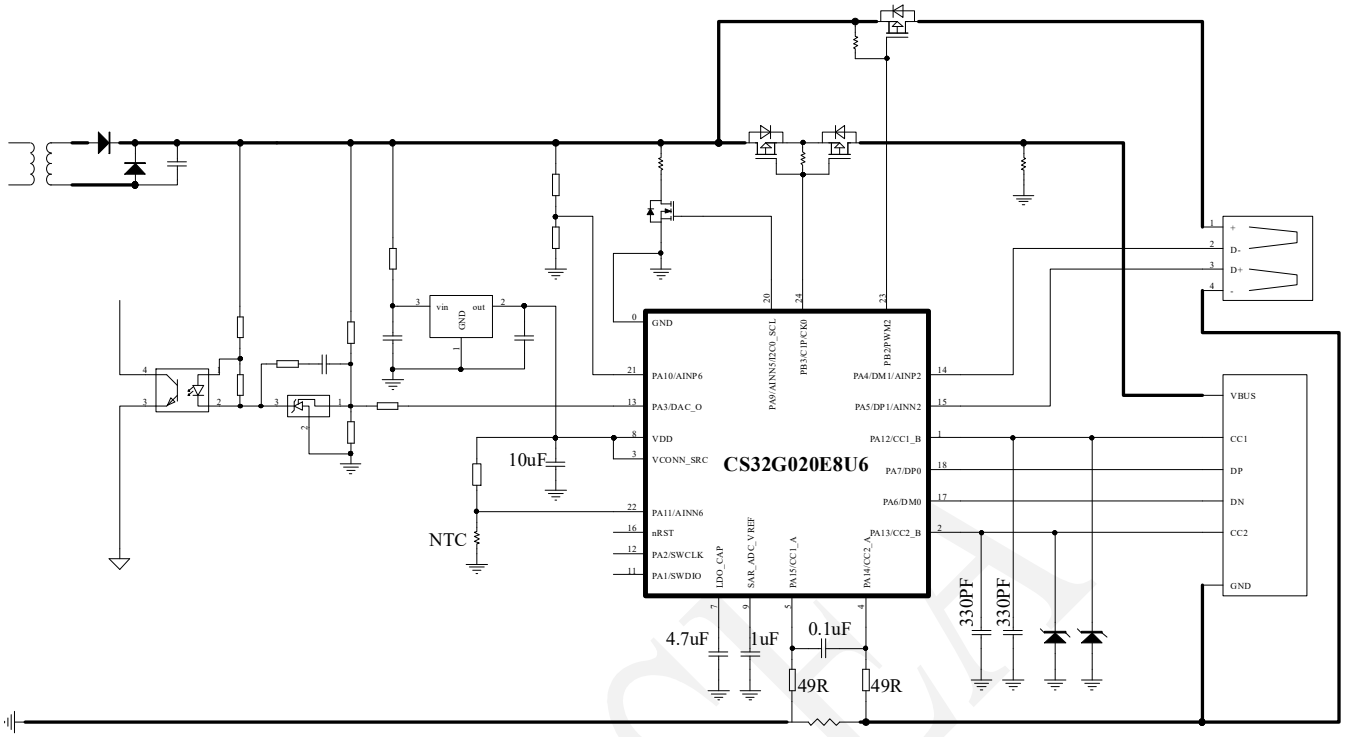


Figure 11 Typical application of AC adapters

6. Electrical characteristics

6.1. Limit value

Table 9 Limit value

Symbol	Parameter	Min Value	Max Value	Unit
V_{DD}-V_{AGND}	Voltage of DC power supply	-0.3	6.0	V
V_{IN}	Input voltage on pin	V_{AGND}-0.3	V_{DD}+0.3	V
V_{CC_PIN}	Input voltage of CC port (PA12, PA13, PA14 and PA15)	-	24	V
V_{VBUS_ENn}	Input voltage of Port VBUS_EN1 (PB3) and VBUS_EN2 (PB2)	-	24	V
T_A	Operating temperature	-40	85	ºC
T_{ST}	Storage temperature	-55	150	ºC
I_{VDD}	Max. inflow current of VDD	-	120	mA
I_{GND}	Max. outflow current of GND	-	120	mA
I_{IO}	Max. sink current of individual pin	-	35	mA
	Max. outflow current of individual pin	-	35	mA
	Aggregated max. sink current of all pins	-	100	mA
	Aggregated max. output current of all pins	-	100	mA

6.2. Electrical characteristics of DC power supplies

Table 10 Electrical characteristics of DC power supplies

(V_{DD} - V_{GND} = 2.5~5.5 V, T_A = 25 °C)

Symbol	Parameter	Min Value	Typical value	Max Value	Unit	Test conditions
V_{DD}	Operating voltage	2.5	5	5.5	V	-40 ºC ~+85 ºC, up to 48MHz
V_{AGND}/ AV_{AGND}	Power ground	-0.3	0	0.3	V	
LDO	Output voltage	1.35	1.5	1.65	V	V_{DD}≥1.8V
R_{PH}	PA, PB and NRST pull-up resistor		40		kΩ	V_{DD}=5V
			70		kΩ	V_{DD}=3V
R_{PD}	PA, PB and TESTEN pull-down resistor		40		kΩ	V_{DD}=5V
			70		kΩ	V_{DD}=3V
I_{LK}	Input leakage current of PA and PB	-1	-	1	μA	V_{DD} = 5 V, 0 < V_{IN} < V_{DD} Open-drain or input modes.
V_{IL1}	Input low level of PA and PB (Schmitt input disabled)	-0.3	-	V_{DD}/2	V	V_{DD}=4.5V
		-0.3	-	V_{DD}/2	V	V_{DD}=3.0V
V_{IH1}	Input high level of PA and PB (Schmitt input disabled)	V_{DD}/2	-	V_{DD}+0.3	V	V_{DD}=5.5V
		V_{DD}/2	-	V_{DD}+0.3	V	V_{DD}=3.0V
V_{ILS1}	Negative threshold voltage of NRST (Schmitt input)	-0.3	-	0.2V_{DD}	V	-
V_{IHS1}	Positive threshold voltage of NRST (Schmitt input)	0.7V_{DD}	-	V_{DD}+0.3	V	-

Symbol	Parameter	Min Value	Typical value	Max Value	Unit	Test conditions
V_{ILS2}	Negative threshold voltage of PA and PB (Schmitt input)	-0.3	-	$0.3V_{DD}$	V	-
V_{IHS2}	Positive threshold voltage of PA and PB (Schmitt input)	$0.7V_{DD}$	-	V_{DD}+0.3	V	-
V_{OL1}	Output low level of PA and PB (except for PA12/PA13/PA14/ PA15/PB2/PB3)	-	0	-	V	-
V_{OH1}	Output high level of PA and PB (except for PA12/PA13/PA14/ PA15/PB2/PB3)	-	V_{DD}	-	V	-
V_{OL2}	Output low level of PA12/PA13/PA14/ PA15/PB2/PB3	-	0	-	V	-
V_{OH2}	Output high level of PA12/PA13/PA14/ PA15/PB2/PB3	-	V_{DD} – 0.7	V_{DD}	V	The output high level depends on load conditions. For capacitive load, no current will flow through, hence it is VDD; while for resistive load, it is determined by the resistance.
I_{OH0}	PB0/PB1/PB7/ PB8/PA10/PA11	-	15	-	mA	V_{DD}=5.0V
I_{OH1}	PA and PB source current other than the ports in I_{OH0} (push-pull output)	-	8	-	mA	V_{DD}=5.0V
I_{OH2}		-	4	-	mA	V_{DD}=3.0V
I_{OL0}	PB0/PB1/PB7/ PB8/PA10/PA11	-	21	-	mA	V_{DD}=5.0V
I_{OL1}	PA and PB sink current other than the ports in I_{OL0} (push-pull output)	-	12	-	mA	V_{DD}=5.0V
I_{OL2}		-	5	-	mA	V_{DD}=3.0V
I_{IDLE1}	Operating current under operation mode @ IRC 24MHz, HCLK = 48 MHz	-	10	-	mA	V_{DD} = 5.0 V, all peripherals enabled, PLL enabled.
I_{IDLE2}		-	8	-	mA	V_{DD} = 5.0 V, all peripherals disabled, PLL disabled.
I_{IDLE3}		-	9	-	mA	V_{DD} = 3.3 V, all peripherals enabled, PLL enabled.
I_{IDLE4}		-	7	-	mA	V_{DD} = 3.3 V, all peripherals disabled, PLL enabled.
I_{IDLE5}	Operating current under operation mode @ IRC8MHz, HCLK = 8 MHz	-	3	-	mA	V_{DD} = 5.0 V, all peripherals enabled, PLL enabled.
I_{IDLE6}		-	2.5	-	mA	V_{DD} = 5.0 V, all peripherals disabled, PLL disabled.
I_{IDLE7}		-	2.5	-	mA	V_{DD} = 3.3 V, all peripherals enabled, PLL enabled.

Symbol	Parameter	Min Value	Typical value	Max Value	Unit	Test conditions
I_{IDLE8}		-	2	-	mA	V_{DD} = 3.3 V, all peripherals disabled, PLL enabled.
I_{IDLE9}	Operating current under operation mode @ IRC 24MHz, HCLK = 24 MHz	-	7	-	mA	V_{DD} = 5.0 V, all peripherals enabled, PLL enabled.
I_{IDLE10}		-	4	-	mA	V_{DD} = 5.0 V, all peripherals disabled, PLL disabled.
I_{IDLE11}		-	6.5	-	mA	V_{DD} = 3.3 V, all peripherals enabled, PLL enabled.
I_{IDLE12}		-	4	-	mA	V_{DD} = 3.3 V, all peripherals disabled, PLL enabled.
I_{IDLE13}	Operating current under operation mode @ IRC 10KHz, HCLK = 10 KHz	-	110	-	µA	V_{DD} = 5.0 V, all peripherals enabled.
I_{IDLE14}		-	105	-	µA	V_{DD} = 5.0 V, all peripherals disabled.
I_{IDLE15}		-	92	-	µA	V_{DD} = 3.3 V, all peripherals enabled.
I_{IDLE16}		-	90	-	µA	V_{DD} = 3.3 V, all peripherals disabled.
I_{PWD1}	Standby current in Deep-Sleep Mode 2 (with LDO on)	-	12	-	µA	V_{DD} = 5.0 V, all oscillators and analog modules closed, IO connected to no load.
I_{PWD2}		-	8	-	µA	V_{DD} = 3.3 V, all oscillators and analog modules closed, IO connected to no load.
I_{PWD3}	Standby current in Power-Down Mode (with LDO off)	-	2.5	-	µA	V_{DD} = 5.0 V, all oscillators and analog modules closed, IO connected to no load.
I_{PWD4}		-	1.5	-	µA	V_{DD} = 3.3 V, all oscillators and analog modules closed, IO connected to no load.

6.3. Electrical characteristics of AC power supplies

6.3.1. Internal 24/8 MHz RC Oscillator

Table 11 Electrical characteristics of AC power supplies of Internal 24/8 MHz RC Oscillator

Symbol	Parameter	Min Value	Typical value	Max Value	Unit	Test conditions
F_{HRC}	Center frequency	-	24	-	MHz	T_A=25 ºC, V_{DD}=5V
	Center frequency	-	8	-	MHz	T_A=25 ºC, V_{DD}=5V
	After calibration	-1	-	+1	%	T_A=25 ºC, V_{DD}=5V
		-2	-	+2	%	T_A=-40~85 ºC, VDD=2.5~5.5V
I_{HRC}	Operating current		400		µA	T_A=25 ºC, V_{DD}=5V

6.3.2. Internal 10 KHz RC Oscillator

Table 12 Electrical characteristics of AC power supplies of Internal 10 KHz RC Oscillator

Symbol	Parameter	Min Value	Typical value	Max Value	Unit	Test conditions
V_{LRC}	Voltage	2.5	-	5.5	V	-
F_{LRC}	Center frequency	-	10	-	KHz	-
	After calibration	-10	-	+10	%	T_A=25 ºC, V_{DD}=5V
		-30	-	+30	%	T_A=-40~85 ºC, VDD=2.5~5.5V
I_{LRC}	Operating current	-	2	-	µA	T_A=25 ºC, V_{DD}=5V

6.3.3. PLL characteristics

Table 13 PLL characteristics

Symbol	Parameter	Min Value	Typical value	Max Value	Unit	Test conditions
F_{PLL_IN}	PLL input clock	2	6	24	MHz	T_A=25 ºC
	Duty ratio of PLL input clock	40	-	60	%	T_A=25 ºC
F_{PLL_OUT}	Frequency multiplication output clock of PLL	16	-	48	MHz	T_A=25 ºC
T_{LOCK}	Locking time of PLL	-	-	200	μs	T_A=25 ºC
$Jitter_{PLL}$	Clock jitter	-	-	300	ps	T_A=25 ºC

6.3.4. I²C characteristics

Table 14 I²C characteristics

Symbol	Parameter	Standard mode		Fast mode		Unit
		Min Value	Max Value	Min Value	Max Value	
$V_{DD}1$	Operating voltage	1.62	5.5	1.62	5.5	V
F_{SCL}	SCL clock rate	0	100	0	400	KHz
T_{HD}:STA	Retention time of START conditions	4	-	0.6	-	μs
T_{LOW}	Low level pulse width of SCL	4.7	-	1.3	-	μs
T_{HIGH}	High level pulse width of SCL	4	-	0.6	-	μs
T_{SU}:STA	Establishment time of repeated START signals	4.7	-	0.6	-	μs
T_{HD}:DAT	Data retention time of I2C bus devices	0	3.45	0	0.9	μs
T_{SU}:DAT	Establishment time of data	250	-	100	-	ns
T_r	Rise time of SCL and SDA signals	-	1000	$20+0.1Cb^2$	300	ns
T_f	Fall time of SCL and SDA signals	-	300	20+0.1Cb	300	ns
T_{SU}:STO	Establishment time of STOP conditions	4	-	0.6	-	μs
T_{BUF}	Bus Idle Time between STOP and START conditions	4.7	-	1.3	-	μs
T_{SP}	Pulse width of glitch that can be screened by input filter.	N/A	N/A	0	50	μs

Note 1: This is the voltage of the pull-up resistor on I²C bus, and it is not necessarily equal to the one of the chip, e.g. when the power voltage of the chip is 5 V, the voltage of the pull-up resistor on I²C bus may be 1.8 V.
Note 2: Cb is the total capacitance in the unit of pF on a single bus.

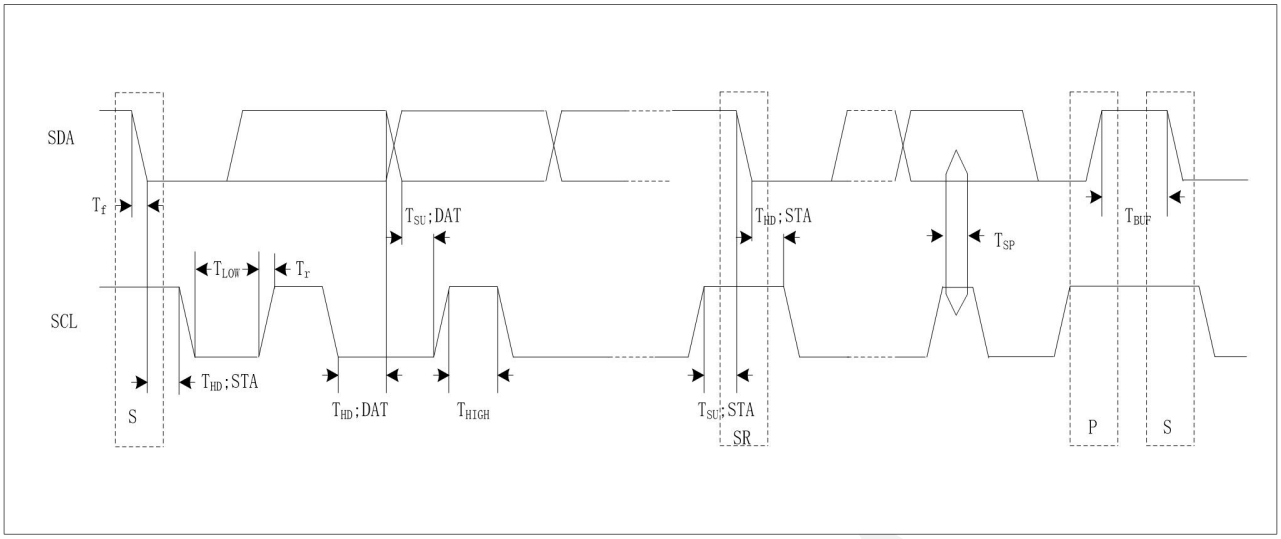


Figure 12 Definition of time sequence under I²C standard and fast modes

6.3.5. Characteristics of Flash

Table 15 Characteristics of Flash

Symbol	Parameter	Min Value	Typical value	Max Value	Unit	Test conditions
T_{ERASE}	Erasing time of Flash Block	4	4.5ms	5	ms	-40~85 ºC
T_{WRITE}	Write time of Flash Word (32 bits)			60	μs	-40~85 ºC
T_E	Erase and Write cycles of Flash			20,000	Times	-40~85 ºC
T_{DR}	Flash retention	100		-	years	25 ºC

6.4. Characteristics of analogs

6.4.1. 12-bit ADC

Table 16 Characteristics of analogs of 12-bit ADC

Symbol	Parameter	Min Value	Typical value	Max Value	Unit	Test conditions
V_{DD}	Operating voltage	2.5	5	5.5	V	-40~85 ºC
V_{IN}	Analog input range	0	-	VDD	V	-
I_{ADC}	Operating current of ADC	-	0.75	-	mA	VDD=5V (VDD as reference voltage)
T_{CONV}	Conversion duration of ADC	5	-	-	μs	VDD=5V
DNL	Non-linear differential	-2	±1	2	LSB	VDD=5V
INL	Non-linear integration (fully differential mode)	-3	-	3	LSB	Fully differential mode VREF = 0.5 V @ [0-60mV], VDD = 5 V
		-2	-	2	LSB	Fully differential mode VREF = 1 V @ [0-60mV], VDD = 5V
		-4	-	4	LSB	Fully differential mode. The voltage reference may not be VDD, VDD = 5 V.
	Non-linear integration (single-ended mode)	-7	-	7	LSB	Single-ended mode, VREF = 0.5 V, VDD = 5 V
		-5	-	5	LSB	Single-ended mode, VREF employs other voltage, VDD =

Symbol	Parameter	Min Value	Typical value	Max Value	Unit	Test conditions
						5 V
E_O	Bias error of fully differential mode	-	±2	-	LSB	VDD=5V
	Bias error of single-ended mode	-	±3	-	LSB	VDD=5V
E_G	Gain error	-4	-	+4	LSB	VDD=5V

Formula for max. external input impedance:

$$R_{ain} < \frac{T_s}{9C_{ADC}} - R_{ADC}$$

Where R_{ADC} = 2.3 k and C_{ADC} = 17.5 pF, representing the sampling resistance and capacitance inside ADC.

Sampling time Ts/us	2	4	8	16
External impedance Rain/k	10.5	23.1	48.5	99.3

Notes: This table is guaranteed by the designer but has not yet been verified with tests. (Where any of AINP7, AINN7, AINP8 and AINN8 is selected as the input port, R_{ADC} = 3.3 k)

6.4.2. 11-bit DAC

Table 17 Characteristics of analogs of 11-bit ADC

Symbol	Parameter	Min Value	Typical value	Max Value	Unit	Test conditions
VDD	Operating voltage	2.5	5	5.5	V	-40~85 ºC
I_{DAC}	Operating current of DAC	-	0.75	-	mA	VDD=5V (VDD as reference voltage)
T_{CONV}	Conversion speed of DAC	5	-		μs	VDD=5V
RLOAD	Resistive load	5	-		kΩ	BUFFER enabled
CLOAD	Capacitive load		-	50	pF	BUFFER enabled
DAC_OUT min	Min. output of DAC	0.2	-		V	BUFFER enabled
DAC_OUT max	Max. output of DAC	-	-	VDD-0.2	V	BUFFER enabled
Tsettling	Establishment time of DAC	-	3	4	μS	CLOAD ≤ 50 pF, RLOAD ≥ 5 K The time from the 10-bit input code jumps from the min. to the max. until DAC_OUT stabilized at the final value ± 1 LSB.
Update rate	Refresh rate	-		200	KS/s	CLOAD ≤ 50 pF, RLOAD ≥ 5 K Change in DAC_OUT with the input code varying 1 LSB
Twakeup	Wakeup time	-	6.5	10	μS	CLOAD ≤ 50 pF, RLOAD ≥ 5 K Values of DAC corresponding to the input code from shutdown to output
DNL	Non-linear differential	-1	-	1	LSB	-
INL	Integral nonlinearity	-4	-	4	LSB	-
E_G	Gain error	-0.5	-	-0.5	%	-

6.4.3. Comparators

Table 18 Comparators

Symbol	Parameter	Min Value	Typical value	Max Value	Unit	Test conditions
V_{CMP}	Operating voltage	2.5	5	5.5	V	-40 ºC ~+85 ºC
T_A	Temperature	-40	25	85	ºC	-
V_{IN}	Input voltage range	0	-	VDD	V	-
Icomp	Operating current		60		μA	VDD=2.5V~5V
PSRR	Supply voltage rejection ratio	-	60	-	dB	-
CMRR	Common mode rejection ratio	-	60	-	dB	-
Tresp	Response time	-	-	10	μS	VDD=2.5V~5V
CMP LSB	Minimum resolution	-	2	-	mV	-
V_{offset}	Offset voltage	-2	-	2	mV	2.5V~5.5V, -40 ºC ~+85 ºC

6.4.4. Internal reference voltage

Table 19 Internal reference voltage

Symbol	Parameter	Min Value	Typical value	Max Value	Unit	Test conditions
V_{RIN}	Internal reference voltage	-1%	1.0	+1%	V	VDD=5.0V, T_A=25 ºC
		-2%	1.0	-2%	V	VDD=2.5~5.5V, T_A=-40~85 ºC
		-1%	2.0	+1%	V	VDD=5.0V, T_A=25 ºC
		-2%	2.0	-2%	V	VDD=2.5~5.5V, T_A=-40~85 ºC
		-1%	3.0	+1%	V	VDD=5.0V, T_A=25 ºC
		-2%	3.0	-2%	V	VDD=3.3~5.5V, T_A=-40~85 ºC
		-1%	4.0	+1%	V	VDD=5.0V, T_A=25 ºC
		-2%	4.0	-2%	V	VDD=4.3~5.5V, T_A=-40~85 ºC
		-	VDD	-	V	VDD=5.0V, T_A=25 ºC
CMP0_VREF	Voltage reference output of Comparator 0	0.00	0.00	0.05	V	VDD>2.7V
		0.275	0.325	0.38	V	VDD>2.7V
		0.55	0.60	0.65	V	VDD>2.7V
		0.85	1.00	1.15	V	VDD>2.7V
		1.80	2.00	2.20	V	VDD>2.7V
		2.40	2.70	3.00	V	VDD>3.2V
		2.70	3.00	3.30	V	VDD>3.5V
		3.00	3.30	3.60	V	VDD>3.8V
		1.00	1.20	1.40	V	VDD>2.7V
		2.25	2.40	2.65	V	VDD>2.9V

Note: The precision of voltage reference may be guaranteed only when VDD is 0.5 V greater than the reference.

6.4.5. Specifications of LDO and Power management

Table 20 Specifications of LDO and Power management

Symbol	Parameter	Min Value	Typical value	Max Value	Unit	Test conditions
V_{DD}	Input voltage	2.5	-	5.5	V	-
V_{LDO}	Output voltage	1.35	1.5	1.65	V	-
T_A	Operating temperature	-40	25	85	ºC	-
C_{LDO}	Capacitance	-	4.7	-	μF	R_{ESR}<1Ω

Note: To ensure power stability, a 4.7 μF capacitor is required between LDO and the nearest VSS.

6.4.6. Low voltage reset

Table 21 Low voltage reset

Symbol	Parameter	Min Value	Typical value	Max Value	Unit	Test conditions
VDD	Operating voltage	0	-	5.5	V	-
T_A	Operating temperature	-40	25	85	ºC	-
I_{BOD}	Quiescent current	-	1	140	μA	VDD=5.5V
V_{BOD}	Low voltage value (Rising edge)	1.65	1.8	1.95	V	T_A=-40~85 ºC
		1.85	2.0	2.15	V	T_A=-40~85 ºC
		2.2	2.4	2.6	V	T_A=-40~85 ºC
		2.5	2.7	2.9	V	T_A=-40~85 ºC
		2.8	3.0	3.2	V	T_A=-40~85 ºC
		3.3	3.6	3.9	V	T_A=-40~85 ºC
		3.6	4.0	4.4	V	T_A=-40~85 ºC
		6.0	6.5	7.0	V	T_A=-40~85 ºC
V_{BOD}	Low voltage value (falling edge)	1.65	1.8	1.95	V	T_A=-40~85 ºC
		1.85	2.0	2.15	V	T_A=-40~85 ºC
		2.2	2.4	2.6	V	T_A=-40~85 ºC
		2.5	2.7	2.9	V	T_A=-40~85 ºC
		2.8	3.0	3.2	V	T_A=-40~85 ºC
		3.3	3.6	3.9	V	T_A=-40~85 ºC
		3.6	4.0	4.4	V	T_A=-40~85 ºC
		6.0	6.5	7.0	V	T_A=-40~85 ºC

6.4.7. Power-on reset

Table 22 Power-on reset

Symbol	Parameter	Min Value	Typical value	Max Value	Unit	Test conditions
T_A	Operating temperature	-40	25	85	ºC	-
V_{POR_th}	Threshold voltage released when reset	-	1.6	-	V	-
V_{POR_start}	Starting voltage upon power-on reset	-	-	100	mV	-
RR_{VDD}	Rate of voltage rise upon power-on reset	0.025	-	-	V/ms	-
T_{POR_Dealy}	Delay upon power-on reset	20ms		120ms		
T_{POR}	Shortest duration requirement of maintaining voltage at V_{POR_start} upon power-on reset	0.5	-	-	ms	-

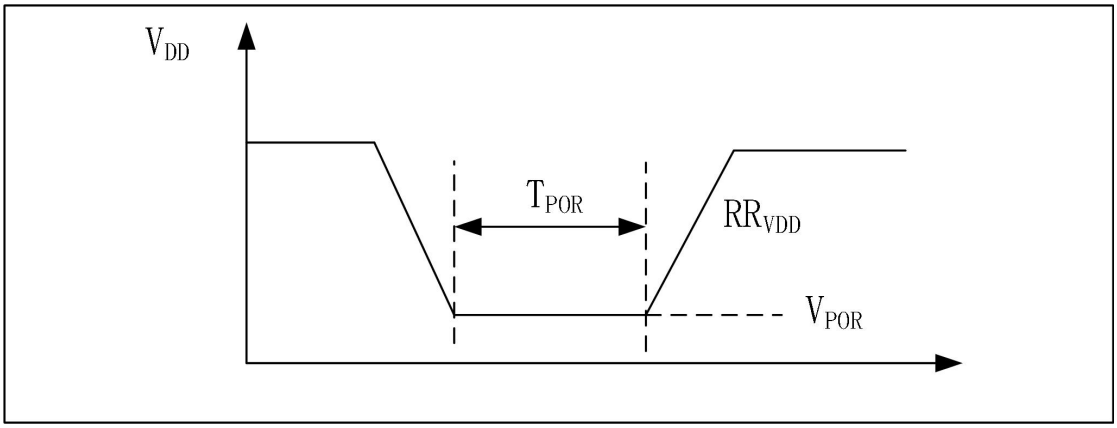


Figure 13 Definition of power-on reset

6.4.8. Characteristics of Type-C

Table 23 Characteristics of Type-C

(VDD = 5V, T_A = 25°C, this is the case unless stated otherwise)

Symbol	Parameter	Min Value	Typical value	Max Value	Unit	Test conditions
VDD	Operating voltage range	2.5	5	5.5	V	25 ºC
		2.7	5	5.5	V	-40 ºC ~+85 ºC
Rp	CC1 and CC2	73	80	87	μA	VDD>3V
		165	180	195	μA	VDD>3V
		303	330	357	μA	VDD>3V
Rd	Pull-down resistor	4.6	5.1	5.6	KΩ	VDD=2.7V~5V
T_{settle_pd}	Rise and fall time of PD square waves	300	-	1300	ns	For CC port, 330 pf capacitors are recommended.

6.4.9. Characteristics of QC3.0

Table 24 Characteristics of QC3.0

(VDD = 5V, T_A = 25°C, this is the case unless stated otherwise)

Symbol	Parameter	Min Value	Typical value	Max Value	Unit	Test conditions
VDD	Operating voltage range	2.5	5	5.5	V	25 ºC
		2.7	5	5.5	V	-40 ºC ~+85 ºC
RDP	DPn pull-down resistance	300	500	1500	KΩ	
RDM	DMn pull-down resistance	16	18	20	KΩ	
	Short-circuited resistance of DPn and DMn	-	20	40	Ω	

7. Package information

7.1. QFN24-PIN (4 mm * 4 mm * 0.55, e = 0.5 mm)

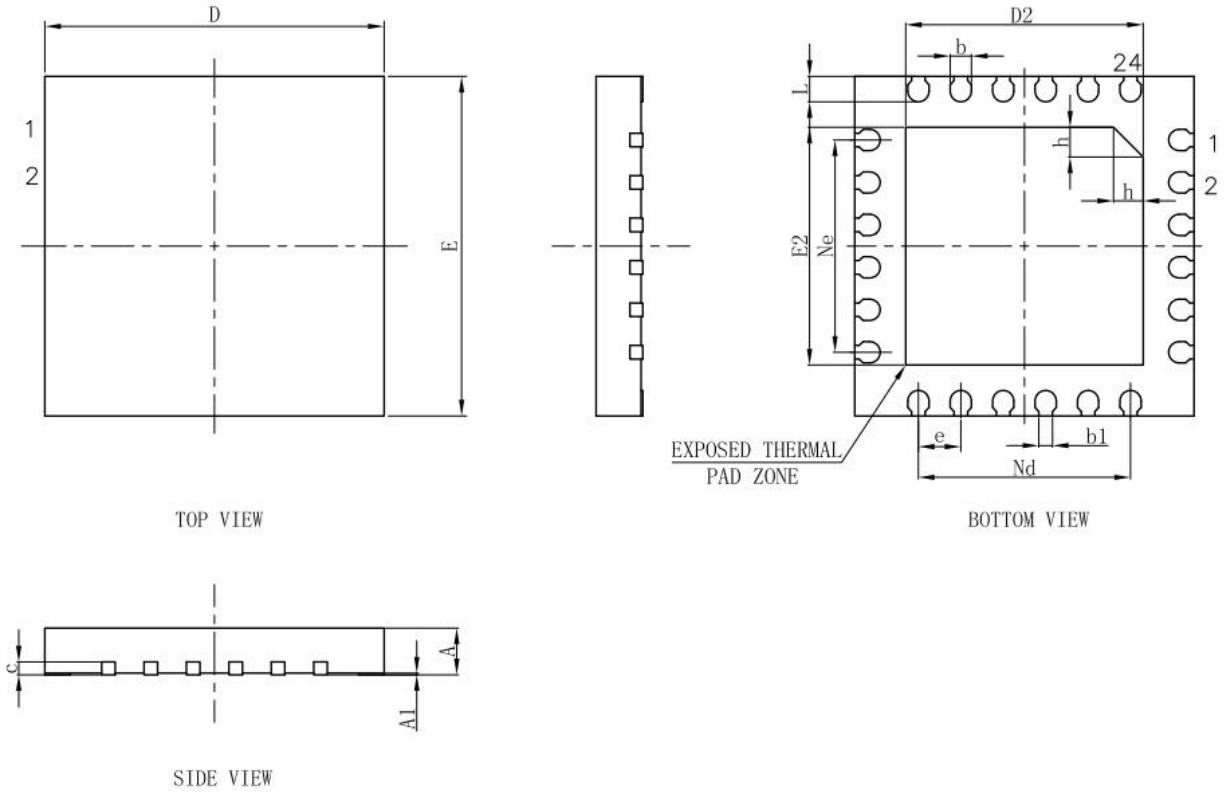


Figure 14 Package diagram of QFN24-PIN

Table 25 Package size of QFN24-PIN

SYMBOLS	MIN	NOR	MAX
	(mm)		
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
c	0.10	0.15	0.20
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
L	0.25	0.30	0.35
h	0.30	0.35	0.40

7.2. QFN32 (5 mm * 5 mm * 0.75 mm, e = 0.5 mm)

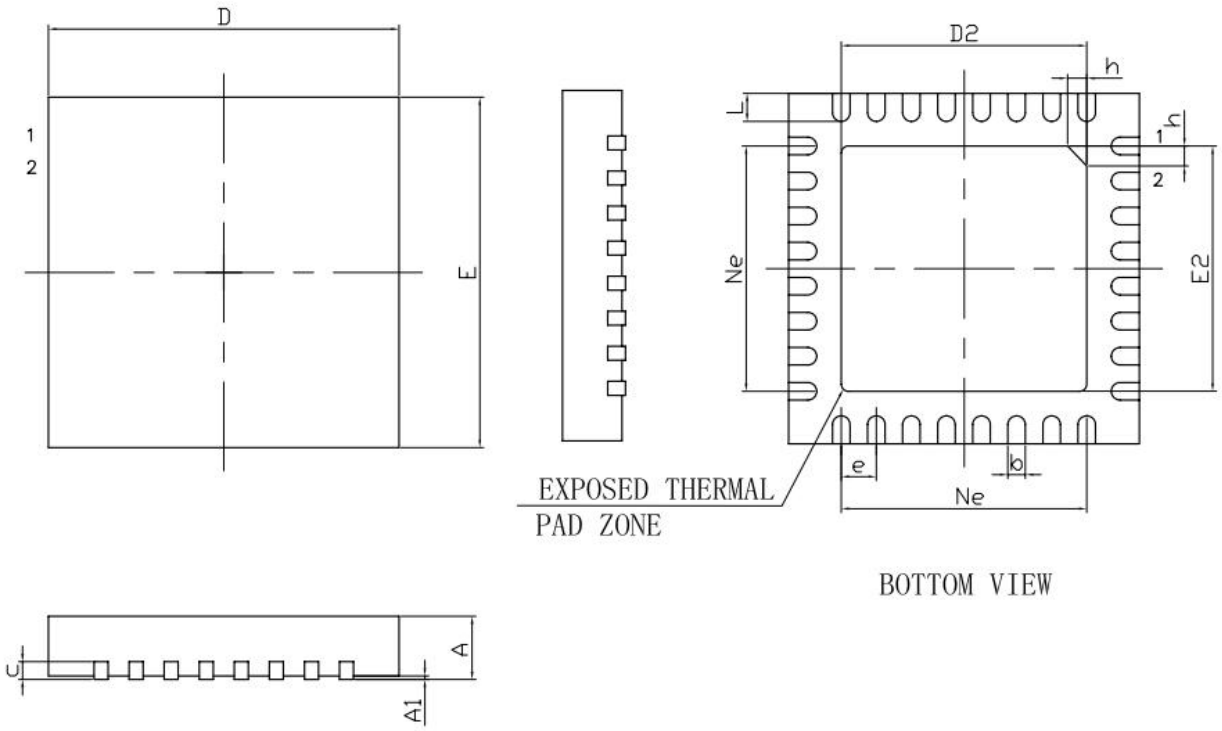


Figure 15 Package diagram of QFN32

Table 26 Package size of QFN32

SYMBOLS	MIN	NOR	MAX
	(mm)		
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
b1	0.16REF		
c	0.15	0.20	0.25
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
e	0.50BSC		
Ne	3.50BSC		
Nd	3.50BSC		
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
L	0.25	0.30	0.35
h	0.30	0.35	0.40

7.3. Thermal characteristics

Table 27 Thermal characteristics of QFN32

Name	Size	Unit
ΘJA, by 2S2P	67.6	℃/W
ΘJC	14.3	℃/W

7.4. Humidity characteristics

Table 28 Humidity characteristics of QFN32

Name	Level
Humidity level	MSL3

8. Naming conventions of products

8.1. Description of product name

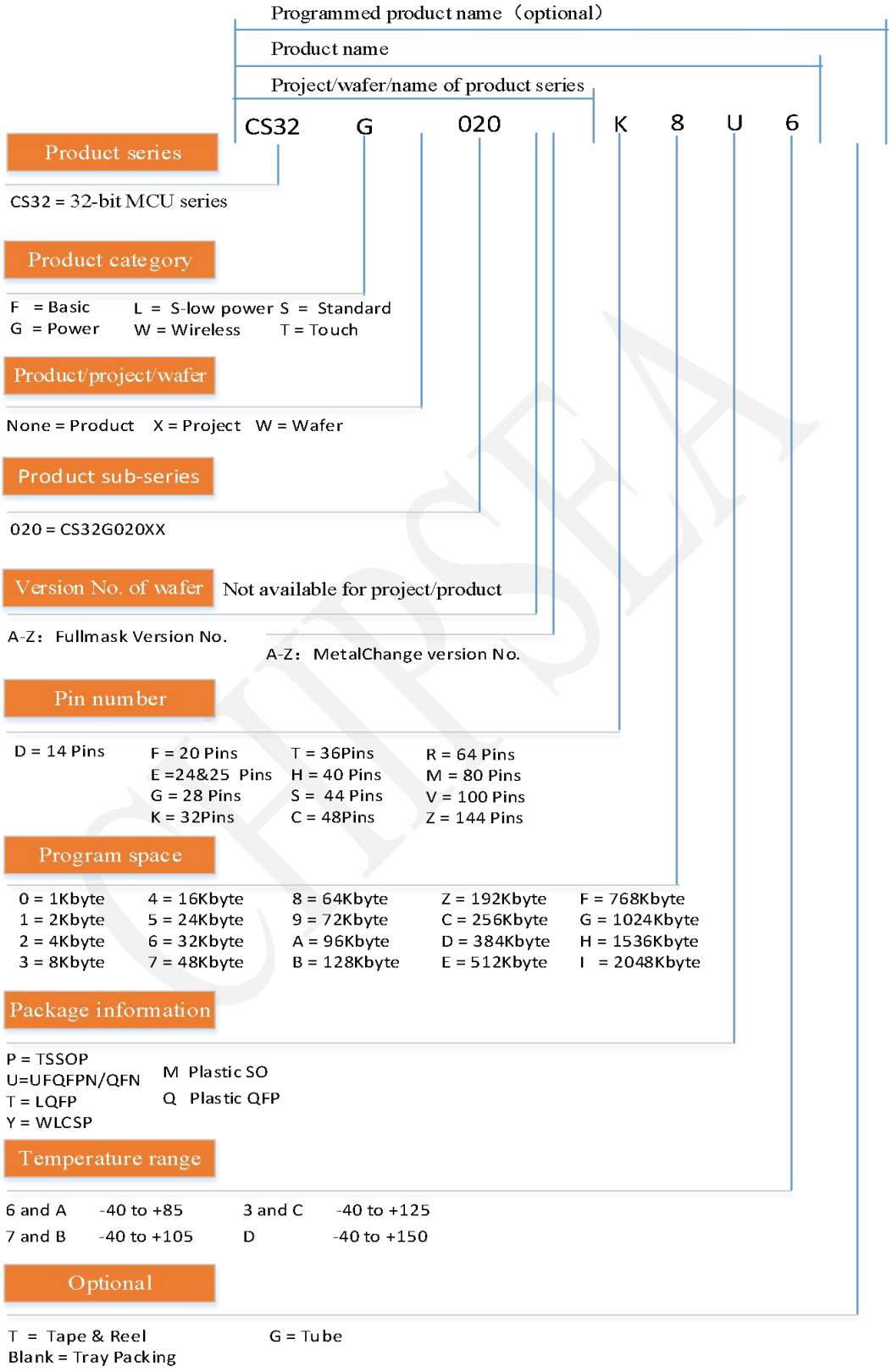
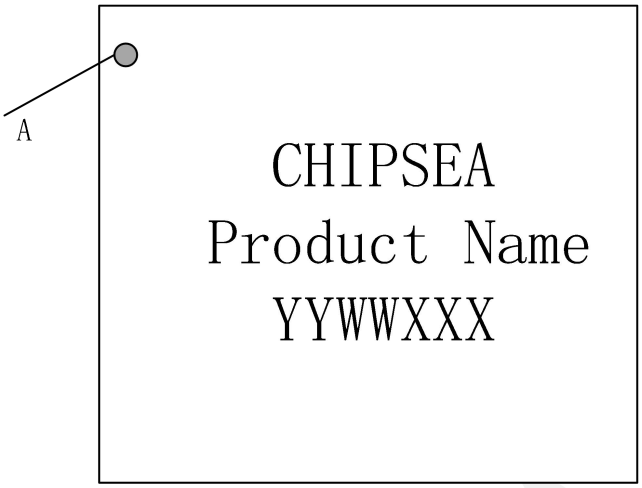


Figure 16 Naming conventions of CS32G020/1 products

8.2. Description of marks on product



There are usually 3 lines on the front of a chip:

The first line shows the company name CHIPSEA.

The second line shows the product model. For some small package sizes, the product model will be spelled in a simplified form.

The third line shows the date code. From the left, the first two numbers are the last two digits of the calendar year; the third and fourth numbers are the number of calendar weeks of the year, the left digit will be zero if the number is not a two-digit one; and the last three numbers are random numbers.

E.g. the marks on CS32G020/1K8U6 are as follows:

9. Order Information

Table 29 Order information

Product model	Pin	Storage (KB)	Package	Package type	Quantity	Operating temperature (℃)	MSL	Silk screen printing
CS32G020K8U6	32	64KB	QFN32	Tray	4900	-40 ~85	3	G020K8U6
CS32G020E8U6	24	64KB	QFN24	Tray	4900	-40 ~85	3	G020E8U6
CS32G021K8U6	32	64KB	QFN32	Tray	4900	-40 ~85	3	G021K8U6
CS32G021E8U6	24	64KB	QFN24	Tray	4900	-40 ~85	3	G021E8U6

10. Reflow curve for reference, peak temperature

Table 30 Lead-free process Package classification Reflow temperature

Package thickness	Volume mm3 <350	Volume mm3 350-2000	Volume mm3 >2000
<1.6 mm	260 +0 °C *	260 +0 °C *	260 +0 °C *
1.6 mm - 2.5 mm	260 +0 °C *	250 +0 °C *	245 +0 °C *
≥2.5 mm	250 +0 °C *	245 +0 °C *	245 +0 °C *
*Tolerances: Equipment manufacturers/suppliers should ensure process compatibility up to and including the stated rating temperature (this means peak Reflow temperature +0° C. For example, 260° C+0° C) at the rated MSL level.			

Table 31 Hierarchical Reflow Curve

Features of curve	Lead-free components
Average ramp rate（Ts_{max} to Tp）	3° C/second max
Preheating − Lowest temperature（Ts_{min}） − Highest temperature（Ts_{max}） − Time（ts_{min} to ts_{max}）	 150 °C 200 °C 60-180 seconds
Lasting time: − Temperature（T_L） − Time（t_L）	 217 °C 60-150 seconds
Peak/Hierarchical temperature（Tp）	Please refer to**Table 30 for details**
Time within 5°C of actual peak temperature (tp)	20-40 seconds
Ramp-down rate	6 °C/second max
Time from 25°C to peak temperature	8 minute max

Note: All temperatures refer to the top temperature of the package, measured on the surface of the package.

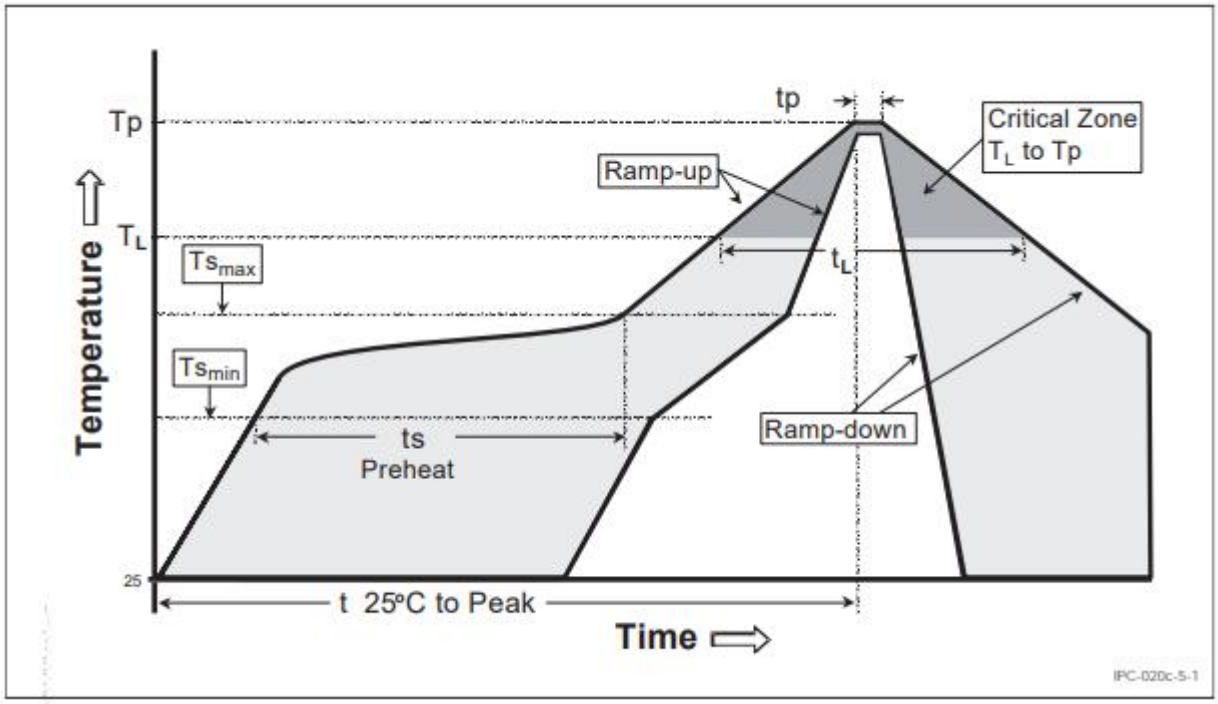


Figure 17 Reflow curve

11. Package information

Package type and quantity:

Product model	Package size	Package type	Quantity/Package
CS32G020K8U6	QFN32 5mm*5mm*0.75mm,e=0.5mm	Tray	490EA/tray, 10 trays（4900EA）+1（empty tray）/box, 6 boxes/carton（29400EA）
CS32G020E8U6	QFN32 4mm*4mm*0.55,e=0.5mm	Tray	490EA/tray, 10 trays（4900EA）+1（empty tray）/box, 6 boxes/carton（29400EA）
CS32G021K8U6	QFN32 5mm*5mm*0.75mm,e=0.5mm	Tray	490EA/tray, 10 trays（4900EA）+1（empty tray）/box, 6 boxes/carton（29400EA）
CS32G021E8U6	QFN32 4mm*4mm*0.55,e=0.5mm	Tray	490EA/tray, 10 trays（4900EA）+1（empty tray）/box, 6 boxes/carton（29400EA）

Packaging specifications list:

Inner packaging material	Tray, cable ties, desiccant, humidity indicator card, aluminum foil bag, bubble bag, inner box label, inner box (with our logo).
External packaging material	Carton (with our logo), tape, outer carton label.
Requirements for carton	Outer carton (with our logo): double-layer corrugated cardboard (thickness ≤6mm), bursting strength ≥14kg/cm^2, the gap between the inner box and the carton ≥1cm must be filled with bubble pads or sponge pads.
Partial carton	Only one partial carton is allowed per batch for the same order.

Inner box	Cable ties	Desiccant	Humidity indicator card	Aluminum foil bag	Bubble bag	Carton	Cable ties
370*150*88 mm	>6mm	Above 10g	6 dots	495*240 mm	440*240mm	385*320*275mm or 395*320*285mm	>6mm

Label description:

Name	Description
P/N	Label model
M/C	Product model
Lot	Lot number of products
Q'ty	Quantity of products, unit is PCS
Carton ID	Serial number on outer carton defined by the test factory The test factory defines the inner traceability identifier: BIN file: (x) means untested, (0) means defective product, (1) means good product BIN1, (2) means good product BIN2, greater than 1 means inferior product. SN code, i.e. the test factory assembly lot number, LY04+ (BIN file) + date (6 digits) + packaging method (2 digits) + serial number (4 digits) Packing: F0 TRAY vacuum bag, F1 TRAY inner box, G0 TRAY outer carton
Box ID	Serial number on inner box defined by the test factory The test factory defines the inner traceability identifier: BIN file: (x) means untested, (0) means defective product, (1) means good product BIN1, (2) means good product BIN2, greater than 1 means inferior product. SN code, i.e. the test factory assembly lot number, LY04+ (BIN file) + date (6 digits) + packaging method (2 digits) + serial number (4 digits)

	Packing: F0 TRAY vacuum bag, F1 TRAY inner box, G0 TRAY outer carton
MMCU	PO NO
MFG Lot	Sub-process card number
D/C	YYWW
DATE	YYYY-MM-DD（packing date）
QR Code	It is comprised of “P/N”, “M/C”, “Lot&MFG Lot”, “Qty”, “PO NO”, “D/C”, “DATE”, “Carton ID(outer carton label)” or “Box ID(inner box label)”, using “)” to separate each item. No Qty unit will be printed and “Date” shall be a blank space.
Font	SimSun, 10 pt, bold

12. HSF Statement

12.1. RoHS

It complies with *The Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment* developed by the EU (EU RoHS2.0) (2011/65/EU & Amendment(EU) 2015/863).

12.2. REACH

REACH SVHC 223 and Annex XVII comply with REACH-EU Regulation “Regulation(EC) No. 1907/2006 of the European Parliament and of the Council of 18 December 2006 concerning the Registration, Evaluation, Authorization and Restriction of Chemicals (REACH)”.