CS35L00

2.8 W Mono Class-D Audio Amplifier with Low Idle Current

CS35L00 Features

- Hybrid Class-D Architecture
  - <1 mA Quiescent Current
  - 1 x 2.8 W into 4 Ω (10% THD+N)
  - 1 x 2.3 W into 4 Ω (1% THD+N)
  - 1 x 1.7 W into 8 Ω (10% THD+N)
  - 1 x 1.4 W into 8 Ω (1% THD+N)
- Advanced ΔΣ Closed-loop Modulation
  - 98 dB Signal-to-Noise Ratio (A-Weighted)
  - 0.02% THD+N @ 1 W (SD & HD Mode)
- Integrated Protection and Automatic Recovery for Output Short-circuit and Thermal Overload
- Thermally Enhanced 10-pin DFN Package with Pin-selectable Gain of +6 dB or +12 dB
- Pop and Click Suppression

Common Applications

- Laptops
- Netbooks
- Portable Navigation Devices
- Active Speakers
- Portable Gaming

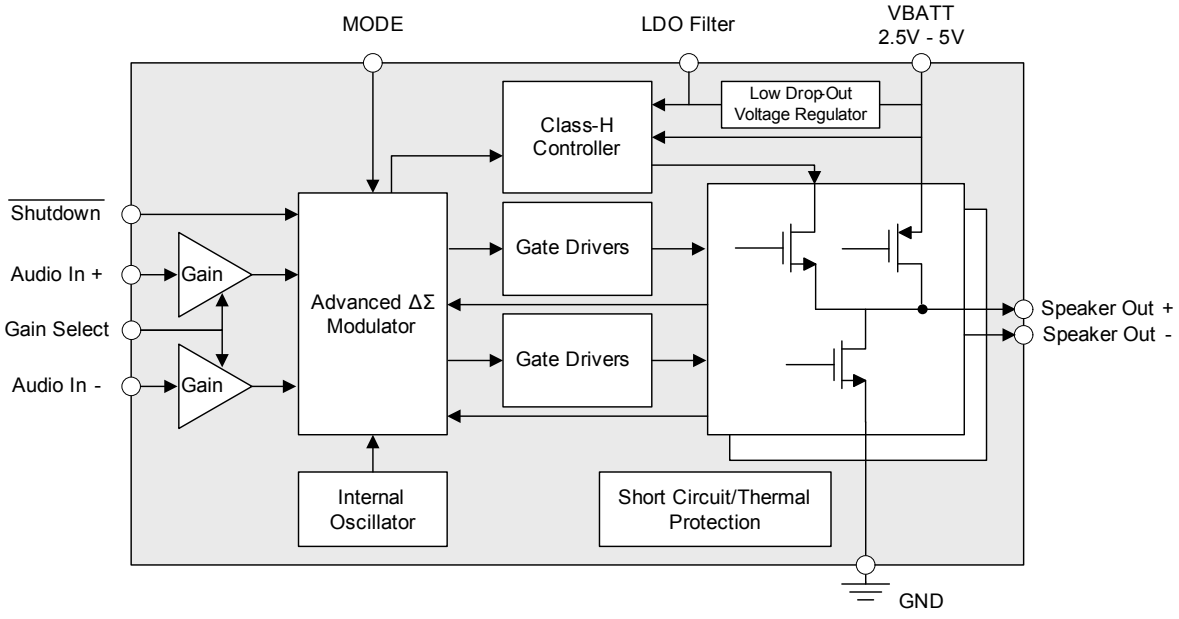
General Description

The CS35L00 is a 2.8 W high efficiency Hybrid Class-D audio amplifier with low idle current consumption and a selectable gain.

The CS35L00 features an advanced closed-loop architecture to provide 0.02% THD+N at 1 W and -88 dB PSRR at 217 Hz.

A flexible Hybrid Class-D output stage offers four modes of operation: Standard Class-D (SD) mode offers full audio bandwidth and high audio performance; Hybrid Class-D (HD) mode offers a substantial reduction in idle power consumption with an integrated Class-H controller; Reduced Frequency Class-D (FSD) mode reduces the output switching frequency, producing lower electromagnetic interference (EMI); and Reduced Frequency Hybrid Class-D (FHD) mode produces both the lower idle power consumption of HD mode and the reduced EMI benefits of FSD mode.

Requiring minimal external components and PCB space, the CS35L00 is available in a 3.0 mm x 3.0 mm, 10-pin DFN package in Commercial grade (-10°C to +70°C). Please see "Ordering Information" on page 33 for package options and gain configurations.



Preliminary Product Information | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

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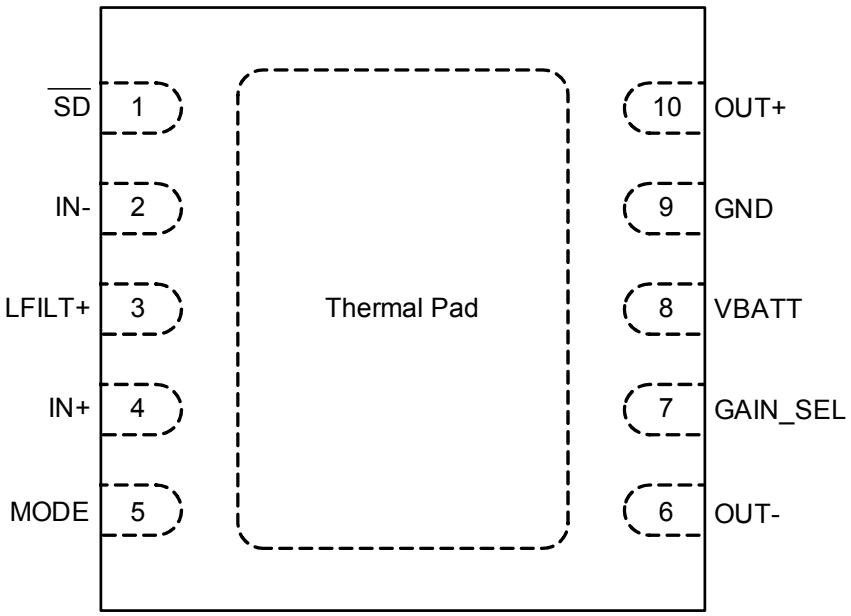


Figure 1. Top View of DFN Pin Out
(Looking down through package)

Pin Name	#	Pin Description
$\overline{SD}$	1	**Shutdown** (*Input*) - Pulling this pin low places the CS35L00 in shutdown.
IN-	2	**Negative Analog Input** (*Input*) - Differential negative audio signal input
LFILT+	3	**Low Drop Out Regulator Filter** (*Output*) - Bypass capacitor connection point for internal LDO. Connecting this net to VBATT places the device into SD mode.
IN+	4	**Positive Analog Input** (*Input*) - Differential positive audio signal input.
MODE	5	**Switching Mode** (*Input*) - Controls the output switching modes of the CS35L00.
OUT-	6	**Negative PWM Output** (*Output*) - Differential negative PWM output.
GAIN_SEL	7	**Gain Select** (*Input*) - Sets the gain of the amplifier. When pulled low, gain is +12 dB. When pulled high, gain is +6 dB.
VBATT	8	**Positive Analog Power Supply** (*Input*) - Positive power supply input.
GND	9	**Ground** (*Input*) - Power supply ground.
OUT+	10	**Positive PWM Output** (*Output*) - Differential Positive PWM output.
Thermal Pad	-	**Thermal Pad** *(Input)* - Thermal relief pad for optimized heat dissipation. Connect to GND. See "DFN Thermal Pad" on page 31 for more information.

2. DIGITAL PIN CONFIGURATIONS

See (Note 1) and (Note 2) below the table.

Power Supply	I/O Name	Pin #	Direction	Internal Connections	Configuration
VBATT	$\overline{SD}$	1	Input	No Internal Pull Up	Hysteresis on CMOS Input
	MODE	5	Input	No Internal Pull Up	Hysteresis on CMOS Input
	GAIN_SEL	7	Input	No Internal Pull Up	Hysteresis on CMOS Input

Note:

1. Refer to specification table "Digital Interface Specifications & Characteristics" on page 14 for details on the digital I/O characteristics.
2. I/O voltage levels must not exceed the voltage listed in table "Absolute Maximum Ratings" on page 8.

3. TYPICAL CONNECTION DIAGRAMS

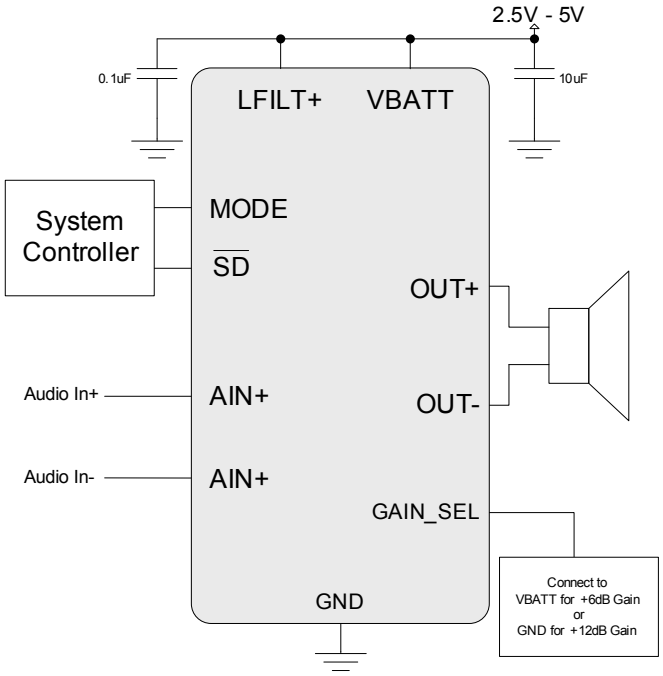


Figure 2. Typical Connection Diagram for SD & FSD Mode

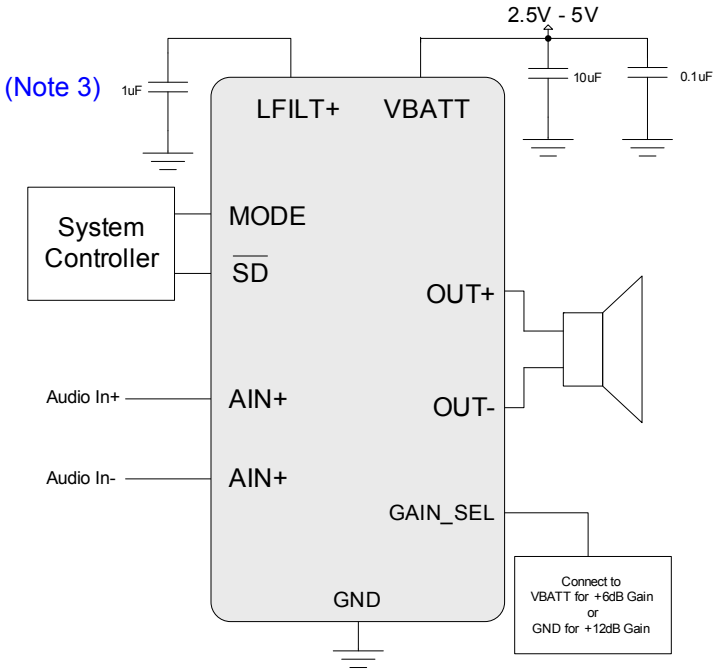


Figure 3. Typical Connection Diagram for HD & FHD Mode

Note:

3. The value of the capacitance connected to the LFILT+ net should not exceed 4.7 µF. Presence of a capacitance above 4.7 µF will prevent proper HD and FHD operation.

4. CHARACTERISTICS & SPECIFICATIONS

Test Conditions (unless otherwise specified): GND = 0 V; All voltages with respect to ground; Input signal = 997 Hz differential sine wave; T_A = 25°C; VBATT = 5.0 V; R_L = 8 Ω; 22 Hz to 20 kHz measurement bandwidth; Measurements taken with AES17 measurement filter and Audio Precision AUX-0025 passive filter.

RECOMMENDED OPERATING CONDITIONS

GND = 0 V; All voltages with respect to ground. Please see (Note 4).

Parameters	Symbol	Min	Typ	Max	Units
DC Power Supply					
Supply Voltage	VBATT	2.5	5.0	5.5	V
Temperature					
Ambient Temperature	T_A	-10	-	+70	°C
Junction Temperature	T_J	-10	-	+150	°C

ABSOLUTE MAXIMUM RATINGS

GND = 0 V; All voltages with respect to ground.

Parameters	Symbol	Min	Max	Units
DC Power Supply				
Supply Voltage	VBATT	-0.3	6.0	V
LFILT+ Current (Note 5)	I_{VDREG}	-	10	µA
Inputs				
Input Current	I_{in}	-	±10	mA
Temperature				
Ambient Operating Temperature (power applied)	T_A	-20	+125	°C
Storage Temperature	T_{stg}	-65	+150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device.

Notes:

4. Functionality is not guaranteed or implied outside of these limits. Operation outside of these limits may adversely affect device reliability.
5. No external loads should be connected to the LFILT+ net. Any connection of a load to this point may result in errant operation or performance degradation in the device.

ELECTRICAL CHARACTERISTICS - ALL OPERATIONAL MODES

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
Max. Current from LFILT+ (Note 6)	I_{LFILT+}		-	10	-	µA
LFILT+ Output Impedance	Z_{LFILT+}		-	0.7	-	Ω
VBATT Limit for HD/FHD Mode (Note 7)	VB_{LIM}		-	3.0	-	VDC
Input Level for Entering LDO Operation in HD/FHD Modes (Note 8)	V_{IN-LDO}	GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	- -	0.015•VBATT 0.029•VBATT	- -	Vrms Vrms
Input Level for Entering VBATT Operation in HD/FHD Modes (Note 9)	$V_{IN-VBATT}$	GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	- -	0.10 0.20	- -	Vrms Vrms
LDO Entry Time Delay	t_{LDO}		-	1200	-	ms
LDO Level for HD/FHD Modes	VLDO		-	1.0	-	V
Output Offset Voltage	V_{OFFSET}	Inputs AC coupled to GND	-	+/-2	-	mV
Amplifier Gain	A_V	GAIN_SEL = Low GAIN_SEL = High	- -	12 6	- -	dB dB
Shutdown Supply Current	$I_{A(SD)}$	$\overline{SD}$ = Low	-	0.05	-	µA
MOSFET On Resistance	$R_{DS(ON)}$	I_{bias} = 0.5 A	-	350	-	mΩ
Thermal Error Threshold (Note 10)	T_{TE}		-	150	-	°C
Thermal Error Retry Time (Note 10)	R_{TE}		-	1200	-	ms
Under Voltage Lockout Threshold (Note 10)	UVLO		-	2.0	-	V
Operating Efficiency	η	Output Levels at 10% THD+N				
		8 Ω + 33µH Load: VBATT = 5 VDC	-	90	-	%
		8 Ω + 33µH Load: VBATT = 3.7 VDC	-	89	-	%
		4 Ω + 33µH Load: VBATT = 5 VDC	-	84	-	%
		4 Ω + 33µH Load: VBATT = 3.7 VDC	-	83	-	%

Note:

6. No external loads should be connected to the LFILT+ net. Any connection of a load to this point may result in errant operation or performance degradation in the device.
7. When VBATT is below this threshold (VB_{LIM}), operation is automatically restricted to SD mode.
8. When operating in HD or FHD mode and the differential input voltage remains below the input level threshold (V_{IN-LDO}) for a period of time (t_{LDO}), the PWM outputs will be powered by the internally generated LDO supply (VLDO).
9. When operating in HD or FHD mode and the differential input voltage is above this input level threshold ($V_{IN-VBATT}$), the PWM outputs will be powered directly from the VBATT supply.
10. Refer to Section 5.5 for more information on Thermal Error functionality.
11. Under Voltage Lockout is the threshold at which a decreasing VBATT supply will disable device operation.

ELECTRICAL CHARACTERISTICS - SD MODE

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
Output Power (Continuous Average)	P_O	THD+N = 1% R_L = 8 Ω (VBATT = 5.0/4.2/3.7 VDC) R_L = 4 Ω (VBATT = 5.0/4.2/3.7 VDC)	- -	1.35/0.95/0.73 2.25/1.58/1.22	- -	W W
		THD+N = 10% R_L = 8 Ω (VBATT = 5.0/4.2/3.7 VDC) R_L = 4 Ω (VBATT = 5.0/4.2/3.7 VDC)	- -	1.67/1.18/0.91 2.82/2.00/1.53	- -	W W
Total Harmonic Distortion + Noise	THD+N	P_O = 1.0 W	-	0.02	-	%
Power Supply Rejection Ratio	PSRR	V_{ripple} = 200 mV_{PP}, AINx AC coupled to GND @ 217 Hz @ 1 kHz	- -	88 82	- -	dB dB
Common-Mode Rejection Ratio	CMRR	V_{ripple} = 1 V_{PP}, f_{ripple} = 217 Hz	-	73	-	dB
Signal to Noise Ratio A-Weighted	SNR_A	Inputs AC Coupled to Ground, Referenced to 1% THD+N (Note 13) GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	 - -	 96 97	 - -	 dB dB
Idle Channel Noise A-Weighted	ICN_A	AIN+ connected to AIN- GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	 - -	 54 49	 - -	 µVrms µVrms
Idle Channel Noise	ICN	AIN+ connected to AIN- GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	 - -	 110 100	 - -	 µVrms µVrms
Frequency Response	FR	20 Hz to 20 kHz	-0.1	0	0.4	dB
Total Group Delay	GD		-	6	-	µs
Output Switching Frequency	f_{sw1}		-	192	-	kHz
Idle Current Draw (Note 12)	I_{IDLE}	AIN+ connected AIN-, No Output Load VBATT = 5.0 VDC VBATT = 4.2 VDC VBATT = 3.7 VDC	 - - -	 1.42 1.31 1.24	 - - -	 mA mA mA
Input Impedance, Single Ended	Z_{IN}	GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	- -	65 100	- -	kΩ kΩ
Input Voltage @ 1 % THD+N	V_{ICLIP}	R_L = 8 Ω (VBATT = 5.0/4.2/3.7 VDC) GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	 - -	 0.85/0.72/0.63 1.70/1.43/1.25	 - -	 Vrms Vrms

ELECTRICAL CHARACTERISTICS - FSD MODE

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
Output Power (Continuous Average)	P_O	THD+N = 1% R_L = 8 Ω (VBATT = 5.0/4.2/3.7 VDC) R_L = 4 Ω (VBATT = 5.0/4.2/3.7 VDC)	- -	1.28/0.90/0.69 2.16/1.51/1.15	- -	W W
		THD+N = 10% R_L = 8 Ω (VBATT = 5.0/4.2/3.7 VDC) R_L = 4 Ω (VBATT = 5.0/4.2/3.7 VDC)	- -	1.65/1.17/0.90 2.76/1.95/1.51	- -	W W
Total Harmonic Distortion + Noise	THD+N	P_O = 1.0 W	-	0.10	-	%
Power Supply Rejection Ratio	PSRR	V_{ripple} = 200 mV_{PP}, AINx AC coupled to GND @ 217 Hz @ 1 kHz	- -	88 80	- -	dB dB
Common-Mode Rejection Ratio	CMRR	V_{ripple} = 1 V_{PP}, f_{ripple} = 217 Hz	-	71	-	dB
Signal to Noise Ratio A-Weighted	SNR_A	Inputs AC Coupled to Ground, Referenced to 1% THD+N (Note 13) GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	 - -	 80 80	 - -	 dB dB
Idle Channel Noise A-Weighted	ICN_A	AIN+ connected to AIN- GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	 - -	 300 290	 - -	 µVrms µVrms
Idle Channel Noise	ICN	AIN+ connected to AIN- GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	 - -	 570 550	 - -	 µVrms µVrms
Frequency Response	FR	20 Hz to 20 kHz	-4.0	0	0.5	dB
Total Group Delay	GD		-	14	-	µs
Output Switching Frequency	f_{sw2}		-	76	-	kHz
Idle Current Draw (Note 12)	I_{IDLE}	AIN+ connected AIN-, No Output Load VBATT = 5 VDC VBATT = 4.2 VDC VBATT = 3.7 VDC	 - - -	 1.07 1.01 0.97	 - - -	 mA mA mA
Input Impedance, Single Ended	Z_{IN}	GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	- -	160 250	- -	kΩ kΩ
Input Voltage @ 1 % THD+N	V_{ICLIP}	R_L = 8 Ω (VBATT = 5.0/4.2/3.7 VDC) GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	 - -	 0.83/0.69/0.61 1.65/1.38/1.21	 - -	 Vrms Vrms

Note:

12. Idle Current Draw (I_{IDLE}) is specified without any output filtering. Refer to Section 5.3 on page 17 for information on output filtering.

ELECTRICAL CHARACTERISTICS - HD MODE

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
Output Power (Continuous Average)	P_O	THD+N = 1% R_L = 8 Ω (VBATT = 5.0/4.2/3.7 VDC) R_L = 4 Ω (VBATT = 5.0/4.2/3.7 VDC)	- -	1.34/0.94/0.73 2.25/1.58/1.22	- -	W W
		THD+N = 10% R_L = 8 Ω (VBATT = 5.0/4.2/3.7 VDC) R_L = 4 Ω (VBATT = 5.0/4.2/3.7 VDC)	- -	1.67/1.18/0.91 2.83/2.00/1.53	- -	W W
Total Harmonic Distortion + Noise	THD+N	P_O = 1.0 W	-	0.02	-	%
Power Supply Rejection Ratio	PSRR	V_{ripple} = 200 mV_{PP}, AINx AC coupled to GND @ 217 Hz @ 1 kHz	- -	88 86	- -	dB dB
Common-Mode Rejection Ratio	CMRR	V_{ripple} = 1 V_{PP}, f_{ripple} = 217 Hz	-	73	-	dB
Signal to Noise Ratio A-Weighted	SNR_A	Inputs AC Coupled to Ground, Referenced to 1% THD+N (Note 13) GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	 - -	 97 98	 - -	 dB dB
Idle Channel Noise A-Weighted	ICN_A	AIN+ connected to AIN- GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	 - -	 49 43	 - -	 µVrms µVrms
Idle Channel Noise	ICN	AIN+ connected to AIN- GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	 - -	 86 83	 - -	 µVrms µVrms
Frequency Response	FR	20 Hz to 20 kHz	-0.1	0	0.4	dB
Total Group Delay	GD		-	6	-	µs
Output Switching Frequency	f_{sw1}		-	192	-	kHz
Idle Current Draw (Note 14)	I_{IDLE}	AIN+ connected AIN-, No Output Load VBATT = 5 VDC VBATT = 4.2 VDC VBATT = 3.7 VDC	 - - -	 1.11 1.06 1.03	 - - -	 mA mA mA
Input Impedance, Single Ended	Z_{IN}	GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	- -	65 100	- -	kΩ kΩ
Input Voltage @ 1 % THD+N	V_{ICLIP}	R_L = 8 Ω (VBATT = 5.0/4.2/3.7 VDC) GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	 - -	 0.85/0.71/0.63 1.70/1.42/1.25	 - -	 Vrms Vrms

ELECTRICAL CHARACTERISTICS - FHD MODE

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
Output Power (Continuous Average)	P_O	THD+N = 1% R_L = 8 Ω (VBATT = 5.0/4.2/3.7 VDC) R_L = 4 Ω (VBATT = 5.0/4.2/3.7 VDC)	- -	1.28/0.89/0.68 2.17/1.51/1.15	- -	W W
		THD+N = 10% R_L = 8 Ω (VBATT = 5.0/4.2/3.7 VDC) R_L = 4 Ω (VBATT = 5.0/4.2/3.7 VDC)	- -	1.65/1.16/0.90 2.76/1.95/1.51	- -	W W
Total Harmonic Distortion + Noise	THD+N	P_O = 1.0 W	-	0.10	-	%
Power Supply Rejection Ratio	PSRR	V_{ripple} = 200 mV_{PP}, AINx AC coupled to GND @ 217 Hz @ 1 kHz	- -	89 85	- -	dB dB
Common-Mode Rejection Ratio	CMRR	V_{ripple} = 1 V_{PP}, f_{ripple} = 217 Hz	-	71	-	dB
Signal to Noise Ratio A-Weighted	SNR_A	Inputs AC Coupled to Ground, Referenced to 1% THD+N (Note 13) GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	 - -	 93 94	 - -	 dB dB
Idle Channel Noise A-Weighted	ICN_A	AIN+ connected to AIN- GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	 - -	 71 63	 - -	 µVrms µVrms
Idle Channel Noise	ICN	AIN+ connected to AIN- GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	 - -	 125 115	 - -	 µVrms µVrms
Frequency Response	FR	20 Hz to 20 kHz	-4.0	0	0.5	dB
Total Group Delay	GD		-	14	-	µs
Output Switching Frequency	f_{sw1}	Input level below V_{IN-LDO}	-	192	-	kHz
Output Switching Frequency	f_{sw2}	Input level above $V_{IN-VBATT}$	-	76	-	kHz
Idle Current Draw (Note 14)	I_{IDLE}	AIN+ connected AIN-, No Output Load VBATT = 5 VDC VBATT = 4.2 VDC VBATT = 3.7 VDC	 - - -	 1.11 1.06 1.03	 - - -	 mA mA mA
Input Impedance, Single Ended	Z_{IN}	GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	- -	160 250	- -	kΩ kΩ
Input Voltage @ 1 % THD+N	V_{ICLIP}	R_L = 8 Ω (VBATT = 5.0/4.2/3.7 VDC) GAIN_SEL = Low (12 dB) GAIN_SEL = High (6 dB)	 - -	 0.83/0.69/0.61 1.65/1.38/1.20	 - -	 Vrms Vrms

Note:

13. SNR_A dB is referenced to the output signal amplitude resulting in the specified output power at THD+N <1%. See "Parameter Definitions" on page 29 for more information.
14. Idle Current Draw (I_{IDLE}) is specified without any output filtering. Refer to Section 5.3 on page 17 for information on output filtering. At idle, the output devices will switch at the same rate in HD and FHD mode. FHD only changes the output switching frequency when the input levels are above the "Input Level for Entering VBATT Operation in HD/FHD Modes ($V_{IN-VBATT}$) given in "Electrical Characteristics - All Operational Modes" on page 9.

DIGITAL INTERFACE SPECIFICATIONS & CHARACTERISTICS

Parameters	Symbol	Min	Max	Units
Input Leakage Current	I_{in}	-	±10	µA
Input Capacitance		-	10	pF
$\overline{SD}$ Pulse Width Requirement		1	-	ms
Logic I/Os (Applicable to GAIN_SEL, MODE, and $\overline{SD}$)				
High-Level Input Voltage	V_{IH}	0.7•VBATT	-	V
Low-Level Input Voltage	V_{IL}	-	0.3•VBATT	V

POWER-UP & POWER-DOWN CHARACTERISTICS

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
Start-Up Time (Note 15)	t_{start}	After “Low” to “High” $\overline{SD}$ Pin transition edge	-	18	-	ms
Zero Crossing Power-Up Timeout	$t_{timeout}$	No audio input applied	-	25	-	ms
Power-Down Time	t_{off}	After “High” to “Low” $\overline{SD}$ Pin transition edge	-	1	-	ms

Note:

15. Start-Up Time (t_{start}) refers to the internal start-up time from when $\overline{SD}$ is released to when the device is ready to activate the PWM outputs. The total power-up time from $\overline{SD}$ release to the PWM outputs becoming active will vary based on the input signal, not exceeding the Start-Up Time + Zero Crossing Power-Up Timeout (t_{start} + $t_{timeout}$). For more information refer to Section 5.4.

5. APPLICATIONS

5.1 MODE Descriptions

The CS35L00 device can be operated in one of four operating modes, determined by the MODE pin and the LFILT+ pin. The four modes of operation are Standard Class-D operation (SD), Reduced Frequency Standard Class-D operation (FSD), Hybrid Class-D operation (HD), and Reduced Frequency Hybrid Class-D operation (FHD). Each of these modes can be leveraged to optimize different performance criteria in an array of applications.

		MODE connected to:	
		GND	VBATT
LFILT+ connected to:	VBATT	Reduced Frequency Class-D Mode (FSD)	Standard Class-D Mode (SD)
	Filter Cap to Ground	Reduced Frequency Hybrid Class-D Mode (FHD)	Hybrid Class-D Mode (HD)

Table 1. LFILT+ and MODE Operation Configurations

5.1.1 Standard Class D Modes of Operation

5.1.1.1 SD Mode

Standard Class-D (SD) mode supports full audio bandwidth with very good SNR and THD+N performance. This mode of operation is characterized by a traditional closed loop, analog ΔΣ modulated Class-D amplifier. With an output switching frequency of 192 kHz, this mode ensures flat frequency response across the entire audio frequency range.

5.1.1.2 FSD Mode

The Reduced Frequency Class-D (FSD) mode provides competitive audio performance and a reduction in radiated emissions by decreasing the switching frequency of the output devices to 76 kHz. This reduction in switching frequency reduces the high frequency energy being created by the output switching events. Idle channel noise is slightly higher in this mode of operation than SD mode, with the trade-off being better EMI performance and power consumption.

5.1.2 Hybrid Class D Modes of Operation

Hybrid Class-D and Reduced Frequency Hybrid Class-D modes of operation allows the rail voltage for the output devices to switch between a high voltage net and a low voltage net depending on the audio content being amplified. This is explained in more detail in Section 5.1.2.1 and Section 5.1.2.2. Operation in these modes requires that the voltage present on the VBATT pin be above the level listed as “VBATT Limit for HD/FHD Mode (VB_{LIM})” in “Electrical Characteristics - All Operational Modes” on page 9. If it is not, HD and FHD modes of operation of the device will automatically be disabled and operation will be limited to the SD mode of operation.

In both HD and FHD mode, the value of the capacitance connected to the LFILT+ pin must not exceed 4.7 µF. If this value is greater than 4.7 µF, it will prevent the rail voltage of the output devices from transitioning properly between VBATT and the internal LDO.

5.1.2.1 HD Mode

Hybrid Class-D mode (HD) provides competitive analog performance with a substantial reduction in idle power dissipation and radiation emissions. In this mode, the output switches at 192 kHz and a secondary supply is derived from VBATT using an internal 1.0 VDC low drop-out linear regulator (LDO). When the output signal is at a low amplitude, the Class-D output stage begins to switch from the lower rail voltage created by the internal LDO. This not only decreases idle power consumption when output capacitors are used, but also reduces electromagnetic emissions by reducing the amplitude of the square waves being created at the output of the CS35L00 when operating at low amplitude or idle power.

5.1.2.2 FHD Mode

The Reduced Frequency Hybrid Class-D (FHD) mode provides the best overall EMI performance and the lowest power consumption with slightly decreased frequency response near the top frequency range of the audio band, for high amplitude signals. In this mode of operation, the output switching frequency is reduced to 76 kHz during high amplitude transients on the output. The threshold at which this transition from 192 kHz to 76 kHz switching rate occurs is given as the Input Level Threshold for FHD Operation in “Electrical Characteristics - FHD Mode” on page 13. Combined with the lower amplitude switching offered by the Hybrid design, this reduction in switching energy dramatically reduces the emissions levels of the output stage and its associated components.

5.2 Reducing the Gain with External Series Resistors

If necessary, it is possible to decrease the gain of the CS35L00 by adding series resistors to the audio input signal as is shown in Figure 4 below.

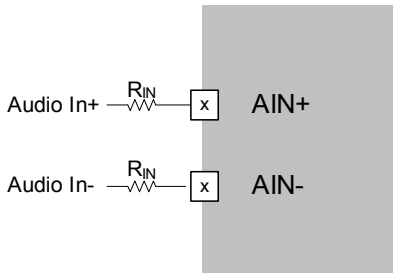


Figure 4. Adjusting Gain via External Series Resistance

If input resistors are added, the new gain of the amplifier can be determined by the following equation:

$$A_{V(adjusted)} = A_V - 20 \times \log\left(\frac{Z_{IN}}{Z_{IN} + Z_{EXT}}\right)$$

Where:

$A_{V(adjusted)}$ = The new, adjusted gain of the system

Z_{IN} = Input impedance of the device being used (See "Electrical Characteristics - SD Mode" on page 10, "Electrical Characteristics - FSD Mode" on page 11, "Electrical Characteristics - HD Mode" on page 12, or "Electrical Characteristics - FHD Mode" on page 13 for this value.)

Z_{EXT} = Value of the resistor added in series with the inputs

A_V = Original gain of the device being used (See "Electrical Characteristics - All Operational Modes" on page 9 for this value.)

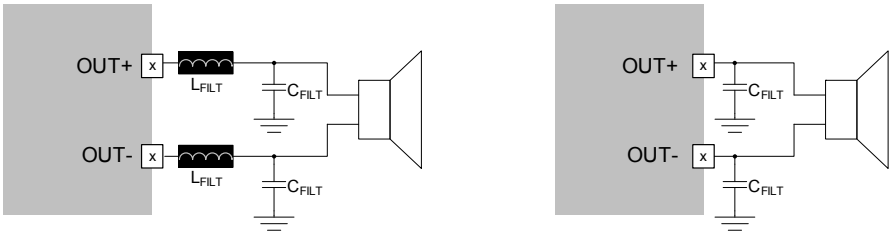
5.3 Output Filtering with the CS35L00

The CS35L00 is specifically designed to minimize radiated electromagnetic interference (EMI) signals. All of the devices are capable of meeting all stated data sheet performance numbers with no special filtering required. Additionally, the device has shown to be below the compliance limits of both FCC and CISPR testing with no external filtering required.

Ultimately, compliance with any radiated emissions requirements depends significantly on the entire system under test. In applications where system-level trade-offs, such as compromised component layout or lengthy speaker wires, have increased emissions levels, a passive output filter can be added to the outputs of the device in order to decrease EMI levels.

5.3.1 Reduced Filter Order with the CS35L00

In applications which require an output filter, the unique design of the CS35L00 allows a much smaller, less expensive output filter to be used than what is normally found in Class D amplifiers. In contrast to a second order filter implemented with a series inductive element (traditional inductor or ferrite beads) and a shunt capacitive element, basic filtering for the CS35L00 is accomplished by a single-order capacitive element attached to the OUTx terminals. This is highlighted in Figure 5 below. Of course, if the system requires more aggressive filtering, a ferrite bead can be added in series with the outputs to further attenuate system level noise.



Traditional 2nd Order Optional Filtering

CS35L00's Minimized Optional Filtering

Figure 5. Optional Output Filter Components

5.3.2 Filter Component Selection

Usually, the need for output filtering is determined after the system under test has failed EMI testing. During this testing, problem frequencies are easily identified by the peaks which appear in the spectral plots gathered in the EMI testing.

Selection of the filter components should ensure that shunt elements (i.e. C_{FILT} in Figure 5 on page 17) present a very low impedance at the frequency corresponding to the tallest peak in the spectral plot. If needed, series components such as ferrite beads (i.e. L_{FILT} in Figure 5 on page 17) should be chosen to present a very high impedance at the frequency corresponding to the tallest peak in the spectral plot.

Careful attention should be paid to the current carrying capabilities of any included ferrite beads and the impedance of the ferrite beads in the audio band. A proper trade-off in ferrite bead selection is one that

allows the ferrite bead to sufficiently attenuate the problematic high-frequency emissions without compromising audio performance.

5.3.3 Output Filter Power Dissipation Considerations

In systems without inductive series elements like inductors or ferrite beads, power losses in the output filter are equal to the switching losses that occur in the system due to the cyclical charging and discharging of capacitors connected to the amplifier outputs. In systems that require an inductive series element, conducted losses also occur due to the series impedance added to the output path.

5.3.3.1 Conduction Losses for All Modes of Operation

For all modes of operation (SD, FSD, HD, and FHD), conduction losses are governed by the following equation:

$$P = I^2 Z$$

Where:

P = Power dissipated in the series impedance.

I = RMS AC output current

Z = impedance of the series element at the frequency of the AC current

This equation neglects any series impedances presented by the PCB traces or speaker wires in the output path.

5.3.3.2 Switching Losses in SD/FSD Mode

Switching losses in SD/FSD Mode are governed by the equation

$$P = \frac{1}{2} C V^2 f$$

Where:

P = Power dissipated in the capacitor (neglecting parasites).

C = Value of filtering capacitor

V = Peak voltage developed across the capacitor

f = Switching frequency of the outputs

These calculations are straightforward, as the peak voltage is simply the voltage level attached to VBATT, the capacitor is the value of capacitor that has been added for filtering (neglecting parasitic board capacitances), and the frequency is 192 kHz for SD and 76 kHz for FSD, respectively.

5.3.3.3 Switching Losses in HD/FHD.

Many factors affect the switching losses when the device is operated in HD/FHD mode. These factors include the frequency of the content being amplified, the voltage level of VBATT, and the amplitude of the output signal will factor into both the voltage presented across the capacitors and the frequency at which the capacitors are charged or discharged.

Static signals (i.e. sine waves at a fixed amplitude) are easier to consider than are dynamic signals (i.e. musical content), as they are governed by the same equation as that listed in Section 5.3.3.1 and Section 5.3.3.2 on page 18. Modifications to that equation are limited to the voltage term (V) and the frequency term (f), depending on whether the static input signal amplitude is causing the output devices to switch at 76 kHz or 192 kHz, and to operate off of the VBATT supply or off of the internally generated LDO.

It is important to note that the HD and FHD modes offer significant improvement over traditional Class D in idle power dissipation when an external output filter is necessary. This is because the voltage term (V) is significantly reduced in HD and FHD mode. As can be seen in the equation, this is notable because reduction in the operating voltage reduces power losses not linearly, but instead *exponentially*- due to the voltage squared term (V^2). It is also notable that when operated at high output levels, FHD modes also offers unique improvement in output filter losses, due to reducing the switching frequency (f) at higher output levels.

5.4 Power-Up and Power-Down

When pulled to a logic low state, the $\overline{SD}$ pin tristates the outputs and shuts down the CS35L00 device, putting it into a low power mode.

5.4.1 Recommended Power-Up Sequence

1. With the $\overline{SD}$ pin pulled low, apply power to the CS35L00 and wait for the power supply to be stable.
2. Set the $\overline{SD}$ pin high to begin normal operation.

5.4.1.1 Zero Crossing on Power-Up Functionality

The CS35L00 implements an input-signal zero-crossing detection function that is enabled during power-up. This function is designed to prevent audible artifacts and eliminate any need to mute the amplifier's input audio signal during the power-up process.

After a minimum start-up time of t_{start}, the CS35L00 will begin to detect input-signal zero-crossings. The amplifier will then enable its switching outputs at the time of the first detected input-signal zero-crossing transition. If no input-signal zero-crossing is detected before $t_{timeout}$, the zero-crossing function will time-out and the outputs will begin switching immediately.

Both t_{start} and $t_{timeout}$ are specified in "Power-Up & Power-Down Characteristics" on page 14.

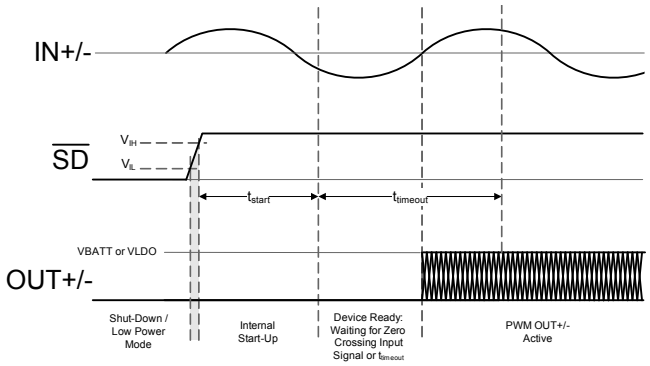


Figure 6. Power-Up Timing with Input Zero-Crossing

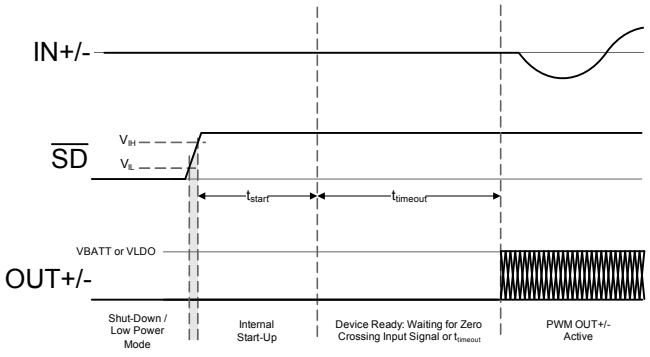


Figure 7. Power Up Timing without Input Zero-Crossing

5.4.2 Recommended Power-Down Sequence

1. Mute the audio supplied to the CS35L00.
2. Pull the $\overline{SD}$ pin low in order to reset the device and put it into the low power mode.
3. The power supply to the CS35L00 can now be removed.

5.5 Over Temperature Protection

The CS35L00 is internally protected against thermal overload. Built in die temperature sensing circuitry monitors the die temperature and will place the device into shut-down if thermal overload occurs. A thermal overload is characterized by the die temperature reaching the Thermal Error Threshold (T_{TE}) at which time the outputs will tristate and shut down.

If the device has entered into shut-down due to a thermal overload, the die temperature must remain below the Thermal Error Threshold (T_{TE}) for the time specified by the Thermal Error Retry Time (R_{TE}) in order for the device to automatically return to normal operation.

Both T_{TE} and R_{TE} are specified in "Electrical Characteristics - All Operational Modes" on page 9.

6. TYPICAL PERFORMANCE PLOTS

Test Conditions (unless otherwise specified): GND = 0 V; All voltages with respect to ground; A_V = 6 dB; Input signal = 997 Hz differential sine wave; T_A = 25°C; VBATT = 5.0 V; R_L = 8 Ω; 10 Hz to 20 kHz measurement bandwidth; Measurements taken with AES17 measurement filter and Audio Precision AUX-0025 passive filter.

6.1 SD Mode Typical Performance Plots

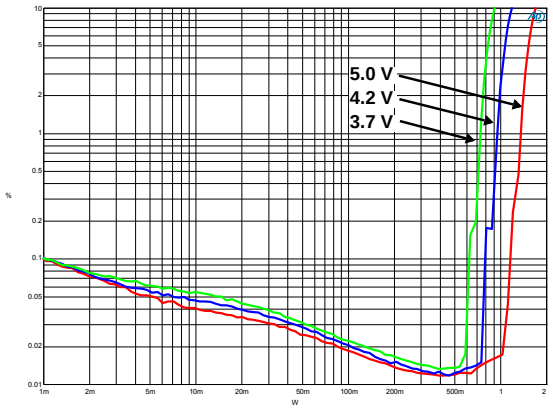


Figure 8. THD+N vs. Output Power - SD Mode
R_L = 8 Ω

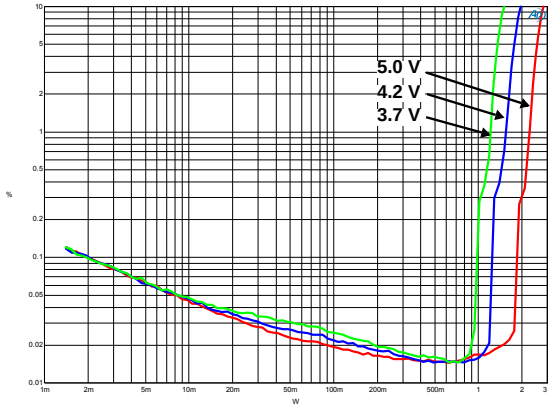


Figure 9. THD+N vs. Output Power - SD Mode
R_L = 4 Ω

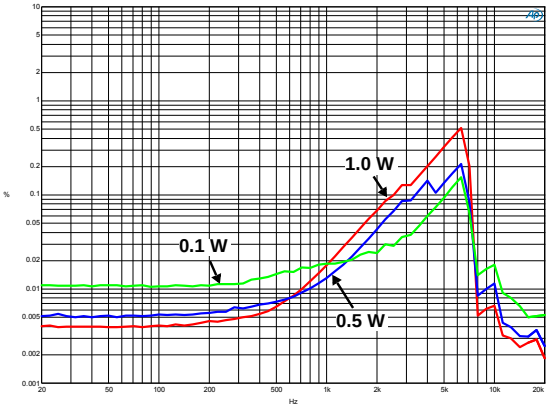


Figure 10. THD+N vs. Frequency - SD Mode
VBATT = 5.0 V

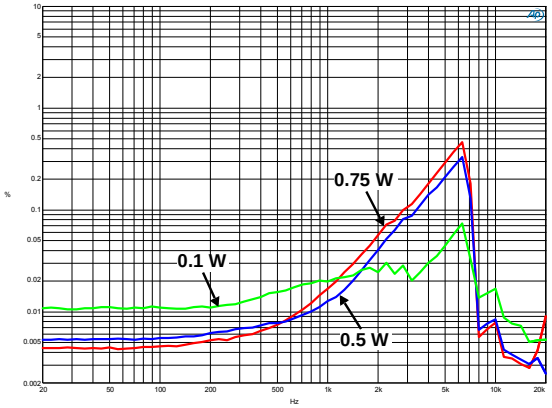


Figure 11. THD+N vs. Frequency - SD Mode
VBATT = 4.2 V

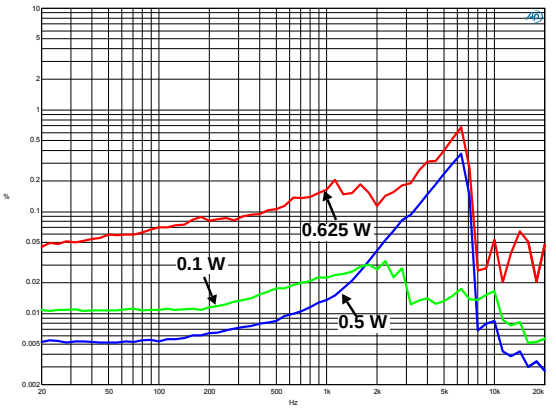


Figure 12. THD+N vs. Frequency - SD Mode
VBATT = 3.7 V

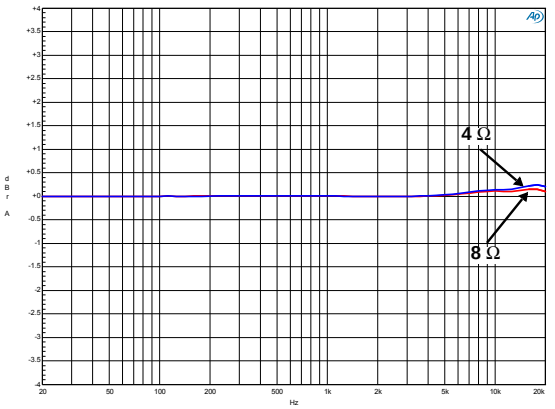


Figure 13. Frequency Response - SD Mode

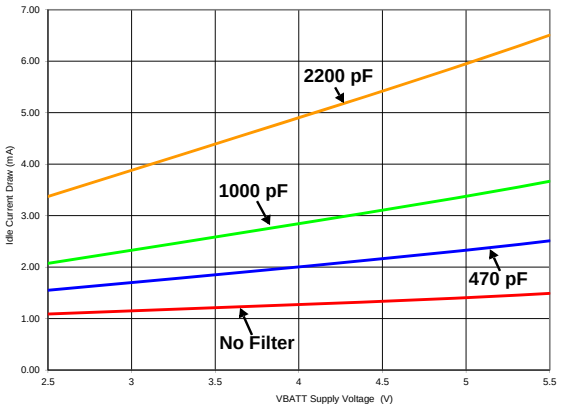


Figure 14. Idle Current Draw vs. VBATT - SD Mode
R_L = 8 Ω + 33 µH (Note 16)

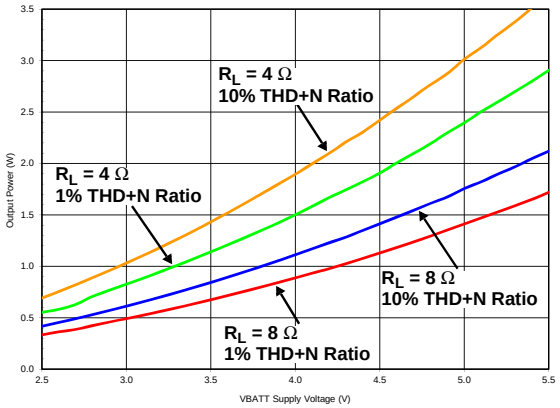


Figure 15. Output Power vs. VBATT - SD Mode

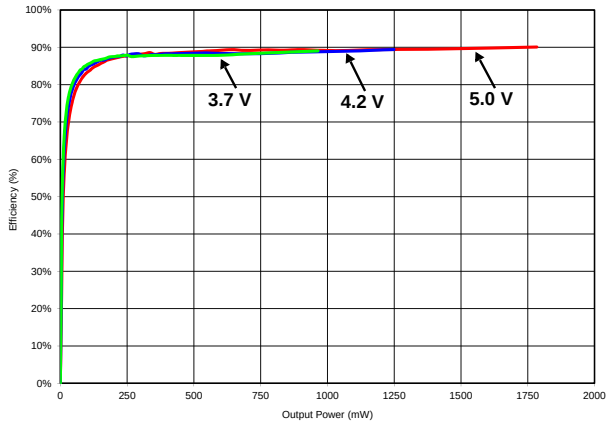


Figure 16. Efficiency vs. Output Power - SD Mode
R_L = 8 Ω + 33 µH

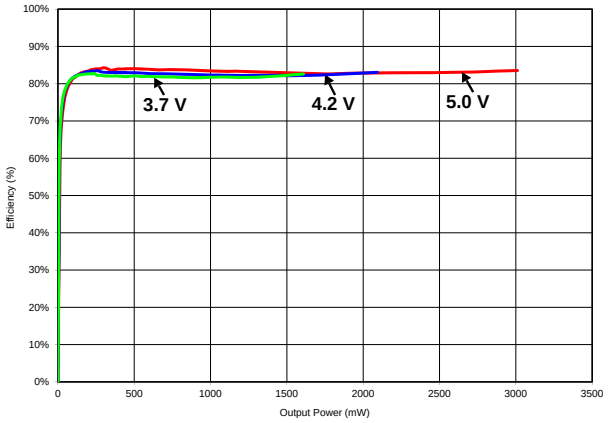


Figure 17. Efficiency vs. Output Power - SD Mode
R_L = 4 Ω + 33 µH

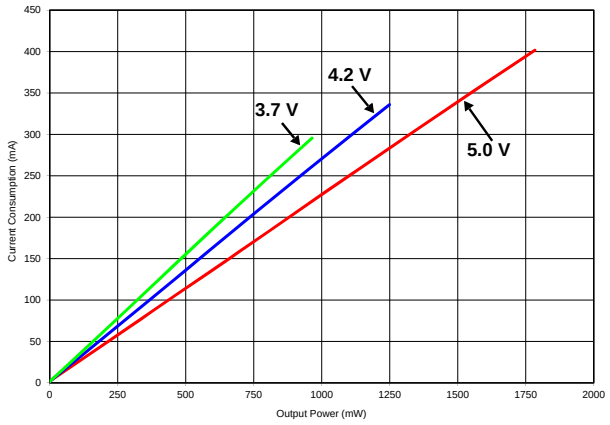


Figure 18. Supply Current vs. Output Power - SD Mode
R_L = 8 Ω + 33 µH

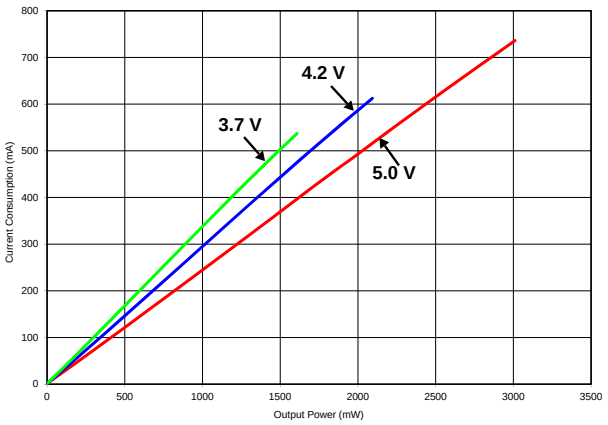


Figure 19. Supply Current vs. Output Power - SD Mode
R_L = 4 Ω + 33 µH

Note:

16. "Idle Current Draw vs. VBATT - SD Mode" capacitor values refer to C_{FILT} when configured as the "CS35L00's Minimized Optional Output Filter", shown in Figure 5 on page 17.

6.2 FSD Mode Typical Performance Plots

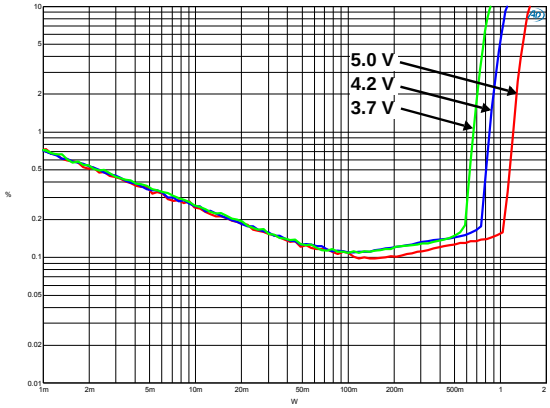


Figure 20. THD+N vs. Output Power - FSD Mode
R_L = 8 Ω

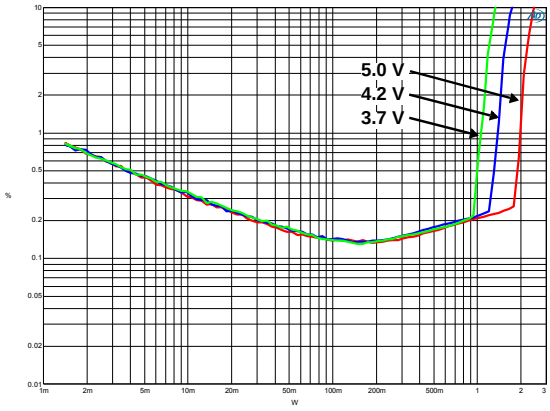


Figure 21. THD+N vs. Output Power - FSD Mode
R_L = 4 Ω

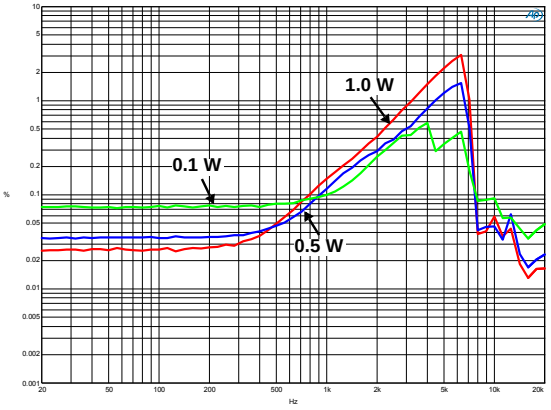


Figure 22. THD+N vs. Frequency - FSD Mode
VBATT = 5.0 V

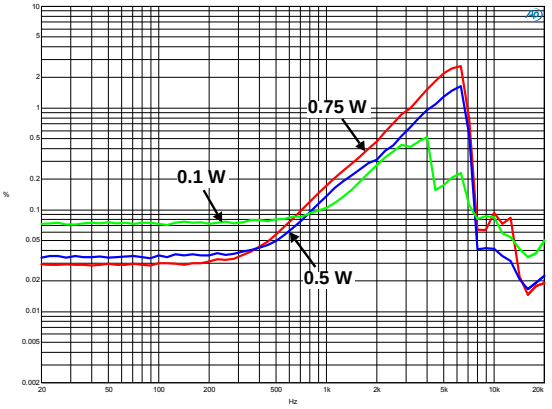


Figure 23. THD+N vs. Frequency - FSD Mode
VBATT = 4.2 V

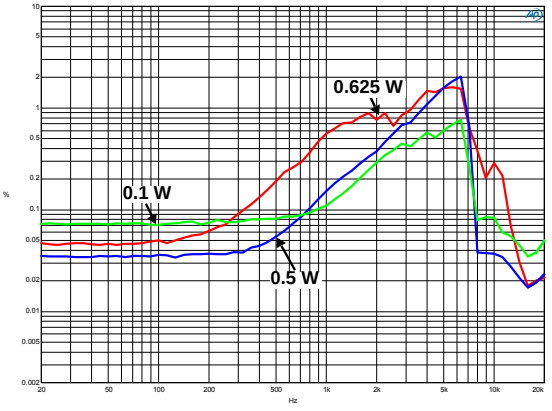


Figure 24. THD+N vs. Frequency - FSD Mode
VBATT = 3.7 V

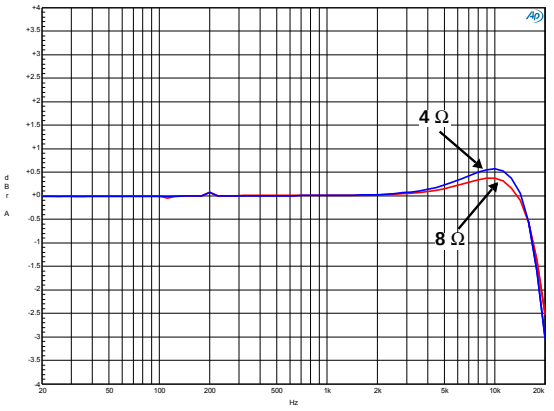


Figure 25. Frequency Response - FSD Mode

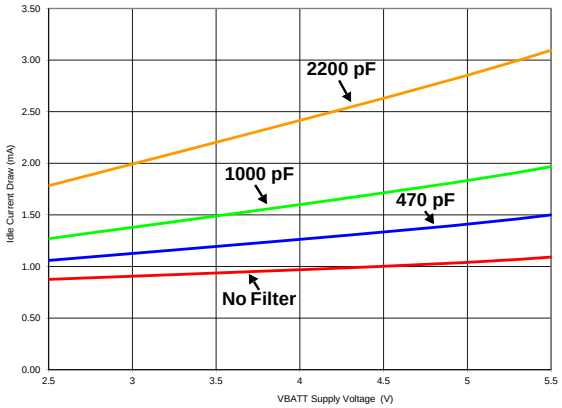


Figure 26. Idle Current Draw vs. VBATT - FSD Mode
R_L = 8 Ω + 33 µH (Note 17)

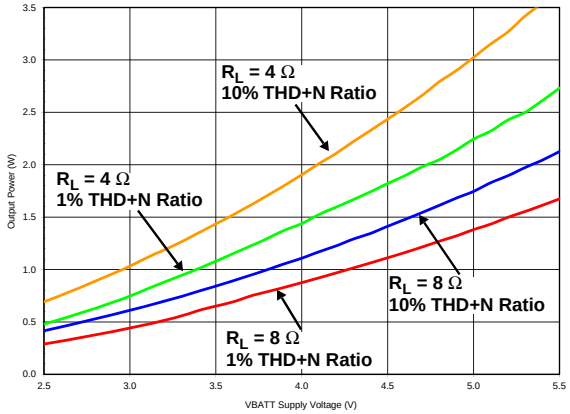


Figure 27. Output Power vs. VBATT - FSD Mode

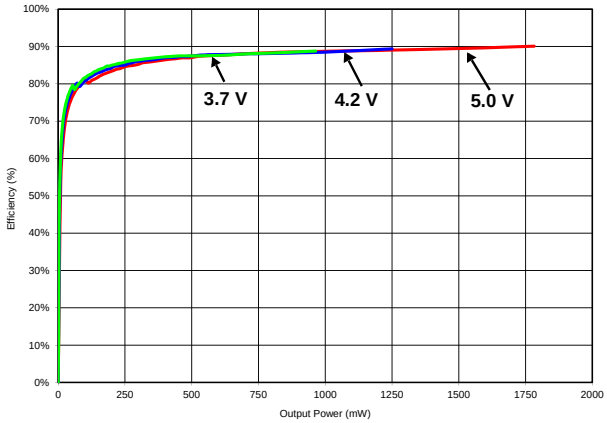


Figure 28. Efficiency vs. Output Power - FSD Mode
R_L = 8 Ω + 33 µH

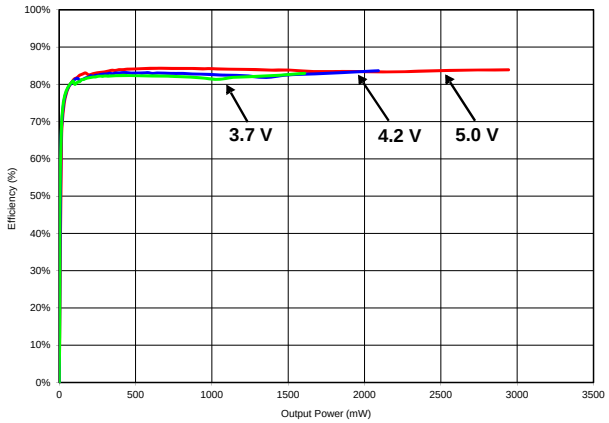


Figure 29. Efficiency vs. Output Power - FSD Mode
R_L = 4 Ω + 33 µH

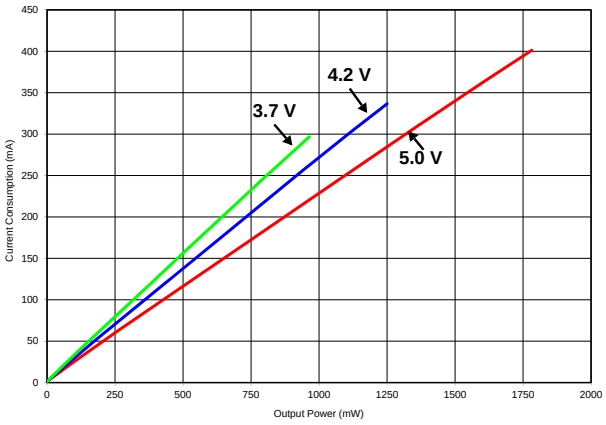


Figure 30. Supply Current vs. Output Power - FSD Mode
R_L = 8 Ω + 33 µH

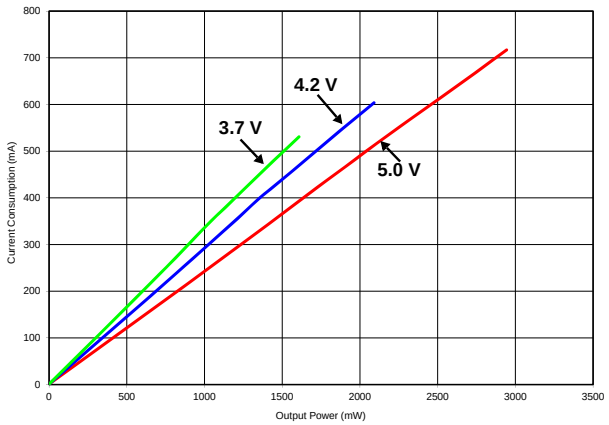


Figure 31. Supply Current vs. Output Power - FSD Mode
R_L = 4 Ω + 33 µH

Note:

17. "Idle Current Draw vs. VBATT - FSD Mode" capacitor values refer to C_{FILT} when configured as the "CS35L00's Minimized Optional Output Filter", shown in Figure 5 on page 17.

6.3 HD Mode Typical Performance Plots

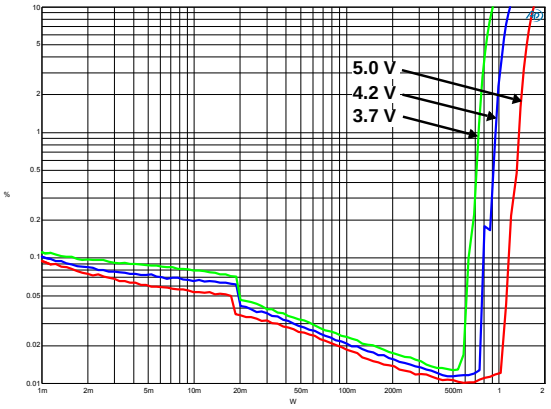


Figure 32. THD+N vs. Output Power - HD Mode
R_L = 8 Ω

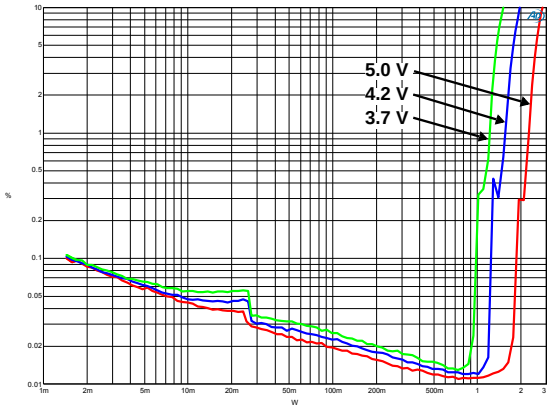


Figure 33. THD+N vs. Output Power - HD Mode
R_L = 4 Ω

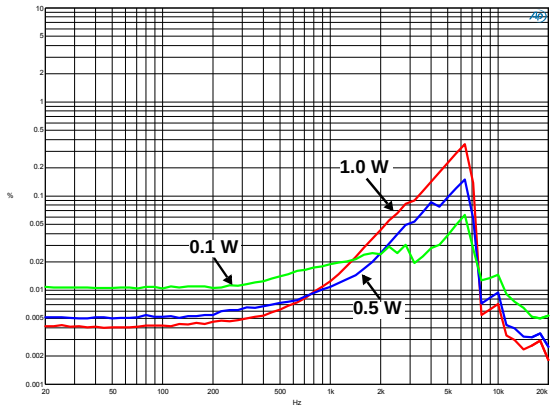


Figure 34. THD+N vs. Frequency - HD Mode
VBATT = 5.0 V

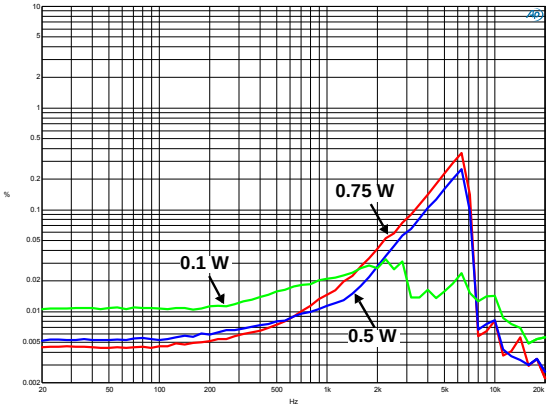


Figure 35. THD+N vs. Frequency - HD Mode
VBATT = 4.2 V

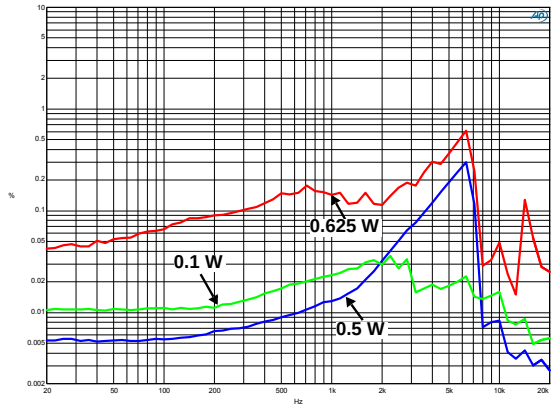


Figure 36. THD+N vs. Frequency - HD Mode
VBATT = 3.7 V

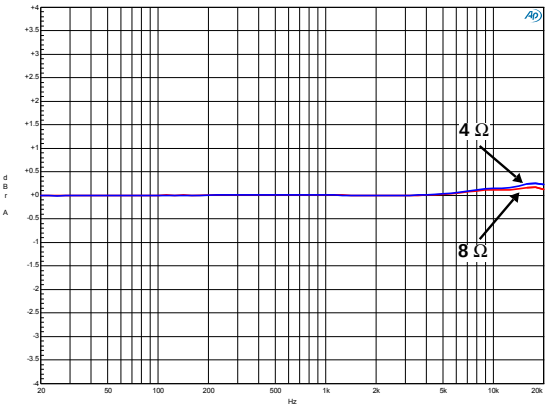


Figure 37. Frequency Response- HD Mode

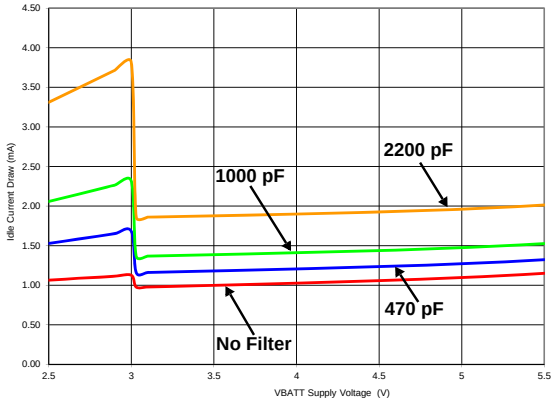


Figure 38. Idle Current Draw vs. VBATT - HD Mode
R_L = 8 Ω + 33 µH (Note 18)

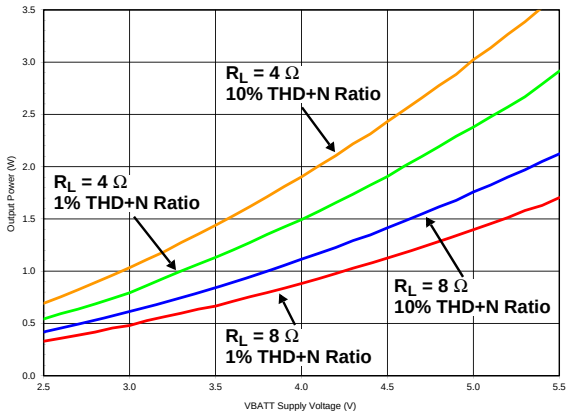


Figure 39. Output Power vs. VBATT - HD Mode

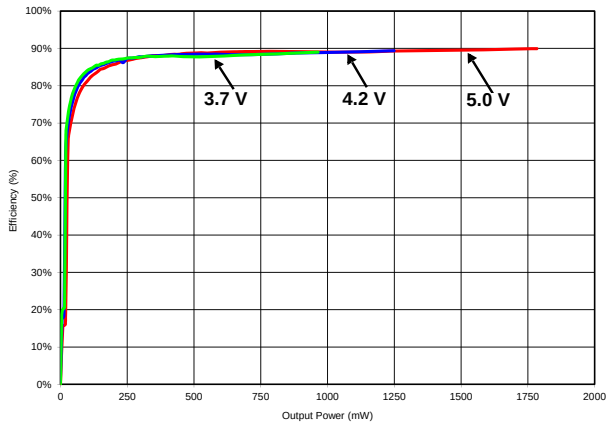


Figure 40. Efficiency vs. Output Power - HD Mode
R_L = 8 Ω + 33 µH

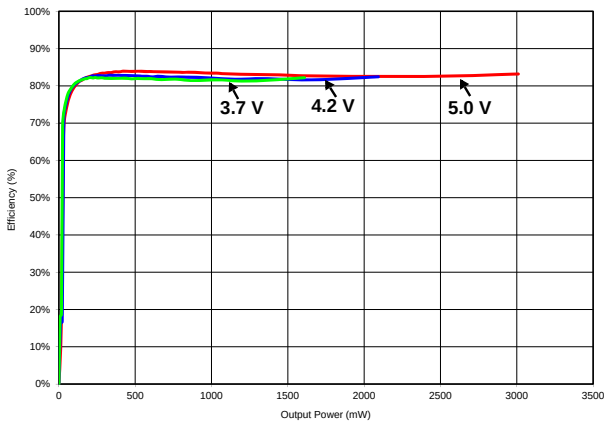


Figure 41. Efficiency vs. Output Power - HD Mode
R_L = 4 Ω + 33 µH

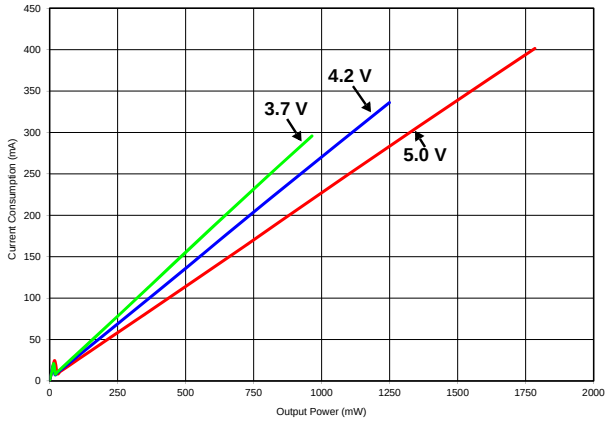


Figure 42. Supply Current vs. Output Power - HD Mode
R_L = 8 Ω + 33 µH

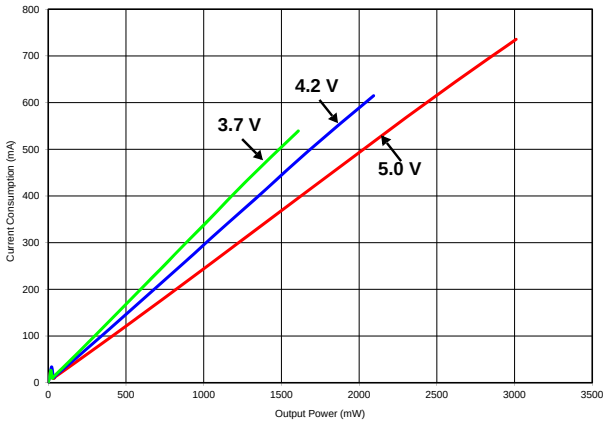


Figure 43. Supply Current vs. Output Power - HD Mode
R_L = 4 Ω + 33 µH

Note:

18. "Idle Current Draw vs. VBATT - HD Mode" capacitor values refer to C_{FILT} when configured as the "CS35L00's Minimized Optional Output Filter", shown in Figure 5 on page 17. When VBATT is below "VBATT Limit for HD/FHD Mode" (VB_{LIM}), operation is restricted to SD Mode.

6.4 FHD Mode Typical Performance Plots

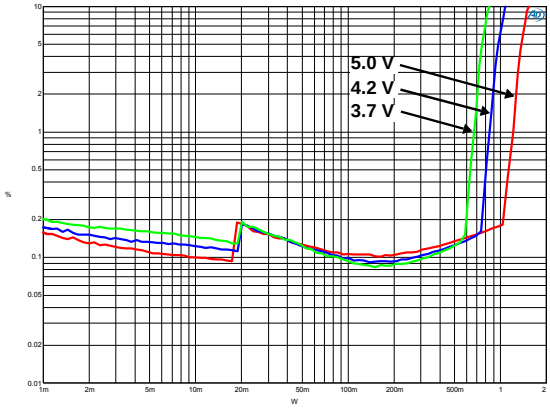


Figure 44. THD+N vs. Output Power - FHD Mode
R_L = 8 Ω

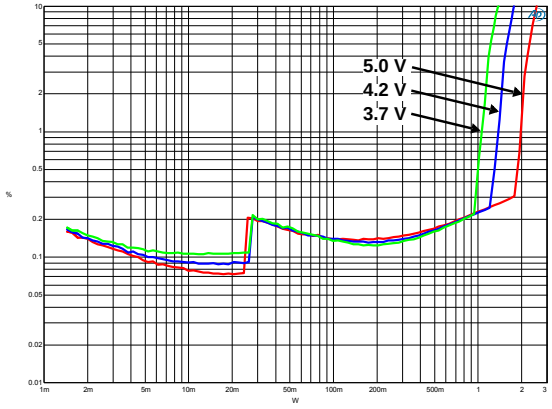


Figure 45. THD+N vs. Output Power - FHD Mode
R_L = 4 Ω

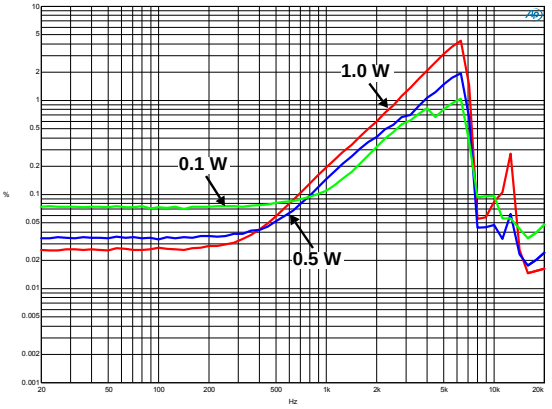


Figure 46. THD+N vs. Frequency - FHD Mode
VBATT = 5.0 V

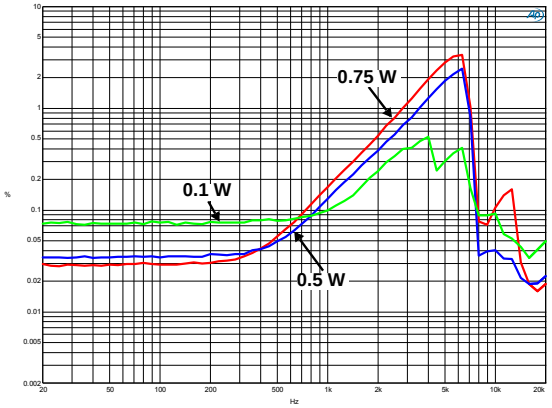


Figure 47. THD+N vs. Frequency - FHD Mode
VBATT = 4.2 V

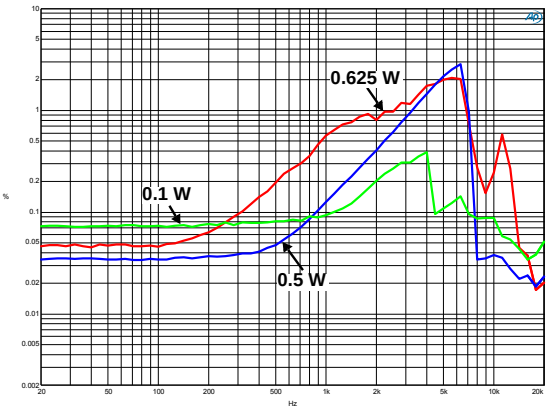


Figure 48. THD+N vs. Frequency - FHD Mode
VBATT = 3.7 V

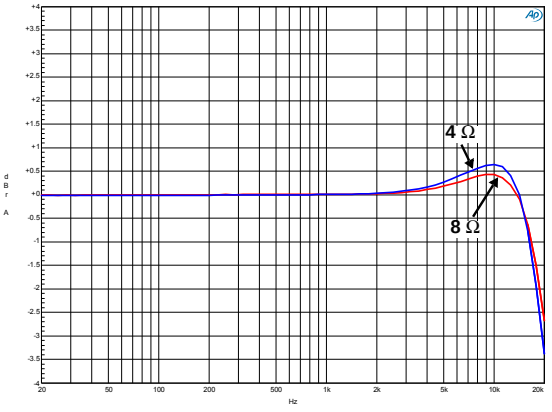


Figure 49. Frequency Response - FHD Mode

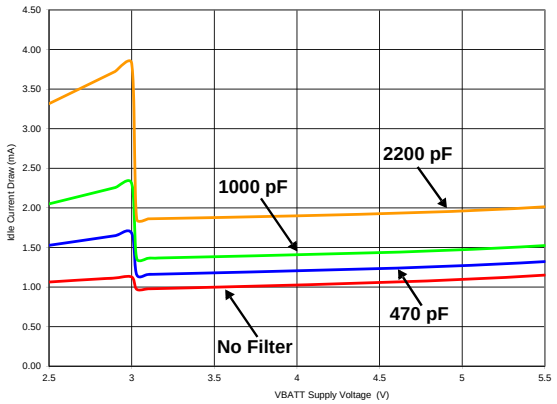


Figure 50. Idle Current Draw vs. VBATT - FHD Mode
R_L = 8 Ω + 33 µH (Note 19)

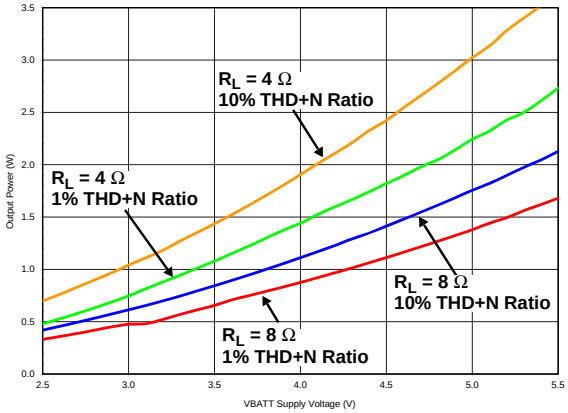


Figure 51. Output Power vs. VBATT - FHD Mode

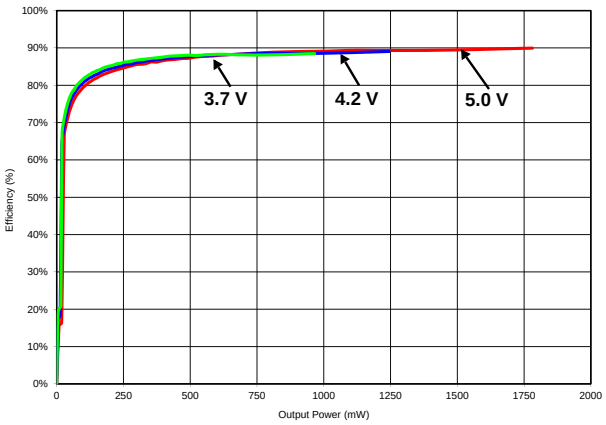


Figure 52. Efficiency vs. Output Power - FHD Mode
R_L = 8 Ω + 33 µH

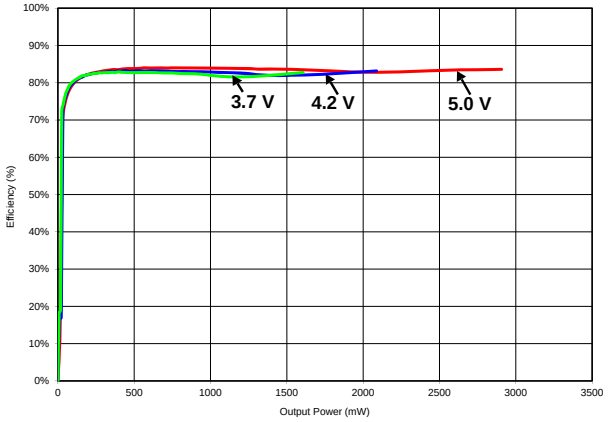


Figure 53. Efficiency vs. Output Power - FHD Mode
R_L = 4 Ω + 33 µH

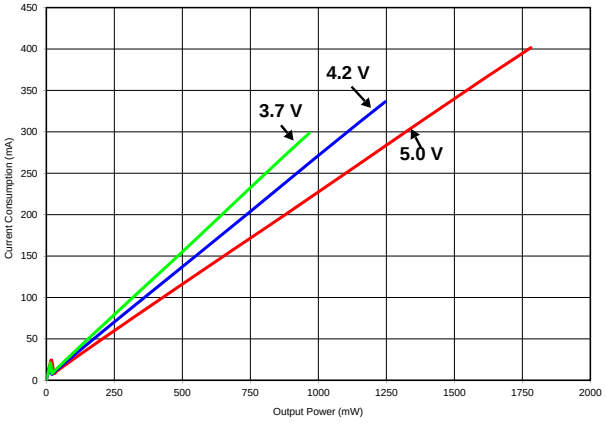


Figure 54. Supply Current vs. Output Power - FHD Mode
R_L = 8 Ω + 33 µH

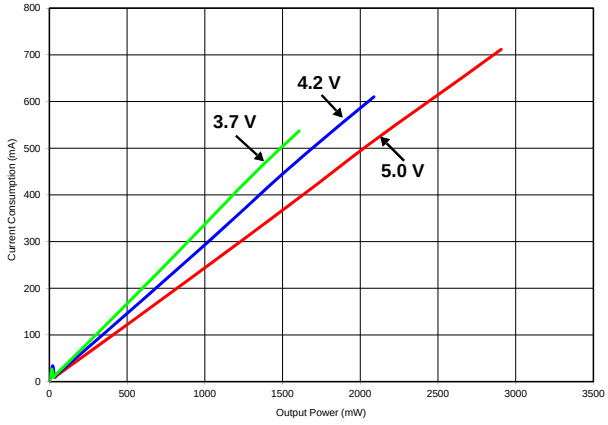


Figure 55. Supply Current vs. Output Power - FHD Mode
R_L = 4 Ω + 33 µH

Note:

19. "Idle Current Draw vs. VBATT - FHD Mode" capacitor values refer to C_{FILT} when configured as the "CS35L00's Minimized Optional Output Filtering" shown in Figure 5 on page 17. When VBATT is below "VBATT Limit for HD/FHD Mode" (VB_{LIM}), operation is restricted to SD Mode.

7. PARAMETER DEFINITIONS

Signal to Noise Ratio (SNR)

The ratio of the RMS value of the output signal, where Pout is equivalent to the specified output power at THD+N<1%, to the RMS value of the noise floor with no input signal applied and measured over the specified bandwidth, typically 20 Hz to 20 kHz. This measurement technique has been accepted by the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

Total Harmonic Distortion + Noise (THD+N)

The ratio of the RMS value of the signal to the RMS sum of all other spectral components over the specified band width (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

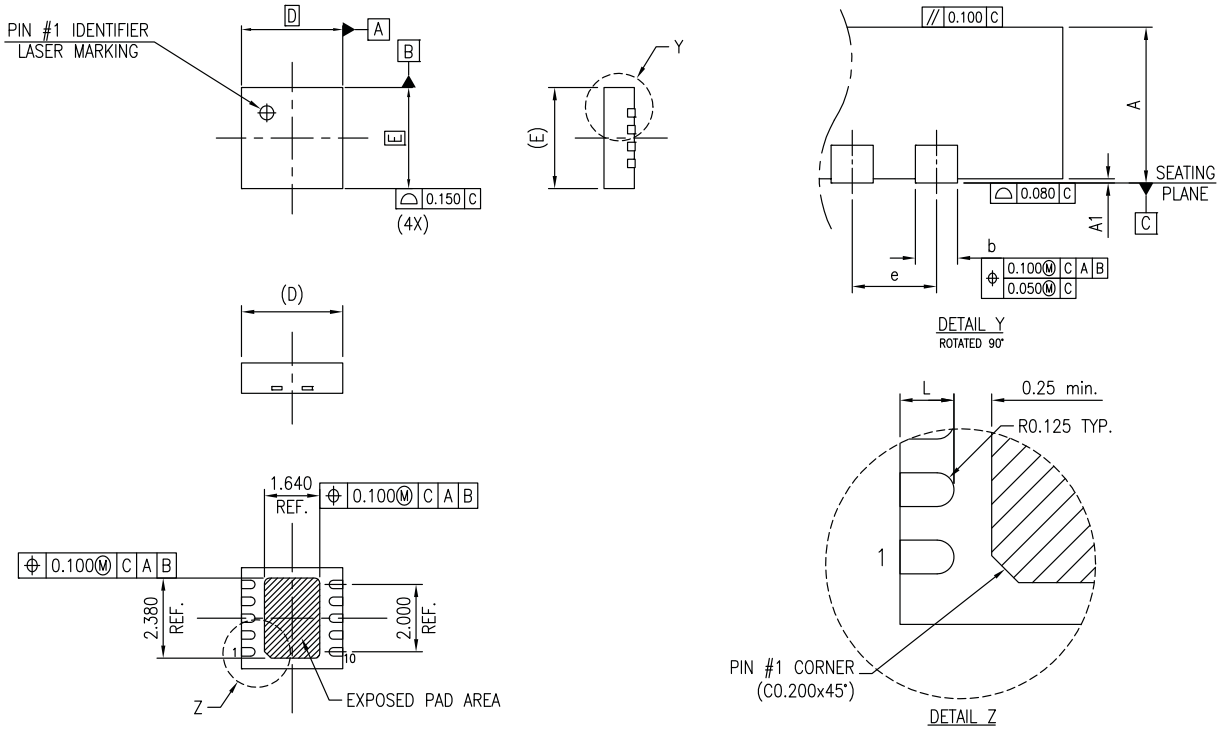
Idle Channel Noise (ICN)

Measure of the signal present on the outputs of the device when no audio signal is presented to the input pins. For this test, both input pins are shorted together, setting the differential signal to them to zero.

8. PACKAGING AND THERMAL INFORMATION

8.1 Package Drawings and Dimensions (Note 20)

10 PIN DFN



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	0.034	0.035	0.037	0.850	0.900	0.950	20
A1	0.000	0.001	0.002	0.000	0.020	0.050	20
D	0.114	0.118	0.122	2.900	3.000	3.100	
E	0.114	0.118	0.122	2.900	3.000	3.100	20
L	0.014	0.016	0.018	0.350	0.400	0.450	20
b	0.008	0.009	0.012	0.200	0.250	0.300	20
e	--	0.019	--	--	0.500	--	20

JEDEC #: MO-220

Controlling Dimension is Millimeters.

Note:

20. Dimensioning and tolerance per ASME Y 14.5M-1994.

8.2 Recommend PCB Footprint and Routing Configuration

To ensure high-yield manufacturability, the PCB footprint for the CS35L00 should be constructed with strict adherence to the specifications given in IPC-610. Departure from this specification significantly increases the probability of solder bridging and other manufacturing defects.

Routing of the traces into and out of the CS35L00 device should also be given consideration to avoid manufacturing issues.

8.3 Package Thermal Performance

Class D amplifiers, though highly efficient, produce heat through the process of amplifying the audio signal. As is well understood, the amount of heat is very small compared to that of traditional Class AB amplifiers. Even so, as power levels increase and package sizes decrease, careful consideration must be given to ensure that thermal energy is removed from the device as efficiently as possible so that its operating temperature is kept under its Over-Temperature Error Threshold.

The thermal impedance, θ_{JA} is a measurement of the impedance to the flow of thermal energy out of the device to the environment surrounding the device. This specification is directly related to the ability of the PCB to which the CS35L00 is attached to transfer the heat from the device. The thermal impedance from the junction of the device to the ambient surrounding the device and the thermal impedance from the device into the PCB is shown in Table 2.

.

Parameter (Note 21), (Note 22)	Symbol	Min	Typical	Max	Units
Junction to Ambient Thermal Impedance	θ_A	-	100	-	°C/Watt
Junction to Printed Circuit Board Thermal Impedance	θ_{PCB}	-	70	-	°C/Watt

Table 2. θ_{JA} Specification for Typical PCB Designs

Note:

21. Test Printed Circuit Board Assembly (PCBA) constructed in accordance with JEDEC standard JESD51-9. Two-signal, two-plane (2s2p) PCB used.
22. Test conducted with still air in accordance with JEDEC standards JESD51, JESD51-2A, and JESD51-8.

8.4 DFN Thermal Pad

The CS35L00 is available in a compact DFN package. The underside of the DFN package reveals a large metal pad that serves as a thermal relief to provide for maximum heat dissipation. This pad must mate with an equally dimensioned copper pad on the PCB and must be electrically connected to PGND. A series of thermal vias should be used to connect this copper pad to one or more larger ground planes on other PCB layers; the copper in these ground planes will act as a heat sink for the CS35L00.

8.4.1 Determining Maximum Ambient Temperature

To determine (to a first order approximation) the maximum ambient temperature in which the CS35L00 will operate, the following equations can be used:

$$T_{op} = \theta_{JA} \times ((1 - \eta) \times P_{max})$$

$$T_{max} = T_{TE} - T_{op}$$

Where:

T_{max} = The maximum ambient temperature in which the device can operate.

T_{op} = The operating temperature of the device, given a dissipated power "**P_{max}**" and a known thermal impedance "θ_{JA}".

T_{TE} = The Over-Temperature Error Threshold, given in the "Characteristics & Specifications" section on page 8.

θ_{JA} = The thermal impedance of the device and PCB. (This value is highly subjective to a number of application specific scenarios. The numbers given in Table 2 on page 31 can be used for a first order approximation, but proper characterization of the application's specific PCB and supporting mechanicals is needed to increase the accuracy of the result achieved here.)

P_{max} = The maximum power at which the amplifier will be operated continuously. (For conservative estimates, the 10% THD+N rated power given in "Characteristics & Specifications" section on page 8 can be used. However, this method will predict higher operating temperatures than what may be seen in the application, since power content of audio signals is much smaller than that of the sine wave used to establish the power specifications.)

η = The efficiency of the device at the power P_{max}. (A safe, conservative assumption is 85%)

9. ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order#
CS35L00	2.8 W Mono Audio Amplifier with selectable gain	10-DFN	Yes	Commercial	-10° to +70°C	Rail	CS35L00-CNZ
						Tape and Reel	CS35L00-CNZR

10.REVISION HISTORY

Release	Changes
A1	Initial Release
A2	– Updated all output switching frequency references to f_{sw1} from 200 kHz to 192 kHz. – Updated all output switching frequency references to f_{sw2} from 80 kHz to 76 kHz. – Updated front page title, features, and common applications. – Updated front page block diagram. – Updated Section 3. Typical Connection Diagrams to show 10 µF and 0.1 µF power-supply decoupling capacitors. – Reorganized location of individual specifications in electrical characteristics tables based on measured device performance in different operational modes ("Electrical Characteristics - All Operational Modes" on page 9, "Electrical Characteristics - SD Mode" on page 10, "Electrical Characteristics - FSD Mode" on page 11, "Electrical Characteristics - HD Mode" on page 12, and "Electrical Characteristics - FHD Mode" on page 13). – The following specification changes have been made in "Electrical Characteristics - SD Mode" on page 10, "Electrical Characteristics - FSD Mode" on page 11, "Electrical Characteristics - HD Mode" on page 12, and "Electrical Characteristics - FHD Mode" on page 13: – Added "Common-Mode Rejection Ratio" test conditions (V_{ripple} = 1 V_{PP} and f_{ripple} = 217 Hz) – Updated "Signal to Noise Ratio" to be specified as A-Weighted – Updated "Idle Channel Noise" to be specified as both A-Weighted & Unweighted – Updated "Idle Current Draw" to be specified with no load at 3 voltages (5.0 V, 4.2 V, and 3.7 V) – Changed "Max Input Before Clipping specification to "Input Voltage @ 1 % THD+N" – Updated specification typical values for 1% Output Power, 10% Output Power, THD+N @ 1 W, SNR A-Weighted, Idle Channel Noise A-Weighted, Idle Channel Noise (unweighted), Frequency Response, Output Switching Frequency, Input Impedance, and Input Voltage @ 1% THD+N – Updated "Operating Efficiency" to be specified with 8 Ω + 33 µH and 4 Ω + 33 µH in "Electrical Characteristics - All Operational Modes" on page 9. – Modified "Power-Up Time" specification into "Start-Up Time" and "Zero Crossing Power-Up" and added a cross-reference in "Power-Up & Power-Down Characteristics" on page 14. – Moved power-up and power-down timing specifications from "Electrical Characteristics - All Operational Modes" on page 9 to their own specification table, "Power-Up & Power-Down Characteristics" on page 14. – Renamed "Thermal Error Wait Time (W_{TE})" to "Thermal Error Retry Time (R_{TE})" in "Electrical Characteristics - All Operational Modes" on page 9 and in Section 5.5 Over Temperature Protection and added (Note 10) Thermal Error cross reference from spec table to description section. – Updated "Operating Efficiency" specification (η) in "Electrical Characteristics - All Operational Modes" on page 9. – Updated "MOSFET On Resistance" specification ($R_{DS(ON)}$) in "Electrical Characteristics - All Operational Modes" on page 9.

A2	– Updated Shutdown Supply Current specification ($I_{A(SD)}$) in "Electrical Characteristics - All Operational Modes" on page 9. – Added "MOSFET On Resistance" test conditions (I_{bias} = 0.5 A) in "Electrical Characteristics - All Operational Modes" on page 9. – Section 5.1.1.1 SD Mode updated to remove references to edge rate control. – Section 5.1.2.1 HD Mode updated to include f_{sw1} switching frequency and clarify the conditions under which radiated emissions gains occur. – Added Section 6. Typical Performance Plots. – Added Section 5.4 Power-Up and Power-Down. – Modified "Input Level Threshold for HD/FHD Modes" to be split up into "Input Level for Entering LDO Operation in HD/FHD Modes" and "Input Level for Entering VBATT Operation in HD/FHD Modes" in "Electrical Characteristics - All Operational Modes" on page 9. – Added "LDO Entry Time Delay" specification in "Electrical Characteristics - All Operational Modes" on page 9. – Updated (Note 8) and added (Note 9) referring to the "Input Level Thresholds". – Updated Section 5.5 Over Temperature Protection functional description. – Updated out of date specification names, symbols, and cross-references in multiple locations throughout the document.
PP1	– Updated output power and PSRR references in the Title, Features, and General Description sections on the Front Page. – Updated "Output Power" (P_O), "Power Supply Rejection Ratio" (PSRR), "Common-Mode Rejection Ratio" (CMRR), "Idle Channel Noise" (ICN_A and ICN), "Total Group Delay" (GD), "Idle Current Draw" (I_{IDLE}), and "Input Voltage @ 1 % THD+N" (V_{ICLIP}) specifications for all modes in "Electrical Characteristics - SD Mode" on page 10, "Electrical Characteristics - FSD Mode" on page 11, "Electrical Characteristics - HD Mode" on page 12, and "Electrical Characteristics - FHD Mode" on page 13. – Updated THD+N at 1W specification for FSD and FHD modes in "Electrical Characteristics - FSD Mode" on page 11 and "Electrical Characteristics - FHD Mode" on page 13. – Updated "Operating Efficiency" (η), "Under Voltage Lockout Threshold" (UVLO), and "LDO Entry Time Delay" (t_{LDO}) specifications in "Electrical Characteristics - All Operational Modes" on page 9. – Added Under Voltage Lockout description in (Note 11). – Updated "THD+N vs. Output Power", "THD+N vs. Frequency", "Idle Current Draw vs. VBATT", "Output Power vs. VBATT", "Efficiency vs. Output Power", and "Supply Current vs. Output Power" typical performance plots for all operational modes in Section 6. Typical Performance Plots.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com.