

## 3.0 W Mono Class-D Audio Amplifier with Low Idle Current

### CS35L01 and CS35L03 Features

- ◆ Filterless Hybrid Class-D Architecture
  - <1 mA Quiescent Current
  - 1 x 3.0 W into 4  $\Omega$  (10% THD+N)
  - 1 x 2.4 W into 4  $\Omega$  (1% THD+N)
  - 1 x 1.7 W into 8  $\Omega$  (10% THD+N)
  - 1 x 1.4 W into 8  $\Omega$  (1% THD+N)
- ◆ Advanced  $\Delta\Sigma$  Closed-loop Modulation
  - 98 dB Signal-to-Noise Ratio (A-Weighted)
  - 0.02% THD+N @ 1 W (SD & HD Mode)
- ◆ Integrated Protection and Automatic Recovery for Output Short-circuit and Thermal Overload
- ◆ Pin-compatible 9-ball WLCSP family for easy upgrade path
  - CS35L01: +6 dB default Gain
  - CS35L03: +12 dB default Gain
- ◆ Pop and Click Suppression

### Common Applications

- ◆ Mobile Phones
- ◆ Laptops/Netbooks/Tablets
- ◆ Portable Navigation Devices
- ◆ Active Speakers
- ◆ Portable Gaming

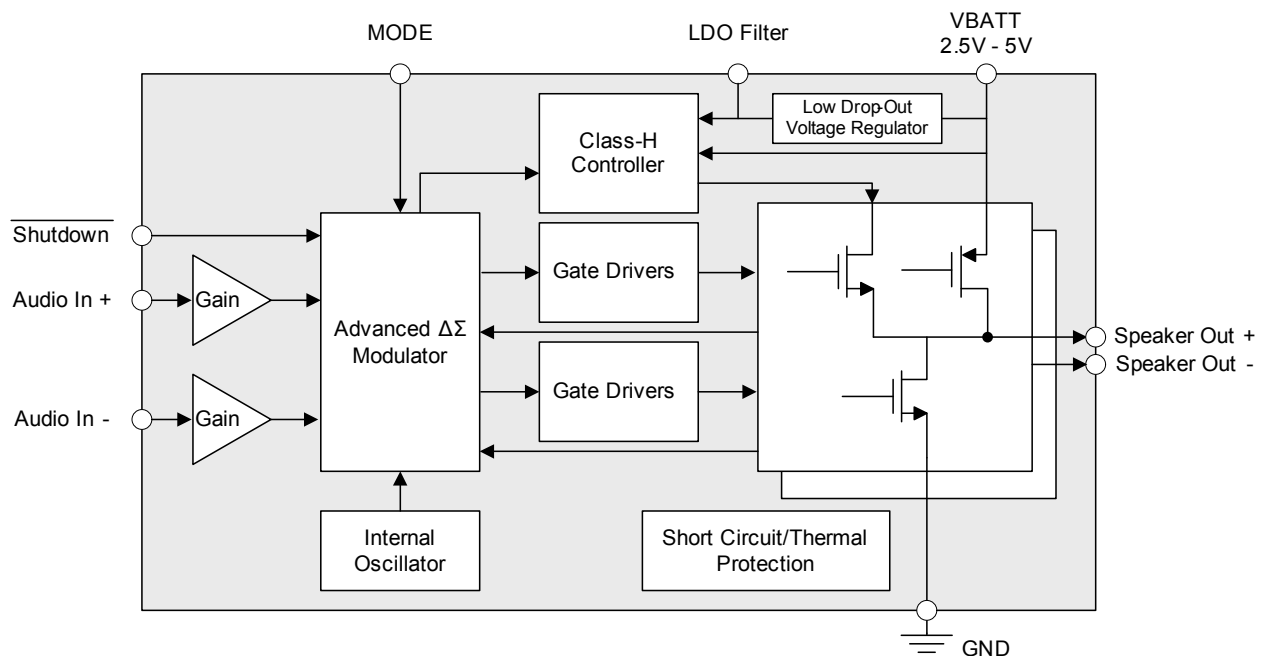
### General Description

The CS35L01 and the CS35L03 are 3.0W high efficiency Hybrid Class-D audio amplifiers with low idle current consumption.

The CS35L01/03 features an advanced closed-loop architecture to provide 0.02% THD+N at 1 W and -87 dB PSRR at 217 Hz.

A flexible Hybrid Class-D output stage offers four modes of operation: Standard Class-D (SD) mode offers full audio bandwidth and high audio performance; Hybrid Class-D (HD) mode offers a substantial reduction in idle power consumption with an integrated Class-H controller; Reduced Frequency Class-D (FSD) mode reduces the output switching frequency, producing lower electromagnetic interference (EMI); and Reduced Frequency Hybrid Class-D (FHD) mode produces both the lower idle power consumption of HD mode and the reduced EMI benefits of FSD mode.

Requiring minimal external components and PCB space, the CS35L01 and CS35L03 are available in a 1.2 mm x 1.2 mm, 9-ball WLCSP package in Commercial grade (-10°C to +70°C). Please see [“Ordering Information” on page 33](#) for package options and gain configurations.



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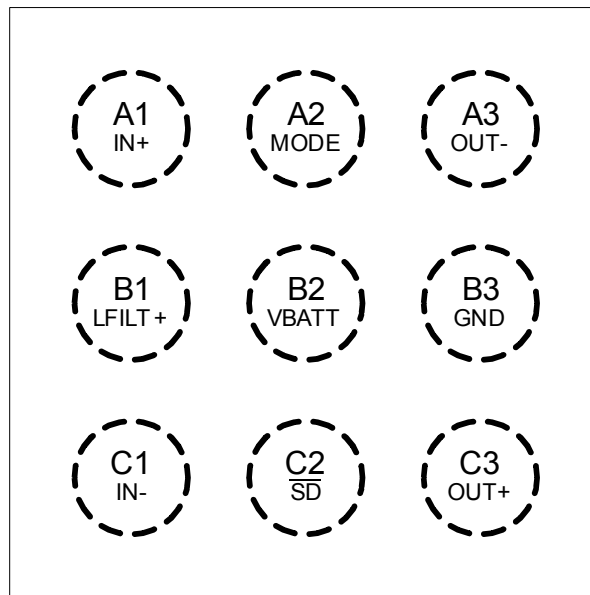
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## 1. BALL DESCRIPTIONS FOR CS35L01 & CS35L03



**Figure 1. Top View of WLCSP Pinout  
(Looking down through die)**

<b>Ball Name</b>	<b>#</b>	<b>Description</b>
IN+	A1	<b>Positive Analog Input (Input)</b> - Differential positive audio signal input.
MODE	A2	<b>Switching Mode (Input)</b> - Controls the output switching modes of the CS35L01/03.
OUT-	A3	<b>Negative PWM Output (Output)</b> - Differential negative PWM output.
LFILT+	B1	<b>Low Drop Out Regulator Filter (Output)</b> - Bypass capacitor connection point for internal LDO. Connecting this net to VBATT places the device into SD mode.
VBATT	B2	<b>Positive Analog Power Supply (Input)</b> - Positive power supply input.
GND	B3	<b>Ground (Input)</b> - Power supply ground.
IN-	C1	<b>Negative Analog Input (Input)</b> - Differential negative audio signal input.
SD	C2	<b>Shutdown (Input)</b> - Pulling this net low places the CS35L01/03 in shutdown.
OUT+	C3	<b>Positive PWM Output (Output)</b> - Differential Positive PWM output.

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## 2. DIGITAL BALL CONFIGURATIONS

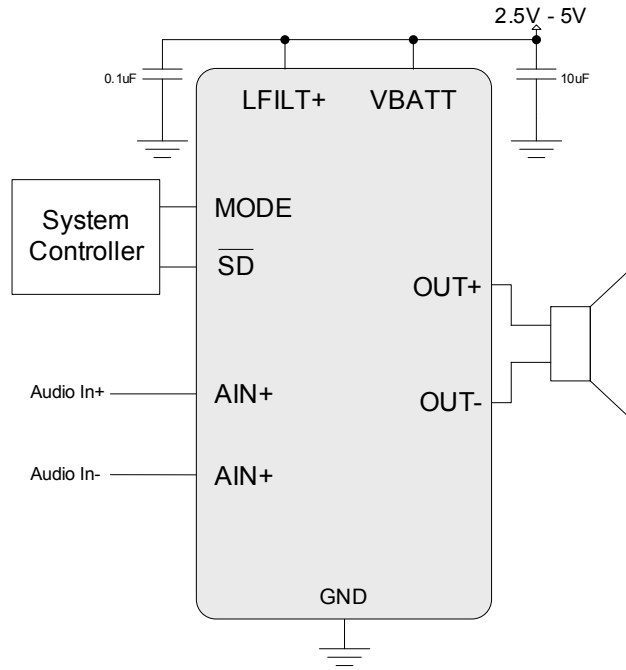
See (Note 1) and (Note 2) below the table.

Power Supply	I/O Name	Ball	Direction	Internal Connections	Configuration
VBATT	$\overline{SD}$	C2	Input	No Internal Pull Up	Hysteresis on CMOS Input
	MODE	A2	Input	No Internal Pull Up	Hysteresis on CMOS Input

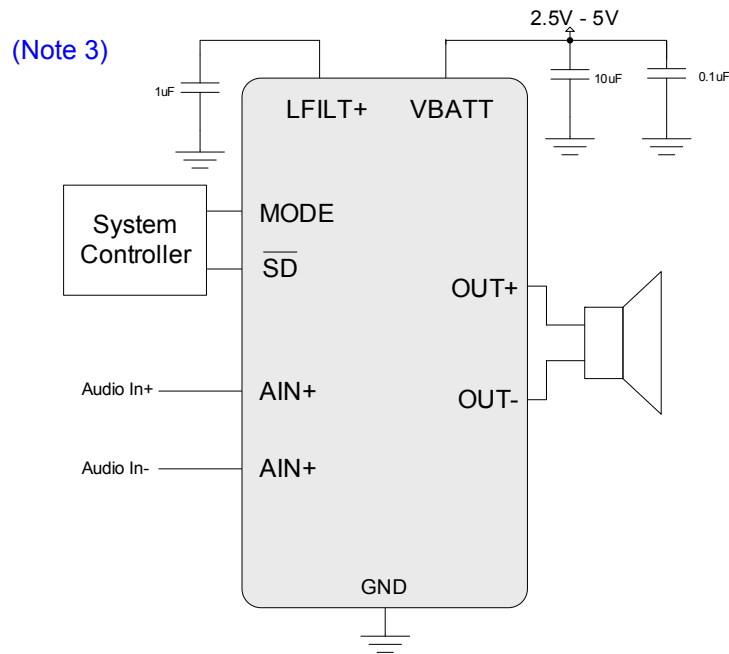
**Note:**

1. Refer to specification table “[Digital Interface Specifications and Characteristics](#)” on page 14 for details on the digital I/O characteristics.
2. I/O voltage levels must not exceed the voltage listed in table “[Absolute Maximum Ratings](#)” on page 8.

### 3. TYPICAL CONNECTION DIAGRAMS



**Figure 2. Typical Connection Diagram for SD & FSD Mode**



**Figure 3. Typical Connection Diagram for HD & FHD Mode**

**Note:**

- The value of the capacitance connected to the LFILT+ net should not exceed 4.7 µF. Presence of a capacitance above 4.7 µF will prevent proper HD and FHD operation.

## 4. CHARACTERISTICS & SPECIFICATIONS

Test Conditions (unless otherwise specified): GND = 0 V; All voltages with respect to ground; Input signal = 997 Hz differential sine wave;  $T_A = 25^\circ\text{C}$ ; VBATT = 5.0 V;  $R_L = 8\ \Omega$ ; 22 Hz to 20 kHz measurement bandwidth; Measurements taken with AES17 measurement filter and Audio Precision AUX-0025 passive filter.

### RECOMMENDED OPERATING CONDITIONS

GND = 0 V; All voltages with respect to ground. Please see (Note 4).

Parameters	Symbol	Min	Typ	Max	Units
<b>DC Power Supply</b>					
Supply Voltage	VBATT	2.5	5.0	5.5	V
<b>Temperature</b>					
Ambient Temperature	$T_A$	-10	-	+70	$^\circ\text{C}$
Junction Temperature	$T_J$	-10	-	+150	$^\circ\text{C}$

### ABSOLUTE MAXIMUM RATINGS

GND = 0 V; All voltages with respect to ground.

Parameters	Symbol	Min	Max	Units
<b>DC Power Supply</b>				
Supply Voltage	VBATT	-0.3	6.0	V
LFILT+ Current (Note 5)	$I_{VDREG}$	-	10	$\mu\text{A}$
<b>Inputs</b>				
Input Current	$I_{in}$	-	$\pm 10$	mA
<b>Temperature</b>				
Ambient Operating Temperature (power applied)	$T_A$	-20	+125	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-65	+150	$^\circ\text{C}$

**WARNING:** Operation at or beyond these limits may result in permanent damage to the device.

#### Notes:

- Functionality is not guaranteed or implied outside of these limits. Operation outside of these limits may adversely affect device reliability.
- No external loads should be connected to the LFILT+ net. Any connection of a load to this point may result in errant operation or performance degradation in the device.



**ELECTRICAL CHARACTERISTICS - ALL OPERATIONAL MODES**

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units	
Max. Current from LFILT+ (Note 6)	$I_{LFILT+}$		-	10	-	$\mu\text{A}$	
LFILT+ Output Impedance	$Z_{LFILT+}$		-	0.7	-	$\Omega$	
VBATT Limit for HD/FHD Mode (Note 7)	$V_{B_{LIM}}$		-	3.0	-	VDC	
Input Level for Entering LDO Operation in HD/FHD Modes (Note 8)	$V_{IN-LDO}$	CS35L03 CS35L01	-	$0.015 \cdot V_{BATT}$ $0.029 \cdot V_{BATT}$	-	Vrms Vrms	
Input Level for Entering VBATT Operation in HD/FHD Modes (Note 9)	$V_{IN-VBATT}$	CS35L03 CS35L01	-	0.09 0.19	-	Vrms Vrms	
LDO Entry Time Delay	$t_{LDO}$		-	1200	-	ms	
LDO Level for HD/FHD Modes	$V_{LDO}$		-	1.0	-	V	
Output Offset Voltage	$V_{OFFSET}$	Inputs AC coupled to GND	-	+/-1.5	-	mV	
Amplifier Gain	$A_V$	CS35L03 CS35L01	-	12 6	-	dB dB	
Shutdown Supply Current	$I_{A(SD)}$	$\overline{SD} = \text{Low}$	-	0.05	-	$\mu\text{A}$	
MOSFET On Resistance	$R_{DS(ON)}$	$I_{bias} = 0.5 \text{ A}$	-	270	-	$\text{m}\Omega$	
Thermal Error Threshold (Note 10)	$T_{TE}$		-	150	-	$^{\circ}\text{C}$	
Thermal Error Retry Time (Note 10)	$R_{TE}$		-	100	-	ms	
Under Voltage Lockout Threshold (Note 11)	UVLO		-	2.0	-	V	
Operating Efficiency	$\eta$	Output Levels at 10% THD+N					
		$8 \Omega + 33 \mu\text{H}$ Load	VBATT = 5 VDC	-	92	-	%
			VBATT = 3.7 VDC	-	91	-	%
		$4 \Omega + 33 \mu\text{H}$ Load	VBATT = 5 VDC	-	87	-	%
			VBATT = 3.7 VDC	-	86	-	%

**Note:**

- No external loads should be connected to the LFILT+ net. Any connection of a load to this point may result in errant operation or performance degradation in the device.
- When VBATT is below this threshold ( $V_{B_{LIM}}$ ), operation is automatically restricted to SD mode.
- When operating in HD or FHD mode and the differential input voltage remains below the input level threshold ( $V_{IN-LDO}$ ) for a period of time ( $t_{LDO}$ ), the PWM outputs will be powered by the internally generated LDO supply ( $V_{LDO}$ ).
- When operating in HD or FHD mode and the differential input voltage is above this input level threshold ( $V_{IN-VBATT}$ ), the PWM outputs will be powered directly from the VBATT supply.
- Refer to [Section 5.5](#) for more information on Thermal Error functionality.
- Under Voltage Lockout is the threshold at which a decreasing VBATT supply will disable device operation.

**ELECTRICAL CHARACTERISTICS - SD MODE**

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
Output Power (Continuous Average)	$P_O$	THD+N = 1% $R_L = 8 \Omega$ (VBATT = 5.0/4.2/3.7 VDC) $R_L = 4 \Omega$ (VBATT = 5.0/4.2/3.7 VDC)	-	1.39/0.98/0.76	-	W
		THD+N = 10% $R_L = 8 \Omega$ (VBATT = 5.0/4.2/3.7 VDC) $R_L = 4 \Omega$ (VBATT = 5.0/4.2/3.7 VDC)	-	1.73/1.23/0.95	-	W
Total Harmonic Distortion + Noise	THD+N	$P_O = 1.0$ W	-	0.02	-	%
Power Supply Rejection Ratio	PSRR	$V_{ripple} = 200$ mV <sub>PP</sub> , AINx AC coupled to GND @ 217 Hz @ 1 kHz	-	87	-	dB
			-	82	-	dB
Common-Mode Rejection Ratio	CMRR	$V_{ripple} = 1$ V <sub>PP</sub> , $f_{ripple} = 217$ Hz	-	73	-	dB
Signal to Noise Ratio A-Weighted	$SNR_A$	Inputs AC Coupled to Ground, Referenced to 1% THD+N (Note 13) CS35L03 CS35L01	-	96	-	dB
			-	97	-	dB
Idle Channel Noise A-Weighted	$ICN_A$	AIN+ connected to AIN- CS35L03 CS35L01	-	54	-	$\mu$ Vrms
			-	49	-	$\mu$ Vrms
Idle Channel Noise	ICN	AIN+ connected to AIN- CS35L03 CS35L01	-	110	-	$\mu$ Vrms
			-	100	-	$\mu$ Vrms
Frequency Response	FR	20 Hz to 20 kHz	-0.1	0	0.4	dB
Total Group Delay	GD		-	6	-	$\mu$ s
Output Switching Frequency	$f_{sw1}$		-	192	-	kHz
Idle Current Draw (Note 12)	$I_{IDLE}$	AIN+ connected to AIN-, No Output Load VBATT = 5.0 VDC VBATT = 4.2 VDC VBATT = 3.7 VDC	-	1.40	-	mA
			-	1.28	-	mA
			-	1.21	-	mA
Input Impedance, Single Ended	$Z_{IN}$	CS35L03 CS35L01	-	65	-	k $\Omega$
			-	100	-	k $\Omega$
Input Voltage @ 1 % THD+N	$V_{ICLIP}$	$R_L = 8 \Omega$ (VBATT = 5.0/4.2/3.7 VDC) CS35L03 CS35L01	-	0.85/0.72/0.63	-	Vrms
			-	1.71/1.44/1.26	-	Vrms

**ELECTRICAL CHARACTERISTICS - FSD MODE**

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
Output Power (Continuous Average)	$P_O$	THD+N = 1% $R_L = 8 \Omega$ (VBATT = 5.0/4.2/3.7 VDC) $R_L = 4 \Omega$ (VBATT = 5.0/4.2/3.7 VDC)	-	1.32/0.94/0.72	-	W
		THD+N = 10% $R_L = 8 \Omega$ (VBATT = 5.0/4.2/3.7 VDC) $R_L = 4 \Omega$ (VBATT = 5.0/4.2/3.7 VDC)	-	1.70/1.21/0.94	-	W
Total Harmonic Distortion + Noise	THD+N	$P_O = 1.0$ W	-	0.10	-	%
Power Supply Rejection Ratio	PSRR	$V_{ripple} = 200$ mV <sub>PP</sub> , AINx AC coupled to GND @ 217 Hz @ 1 kHz	-	88	-	dB
			-	81	-	dB
Common-Mode Rejection Ratio	CMRR	$V_{ripple} = 1$ V <sub>PP</sub> , $f_{ripple} = 217$ Hz	-	71	-	dB
Signal to Noise Ratio A-Weighted	$SNR_A$	Inputs AC Coupled to Ground, Referenced to 1% THD+N (Note 13) CS35L03 CS35L01	-	80	-	dB
			-	80	-	dB
Idle Channel Noise A-Weighted	$ICN_A$	AIN+ connected to AIN- CS35L03 CS35L01	-	300	-	$\mu$ Vrms
			-	290	-	$\mu$ Vrms
Idle Channel Noise	ICN	AIN+ connected to AIN- CS35L03 CS35L01	-	570	-	$\mu$ Vrms
			-	550	-	$\mu$ Vrms
Frequency Response	FR	20 Hz to 20 kHz	-4.0	0	0.5	dB
Total Group Delay	GD		-	14	-	$\mu$ s
Output Switching Frequency	$f_{sw2}$		-	76	-	kHz
Idle Current Draw (Note 12)	$I_{IDLE}$	AIN+ connected AIN-, No Output Load VBATT = 5.0 VDC VBATT = 4.2 VDC VBATT = 3.7 VDC	-	1.04	-	mA
			-	0.98	-	mA
			-	0.95	-	mA
Input Impedance, Single Ended	$Z_{IN}$	CS35L03 CS35L01	-	160	-	k $\Omega$
			-	240	-	k $\Omega$
Input Voltage @ 1 % THD+N	$V_{ICLIP}$	$R_L = 8 \Omega$ (VBATT = 5.0/4.2/3.7 VDC) CS35L03 CS35L01	-	0.83/0.70/0.61	-	Vrms
			-	1.66/1.39/1.22	-	Vrms

**Note:**

12. Idle Current Draw ( $I_{IDLE}$ ) is specified without any output filtering. Refer to [Section 5.3 on page 17](#) for information on output filtering.

**ELECTRICAL CHARACTERISTICS - HD MODE**

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
Output Power (Continuous Average)	P <sub>O</sub>	THD+N = 1% R <sub>L</sub> = 8 Ω (VBATT = 5.0/4.2/3.7 VDC) R <sub>L</sub> = 4 Ω (VBATT = 5.0/4.2/3.7 VDC)	-	1.39/0.99/0.76	-	W
		THD+N = 10% R <sub>L</sub> = 8 Ω (VBATT = 5.0/4.2/3.7 VDC) R <sub>L</sub> = 4 Ω (VBATT = 5.0/4.2/3.7 VDC)	-	1.73/1.23/0.95	-	W
Total Harmonic Distortion + Noise	THD+N	P <sub>O</sub> = 1.0 W	-	0.02	-	%
Power Supply Rejection Ratio	PSRR	V <sub>ripple</sub> = 200 mV <sub>PP</sub> , AINx AC coupled to GND @ 217 Hz @ 1 kHz	-	89	-	dB
			-	86	-	dB
Common-Mode Rejection Ratio	CMRR	V <sub>ripple</sub> = 1 V <sub>PP</sub> , f <sub>ripple</sub> = 217 Hz	-	73	-	dB
Signal to Noise Ratio A-Weighted	SNR <sub>A</sub>	Inputs AC Coupled to Ground, Referenced to 1% THD+N (Note 13) CS35L03 CS35L01	-	97	-	dB
			-	98	-	dB
Idle Channel Noise A-Weighted	ICN <sub>A</sub>	AIN+ connected to AIN- CS35L03 CS35L01	-	49	-	μVrms
			-	43	-	μVrms
Idle Channel Noise	ICN	AIN+ connected to AIN- CS35L03 CS35L01	-	86	-	μVrms
			-	83	-	μVrms
Frequency Response	FR	20 Hz to 20 kHz	-0.1	0	0.4	dB
Total Group Delay	GD		-	6	-	μs
Output Switching Frequency	f <sub>sw1</sub>		-	192	-	kHz
Idle Current Draw (Note 14)	I <sub>IDLE</sub>	AIN+ connected AIN-, No Output Load VBATT = 5.0 VDC VBATT = 4.2 VDC VBATT = 3.7 VDC	-	1.09	-	mA
			-	1.04	-	mA
			-	1.01	-	mA
Input Impedance, Single Ended	Z <sub>IN</sub>	CS35L03 CS35L01	-	65	-	kΩ
			-	100	-	kΩ
Input Voltage @ 1% THD+N	V <sub>ICLIP</sub>	R <sub>L</sub> = 8 Ω (VBATT = 5.0/4.2/3.7 VDC) CS35L03 CS35L01	-	0.85/0.72/0.63	-	Vrms
			-	1.71/1.44/1.26	-	Vrms

**ELECTRICAL CHARACTERISTICS - FHD MODE**

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
Output Power (Continuous Average)	P <sub>O</sub>	THD+N = 1% R <sub>L</sub> = 8 Ω (VBATT = 5.0/4.2/3.7 VDC) R <sub>L</sub> = 4 Ω (VBATT = 5.0/4.2/3.7 VDC)	-	1.33/0.94/0.72	-	W
		THD+N = 10% R <sub>L</sub> = 8 Ω (VBATT = 5.0/4.2/3.7 VDC) R <sub>L</sub> = 4 Ω (VBATT = 5.0/4.2/3.7 VDC)	-	2.31/1.63/1.23	-	W
		THD+N = 10% R <sub>L</sub> = 8 Ω (VBATT = 5.0/4.2/3.7 VDC) R <sub>L</sub> = 4 Ω (VBATT = 5.0/4.2/3.7 VDC)	-	1.71/1.21/0.94	-	W
		THD+N = 10% R <sub>L</sub> = 8 Ω (VBATT = 5.0/4.2/3.7 VDC) R <sub>L</sub> = 4 Ω (VBATT = 5.0/4.2/3.7 VDC)	-	2.95/2.09/1.61	-	W
Total Harmonic Distortion + Noise	THD+N	P <sub>O</sub> = 1.0 W	-	0.11	-	%
Power Supply Rejection Ratio	PSRR	V <sub>ripple</sub> = 200 mV <sub>PP</sub> , AINx AC coupled to GND	-	89	-	dB
		@ 217 Hz	-	85	-	dB
		@ 1 kHz	-	85	-	dB
Common-Mode Rejection Ratio	CMRR	V <sub>ripple</sub> = 1 V <sub>PP</sub> , f <sub>ripple</sub> = 217 Hz	-	71	-	dB
Signal to Noise Ratio A-Weighted	SNR <sub>A</sub>	Inputs AC Coupled to Ground, Referenced to 1% THD+N (Note 13)	-	93	-	dB
		CS35L03	-	94	-	dB
		CS35L01	-	94	-	dB
Idle Channel Noise A-Weighted	ICN <sub>A</sub>	AIN+ connected to AIN-	-	71	-	μVrms
		CS35L03	-	63	-	μVrms
		CS35L01	-	63	-	μVrms
Idle Channel Noise	ICN	AIN+ connected to AIN-	-	125	-	μVrms
		CS35L03	-	115	-	μVrms
		CS35L01	-	115	-	μVrms
Frequency Response	FR	20 Hz to 20 kHz	-4.0	0	0.5	dB
Output Switching Frequency	f <sub>sw1</sub>	LDO Operation	-	192	-	kHz
Total Group Delay	GD		-	14	-	μs
Output Switching Frequency	f <sub>sw2</sub>	VBATT Operation	-	76	-	kHz
Idle Current Draw (Note 14)	I <sub>IDLE</sub>	AIN+ connected AIN-, No Output Load	-	1.09	-	mA
		VBATT = 5.0 VDC	-	1.04	-	mA
		VBATT = 4.2 VDC	-	1.01	-	mA
		VBATT = 3.7 VDC	-	1.01	-	mA
Input Impedance, Single Ended	Z <sub>IN</sub>	CS35L03	-	160	-	kΩ
		CS35L01	-	240	-	kΩ
Input Voltage @ 1 % THD+N	V <sub>ICLIP</sub>	R <sub>L</sub> = 8 Ω (VBATT = 5.0/4.2/3.7 VDC)	-	0.83/0.70/0.62	-	Vrms
		CS35L03	-	1.66/1.39/1.22	-	Vrms
		CS35L01	-	1.66/1.39/1.22	-	Vrms

**Note:**

- SNR<sub>A</sub> dB is referenced to the output signal amplitude resulting in the specified output power at THD+N < 1 %. See [“Parameter Definitions” on page 29](#) for more information.
- Idle Current Draw (I<sub>IDLE</sub>) is specified without any output filtering. Refer to [Section 5.3 on page 17](#) for information on output filtering. At idle, the output devices will switch at the same rate in HD and FHD mode. FHD only changes the output switching frequency when the input levels are above the “Input Level for Entering VBATT Operation in HD/FHD Modes (V<sub>IN-VBATT</sub>)” given in [“Electrical Characteristics - All Operational Modes” on page 9](#).

## DIGITAL INTERFACE SPECIFICATIONS AND CHARACTERISTICS

Parameters	Symbol	Min	Max	Units
Input Leakage Current	$I_{in}$	-	±10	μA
Input Capacitance		-	10	pF
$\overline{SD}$ Pulse Width Requirement		1	-	ms
<b>Logic I/Os (Applicable to GAIN_SEL, MODE, and <math>\overline{SD}</math>)</b>				
High-Level Input Voltage	$V_{IH}$	0.7•VBATT	-	V
Low-Level Input Voltage	$V_{IL}$	-	0.3•VBATT	V

## POWER-UP & POWER-DOWN CHARACTERISTICS

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
Start-Up Time (Note 15)	$t_{start}$	After low-to-high $\overline{SD}$ pin transition edge	-	18	-	ms
Zero Crossing Power-Up Timeout	$t_{timeout}$	No audio input applied	-	25	-	ms
Power-Down Time	$t_{off}$	After high-to-low $\overline{SD}$ pin transition edge	-	1	-	ms

**Note:**

- Start-Up Time ( $t_{start}$ ) refers to the internal start-up time from when  $\overline{SD}$  is released to when the device is ready to activate the PWM outputs. The total power-up time from  $\overline{SD}$  release to the PWM outputs becoming active will vary based on the input signal, not exceeding the Start-Up Time + Zero Crossing Power-Up Timeout ( $t_{start} + t_{timeout}$ ). For more information, refer to [Section 5.4](#).

## 5. APPLICATIONS

### 5.1 MODE Descriptions

The CS35L01/03 devices can be operated in one of four operating modes, determined by the MODE pin and the LFILT+ pin. The four modes of operation are Standard Class-D operation (SD), Reduced Frequency Standard Class-D operation (FSD), Hybrid Class-D operation (HD), and Reduced Frequency Hybrid Class-D operation (FHD). Each of these modes can be leveraged to optimize different performance criteria in an array of applications.

		MODE connected to:	
		GND	VBATT
LFILT+ connected to:	VBATT	Reduced Frequency Class-D Mode (FSD)	Standard Class-D Mode (SD)
	Filter Cap to Ground	Reduced Frequency Hybrid Class-D Mode (FHD)	Hybrid Class-D Mode (HD)

**Table 1. LFILT+ and MODE Operation Configurations**

#### 5.1.1 Standard Class-D Modes of Operation

##### 5.1.1.1 SD Mode

Standard Class-D (SD) mode supports full audio bandwidth with very good SNR and THD+N performance. This mode of operation is characterized by a traditional closed loop, analog  $\Delta\Sigma$  modulated Class-D amplifier. With an output switching frequency of 192 kHz, this mode ensures flat frequency response across the entire audio frequency range.

##### 5.1.1.2 FSD Mode

The Reduced Frequency Class-D (FSD) mode provides competitive audio performance and a reduction in radiated emissions by decreasing the switching frequency of the output devices to 76 kHz. This reduction in switching frequency reduces the high-frequency energy being created by the output switching events. Idle channel noise is slightly higher in this mode of operation than SD mode, with the trade-off being better EMI performance and power consumption.

#### 5.1.2 Hybrid Class-D Modes of Operation

Hybrid Class-D and Reduced Frequency Hybrid Class-D modes of operation allows the rail voltage for the output devices to switch between a high voltage net and a low voltage net depending on the audio content being amplified. This is explained in more detail in [Section 5.1.2.1](#) and [Section 5.1.2.2](#). Operation in these modes requires that the voltage present on the VBATT pin be above the level listed as “VBATT Limit for HD/FHD Mode ( $V_{B\_LIM}$ )” in [“Electrical Characteristics - All Operational Modes” on page 9](#). If it is not, HD and FHD modes of operation of the device will automatically be disabled and operation will be limited to the SD mode of operation.

In both HD and FHD mode, the value of the capacitance connected to the LFILT+ pin must not exceed 4.7  $\mu\text{F}$ . If this value is greater than 4.7  $\mu\text{F}$ , it will prevent the rail voltage of the output devices from transitioning properly between VBATT and the internal LDO.

### 5.1.2.1 HD Mode

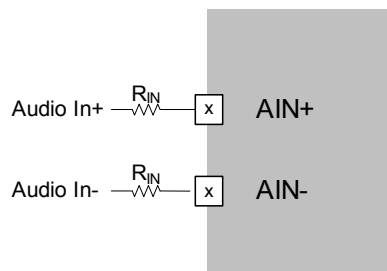
Hybrid Class-D mode (HD) provides competitive analog performance with a substantial reduction in idle power dissipation and radiation emissions. In this mode, the output switches at 192 kHz and a secondary supply is derived from VBATT using an internal 1.0-VDC low drop-out linear regulator (LDO). When the output signal is at a low amplitude, the Class-D output stage begins to switch from the lower rail voltage created by the internal LDO. This not only decreases idle power consumption when output capacitors are used, but also reduces electromagnetic emissions by reducing the amplitude of the square waves being created at the output of the CS35L01/03 when operating at low amplitude or idle power.

### 5.1.2.2 FHD Mode

The Reduced Frequency Hybrid Class-D (FHD) mode provides the best overall EMI performance and the lowest power consumption with slightly decreased frequency response near the top frequency range of the audio band, for high amplitude signals. In this mode of operation, the output switching frequency is reduced to 76 kHz during high amplitude transients on the output. The threshold at which this transition from 192-kHz to 76-kHz switching rate occurs is given as the Input Level Threshold for FHD Operation in [“Electrical Characteristics - FHD Mode” on page 13](#). Combined with the lower amplitude switching offered by the Hybrid design, this reduction in switching energy dramatically reduces the emissions levels of the output stage and its associated components.

## 5.2 Reducing the Gain with External Series Resistors

If necessary, it is possible to decrease the gain of the CS35L01/03 by adding series resistors to the audio input signal as is shown in [Figure 4](#) below.



**Figure 4. Adjusting Gain via External Series Resistance**

If input resistors are added, the new gain of the amplifier can be determined by the following equation:

$$A_{V(\text{adjusted})} = A_V - 20 \times \log\left(\frac{Z_{IN}}{Z_{IN} + Z_{EXT}}\right)$$

Where:

$A_{V(\text{adjusted})}$  = The new, adjusted gain of the system

$Z_{IN}$  = Input impedance of the device being used (See [“Electrical Characteristics - SD Mode” on page 10](#), [“Electrical Characteristics - FSD Mode” on page 11](#), [“Electrical Characteristics - HD Mode” on page 12](#), or [“Electrical Characteristics - FHD Mode” on page 13](#) for this value.)

$Z_{EXT}$  = Value of the resistor added in series with the inputs



$A_V$  = Original gain of the device being used (See “Electrical Characteristics - All Operational Modes” on page 9 for this value.)

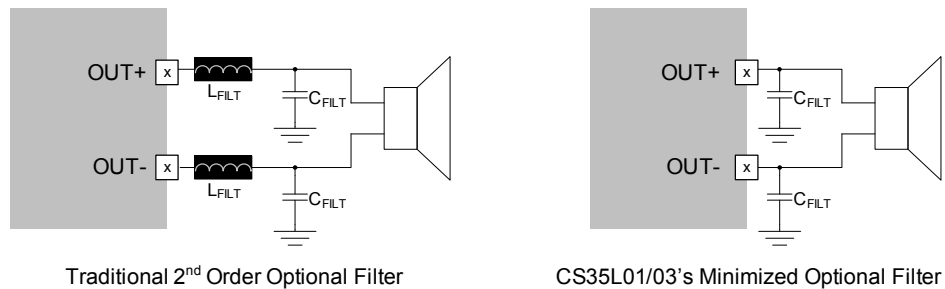
### 5.3 Output Filtering with the CS35L01/03

The CS35L01/03 is specifically designed to minimize radiated electromagnetic interference (EMI) signals. All of the devices are capable of meeting all stated data sheet performance numbers with no special filtering required. Additionally, the device has shown to be below the compliance limits of both FCC and CISPR testing with no external filtering required.

Ultimately, compliance with any radiated emissions requirements depends significantly on the entire system under test. In applications where system-level trade-offs such as compromised component layout or lengthy speaker wires have increased emissions levels, a passive output filter can be added to the outputs of the device in order to decrease EMI levels.

#### 5.3.1 Reduced Filter Order with the CS35L01/03

In applications which require an output filter, the unique design of the CS35L01/03 allows a much smaller, less expensive output filter to be used than what is normally found in Class-D amplifiers. In contrast to a second order filter implemented with a series inductive element (traditional inductor or ferrite beads) and a shunt capacitive element, basic filtering for the CS35L01/03 is accomplished by a single-order capacitive element attached to the OUTx terminals. This is highlighted in Figure 5 below. Of course, if the system requires more aggressive filtering, a ferrite bead can be added in series with the outputs to further attenuate system level noise.



**Figure 5. Optional Output Filter Components**

#### 5.3.2 Filter Component Selection

Usually, the need for output filtering is determined after the system under test has failed EMI testing. During this testing, problem frequencies are easily identified by the peaks which appear in the spectral plots gathered in the EMI testing.

Selection of the filter components should ensure that shunt elements (i.e.  $C_{FILT}$  in Figure 5) present a very low impedance at the frequency corresponding to the tallest peak in the spectral plot. If needed, series components such as ferrite beads (i.e.  $L_{FILT}$  in Figure 5) should be chosen to present a very high impedance at the frequency corresponding to the tallest peak in the spectral plot.

Careful attention should be paid to the current-carrying capabilities of any included ferrite beads and the impedance of the ferrite beads in the audio band. A proper trade-off in ferrite bead selection is one that allows the ferrite bead to sufficiently attenuate the problematic high-frequency emissions without compromising audio performance.

### 5.3.3 Output Filter Power Dissipation Considerations

In systems without inductive series elements like inductors or ferrite beads, power losses in the output filter are equal to the switching losses that occur in the system due to the cyclical charging and discharging of capacitors connected to the amplifier outputs. In systems that require an inductive series element, conducted losses also occurs due to the series impedance added to the output path.

#### 5.3.3.1 Conduction Losses for All modes of Operation

For all modes of operation (SD, FSD, HD, and FHD) of the CS35L01/03, the conduction losses are governed by the equation:

$$P = I^2Z$$

Where:

**P** = Power dissipated in the series impedance.

**I** = RMS AC output current

**Z** = impedance of the series element at the frequency of the AC current

This equation neglects any series impedances presented by the PCB traces or speaker wires in the output path.

#### 5.3.3.2 Switching Losses in SD/FSD Mode

Switching losses in SD/FSD Mode are governed by the equation

$$P = \frac{1}{2}CV^2f$$

Where:

**P** = Power dissipated in the capacitor (neglecting parasites).

**C** = Value of filtering capacitor

**V** = Peak voltage developed across the capacitor

**f** = Switching frequency of the outputs

These calculations are straightforward, as the peak voltage is simply the voltage level attached to VBATT, the capacitor is the value of capacitor that has been added for filtering (neglecting parasitic board capacitances), and the frequency is 192 kHz or 76 kHz for SD and FSD, respectively.

#### 5.3.3.3 Switching Losses in HD/FHD.

Many factors affect the switching losses when the device is operated in HD/FHD mode. These factors include the frequency of the content being amplified, the voltage level of VBATT, and the amplitude of the output signal will factor into both the voltage presented across the capacitors and the frequency at which the capacitors are charged or discharged.

Static signals (i.e. sine waves at a fixed amplitude) are easier to consider than are dynamic signals (i.e. musical content), as they are governed by the same equation as that listed in [Section 5.3.3.1](#) and [Section 5.3.3.2 on page 18](#). Modifications to that equation are limited to the voltage term (V) and the frequency term (f), depending on whether the static input signal amplitude is causing the output devices to switch at 76 kHz or 192 kHz, and to operate off of the VBATT supply or off of the internally generated LDO.

It is important to note that the HD and FHD modes offer significant improvement over traditional Class-D in idle power dissipation when an external output filter is necessary. This is because the voltage term ( $V$ ) is significantly reduced in HD and FHD mode. As can be seen in the equation, this is notable because reduction in the operating voltage reduces power losses not linearly, but instead *exponentially*- due to the voltage squared term ( $V^2$ ). It is also notable that when operated at high output levels, FHD modes also offers unique improvement in output filter losses, due to reducing the switching frequency ( $f$ ) at higher output levels.

## 5.4 Power-Up and Power-Down

When pulled to a logic low state, the  $\overline{SD}$  pin tristates the outputs and shuts down the CS35L01/03 device, putting it into a low power mode.

### 5.4.1 Recommended Power-Up Sequence

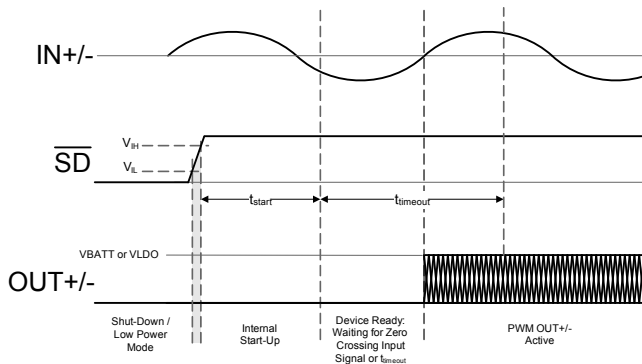
1. With the  $\overline{SD}$  pin pulled low, apply power to the CS35L01/03 and wait for the power supply to be stable.
2. Set the  $\overline{SD}$  pin high to begin normal operation.

#### 5.4.1.1 Zero-Crossing on Power-Up Functionality

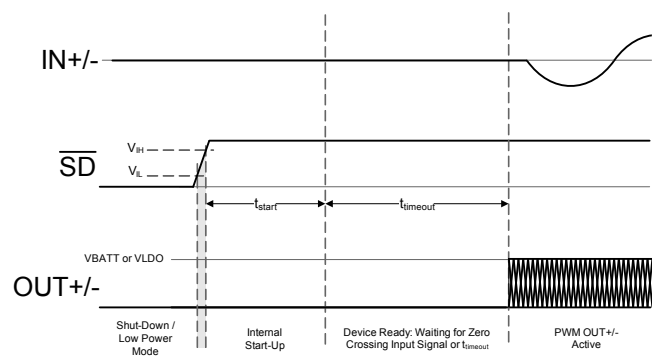
The CS35L01/03 implements an input-signal zero-crossing detection function that is enabled during power-up. This function is designed to prevent audible artifacts and eliminate any need to mute the amplifier's input audio signal during the power-up process.

After a minimum start-up time of  $t_{start}$ , the CS35L01/03 will begin to detect input-signal zero-crossings. The amplifier will then enable its switching outputs at the time of the first detected input-signal zero-crossing transition. If no input-signal zero-crossing is detected before  $t_{timeout}$ , the zero-crossing function will timeout and the outputs will begin switching immediately.

Both  $t_{start}$  and  $t_{timeout}$  are specified in “Power-Up & Power-Down Characteristics” on page 14.



**Figure 6. Power-Up Timing with Input Zero-Crossing**



**Figure 7. Power Up Timing without Input Zero-Crossing**

### 5.4.2 Recommended Power-Down Sequence

1. Mute the audio supplied to the CS35L01/03.
2. Pull the  $\overline{SD}$  pin low in order to reset the device and put it into the low power mode.
3. The power supply to the CS35L01/03 can now be removed.

## 5.5 Over Temperature Protection

The CS35L01/03 is internally protected against thermal overload. Built in die temperature sensing circuitry monitors the die temperature and will place the device into shut-down if thermal overload occurs. A thermal overload is characterized by the die temperature reaching the Thermal Error Threshold ( $T_{TE}$ ) at which time the outputs will tristate and shut down.

If the device has entered into shut-down due to a thermal overload, the die temperature must remain below the Thermal Error Threshold ( $T_{TE}$ ) for the time specified by the Thermal Error Retry Time ( $R_{TE}$ ) in order for the device to automatically return to normal operation.

Both  $T_{TE}$  and  $R_{TE}$  are specified in [“Electrical Characteristics - All Operational Modes” on page 9](#).

## 6. TYPICAL PERFORMANCE PLOTS

Test Conditions (unless otherwise specified): GND = 0 V; All voltages with respect to ground;  $A_V = 6$  dB; Input signal = 997 Hz differential sine wave;  $T_A = 25^\circ\text{C}$ ; VBATT = 5.0 V;  $R_L = 8 \Omega$ ; 10 Hz to 20 kHz Measurement Bandwidth; Measurements taken with AES17 measurement filter and Audio Precision AUX-0025 passive filter.

### 6.1 SD Mode Typical Performance Plots

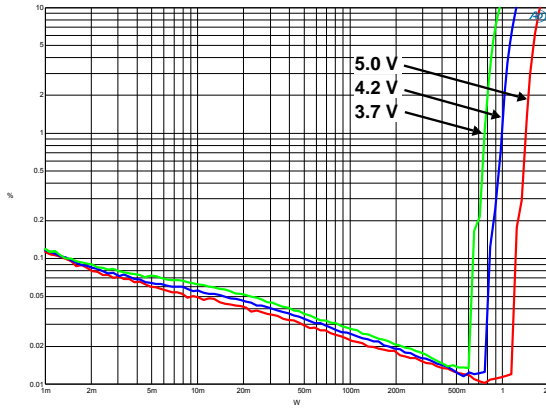


Figure 8. THD+N vs. Output Power - SD Mode  
 $R_L = 8 \Omega$

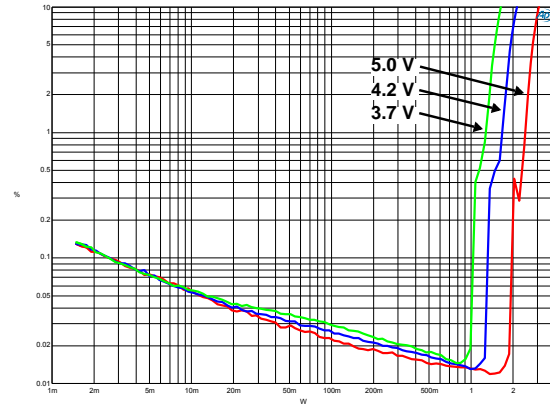


Figure 9. THD+N vs. Output Power - SD Mode  
 $R_L = 4 \Omega$

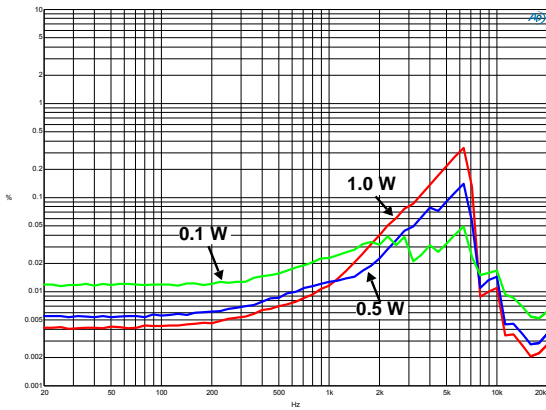


Figure 10. THD+N vs. Frequency - SD Mode  
VBATT = 5.0 V

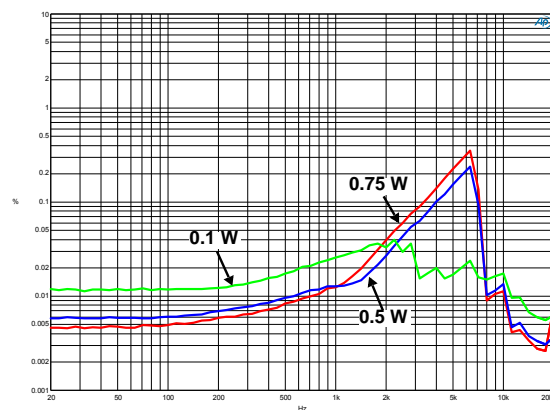


Figure 11. THD+N vs. Frequency - SD Mode  
VBATT = 4.2 V

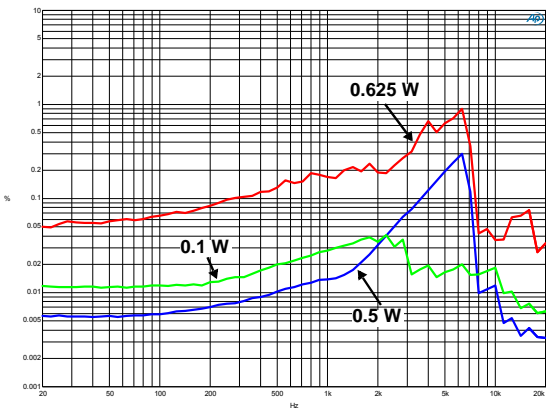


Figure 12. THD+N vs. Frequency - SD Mode  
VBATT = 3.7 V

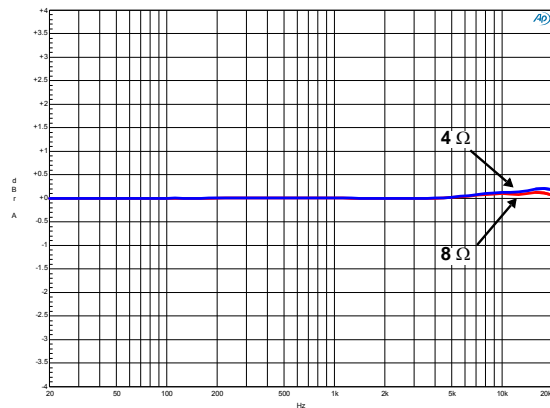
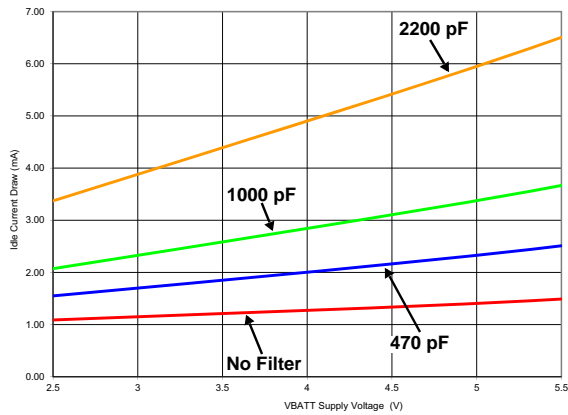
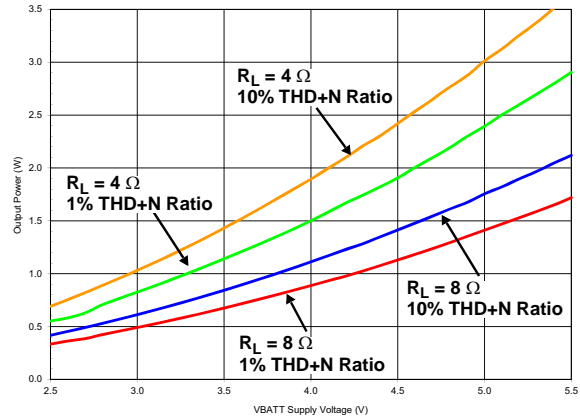


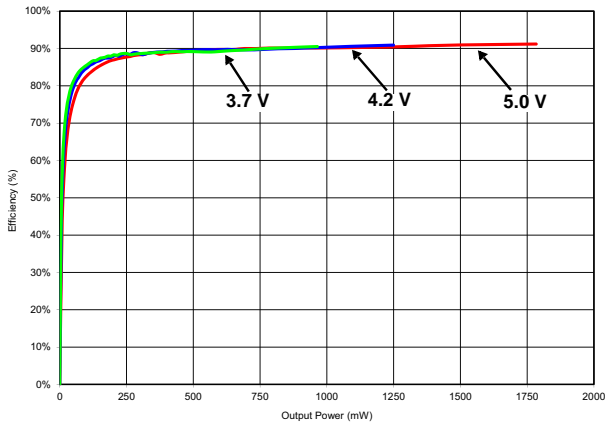
Figure 13. Frequency Response - SD Mode



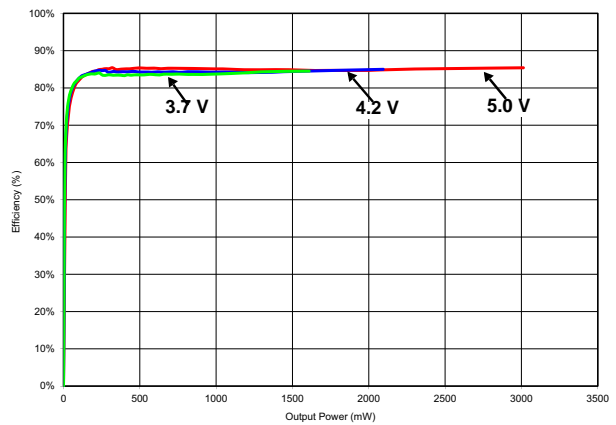
**Figure 14. Idle Current Draw vs. VBATT - SD Mode**  
 $R_L = 8 \Omega + 33 \mu\text{H}$  (Note 16)



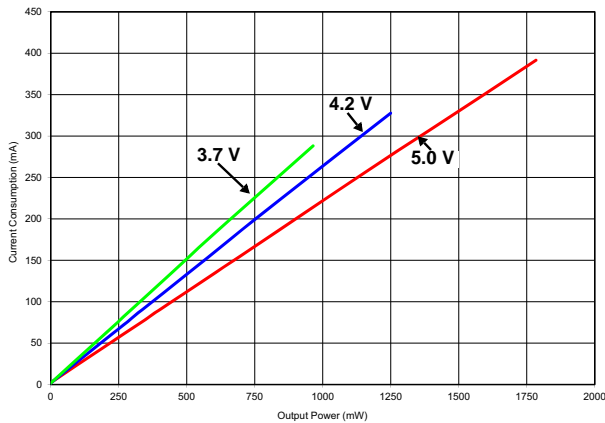
**Figure 15. Output Power vs. VBATT - SD Mode**



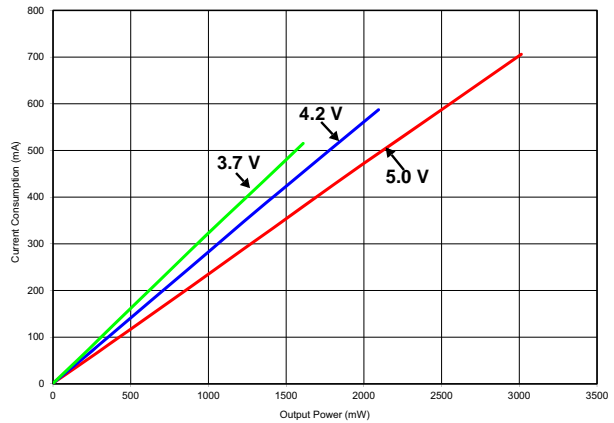
**Figure 16. Efficiency vs. Output Power - SD Mode**  
 $R_L = 8 \Omega + 33 \mu\text{H}$



**Figure 17. Efficiency vs. Output Power - SD Mode**  
 $R_L = 4 \Omega + 33 \mu\text{H}$



**Figure 18. Supply Current vs. Output Power - SD Mode**  
 $R_L = 8 \Omega + 33 \mu\text{H}$



**Figure 19. Supply Current vs. Output Power - SD Mode**  
 $R_L = 4 \Omega + 33 \mu\text{H}$

**Note:**

16. "Idle Current Draw vs. VBATT - SD Mode" capacitor values refer to  $C_{\text{FILT}}$  when configured as the "CS35L01/03's Minimized Optional Output Filter," shown in Figure 5 on page 17.

## 6.2 FSD Mode Typical Performance Plots

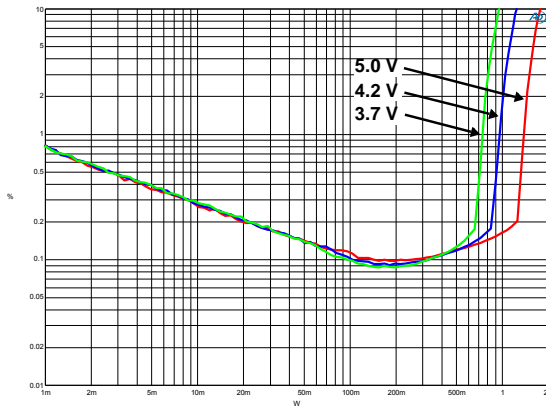


Figure 20. THD+N vs. Output Power - FSD Mode  
 $R_L = 8 \Omega$

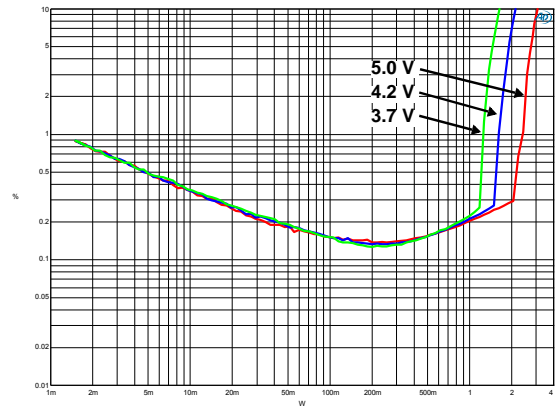


Figure 21. THD+N vs. Output Power - FSD Mode  
 $R_L = 4 \Omega$

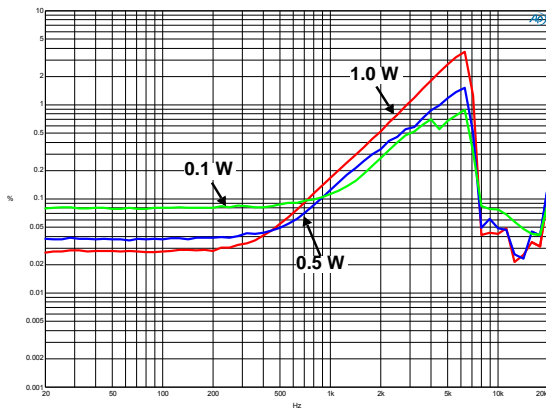


Figure 22. THD+N vs. Frequency - FSD Mode  
 $V_{BATT} = 5.0 V$

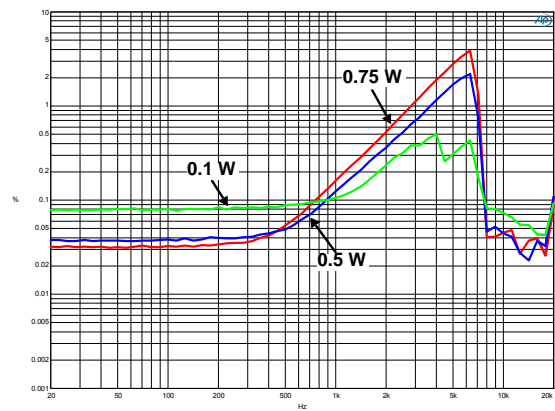


Figure 23. THD+N vs. Frequency - FSD Mode  
 $V_{BATT} = 4.2 V$

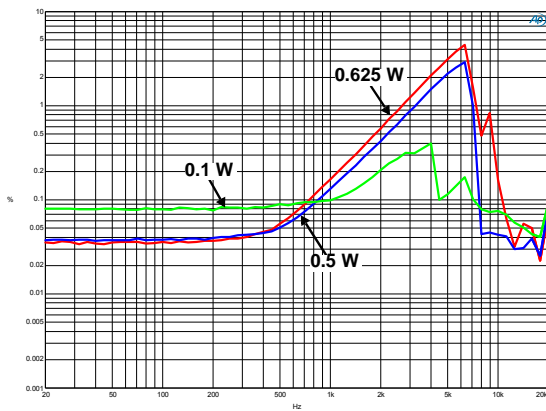


Figure 24. THD+N vs. Frequency - FSD Mode  
 $V_{BATT} = 3.7 V$

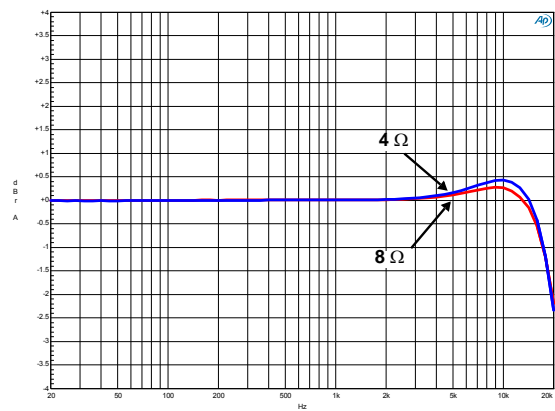
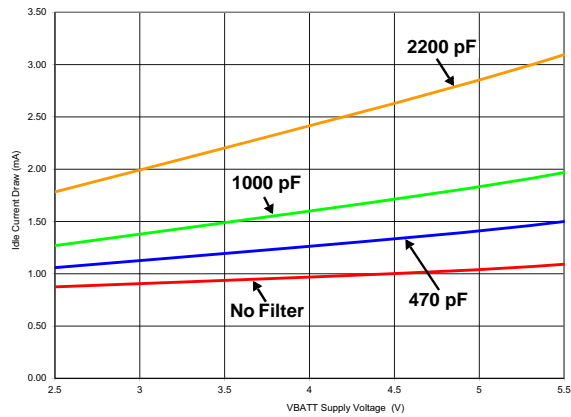
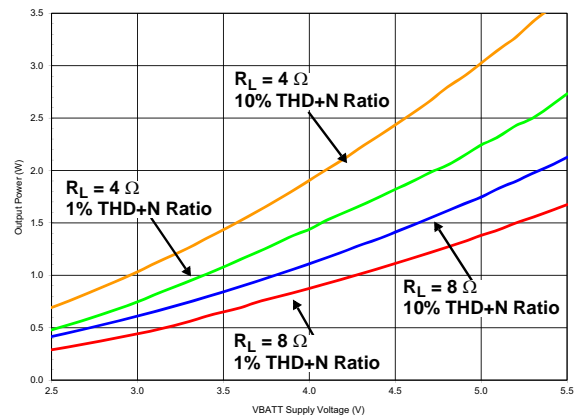


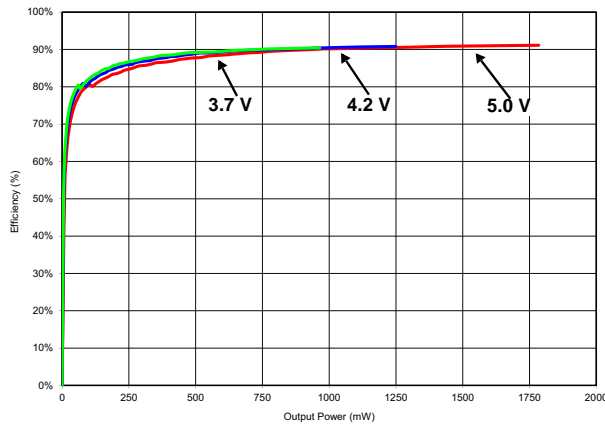
Figure 25. Frequency Response - FSD Mode



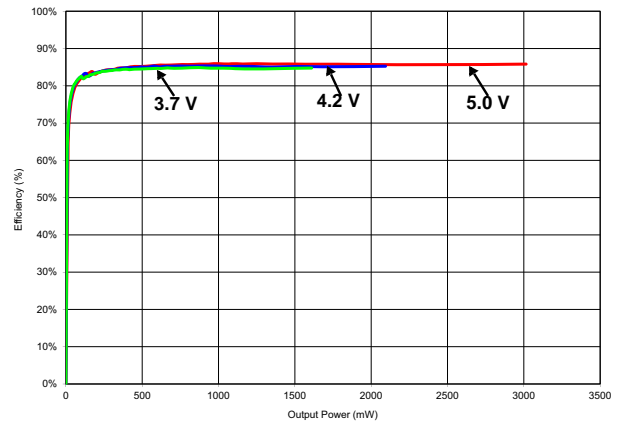
**Figure 26. Idle Current Draw vs. VBATT - FSD Mode**  
 $R_L = 8 \Omega + 33 \mu\text{H}$  (Note 17)



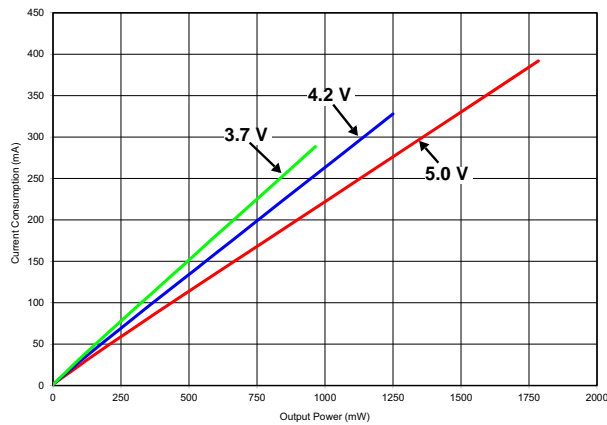
**Figure 27. Output Power vs. VBATT - FSD Mode**



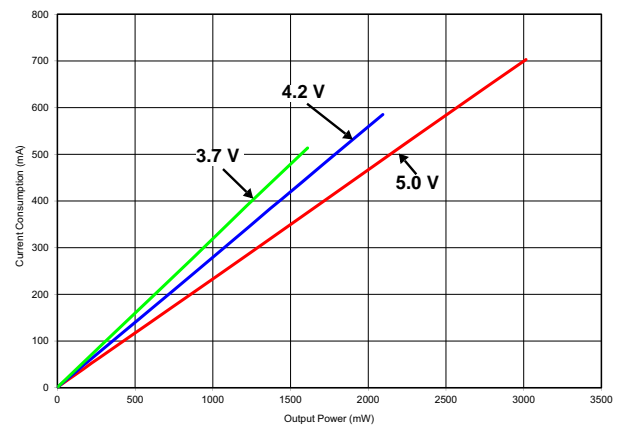
**Figure 28. Efficiency vs. Output Power - FSD Mode**  
 $R_L = 8 \Omega + 33 \mu\text{H}$



**Figure 29. Efficiency vs. Output Power - FSD Mode**  
 $R_L = 4 \Omega + 33 \mu\text{H}$



**Figure 30. Supply Current vs. Output Power - FSD Mode**  
 $R_L = 8 \Omega + 33 \mu\text{H}$



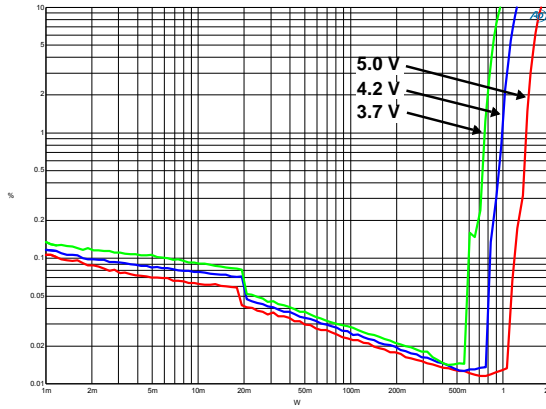
**Figure 31. Supply Current vs. Output Power - FSD Mode**  
 $R_L = 4 \Omega + 33 \mu\text{H}$

**Note:**

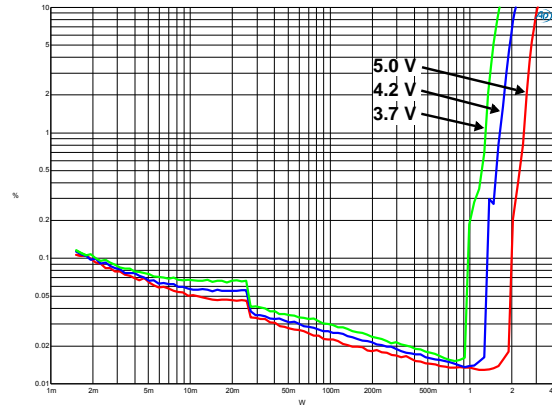
17. "Idle Current Draw vs. VBATT - FSD Mode" capacitor values refer to  $C_{\text{FILT}}$  when configured as the "CS35L01/03's Minimized Optional Output Filter", shown in [Figure 5](#) on [page 17](#).



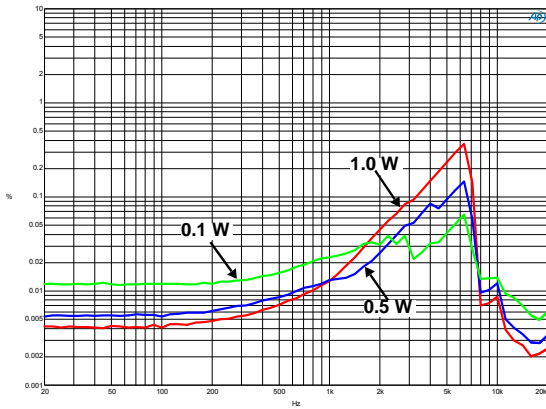
### 6.3 HD Mode Typical Performance Plots



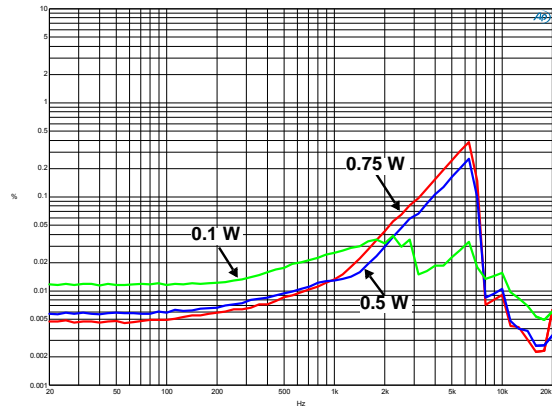
**Figure 32. THD+N vs. Output Power - HD Mode**  
 $R_L = 8 \Omega$



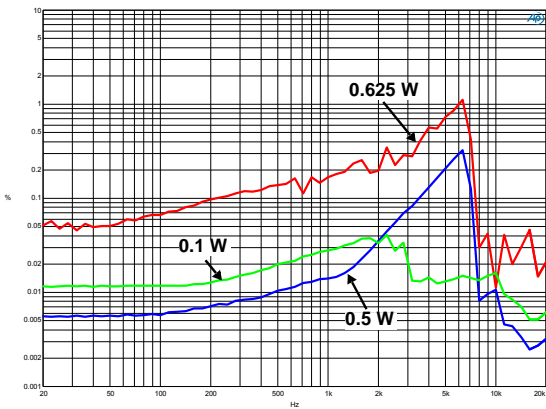
**Figure 33. THD+N vs. Output Power - HD Mode**  
 $R_L = 4 \Omega$



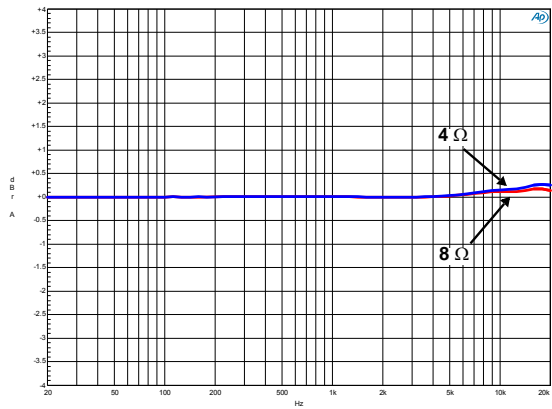
**Figure 34. THD+N vs. Frequency - HD Mode**  
 $V_{BATT} = 5.0 \text{ V}$



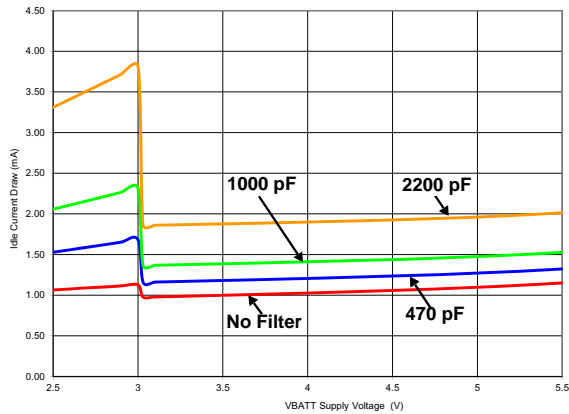
**Figure 35. THD+N vs. Frequency - HD Mode**  
 $V_{BATT} = 4.2 \text{ V}$



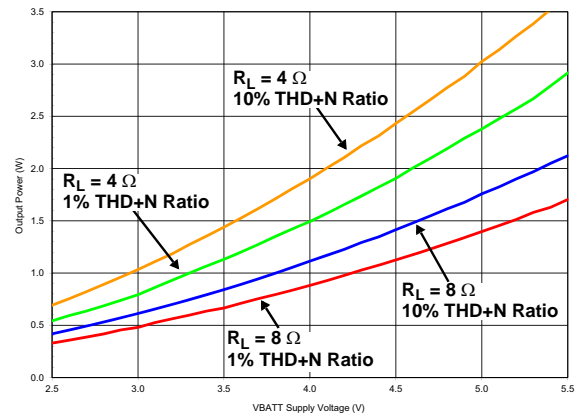
**Figure 36. THD+N vs. Frequency - HD Mode**  
 $V_{BATT} = 3.7 \text{ V}$



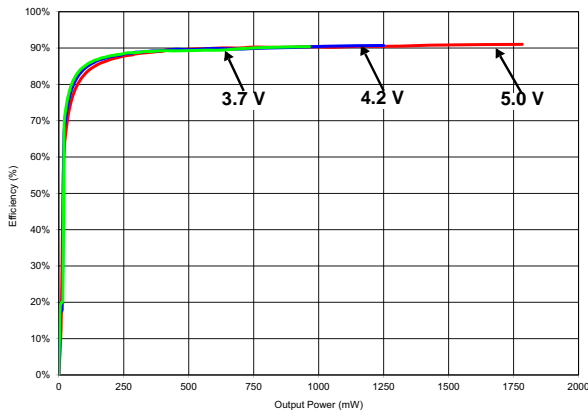
**Figure 37. Frequency Response - HD Mode**



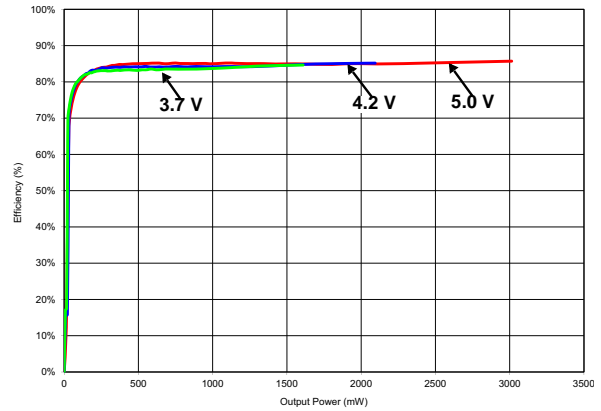
**Figure 38. Idle Current Draw vs. VBATT - HD Mode**  
 $R_L = 8 \Omega + 33 \mu\text{H}$  (Note 18)



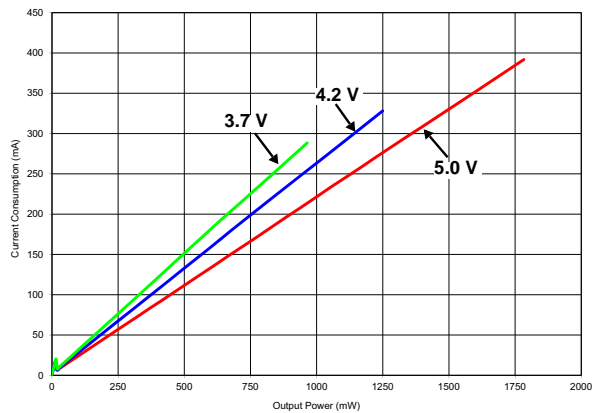
**Figure 39. Output Power vs. VBATT - HD Mode**



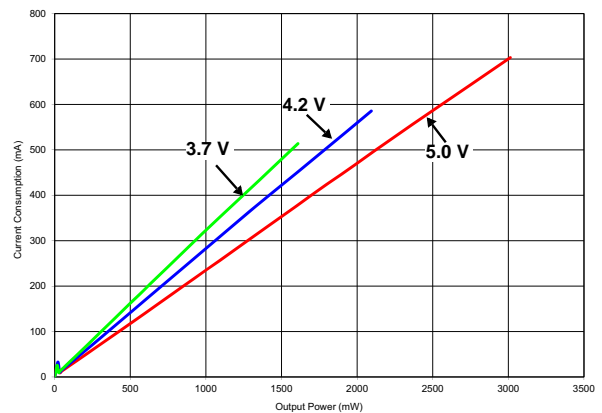
**Figure 40. Efficiency vs. Output Power - HD Mode**  
 $R_L = 8 \Omega + 33 \mu\text{H}$



**Figure 41. Efficiency vs. Output Power - HD Mode**  
 $R_L = 4 \Omega + 33 \mu\text{H}$



**Figure 42. Supply Current vs. Output Power - HD Mode**  
 $R_L = 8 \Omega + 33 \mu\text{H}$



**Figure 43. Supply Current vs. Output Power - HD Mode**  
 $R_L = 4 \Omega + 33 \mu\text{H}$

**Note:**

18. "Idle Current Draw vs. VBATT - HD Mode" capacitor values refer to  $C_{\text{FILT}}$  when configured as the "CS35L01/03's Minimized Optional Output Filter", shown in Figure 5 on page 17. When VBATT is below "VBATT Limit for HD/FHD Mode" ( $V_{\text{BLIM}}$ ), operation is restricted to SD Mode.

## 6.4 FHD Mode Typical Performance Plots

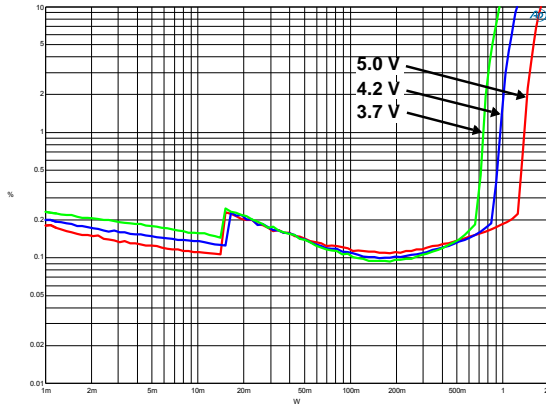


Figure 44. THD+N vs. Output Power - FHD Mode  
 $R_L = 8 \Omega$

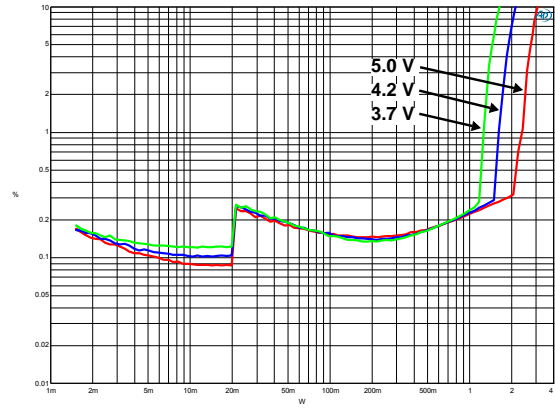


Figure 45. THD+N vs. Output Power - FHD Mode  
 $R_L = 4 \Omega$

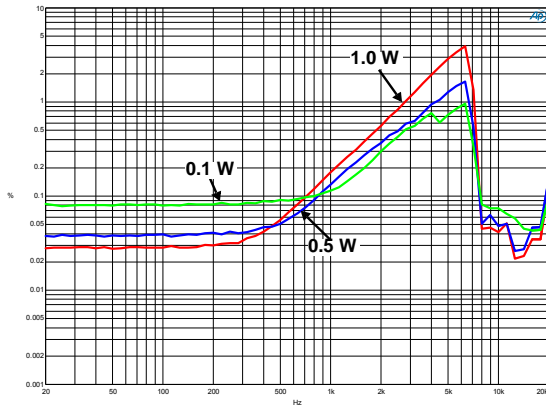


Figure 46. THD+N vs. Frequency - FHD Mode  
 $V_{BATT} = 5.0 V$

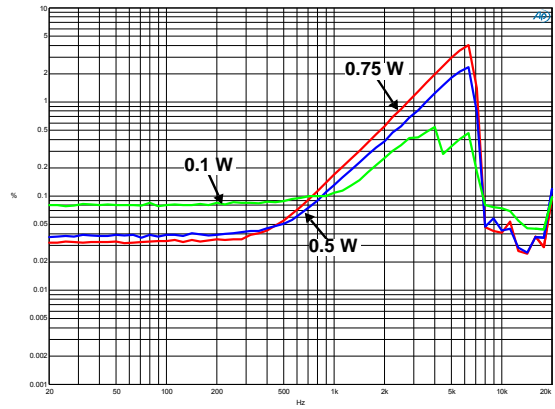


Figure 47. THD+N vs. Frequency - FHD Mode  
 $V_{BATT} = 4.2 V$

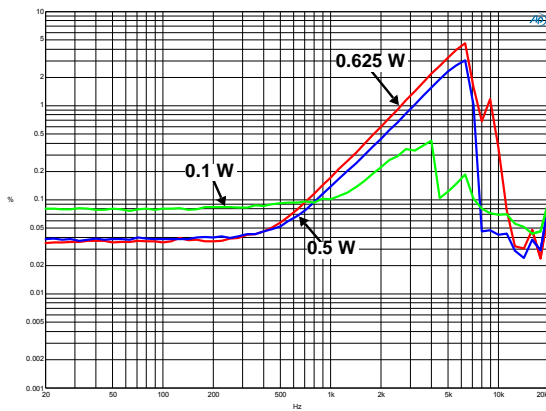


Figure 48. THD+N vs. Frequency - FHD Mode  
 $V_{BATT} = 3.7 V$

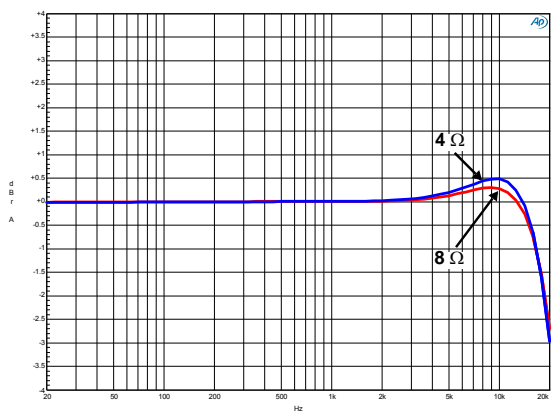
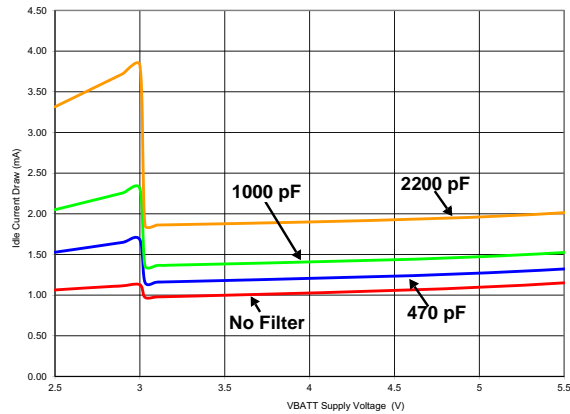
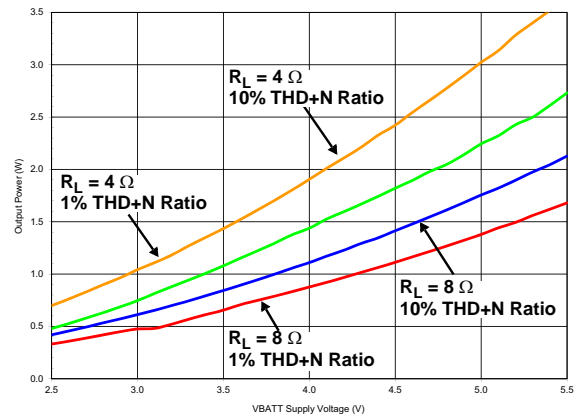


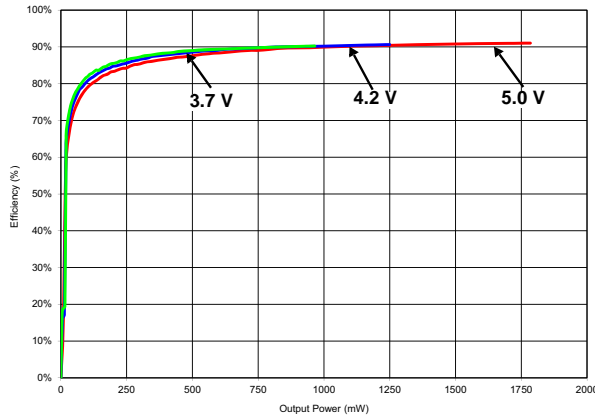
Figure 49. Frequency Response - FHD Mode



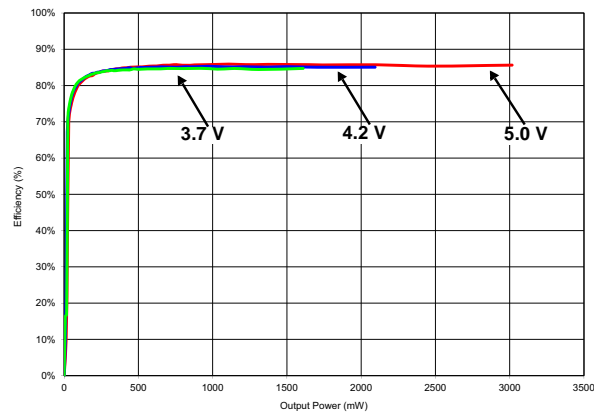
**Figure 50. Idle Current Draw vs. VBATT - FHD Mode**  
 $R_L = 8 \Omega + 33 \mu\text{H}$  (Note 19)



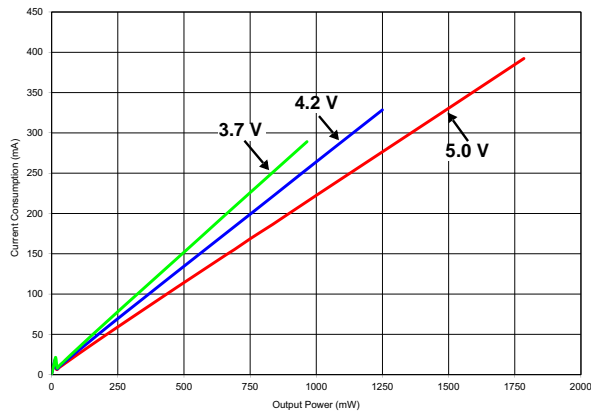
**Figure 51. Output Power vs. VBATT - FHD Mode**



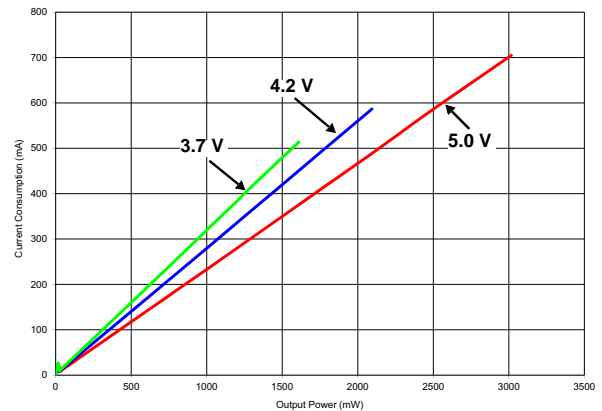
**Figure 52. Efficiency vs. Output Power - FHD Mode**  
 $R_L = 8 \Omega + 33 \mu\text{H}$



**Figure 53. Efficiency vs. Output Power - FHD Mode**  
 $R_L = 4 \Omega + 33 \mu\text{H}$



**Figure 54. Supply Current vs. Output Power - FHD Mode**  
 $R_L = 8 \Omega + 33 \mu\text{H}$



**Figure 55. Supply Current vs. Output Power - FHD Mode**  
 $R_L = 4 \Omega + 33 \mu\text{H}$

**Note:**

19. "Idle Current Draw vs. VBATT - FHD Mode" capacitor values refer to  $C_{\text{FILT}}$  when configured as the "CS35L01/03's Minimized Optional Output Filtering" shown in Figure 5 on page 17. When VBATT is below "VBATT Limit for HD/FHD Mode" ( $V_{\text{BLIM}}$ ), operation is restricted to SD Mode.

## 7. PARAMETER DEFINITIONS

### Signal to Noise Ratio (SNR)

The ratio of the RMS value of the output signal, where  $P_{out}$  is equivalent to the specified output power at  $THD+N < 1\%$ , to the RMS value of the noise floor with no input signal applied and measured over the specified bandwidth, typically 20 Hz to 20 kHz. This measurement technique has been accepted by the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

### Total Harmonic Distortion + Noise (THD+N)

The ratio of the RMS value of the signal to the RMS sum of all other spectral components over the specified band width (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

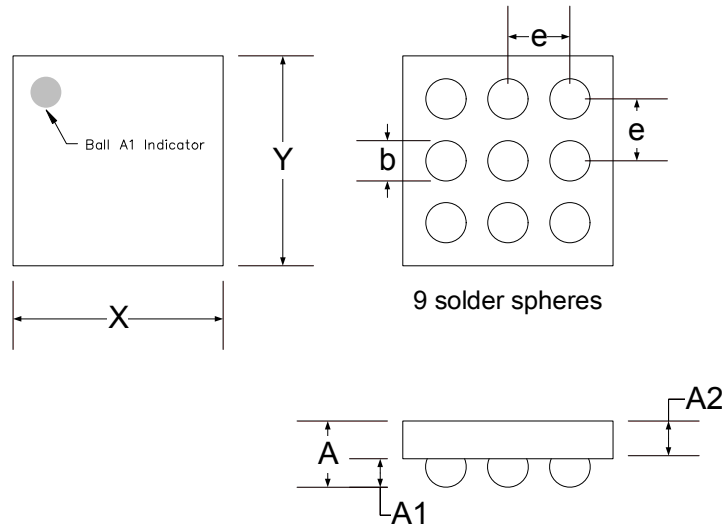
### Idle Channel Noise (ICN)

Measure of the signal present on the outputs of the device when no audio signal is presented to the input pins. For this test, both input pins are shorted together, setting the differential signal to them to zero.

## 8. PACKAGING AND THERMAL INFORMATION

### 8.1 Package Drawings and Dimensions (Note 20)

#### 9 BALL WLCSP



DIM	INCHES			MILLIMETERS			NOTE
	MIN	NOM	MAX	MIN	NOM	MAX	
X	0.047	0.048	0.049	1.195	1.215	1.235	20
Y	0.047	0.048	0.049	1.195	1.215	1.235	20
b	0.009	0.011	0.012	0.240	0.270	0.300	
e	-	0.015	-	-	0.400 BSC	-	20
A	0.018	0.020	0.022	0.475	0.515	0.555	20
A1	0.006	0.007	0.008	0.175	0.190	0.205	20
A2	0.012	0.013	0.014	0.300	0.325	0.350	20

**JEDEC #: MO-220**

Controlling Dimension is Millimeters.

**Note:**

20. Dimensioning and tolerance per ASME Y 14.5M-1994.

## 8.2 Recommend PCB Footprint and Routing Configuration

To ensure high-yield manufacturability, the PCB footprint for the CS35L01/03 should be constructed with strict adherence to the specifications given in IPC-610. Departure from this specification significantly increases the probability of solder bridging and other manufacturing defects.

Routing of the traces into and out of the CS35L01/03 device should also be given consideration to avoid manufacturing issues.

## 8.3 Package Thermal Performance

Class-D amplifiers, though highly efficient, will produce some amount of heat through the process of amplifying the audio signal. As is well understood, this amount of heat is very small compared to traditional Class AB amplifiers. Even so, as power levels increase and package sizes decrease, careful consideration must be given to ensure thermal energy is removed from the device as efficiently as possible so that its operating temperature is kept under its Over-Temperature Error Threshold.

The thermal impedance,  $\theta_{JA}$  is a measurement of the impedance to the flow of thermal energy out of the device to the environment surrounding the device. This specification is directly related to the ability of the PCB to which the CS35L01/03 is attached to transfer the heat from the device. The thermal impedance from the junction of the device to the ambient surrounding the device and the thermal impedance from the device into the PCB is shown in [Table 2](#).

Parameter (Note 21), (Note 22)	Symbol	Min	Typical	Max	Units
Junction to Ambient Thermal Impedance	$\theta_A$	-	92	-	°C/Watt
Junction to Printed Circuit Board Thermal Impedance	$\theta_{PCB}$	-	67	-	°C/Watt

**Table 2.  $\theta_{JA}$  Specification for Typical PCB Designs**

**Note:**

21. Test Printed Circuit Board Assembly (PCBA) constructed in accordance with JEDEC standard JESD51-9. Two signal, two plane (2s2p) PCB utilized.
22. Test conducted with still air in accordance with JEDEC standards JESD51, JESD51-2A, and JESD51-8.

### 8.3.1 Determining Maximum Ambient Temperature

To determine (to a first order approximation) the maximum ambient temperature in which the CS35L01/03 will operate, the following equations can be used:

$$T_{op} = \theta_{JA} \times ((1 - \eta) \times P_{max})$$

$$T_{max} = T_{TE} - T_{op}$$

Where:

$T_{max}$  = The maximum ambient temperature in which the device can operate.

$T_{op}$  = The operating temperature of the device, given a dissipated power " $P_{max}$ " and a known thermal impedance " $\theta_{JA}$ ".

$T_{TE}$  = The Over-Temperature Error Threshold, given in the ["Electrical Characteristics - All Operational Modes" section on page 9](#).

$\theta_{JA}$  = The thermal impedance of the device and PCB. (This value is highly subjective to a number of application specific scenarios. The numbers given in [Table 2 on page 31](#) can be used for a first order approximation, but proper characterization of the application's specific PCB and supporting mechanicals is needed to increase the accuracy of the result achieved here.)

$P_{max}$  = The maximum power at which the amplifier will be operated continuously. (For conservative estimates, the 10% THD+N rated power given in ["Electrical Characteristics - SD Mode" section on page 10](#), ["Electrical Characteristics - FSD Mode" section on page 11](#), ["Electrical Characteristics - HD Mode" section on page 12](#), or ["Electrical Characteristics - FHD Mode" section on page 13](#) can be used. However, this method will predict higher operating temperatures than what may be seen in the application, since power content of audio signals is much smaller than that of the sine wave used to establish the power specifications.)

$\eta$  = The efficiency of the device at the power  $P_{max}$ .



## 9. ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order#
CS35L01	3.0 W Mono Audio Amplifier with default +6 dB gain	9-WLCSP	Yes	Commercial	-10° to +70°C	Tape and Reel	CS35L01-CWZR
CS35L03	3.0 W Mono Audio Amplifier with default +12 dB gain	9-WLCSP	Yes	Commercial	-10° to +70°C	Tape and Reel	CS35L03-CWZR

## 10. REVISION HISTORY

Release	Changes
F1	– Initial release

### Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.

To find one nearest you, go to [www.cirrus.com](http://www.cirrus.com).

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