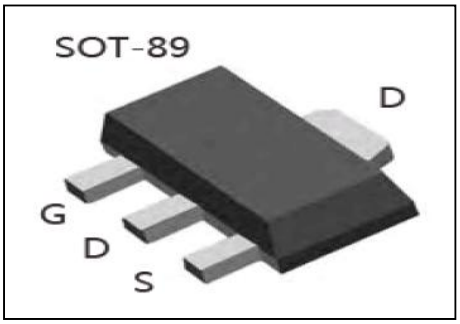
Silicon N-Channel Power MOSFET ®

CS3N20 ATH

V_{DSS}	200	V
I_D	3	A
$P_D(T_C=25℃)$	2.5	W
$R_{DS(ON)Typ}$	1.2	Ω



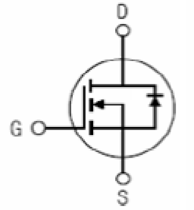
General Description:

CS3N20 ATH, the silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is SOT-89, which accords with the RoHS standard.

Features:

- **Fast Switching**
- **Low ON Resistance(Rdson**≤1.5Ω)
- **Low Gate Charge (Typical Data: 4.3nC)**
- **Low Reverse transfer capacitances(Typical:5.5pF)**
- **100% Single Pulse avalanche energy Test**

Inner Equivalent Principium Chart



Applications:

Power switch circuit of adaptor and charger.

Absolute（Tc= 25℃ unless otherwise specified）:

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	200	V
I_D	Continuous Drain Current	3	A
	Continuous Drain Current T_C = 100 °C	1.9	A
I_{DM} [a1]	Pulsed Drain Current	12	A
V_{GS}	Gate-to-Source Voltage	±30	V
E_{AS} [a2]	Single Pulse Avalanche Energy	28	mJ
dv/dt [a3]	Peak Diode Recovery dv/dt	5.0	V/ns
P_D	Power Dissipation	2.5	W
	Derating Factor above 25°C	0.02	W/℃
T_J，T_{stg}	Operating Junction and Storage Temperature Range	150，–55 to 150	℃
T_L	Maximum Temperature for Soldering	300	℃

Electrical Characteristics（Tc= 25℃ unless otherwise specified）:

OFF Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	200	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Bvdss Temperature Coefficient	ID=250uA,Reference25℃	--	0.25	--	V/℃
I_{DSS}	Drain to Source Leakage Current	V_{DS} =200V, V_{GS}= 0V, T_a = 25℃	--	--	1	μA
		V_{DS} =160V, V_{GS}= 0V, T_a = 125℃	--	--	100	μA
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS} =+30V	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS} =-30V	--	--	-100	nA

ON Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	V_{GS}=10V,I_D=1.5A	--	1.2	1.5	Ω
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	2.0	--	4.0	V
Pulse width tp≤300μs, δ ≤2%						

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
C_{iss}	Input Capacitance	V_{GS} = 0V V_{DS} = 25V f = 1.0MHz	--	101	--	pF
C_{oss}	Output Capacitance		--	23	--	
C_{rss}	Reverse Transfer Capacitance		--	5.5	--	

Resistive Switching Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	I_D =3A V_{DD} = 100V R_G =10Ω	--	7	--	ns
tr	Rise Time		--	12	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	27	--	
t_f	Fall Time		--	7	--	
Q_g	Total Gate Charge	I_D =3A V_{DD} =160V V_{GS} = 10V	--	4.3	--	nC
Q_{gs}	Gate to Source Charge		--	1.4	--	
Q_{gd}	Gate to Drain (“Miller”)Charge		--	1.6	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current (Body Diode)		--	--	3	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	12	A
V_{SD}	Diode Forward Voltage	I_S=3.0A,V_{GS}=0V	--	--	1.5	V
trr	Reverse Recovery Time	I_S=3.0A,T_j = 25℃ dI_F/dt=100A/us, V_{GS}=0V	--	87	--	ns
Qrr	Reverse Recovery Charge		--	223	--	nC
I_{RRM}	Reverse Recovery Current		--	5.2	--	A
Pulse width tp≤300μs, δ ≤2%						

Symbol	Parameter	Max.	Units
$R_{\theta JC}$	Junction-to-Case	50	℃/W
$R_{\theta JA}$	Junction-to-Ambient	200	℃/W

[a1]: Repetitive rating; pulse width limited by maximum junction temperature

[a2]: L=10mH, I_D=2.4A, Start T_J=25℃

[a3]: I_{SD} =3A,di/dt ≤100A/us,V_{DD}≤BV_{DS}, Start T_J=25℃

Characteristics Curve:

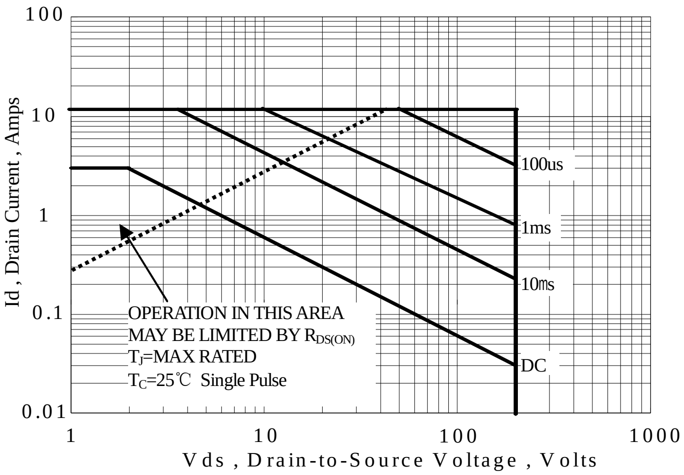


Figure 1 Maximum Forward Bias Safe Operating Area

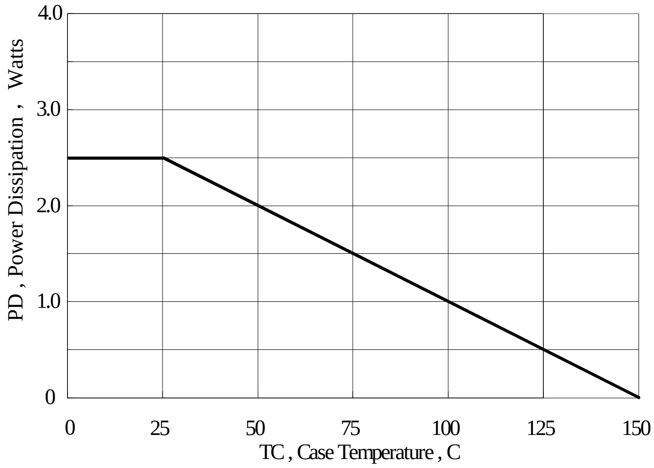


Figure 2 Maximum Power Dissipation vs Case Temperature

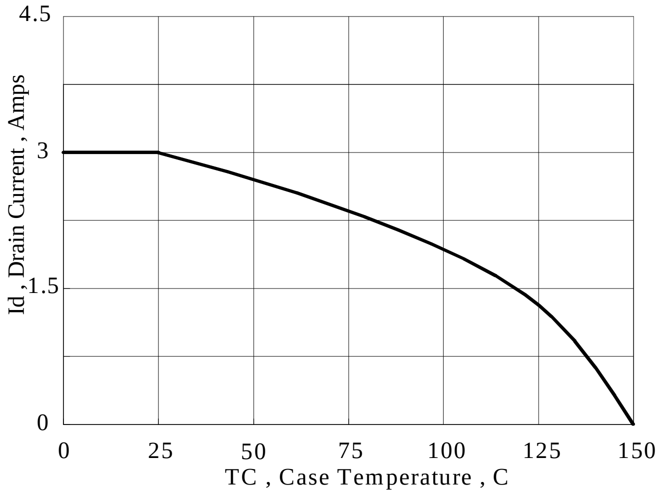


Figure 3 Maximum Continuous Drain Current vs Case Temperature

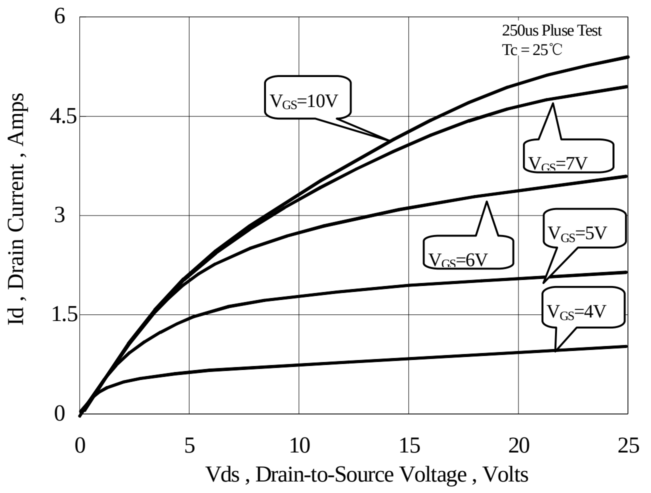


Figure 4 Typical Output Characteristics

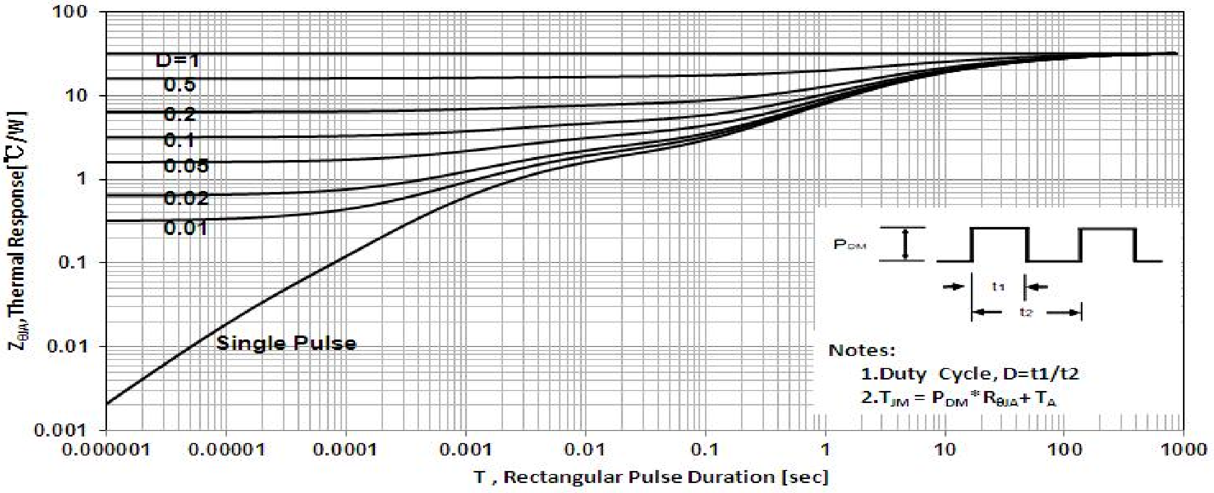


Figure 5 Maximum Effective Thermal Impedance , Junction to Case

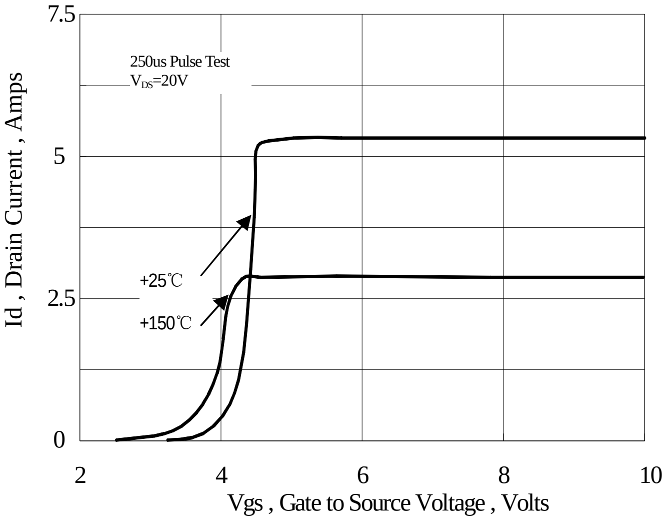


Figure 6 Typical Transfer Characteristics

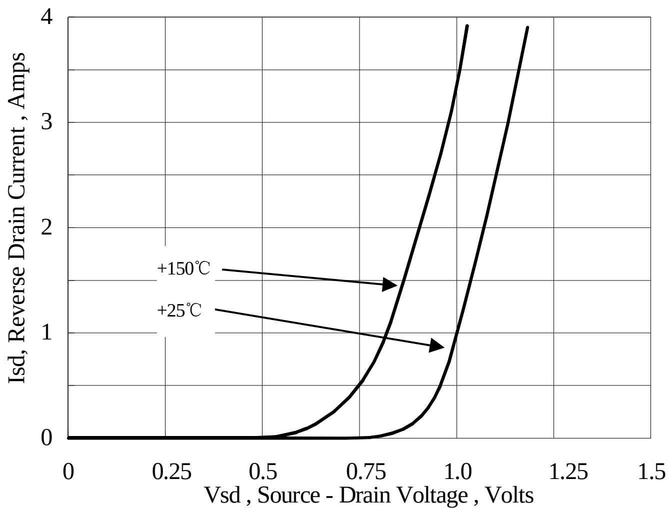


Figure 7 Typical Body Diode Transfer Characteristics

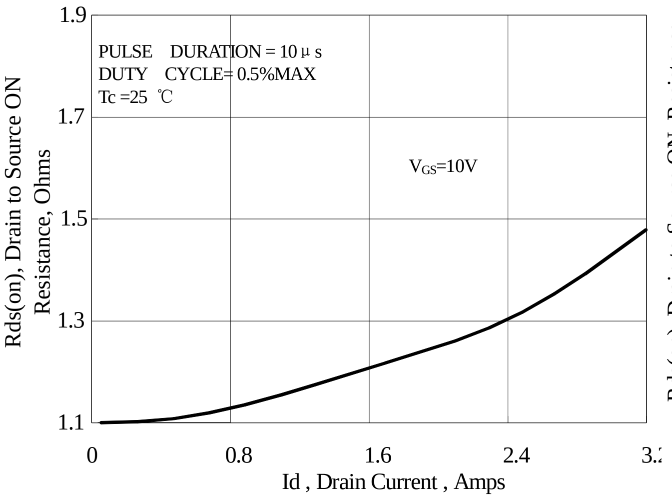


Figure 8 Typical Drain to Source ON Resistance
vs Drain Current

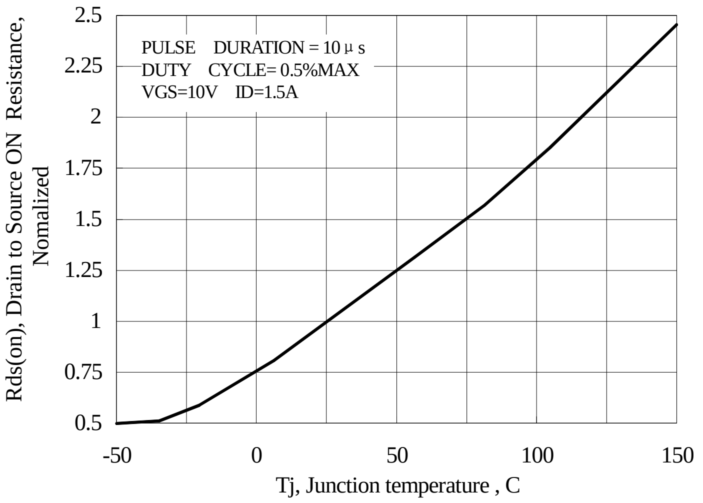


Figure 9 Typical Drian to Source on Resistance
vs Junction Temperature

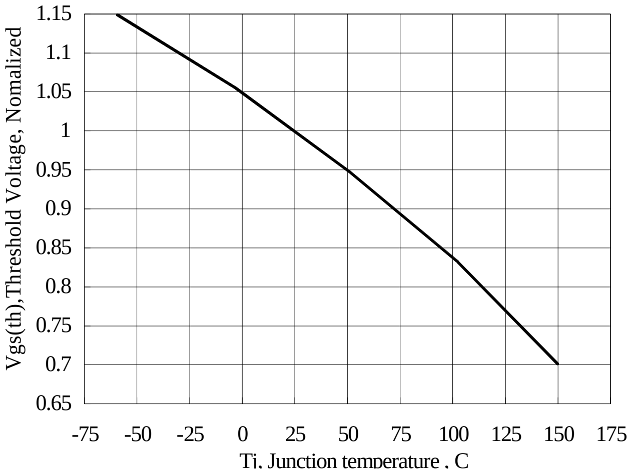


Figure 10 Typical Theshold Voltage vs Junction Temperature

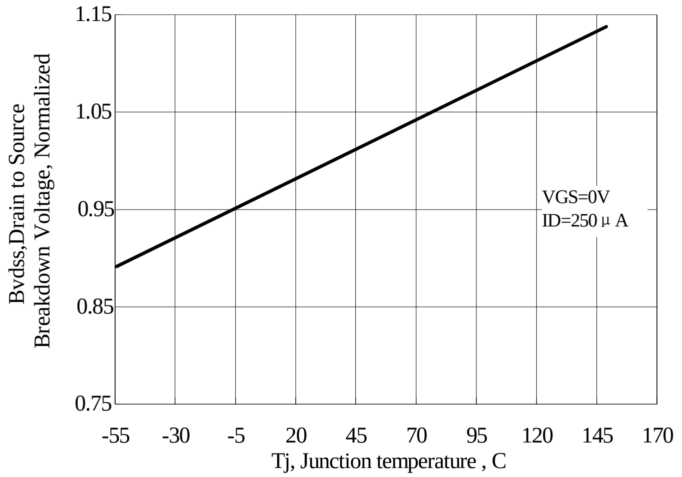


Figure 11 Typical Breakdown Voltage vs Junction Temperature

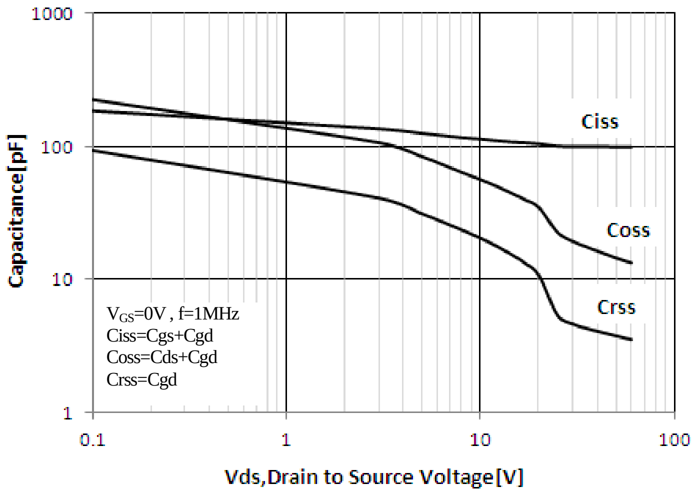


Figure 12 Typical Capacitance vs Drain to Source Voltage

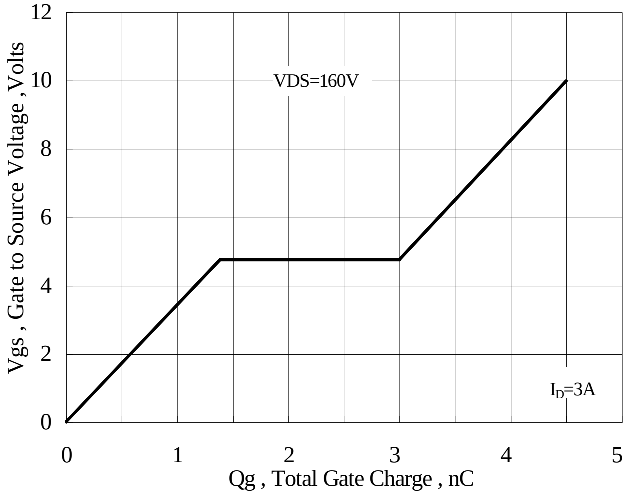


Figure 13 Typical Gate Charge vs Gate to Source Voltage

Test Circuit and Waveform：

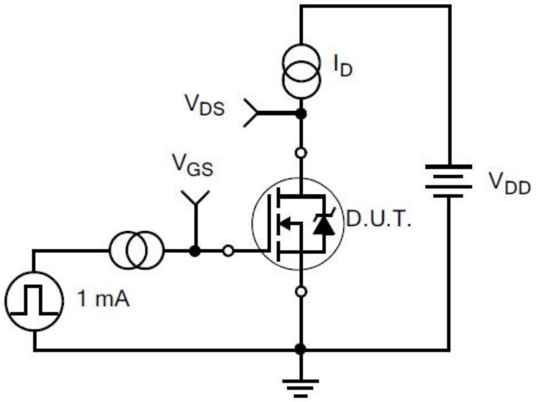


Figure 17. Gate Charge Test Circuit

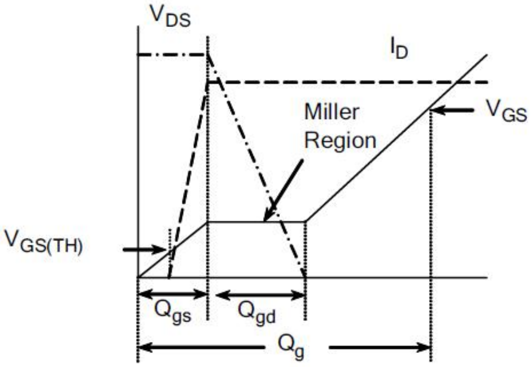


Figure 18. Gate Charge Waveform

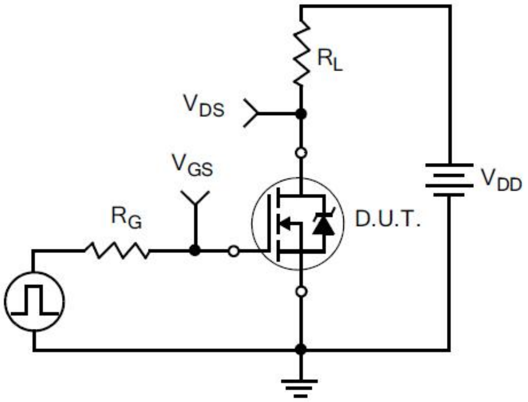


Figure 19. Resistive Switching Test Circuit

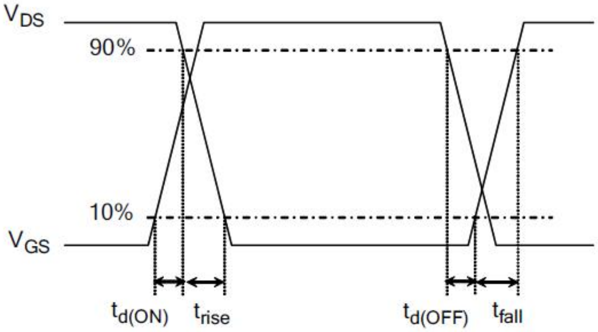


Figure 20. Resistive Switching Waveforms

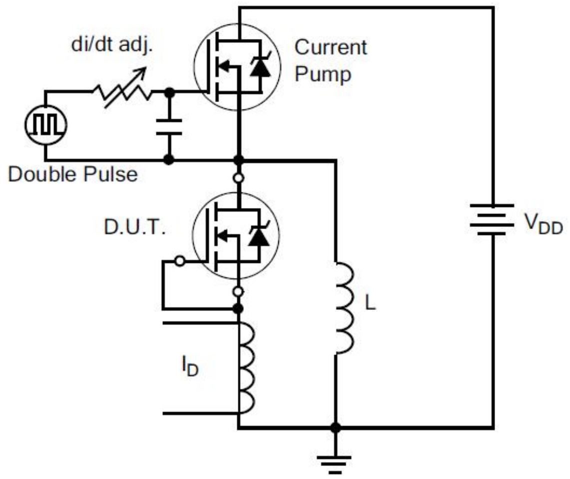


Figure 21. Diode Reverse Recovery Test Circuit

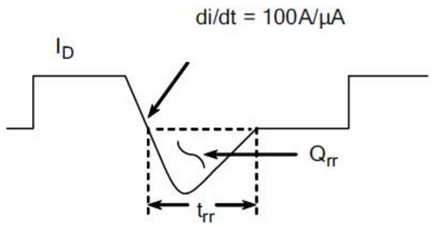


Figure 22. Diode Reverse Recovery Waveform

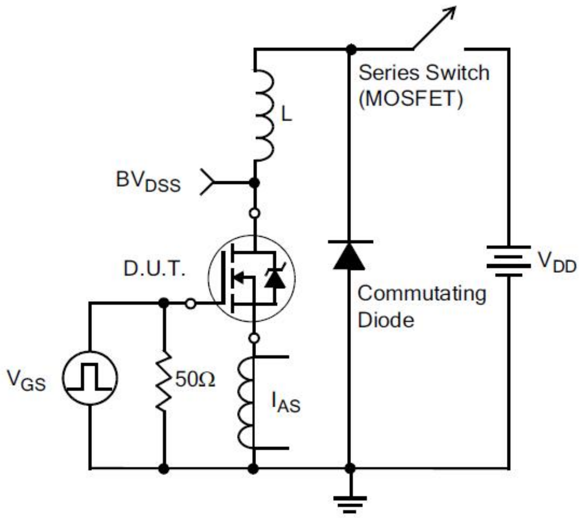
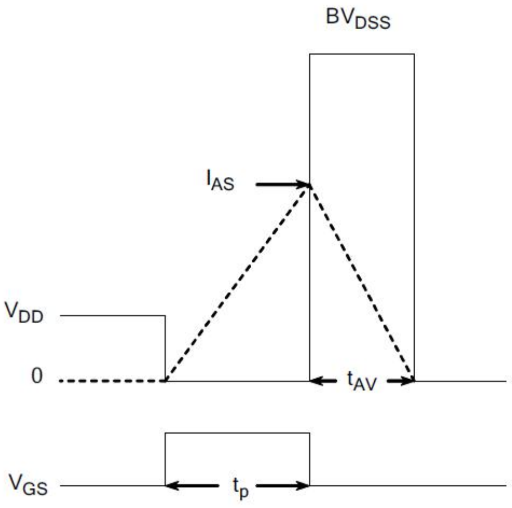


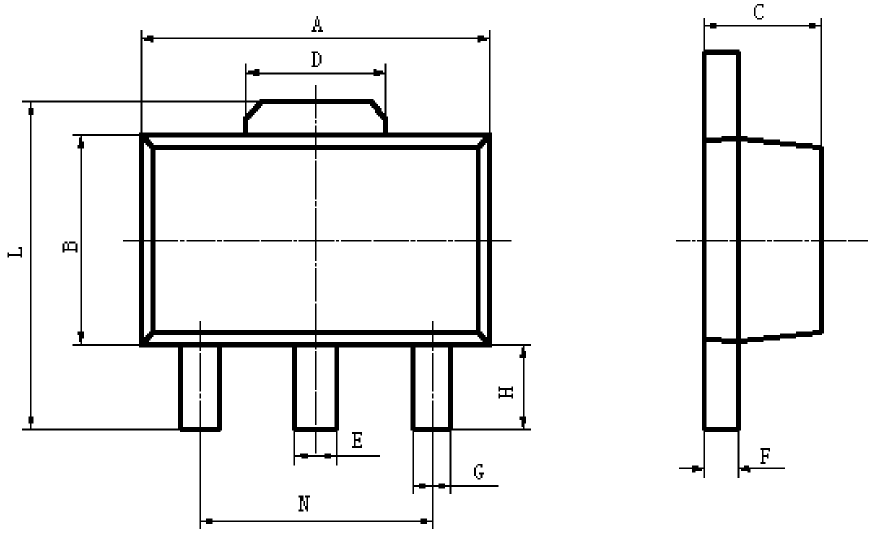
Figure 23. Unclamped Inductive Switching Test Circuit



$$E_{AS} = \frac{I_{AS}{}^2 L}{2}$$

Figure 24. Unclamped Inductive Switching Waveforms

Package Information:



Items	Values(mm)	
	MIN	MAX
A	4.30	4.70
B	2.20	2.70
C	1.30	1.70
D	1.30	1.90
E	0.36	0.56
F	0.35	0.45
G	0.32	0.52
H	0.70	1.20
L	3.75	4.35
N	2.90	3.10

SOT-89 Package

The name and content of poisonous and harmful material in products

Part’s Name	**Hazardous Substance**									
	Pb	Hg	Cd	Cr(VI)	PBB	PBDE	DIBP	DEHP	DBP	BBP
Limit	≤ 0.1%	≤ 0.1%	≤ 0.01%	≤0.1%	≤0.1%	≤0.1%	≤0.1%	≤0.1%	≤0.1%	≤0.1%
Lead Frame	○	○	〇	〇	〇	〇	〇	〇	〇	〇
Molding	○	○	〇	〇	〇	〇	〇	〇	〇	〇
Chip	○	○	〇	〇	〇	〇	〇	〇	〇	〇
Wire Bonding	○	○	〇	〇	〇	〇	〇	〇	〇	〇
Solder	×	○	〇	〇	〇	〇	〇	〇	〇	〇
Note	○：Means the hazardous material is under the criterion of 2011/65/EU. ×：Means the hazardous material exceeds the criterion of 2011/65/EU. The plumbum element of solder exist in products presently, but within the allowed range of Eurogroup’s RoHS.									

Warnings

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. It is suggested to be used under 80 percent of the maximum ratings of the device.
2. When installing the heat sink, please pay attention to the torsional moment and the smoothness of the heat sink.
3. VDMOSFETs is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
4. This publication is made by Huajing Microelectronics and subject to regular change without notice.

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