FEATURES

- **Full DOS Games Compatibility via PC/PCI, DDMA, and CrystalClear Legacy Support™**
- **PCI Version 2.1 Bus Master**
- **PC'97 and PC'98 Compliance (and compliance with preliminary PC '99)**
- **MPU-401 interface, FM synthesizer, and Game Port**
- **Full Duplex Operation**
- **Hardware Volume Control**
- **Win 95®, 98 (WDM), WinNT® 4.0, WinNT 5.0 (WDM) Drivers**
- **Pin-compatible Upgrade Path to CS4614, CS4622 and CS4624 with Common Software Stack**
- **Advanced Power Management (PPMI)**
- **Asynchronous Digital Serial Interface (ZV Port)**
- **Digital Docking Solution with AC97 2.0 Codec**

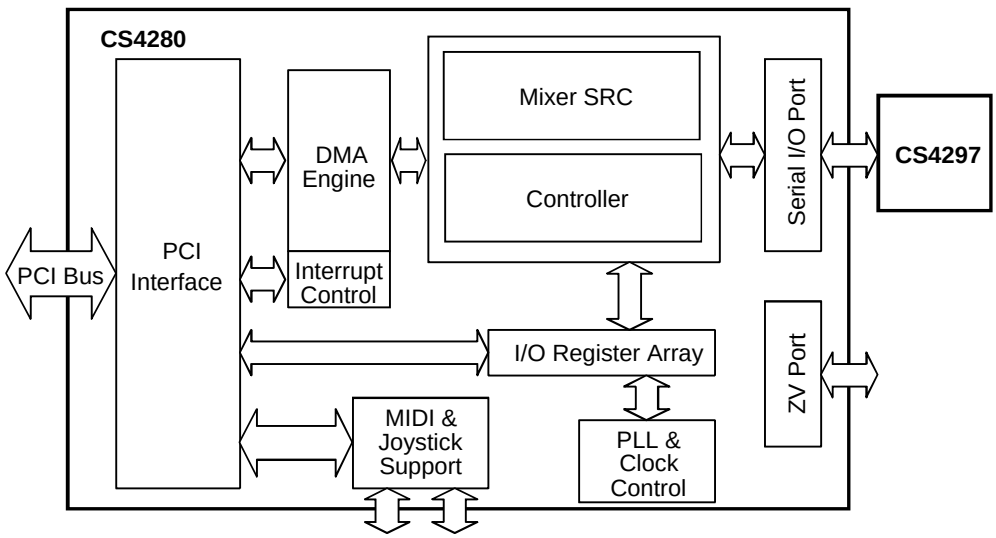
CrystalClear™ PCI Audio Interface

DESCRIPTION

The CS4280 is a PCI audio controller with integrated legacy games support suitable for desktop and notebook PC designs. When combined with driver software and an AC '97 codec such as the CS4297, this device provides a complete high quality audio solution. Legacy compatibility is achieved via PC-PCI, DDMA, and CrystalClear Legacy Support. The product includes an integrated FM synthesizer and Plug-and-Play interface. In addition, the CS4280 offers hardware volume control and power management features. WDM drivers provide support for Windows 98 and Windows NT. When used with the CS4297, the CS4280 is fully compliant with Microsoft's PC '98 audio requirements. In the 100-pin MQFP package, the CS4280 is pin-compatible with the CS4614, and the 128-pin TQFP package is a pin compatible subset of the CS4622/24.

ORDERING INFORMATION

CS4280-CM	100-pin MQFP	20x14x3.07 mm
CS4280-CQ	128-pin TQFP	20x14x1.60 mm



ABSOLUTE MAXIMUM RATINGS

(PCIGND = CGND = CRYGND = 0 V, all voltages with respect to 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Power Supplies	PCIVDD	-	-	4.6	V
	CVDD	-	-	4.6	V
	CRYVDD	-	-	4.6	V
	VDD5REF	-	-	5.5	V
Total Power Dissipation (Note 1)		-	-	1.5	W
Input Current per Pin, DC (Except supply pins)		-	-	10	mA
Output current per pin, DC		-	-	10	mA
Input voltage (Note 2)		-0.3	-	5.75	V
Ambient temperature (power applied) (Note 3)		-45	-	85	°C
Storage temperature		-55	-	150	°C

Notes: 1. Includes all power generated by AC and/or DC output loading.
2. The power supply pins are at recommended maximum values.
3. At ambient temperatures above 70° C, total power dissipation must be limited to less than 0.4 Watts.

WARNING: Operation beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(PCIGND = CGND = CRYGND = 0 V, all voltages with respect to 0 V)

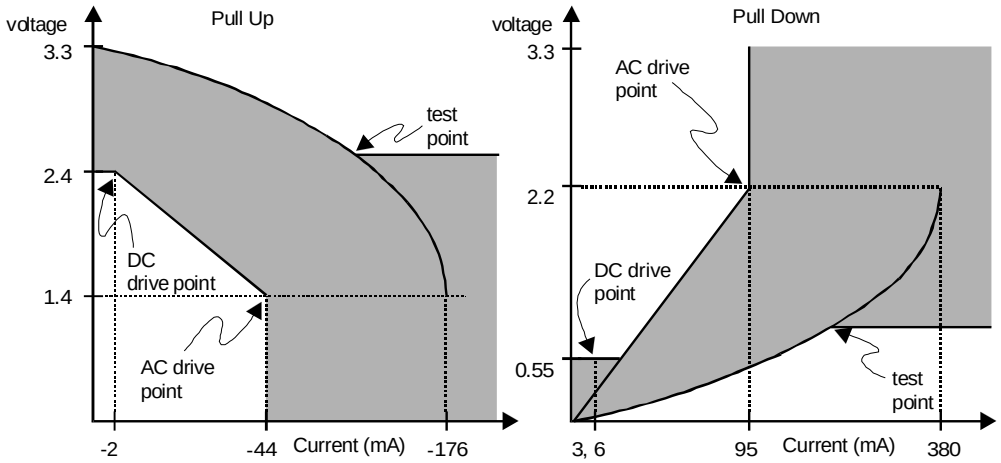
Parameter	Symbol	Min	Typ	Max	Unit
Power Supplies	PCIVDD	3	3.3	3.6	V
	CVDD	3	3.3	3.6	V
	CRYVDD	3	3.3	3.6	V
	VDD5REF	4.75	5	5.25	V
Operating Ambient Temperature	T_A	0	25	70	°C

Specifications are subject to change without notice.

AC CHARACTERISTICS (PCI SIGNAL PINS ONLY) (T_A = 70° C; PCIVDD = CVDD = CRYVDD = 3.3 V; VDD5REF = 5 V; PCIGND = CGND = CRYGND = 0 V; Logic 0 = 0 V, Logic 1 = 3.3 V; Reference levels = 1.4 V; unless otherwise noted; (Note 4))

Parameter			Symbol	Min	Max	Unit
Switching Current High		(Note 5)	I_{OH}			
		0 < Vout < 1.4		-44	-	mA
		1.4 < Vout < 2.4		$-44 + \frac{Vout - 1.4}{0.024}$	-	mA
		3.1 < Vout < 3.3		-	(Note 7)	
Switching Current Low		(Note 5)	I_{OL}			
		Vout > 2.2		95	-	mA
		2.2 > Vout > 0.55		Vout/0.023	-	mA
		0.71 > Vout > 0		-	(Note 8)	
Low Clamp Current		-5 < Vin < -1	I_{CL}	$-25 + \frac{Vin + 1}{0.015}$	-	mA
Output rise slew rate	0.4 V - 2.4 V load	(Note 6)	slewr	1	5	V/ns
Output fall slew rate	2.4 V - 0.4 V load	(Note 6)	slewf	1	5	V/ns

Notes:
4. Specifications guaranteed by characterization and not production testing.
5. Refer to V/I curves in Figure 1. Specification does not apply to PCICLK and RST# signals. Switching CurrentHighspecificationdoesnotapplytoSERR#,PME#,CLKRUN#,andINTA#whichareopendrainoutputs.
6. Cumulative edge rate across specified range. Rise slew rates do not apply to open drain outputs.
7. Equation A: I_{OH} = 11.9 * (Vout - 5.25) * (Vout + 2.45) for 3.3 V > Vout > 3.1 V
8. Equation B: I_{OL} = 78.5 * Vout * (4.4 - Vout) for 0 V < Vout < 0.71 V



Equation A:

$I_{OH} = 11.9*(Vout-5.25)*(Vout+2.45)$ for $3.3V > Vout > 3.1V$

Equation B:

$I_{OL} = 78.5*Vout*(4.4-Vout)$ for $0V < Vout < 0.71V$

Figure 1. AC Characteristics

DC CHARACTERISTICS (T_A = 70° C; PCIVDD = CVDD = CRYVDD = 3.3 V; VDD5REF = 5 V; PCIGND = CGND = CRYGND = 0 V; all voltages with respect to 0 V unless otherwise noted)

Parameter			Symbol	Min	Typ	Max	Unit
PCI Interface Signal Pins							
High level input voltage			V_{IH}	2	-	5.75	V
Low level input voltage			V_{IL}	-0.5	-	0.8	V
High level output voltage	Iout = -2 mA		V_{OH}	2.4	-	-	V
Low level output voltage	Iout = 3 mA, 6 mA	(Note 9)	V_{OL}	-	-	0.55	V
High level leakage current	Vin = 2.7 V	(Note 10)	I_{IH}	-	-	70	µA
Low level leakage current	Vin = 0.5 V(Note 10)		I_{IL}	-	-	-70	µA
Non-PCI Interface Signal Pins							
High level output voltage	Iout = -4 mA	(Note 11)	V_{OH}	2.4	-	-	V
Low level output voltage	Iout = 4 mA		V_{OL}	-	-	0.4	V
High level leakage current	Vin = 5.25 V		I_{IH}	-	-	10	µA
Low level leakage current	Vin = 0		I_{IL}	-	-	-10	µA

Parameter		Min	Typ	Max	Unit
Power Supply Pins (Outputs Unloaded)					
Power Supply Current: VDD5REF		-	0.6	-	mA
PCIVDD/CVDD/CRYVDD Total	(Notes 4)	-	164	TBD	mA
Low Power Mode Supply Current		-	10	-	mA

Notes:
9. The following signals are tested to 6 mA: FRAME#, TRDY#, IRDY#, DEVSEL#, STOP#, SERR#, PERR#, and INTA#. All other PCI interface signals are tested to 3 mA.
10. Input leakage currents include hi-Z output leakage for all bi-directional buffers with three-state outputs.
11. For open drain pins, high level output voltage is dependent on external pull-up used and number of attached gates.

PCI INTERFACE PINS (T_A = 0 to 70° C; PCIVDD = CVDD = CRYVDD = 3.3 V; VDD5REF = 5 V; PCIGND = CGND = CRYGND = 0 V; Logic 0 = 0 V, Logic 1 = 3.3 V; Timing reference levels = 1.4 V)

Parameter		Symbol	Min	Max	Unit
PCICLK cycle time		t_{cyc}	30	-	ns
PCICLK high time		t_{high}	11	-	ns
PCICLK low time		t_{low}	11	-	ns
PCICLK to signal valid delay - bused signals		t_{val}	2	11	ns
PCICLK to signal valid delay - point to point		$t_{val(p+p)}$	2	12	ns
Float to active delay	(Note 12)	t_{on}	2	-	ns
Active to Float delay	(Note 12)	t_{off}	-	28	ns
Input Set up Time to PCICLK - bused signals		t_{su}	7	-	ns
Input Set up Time to PCICLK - point to point		$t_{su(p+p)}$	10, 12	-	ns
Input hold time for PCICLK		t_h	0	-	ns
Reset active time after PCICLK stable	(Note 13)	$t_{rst-clk}$	100	-	µs
Reset active to output float delay	(Notes 12, 13, 14)	$t_{rst-off}$	-	40	ns

Notes: 12. For Active/Float measurements, the Hi-Z or “off” state is when the total current delivered is less than or equal to the leakage current. Specification is guaranteed by design, not production tested.
13. RST# is asserted and de-asserted asynchronously with respect to PCICLK.
14. All output drivers are asynchronously floated when RST# is active.

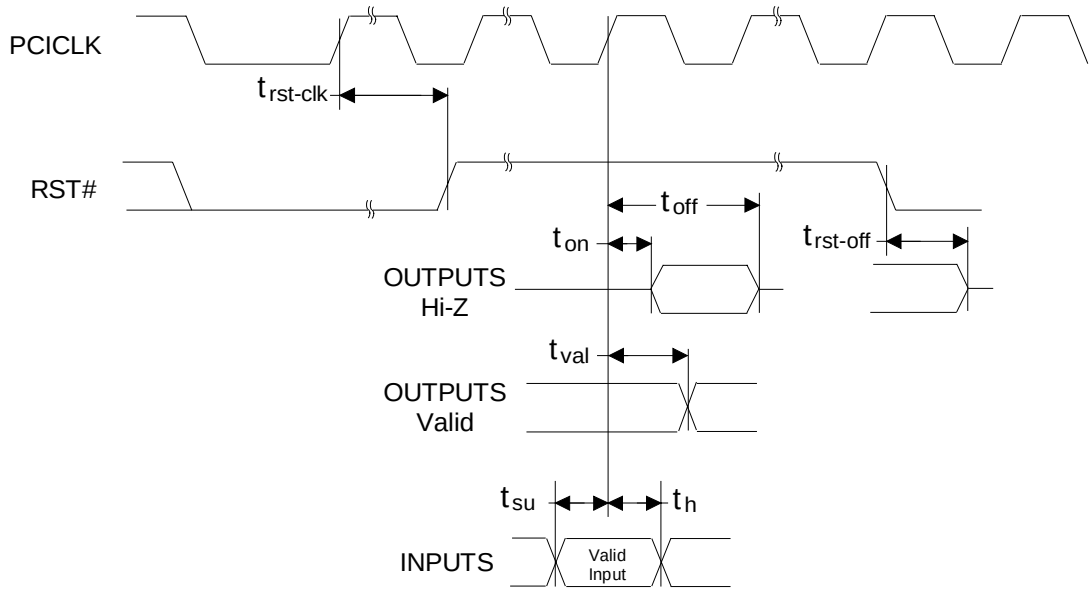


Figure 2. PCI Timing Measurement Conditions

AC '97 SERIAL INTERFACE TIMING (T_A = 0 to 70° C; PCIVDD = CVDD = CRYVDD = 3.3 V; VDD5REF = 5 V; VDD5REF = 5 V; PCIGND = CGND = CRYGND = 0 V; Logic 0 = 0 V, Logic 1 = 3.3 V; Timing reference levels = 1.4 V; unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit
ABITCLK cycle time	t_{aclk}	78	81.4	-	ns
ABITCLK rising to ASDOUT valid	t_{pd5}	-	17	25	ns
ASDIN valid to ABITCLK falling	t_{s5}	15	-	-	ns
ASDIN hold after ABITCLK falling	t_{h5}	5	-	-	ns
PCICLK rising to ARST# valid	t_{pd6}	-	10	-	ns

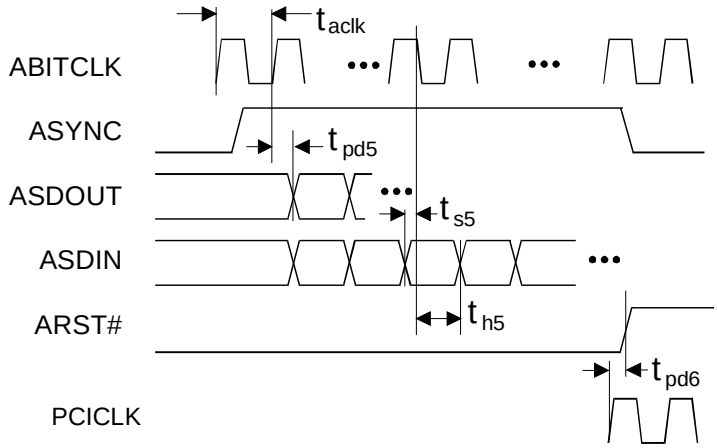


Figure 3. AC '97 Configuration Timing Diagram

ZV PORT TIMING

Parameter	Symbol	Min	Max	Unit
ZLRCK delay after ZSCLK rising	t_{slrd}	2	-	ns
ZLRCK setup before ZSCLK rising	t_{slrs}	32	-	ns
ZSCLK low period	t_{sclk}	22	-	ns
ZSCLK high period	t_{sclkh}	22	-	ns
ZSDATA setup to ZSCLK rising	t_{sdlrs}	32	-	ns
ZSDATA hold after ZSCLK rising	t_{sdh}	2	-	ns

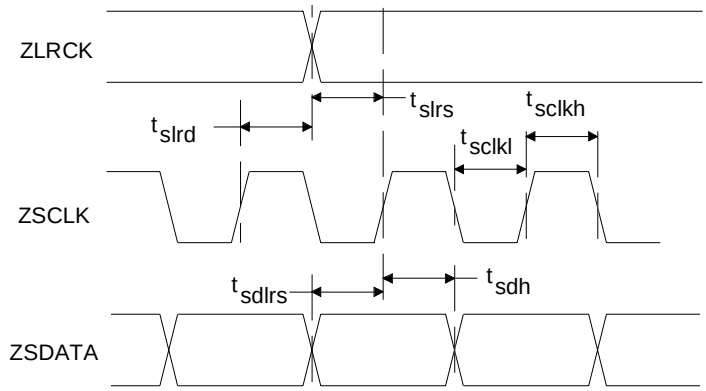


Figure 4. ZV PORT

EEPROM TIMING CHARACTERISTICS

Note 4. (T_A = 0 to 70 °C, PCIVDD = CVDD = CRYVDD = 3.3 V; VDD5REF = 5 V; VDD5REF = 5 V; PCIGND = CGND = CRYGND = 0 V; Logic 0 = 0 V, Logic 1 = 3.3 V; Timing reference levels = 1.4 V; PCI clock frequency = 33 MHz; unless otherwise noted)

Parameter	Symbol	Min	Max	Units
EECLK Low to EEDAT Data Out Valid	t_{AA}	0	7.0	µs
Start Condition Hold Time	$t_{HD:STA}$	5.0	-	µs
EECLK Low	t_{LEECLK}	10	-	µs
EECLK High	t_{HEECLK}	10	-	µs
Start Condition Setup Time (for a Repeated Start Condition)	$t_{SU:STA}$	5.0	-	µs
EEDAT In Hold Time	$t_{HD:DAT}$	0	-	µs
EEDAT In Setup Time	$t_{SU:DAT}$	250	-	ns
EEDAT/EECLK Rise Time (Note 15)	t_R	-	1	µs
EEDAT/EECLK Fall Time	t_F	-	300	ns
Stop Condition Setup Time	$t_{SU:STO}$	5.0	-	µs
EEDAT Out Hold Time	t_{DH}	0	-	µs

Notes: 15. Rise time on EEDAT is determined by the capacitance on the EEDAT line with all connected gates and the required external pull-up resistor.

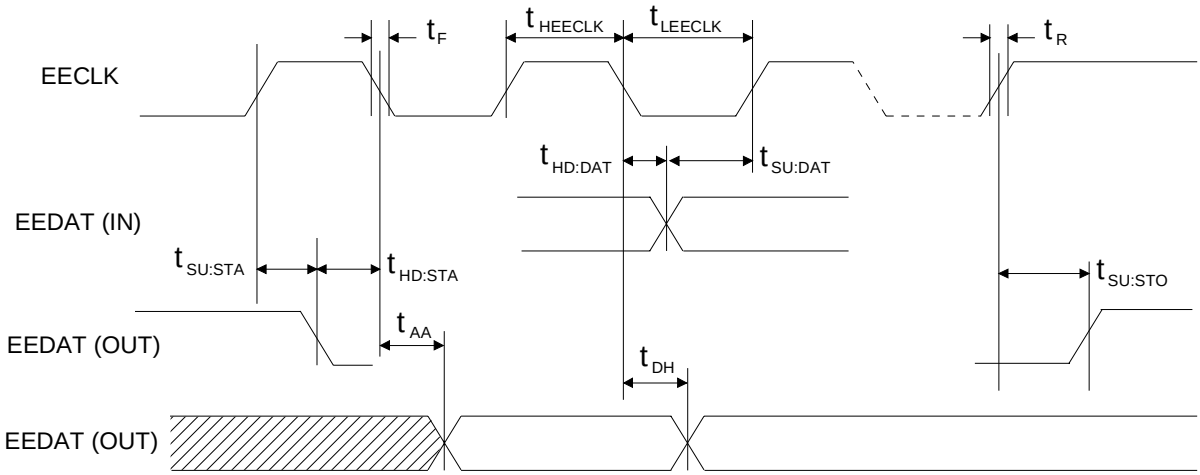


Figure 5. EEPROM Timing

OVERVIEW

The CS4280 provides a low-cost PCI audio solution with Legacy Game compatibility for the PC environment. The CS4280 is compatible with the CS4614, CS4622, and CS4624.

There are two main functional blocks within the CS4280: the PCI Interface, and the DMA Engine. A block diagram of the CS4280 device is shown on the front cover.

The CS4280 provides an extremely efficient bus mastering interface to the PCI bus. The PCI Interface function allows economical burst mode transfers of audio data between host system memory buffers and the CS4280 device.

The DMA Engine provides dedicated hardware to manage transfer of up to 4 concurrent audio/data streams to and from host memory buffers. The DMA Engine provides hardware scatter-gather support, allowing simple buffer allocation and management. This implementation improves system efficiency by minimizing the number of host interrupts.

The CS4280 supports the CS4297 PCI CrystalClear audio AC'97 Codec. The system's flexibility is further enhanced by the ZV Port interface, a bidirectional serial MIDI port, a joystick port, a hardware volume control interface, and a serial data port which allows connection of an optional external EEPROM device.

Legacy Support

Legacy games are supported by CrystalClear Legacy Support (CCLS), DDMA, or by the PC/PCI interface.

In both motherboard and add-in card designs, CCLS and DDMA provide support for legacy games by providing a hardware interface that supports a Sound Blaster Pro compatible interface, as well as support for FM, MPU-401, and joystick interfaces. These hardware interfaces provide PCI-only games compatibility for real-mode DOS and Windows DOS-box support.

For motherboard designs, PC/PCI can be used by connecting the PCGNT# and PCREQ# pins to the appropriate pins on the south bridge motherboard chip. The PC/PCI interface is compliant with Intel's PC/PCI spec. (version 1.2). The BIOS must enable the PC/PCI mechanism at boot time on both the CS461422/24 and the south bridge.

SYSTEM ARCHITECTURES

A typical system diagram depicting connection of the CS4280 to the CrystalClear CS4297 AC '97 Codec is given in Figure 6. All analog audio inputs and outputs are connected to the CS4297. Audio data is passed between the CS4297 and the CS4280 over the serial AC-Link. The CS4280 provides a hardware interface for connection of a joystick and MIDI devices.

HOST INTERFACE

The CS4280 host interface is comprised of two separate interface blocks which are memory mapped into host address space. The interface blocks can be located anywhere in the host 32-bit physical address space. The interface block locations are defined by the addresses programmed into the two Base Address Registers in the PCI Configuration Space. These base addresses are normally set up by the system's Plug and Play BIOS. The first interface block (located by Base Address 0) is a 4 kByte register block containing general purpose configuration, control, and status registers for the device. The second interface block (located by Base Address 1) is a 1 MByte block which maps all of the internal DMA and controller memories into host memory space. The relationship between the Base Address Registers in the CS4280 PCI Configuration Space and the host memory map is depicted in Figure 7.

The bus mastering PCI bus interface complies with the PCI Local Bus Specification (version 2.1).

PCI bus transactions

As a target of a PCI bus transaction, the CS4280 supports the Memory Read (from internal registers or memory), Memory Write (to internal registers or memory), Configuration Read (from CS4280 configuration registers), Configuration Write (to CS4280 configuration registers), Memory Read Multiple (aliased to Memory Read), Memory Read Line (aliased to Memory Read), and the Memory Write and Invalidate (aliased to Memory Write) transfer cycles. The I/O Read, I/O Write, Interrupt Acknowledge, Special Cycles, and Dual Address Cycle transactions are not supported.

As Bus Master, the CS4280 generates the Memory Read Multiple and Memory Write transactions. The Memory Read, Configuration Read, Configuration Write, Memory Read Line, Memory Write and Invalidate, I/O Read, I/O Write, Interrupt Acknowledge, Special Cycles, and Dual Address Cycle transactions are not generated.

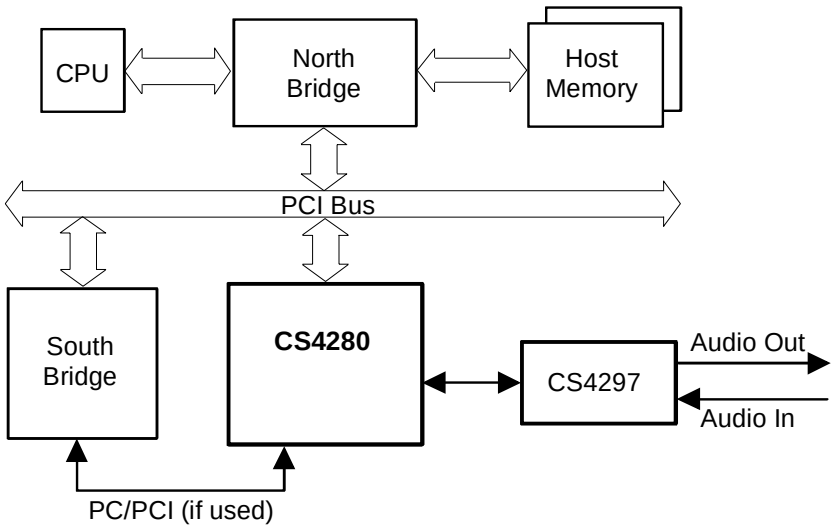


Figure 6. AC '97 Codec Interface

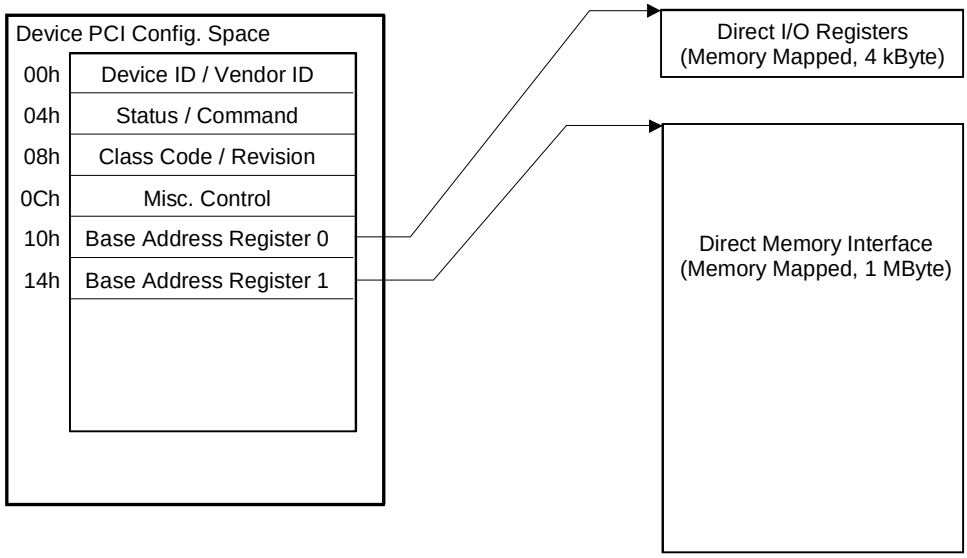


Figure 7. Host Interface Base Address Registers

The PCI bus transactions supported by the CS4280 device are summarized in Table 1. Note that no Target Abort conditions are signalled by the device. Byte, Word, and Doubleword transfers are supported for Configuration Space accesses. Only Doubleword transfers are supported for Register or Memory area accesses. Bursting is not supported for host-initiated transfers to/from the CS4280 internal register space, RAM memory space, or PCI configuration space (disconnect after first phase of transaction is completed).

Configuration Space

The content and format of the PCI Configuration Space is given in Table 2.

Initiator	Target	Type	PCI Dir
Host	Registers (BA0)	Mem Write	In
Host	Registers (BA0)	Mem Read	Out
Host	Memories (BA1)	Mem Write	In
Host	Memories (BA1)	Mem Read	Out
Host	Config Space 1	Config Write	In
Host	Config Space 1	Config Read	Out
DMA	Host System	Mem Write	Out
DMA	Host System	Mem Read	In

Table 1. PCI Interface Transaction Summary

Byte 3	Byte 2	Byte 1	Byte 0	Offset
Device ID: R/O, 6003h		Vendor ID: R/O, 1013h		00h
Status Register, bits 15-0: Bit 15 Detected Parity Error: Error Bit Bit 14 Signalled SERR: Error Bit Bit 13 Received Master Abort: Error Bit Bit 12 Received Target Abort: Error Bit Bit 11 Signalled Target Abort: Error Bit Bit 10-9 DEVSEL Timing: R/O, 01b (medium) Bit 8 Data Parity Error Detected: Error Bit Bit 7 Fast Back to Back Capable: R/O 0 Bit 6-0 UDF, 66MHz, Reserved: R/O 0000000 Reset Status State: 0200h Write of 1 to any error bit position clears it.		Command Register, bits 15-0: Bit 15-10: Reserved, R/O 0 Bit 9 Fast B2B Enable: R/O 0 Bit 8 SERR Enable: R/W, default 0 Bit 7 Wait Control: R/O 0 Bit 6 Parity Error Response: R/W, default 0 Bit 5 VGA Palette Snoop: R/O 0 Bit 4 MWI Enable: R/O 0 Bit 3 Special Cycles: R/O 0 Bit 2 Bus Master Enable: R/W, default 0 Bit 1 Memory Space Enable: R/W, default 0 Bit 0 IO Space Enable: R/O 0		04h
Class Code: R/O 040100h Class 04h (multimedia device), Sub-class 01h (audio), Interface 00h			Revision ID: R/O 01h	08h
BIST: R/O 0	Header Type: Bit 7: R/O 0 Bit 6-0: R/O 0 (type 0)	Latency Timer: Bit 7-3: R/W,default 0 Bit 2-0: R/O 0	Cache Line Size: R/O 0	0Ch
Base Address Register 0 Device Control Register space, memory mapped. 4 kByte size Bit 31-12: R/W, default 0. Compare address for register space accesses Bit 11 - 4: R/O 0, specifies 4 kByte size Bit 3: R/O 0, Not Prefetchable (Cacheable) Bit 2-1: R/O 00, Location Type - Anywhere in 32 bit address space Bit 0: R/O 0, Memory space indicator				10h
Base Address Register 1 Device Memory Array mapped into host system memory space, 1 MByte size Bit 31-20: R/W, default 0. Compare address for memory array accesses Bit 19 - 4: R/O 0, specifies 1 MByte size Bit 3: R/O 0, Not Prefetchable (Cacheable) Bit 2-1: R/O 00, Location Type - Anywhere in 32 bit address space Bit 0: R/O 0, Memory space indicator				14h
Base Address Register 2: R/O 00000000h, Unused				18h
Base Address Register 3: R/O 00000000h, Unused				1Ch
Base Address Register 4: R/O 00000000h, Unused				20h
Base Address Register 5: R/O 00000000h, Unused				24h
Cardbus CIS Pointer: R/O 00000000h, Unused				28h
Subsystem ID R/O 0000h if EXTEE not present, otherwise R/W, loaded from EEPROM		Subsystem Vendor ID R/O 0000h if EXTEE not present, otherwise R/W, loaded from EEPROM		2Ch

Table 2. PCI Configuration Space

Byte 3	Byte 2	Byte 1	Byte 0	Offset
Expansion ROM Base Address: R/O 00000000h, Unused				30h
Reserved: R/O 01000000h				34h
Reserved: R/O 00000000h				38h
Max_Lat: R/O 18h 24 x 0.25uS = 6 uS	Min_Gnt: R/O 04h 4 x 0.25uS = 1uS	Interrupt Pin: R/O 01h, INTA used	Interrupt Line: R/W, default 0	3Ch
PMC Bit 15: PME# from D3cold: R/O 0 Bit 14: PME# from D3hot: R/O 1 Bit 13: PME# from D2: R/O 1 Bit 12: PME# from D1: R/O 1 Bit 11: PME# from D0: R/O 1 Bit 10: D2 support: R/O 1 Bit 9: D1 support: R/O 1 Bit 8-6: Auxillary current: R/O 000 Bit 5: Device Specific init: R/O 1 Bit 4: Auxiliary power: R/O 0 Bit 3: PME# clock: R/O 1 Bit 2-0: Version: R/O 010		Next Item Pointer: R/O 0h	Capability ID: R/O 1h	40h
Data: R/O 0	PMCSR_BSE: R/O 0	PMCSR Bit 15: PME# status: R/W 0 Bit 14-13: Data scale: R/O 00 Bit 12-9: Data select: R/O 0000 Bit 8: PME_En: R/W 0 Bit 7-2: Reserved: R/O 000000 Bit 1-0: Power state: R/W 00		44h

Table 2. PCI Configuration Space *(cont.)*

Subsystem Vendor ID Fields

The Subsystem ID and Subsystem Vendor ID fields in the PCI Configuration Space default to value 0000h unless an external EEPROM device is detected or unless the host has written to the appropriate internal register to program the values.

Interrupt Signal

The CS4280 PCI Interface includes an interrupt controller function which receives interrupt requests from multiple sources within the CS4280 device, and presents a single interrupt line (INTA) to the host system. Interrupt control registers in the CS4280 provide the host interrupt service routine with the ability to identify the source of the interrupt and to clear the interrupt sources. In the CS4280, the single external interrupt is expanded by the use of “virtual channels”. Each data stream which is read from or written to a modular buffer is assigned a virtual channel number. This virtual channel number is signalled by the DMA subsystem anytime the associated modulo buffer pointer passes the mid-point or wraps around.

AC’97 LINK

The CrystalClear solution includes a CS4280 plus a CS4297. The CS4280 communicates with the CS4297 over the AC-link as specified in the Intel® Audio Codec ‘97 Specification (version 1.03) with support for the 2.0 extensions. A block diagram for the AC’97 Controller configuration is given in Fig-

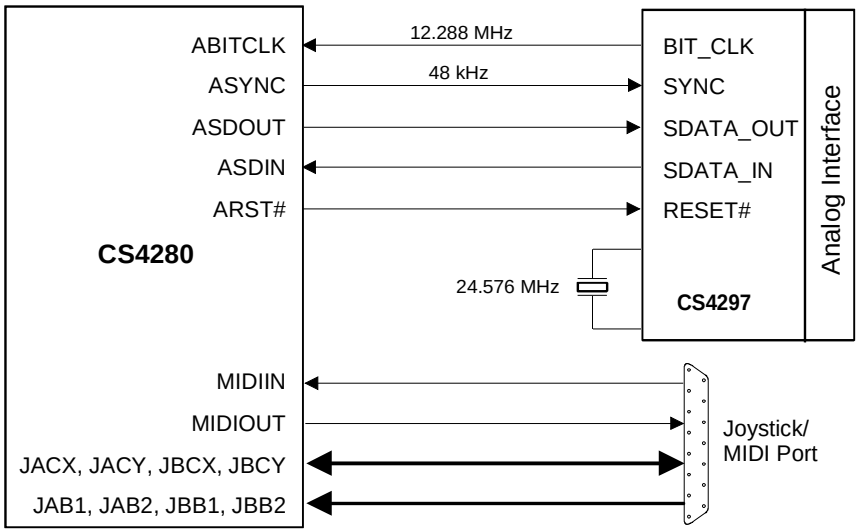


Figure 8. AC '97 Codec Connection Diagram

ure 6. The signal connections between the CS4280 and the AC '97 Codec are indicated in Figure 8. The AC '97 Codec is the timing master for the digital audio link. The ASDOUT output supports data transmission on all ten possible sample slots (output slots 3 - 12). The ASDIN input supports receiving of audio sample data on all input sample slots (input slots 3 - 12).

MIDI Port

In the AC '97 controller configuration, a bi-directional MIDI interface is provided to allow connection of external MIDI devices. The MIDI interface includes 16-byte FIFOs for the MIDI transmit and receive paths.

Joystick Port

In the AC '97 controller configuration, a joystick port is provided. The joystick port supports four "coordinate" channels and four "button" channels. The coordinate channels provide joystick positional information to the host, and the button channels provide user button event information. The joystick interface is capable of operating in the traditional "polled" mode. The Joystick schematic is illustrated in Figure 9.

EEPROM INTERFACE

The EEPROM configuration interface allows the connection of an optional external EEPROM device to provide power-up configuration information. The external EEPROM is not required for proper operation; however, in some applications power-up configuration settings other than the default values may be required to support specific Operating System compatibility requirements.

After a hardware reset, an internal state machine in the CS4280 will automatically detect the presence of an external EEPROM device and load the Subsystem ID and Subsystem Vendor ID fields, along with two bytes of general configuration information, into internal registers. At power-up, the CS4280 will attempt to read from the external device, and will check the data received from the device for a valid signature header. If the header data is invalid, the data transfer is aborted. After power-up, the host can read or write from/to the EEPROM device by accessing specific registers in the CS4280. Cirrus Logic provides software to read and write the EEPROM.

The two-wire interface for the optional external EEPROM device is depicted in Figure 10. During data transfers, the data line (EEDAT) can change

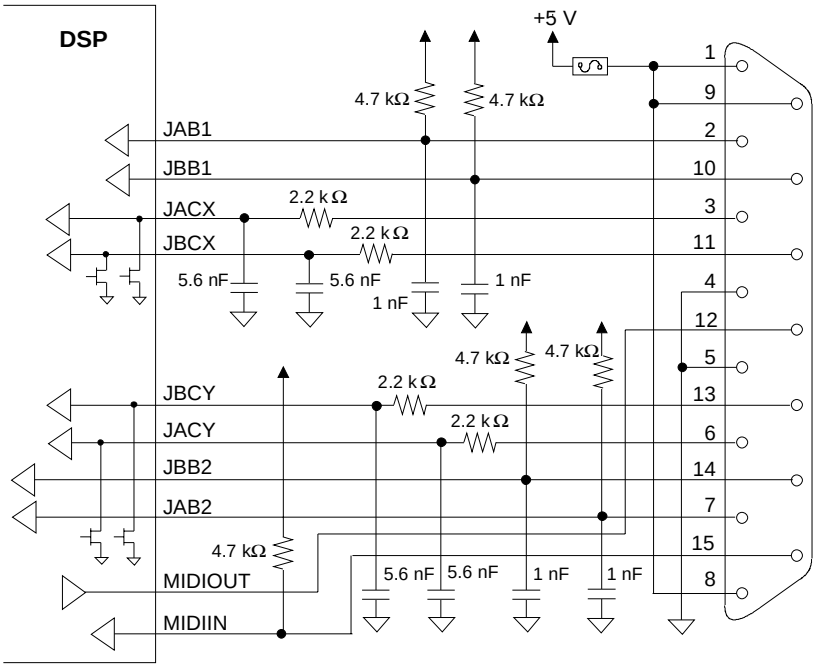


Figure 9. Joystick Logic

state only while the clock signal (EECLK) is low. A state change of the data line while the clock signal is high indicates a start or stop condition to the EEPROM device.

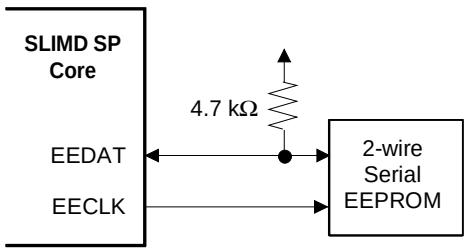


Figure 10. External EEPROM Connection

The EEPROM device read access sequence is shown in the Figure 11. The timing follows that of a random read sequence. The CS4280 first performs a "dummy" write operation, then generates a start condition followed by the slave device address and the byte address of zero. The CS4280 always begins access at byte address zero and continues access a byte at a time, using a sequential read, until all needed bytes in the EEPROM are read. Since only 7 bytes are needed, the smallest EEPROM available will suffice.

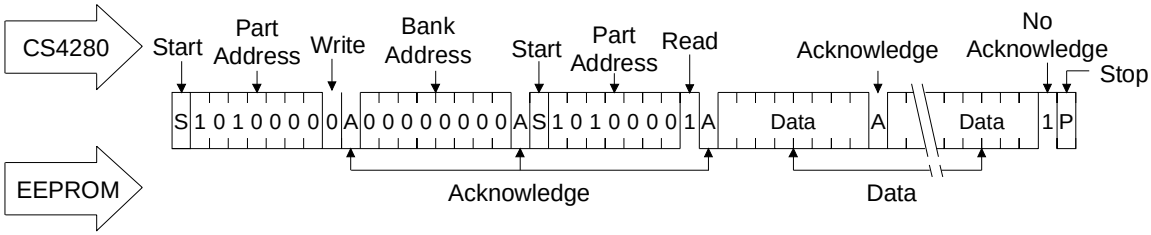


Figure 11. EEPROM Read Sequence

GENERAL PURPOSE I/O PINS

Many of the CS4280 signal pins are internally multiplexed to serve different functions depending on the environment in which the device is being used. Several of the CS4280 signal pins may be used as general purpose I/O pins when not required for other specific functions in a given application.

ZV PORT SERIAL INTERFACE

The ZV PORT interface consists of three input pins: ZLRCK, ZSCLK, and ZSDATA. ZLRCK is the Left/Right clock indicating which channel is currently being received. ZSCLK is the serial bit clock where ZLRCK and ZSDATA change on the falling edge and serial data is internally latched on the rising edge. Note that the serial data starts one ZSCLK period after ZLRCK transitions. Figure 12 illustrates the clocking on the ZV PORT pins. ZV PORT is available only in the CS4280-CQ.

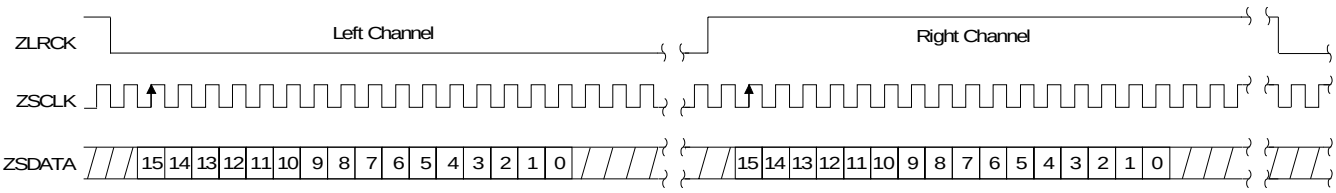
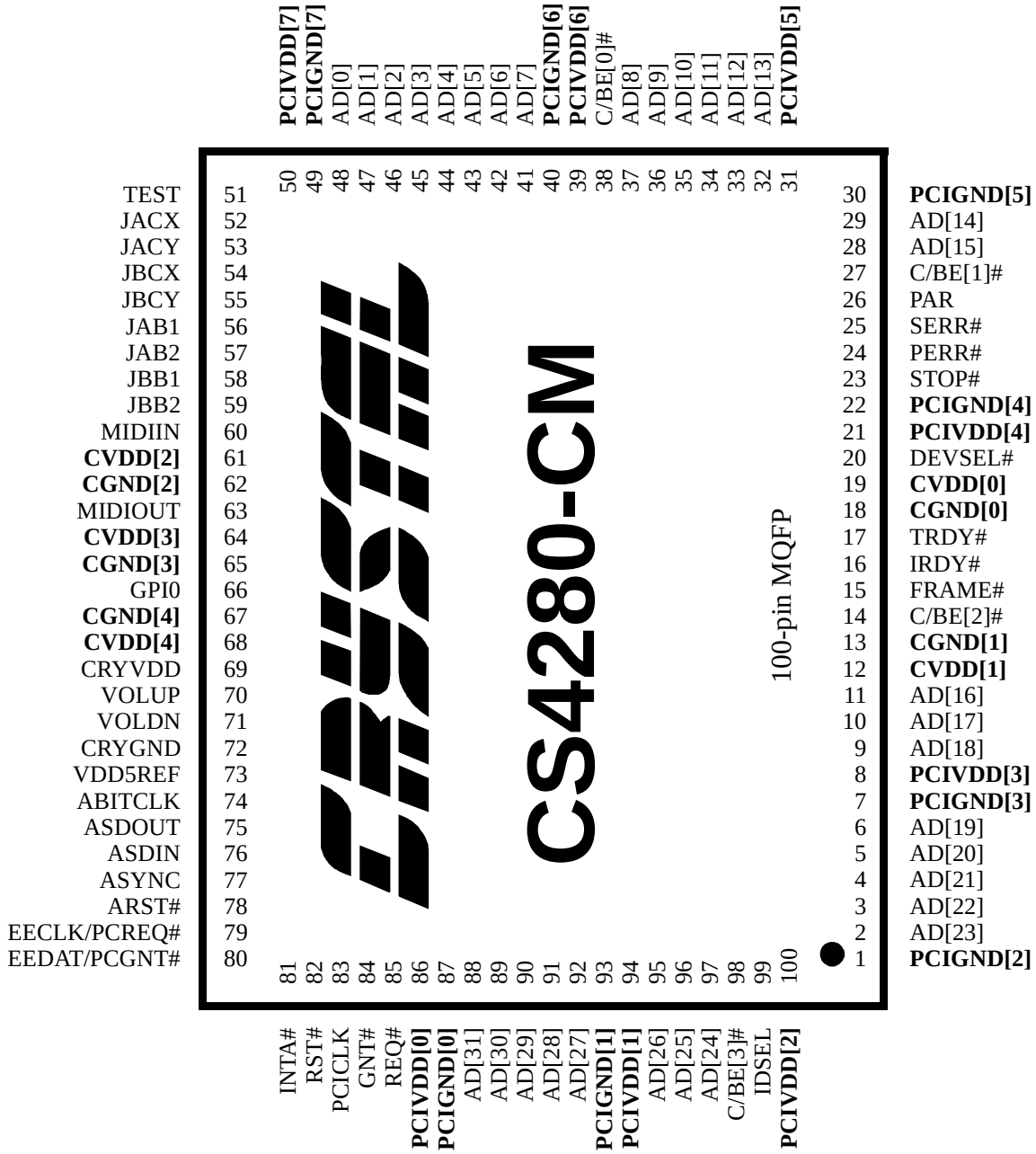
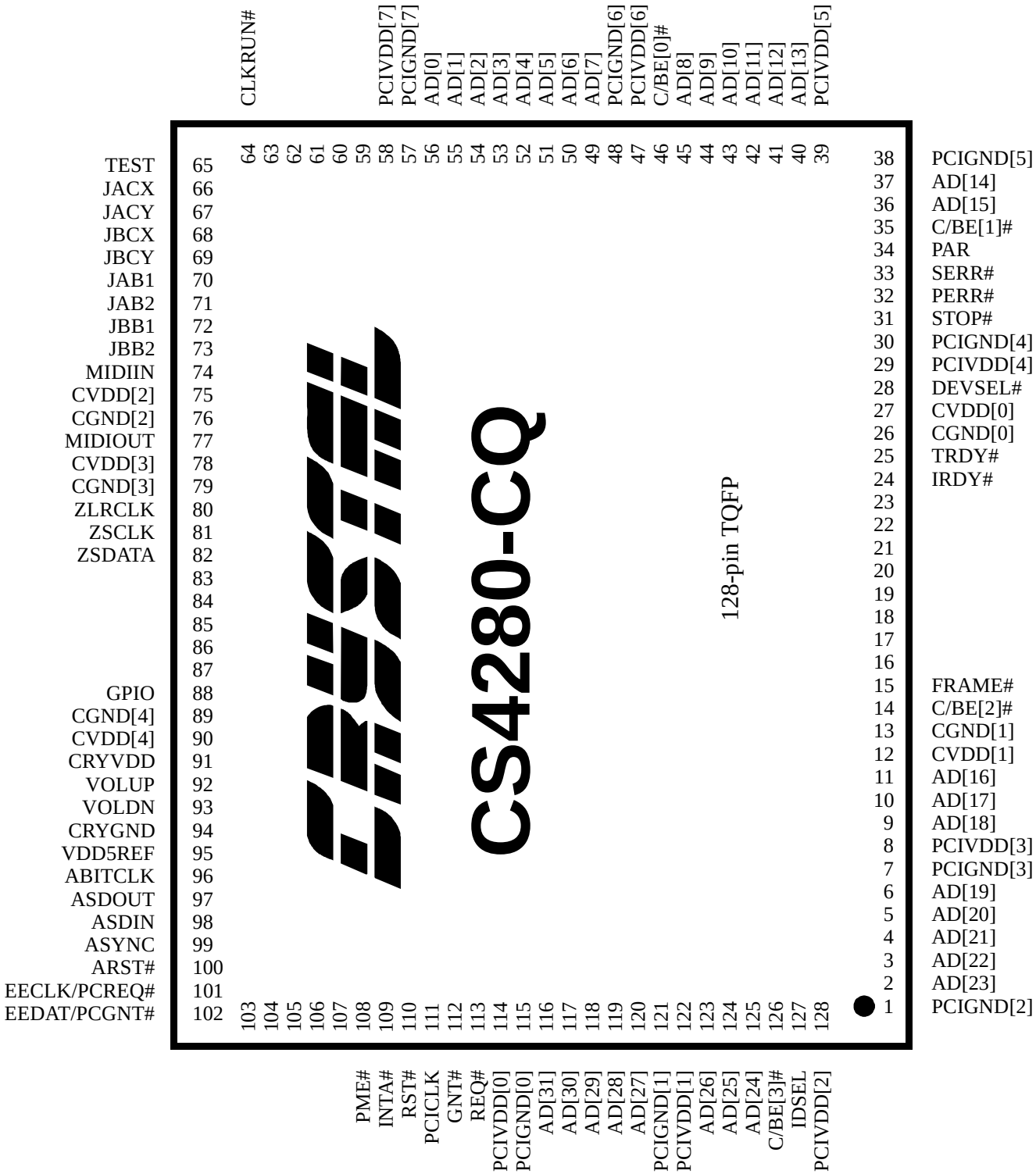


Figure 12. ZV Port Clocking Format

PIN DESCRIPTION




CS4280-CQ
128-pin TQFP
1 PCIGND[2]
2 AD[23]
3 AD[22]
4 AD[21]
5 AD[20]
6 AD[19]
7 PCIGND[3]
8 PCIVDD[3]
9 AD[18]
10 AD[17]
11 AD[16]
12 CVDD[1]
13 CGND[1]
14 C/BE[2]#
15 FRAME#
16
17
18
19
20
21
22
23
24 IRDY#
25 TRDY#
26 CGND[0]
27 CVDD[0]
28 DEVSEL#
29 PCIVDD[4]
30 PCIGND[4]
31 STOP#
32 PERR#
33 SERR#
34 PAR
35 C/BE[1]#
36 AD[15]
37 AD[14]
38 PCIGND[5]
39 PCIVDD[5]
40 AD[13]
41 AD[12]
42 AD[11]
43 AD[10]
44 AD[9]
45 AD[8]
46 C/BE[0]#
47 PCIVDD[6]
48 PCIGND[6]
49 AD[7]
50 AD[6]
51 AD[5]
52 AD[4]
53 AD[3]
54 AD[2]
55 AD[1]
56 AD[0]
57 PCIGND[7]
58 PCIVDD[7]
59
60
61
62
63
64 CLKRUN#
65 TEST
66 JACX
67 JACY
68 JBCX
69 JBCY
70 JAB1
71 JAB2
72 JBB1
73 JBB2
74 MIDIIN
75 CVDD[2]
76 CGND[2]
77 MIDIOUT
78 CVDD[3]
79 CGND[3]
80 ZLRCLK
81 ZSCLK
82 ZSDATA
83
84
85
86
87
88 GPIO
89 CGND[4]
90 CVDD[4]
91 CRYVDD
92 VOLUP
93 VOLDN
94 CRYGND
95 VDD5REF
96 ABITCLK
97 ASDOUT
98 ASDIN
99 ASYNC
100 ARST#
101 EECLK/PCREQ#
102 EEDAT/PCGNT#
103 PME#
104 INTA#
105 RST#
106 PCICLK
107 GNT#
108 REQ#
109 PCIVDD[0]
110 PCIGND[0]
111 AD[31]
112 AD[30]
113 AD[29]
114 AD[28]
115 AD[27]
116 PCIGND[1]
117 PCIVDD[1]
118 AD[26]
119 AD[25]
120 AD[24]
121 C/BE[3]#
122 IDSEL
123 PCIVDD[2]

A '#' sign suffix on a pin names indicates an active-low signal.

PCI Interface

AD[31:0] - Address/Data Bus, I/O

These pins form the multiplexed address / data bus for the PCI interface.

C/BE[3:0]# - Command Type / Byte Enables, I/O

These four pins are the multiplexed command / byte enables for the PCI interface. During the address phase of a transaction, these pins indicate cycle type. During the data phases of a transaction, active low byte enable information for the current data phase is indicated. These pins are inputs during slave operation and they are outputs during bus mastering operation.

PAR - Parity, I/O

The Parity pin indicates even parity across AD[31:0] and C_BE[3:0] for both address and data phases. The signal is delayed one PCI clock from either the address or data phase for which parity is generated.

FRAME# - Cycle Frame, I/O

FRAME# is driven by the current PCI bus master to indicate the beginning and duration of a transaction.

IRDY# - Initiator Ready, I/O

IRDY# is driven by the current PCI bus master to indicate that as the initiator it is ready to transmit or receive data (complete the current data phase).

TRDY# - Target Ready, I/O

TRDY# is driven by the current PCI bus target to indicate that as the target device it is ready to transmit or receive data (complete the current data phase).

STOP# - Transition Stop, I/O

STOP# is driven active by the current PCI bus target to indicate a request to the master to stop the current transaction.

IDSEL - Initialize Device Select, Input

IDSEL is used as a chip select during PCI configuration read and write cycles.

DEVSEL# - Device Select, I/O

DEVSEL# is driven by the PCI bus target device to indicate that it has decoded the address of the current transaction as its own chip select range.

REQ# - Master Request, Three-State Output

REQ# indicates to the system arbiter that this device is requesting access to the PCI bus. This pin is high-impedance when RST# is active.

GNT# - Master Grant, Input

GNT# is driven by the system arbiter to indicate to the device that the PCI bus has been granted.

PERR# - Parity Error, I/O

PERR# is used for reporting data parity errors on the PCI bus.

SERR# - System Error, Open Drain Output

SERR# is used for reporting address parity errors and other catastrophic system errors.

INTA# - Host Interrupt A, Open Drain Output

INTA# is the level triggered interrupt pin dedicated to servicing internal device interrupt sources.

PCICLK - PCI Bus Clock, Input

PCICLK is the PCI bus clock for timing all PCI transactions. All PCI synchronous signals are generated and sampled relative to the rising edge of this clock.

RST# - PCI Device Reset

RST# is the PCI bus master reset.

VDD5REF - Clean 5 V Power Supply

VDD5REF is the power connection pin for the 5 V PCI pseudo supply for the PCI bus drivers. The internal core logic runs on 3.3 Volts. This pin enables the PCI interface to support and be tolerant of 5 Volt signals. Must be connected to +5 Volts.

PCIVDD[7:0] - PCI Bus Driver Power Supply

PCIVDD pins are the PCI driver power supply pins. These pins must have a nominal +3.3 Volts.

PCIGND[7:0] - PCI Bus Driver Ground Pins

PCIGND pins are the PCI driver ground reference pins.

PME# - PCI Power Management Event, Open Drain Output

PME# signals a power management event. This signal can go low because of an AC ‘97 2.0 Codec event.

External Interface Pins

TEST - Test Mode Strap, Input

This pin is sampled at reset for test mode entry. If it is high at reset, test mode is enabled. This pin must be pulled to ground for normal operation.

EEDAT/PCGNT# - EEPROM Data Line / PC/PCI Grant, I/O

For expansion card designs, this is the data line for external serial EEPROM containing device configuration data. When used with an external EEPROM, a 4.7 kΩ pullup resistor is required. In motherboard designs using PC/PCI, this pin is the PC/PCI serialized grant input. In designs with neither of the above requirements, this pin can be used as a general purpose input or open drain output (GPIO2).

EECLK/PCREQ# - EEPROM Clock Line / PC/PCI Request, Output

For expansion card designs, this is the clock line for external serial EEPROM containing device configuration data. In motherboard designs using PC/PCI, this pin is the PC/PCI serialized request output. In designs with neither of the above requirements, this pin can be used as a general purpose output pin (GPOUT).

GPIO - General Purpose I/O Pin, I/O

This pin defaults as a general purpose I/O pin.

VOLUP - Volume-Up Button, Input

This pin is the volume-up button control input. This pin may also be used as a general purpose input if its primary function is not needed.

VOLDN - Volume-Down Button, I/O

This pin is the volume-down button control input. This pin may also be used as a general purpose input if its primary function is not needed.

Clock / Miscellaneous

CLKRUN# - Optional System Clock Control, Output, Open Drain

CLKRUN# is an optional PCI signal defined for mobile operations. This is an open drain output signalling the system that the PCI clock is required. This signal pin is not available on the add-in card connector. Only available on CS4280-CQ.

CRYVDD - Crystal & PLL Power Supply

Power pin for crystal oscillator and internal phase locked loop. This pin must be connected to a nominal +3.3 Volts.

CRYGND - Crystal & PLL Ground Supply

Ground pin for crystal oscillator and internal phase locked loop.

JACX, JACY, JBCX, JBCY - Joystick A and B X/Y Coordinates, I/O

These pins are the 4 axis coordinates for the joystick port. These pins may also be used as a general purpose inputs or open drain outputs if their primary function is not needed.

JAB1, JAB2, JBB1, JBB2 - Joystick A and B Button Inputs, Input

These pins are the 4 button switch inputs for the joystick port. These pins can also be a general purpose polled inputs.

MIDIIN - MIDI Data Input

This is the serial input pin for the internal MIDI port.

MIDIOUT - MIDI Data Output

This is the serial output pin for the internal MIDI port.

CVDD[4:0] - Core Power Supply

Core power pins. These pins must be connected to a nominal +3.3 Volts.

CGND[4:0] - Core Ground Supply

Core ground reference pins.

Serial Codec Interface

ABITCLK - AC '97 Bit Clock, Input

Master timing clock for serial audio data. This pin is an input which drives the timing for the AC '97 interface, along with providing the source clock for the CS4280.

ASYNC - AC '97 Frame Sync, Output

Framing clock for serial audio data. This pin is an output which indicates the framing for the AC '97 link.

ASDOUT - AC '97 Data Out, Output

AC '97 serial data out.

ARST# - AC '97 Reset, Output

AC '97 link reset pin.

ASDIN - AC '97 Data In, Input

Serial audio input data.

ZV Port Serial Interface

ZSCLK - ZV Port Serial Clock, Input

ZV Port serial bit clock.

ZLRCLK - ZV Port Left/Right Clock, Input

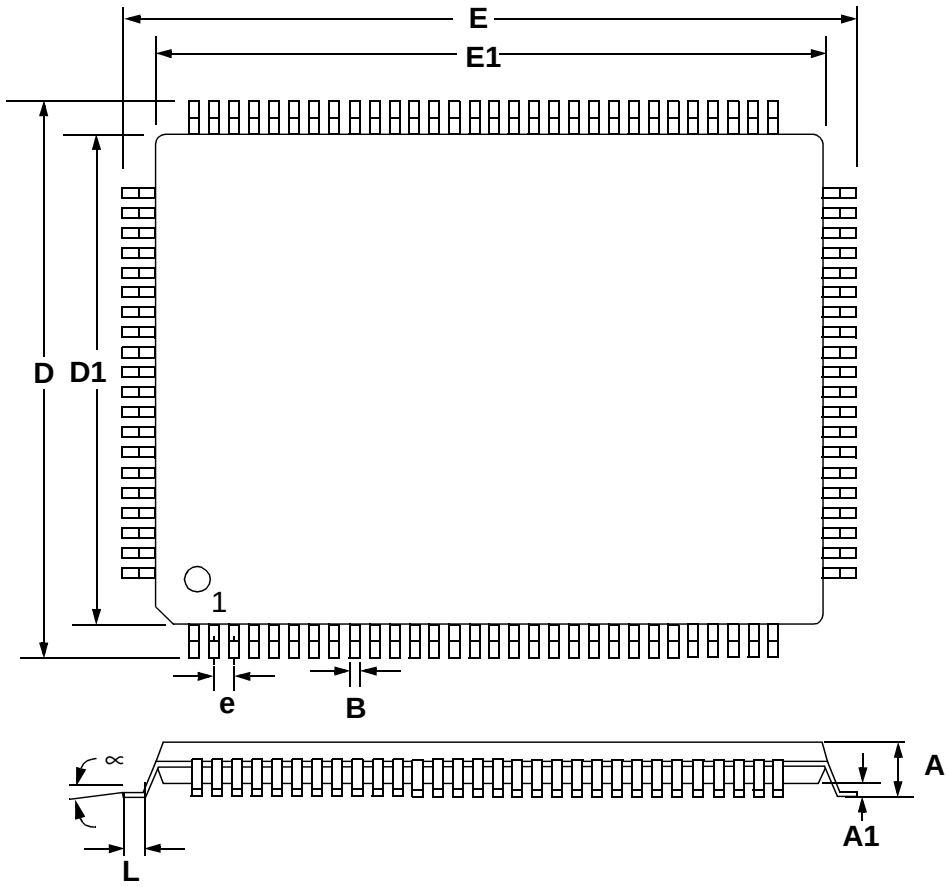
ZV Port left/right channel delineation.

ZSDATA - ZV Port Serial Data In, Input

ZV Port serial data input pin.

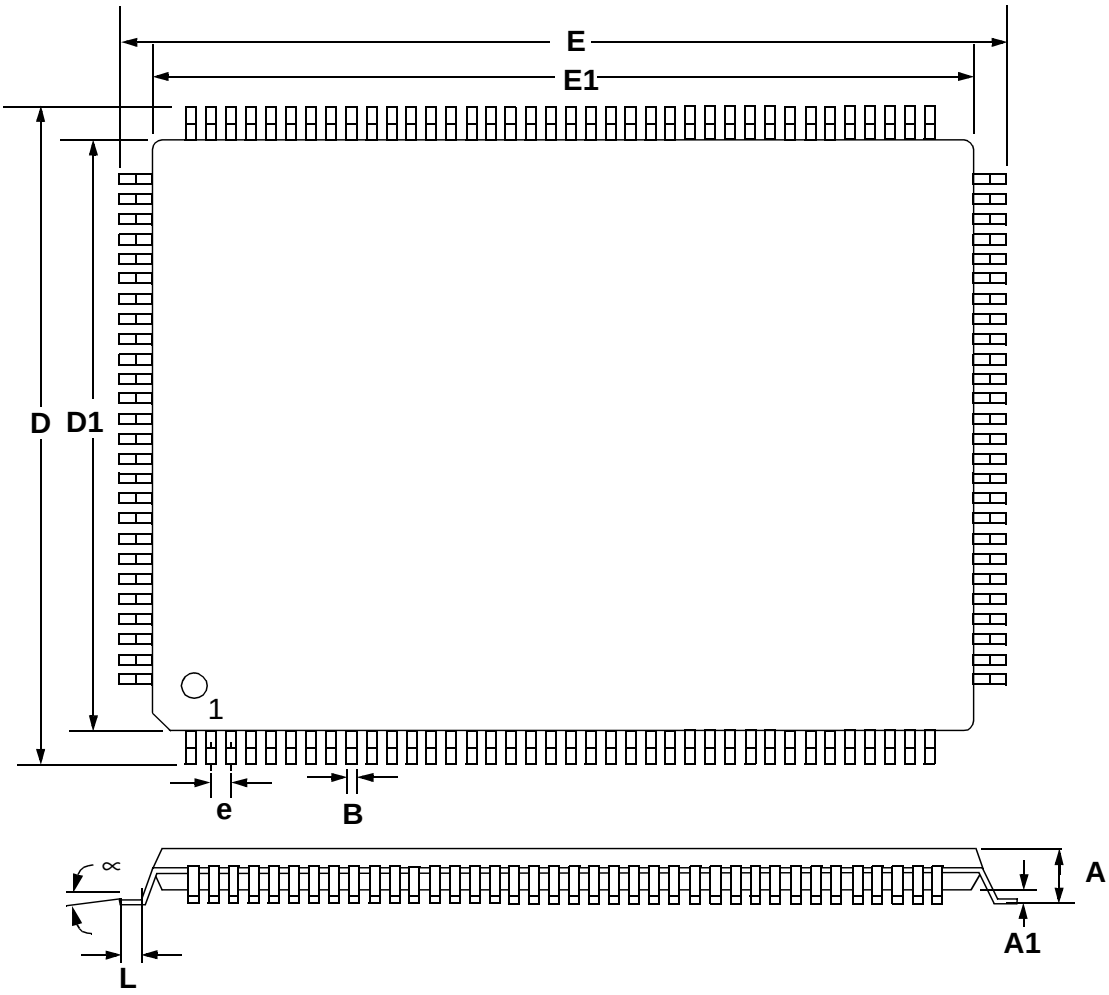
PACKAGE OUTLINE

'M' Package 100-pin MQFP



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.000	0.134	0.000	3.400
A1	0.010	0.014	0.250	0.350
B	0.009	0.015	0.220	0.380
D	0.667	0.687	16.950	17.450
D1	0.547	0.555	13.900	14.100
E	0.904	0.923	22.950	23.450
E1	0.783	0.791	19.900	20.100
e	0.022	0.030	0.550	0.750
∝	0.000	7.000	0.000	7.00
L	0.018	0.030	0.450	0.750

'Q' Package 128-pin TQFP



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.000	0.063	0.000	1.600
A1	0.002	0.006	0.050	0.150
B	0.007	0.011	0.170	0.270
D	0.626	0.634	15.900	16.100
D1	0.547	0.555	13.900	14.100
E	0.862	0.870	21.900	22.100
E1	0.783	0.791	19.900	20.100
e	0.016	0.024	0.400	0.600
∝	0.000	7.000	0.000	7.000
L	0.018	0.030	0.450	0.750