CS4304P

High Performance Multichannel Audio DAC

Features

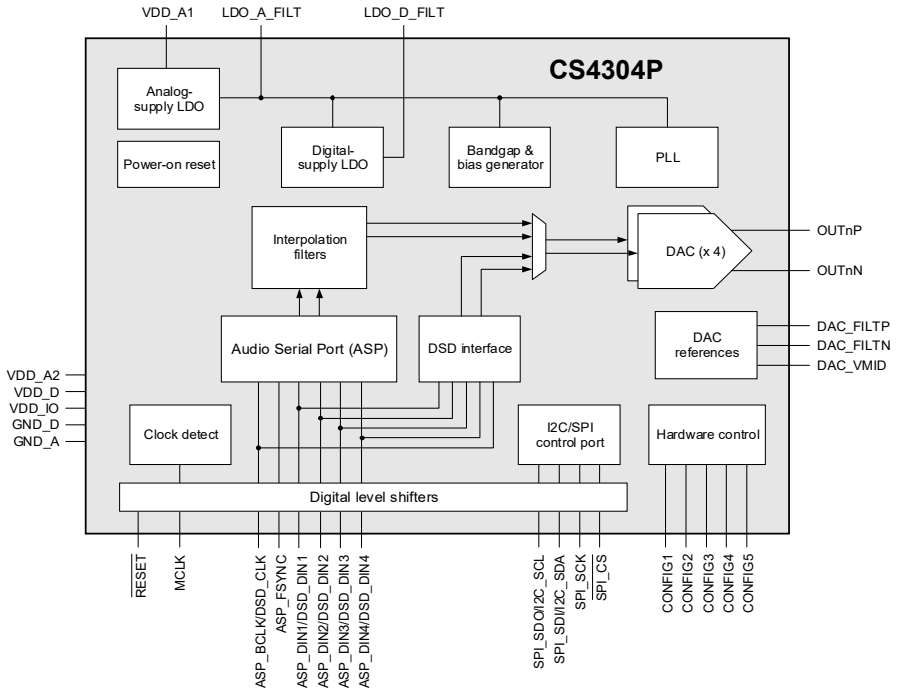
- High performance four-channel DAC
  - Differential analog architecture
  - High-resolution 32-bit digital architecture
  - Low-latency digital filters and digital volume control
- Current-mode output for optimal dynamic range into application-specific output buffer
- PLL supports range of external system-clock references
- Sample timing alignment across multiple devices
- Audio serial port (ASP) sample rates up to 768 kHz
  - I²S, left-justified, and TDM data formats
- DSD interface operating up to 512×fs oversample rate
- Hardware and software control modes
  - I²C control port up to 1 MHz
  - SPI control port up to 24 MHz
  - Hardware control with no host processor required
- Single-supply operation at 3.3 V
  - Support for 1.8 V–3.3 V digital input/outputs
- 48-pin QFN package

Specifications

- Enhanced oversampling sigma-delta DAC
  - 123 dB dynamic range (A-weighted)
  - –115 dB total harmonic distortion + noise (THD+N)
  - 4.5/Fs group delay at 96 kHz sample rate (slow roll-off, minimum-phase filter)

Applications

- A/V receivers
- Digital mixing consoles
- High-performance speakers and soundbars
- DAW interfaces
- Musical instruments



Advanced Product Information

This document contains information for a product under development. Cirrus Logic reserves the right to modify this product without notice.

DS1316A3
DEC 2024

General Description

The CS4304P is a high-performance, 32-bit resolution, four-channel DAC. Digital input is supported via the audio serial port (ASP) at sample rates up to 768 kHz. Configurable low-latency digital-interpolation filters are provided. A DSD input path is also available, supporting direct playback modes at up to 512×fs oversample rate.

The DAC incorporates a proprietary analog FIR architecture to reduce out-of-band noise and minimize the external component requirements. The differential current-mode output enables a single-stage external op-amp circuit to combine the current-to-voltage conversion and out-of-band filtering, supporting flexible integration and optimal dynamic range for the target application.

The CS4304P can be configured using a control interface supporting I²C and SPI modes of operation. The device can also be operated in hardware mode, using external resistors to select the required configuration. Multiple hardware-control options are supported, including system clocking, ASP format, sample rate, and digital-filter selection.

The low-latency digital filters are optimized for the applicable sample rate. Fast or slow roll-off filters can be combined with minimum or linear phase responses to support the desired signal characteristics. A de-emphasis filter is also available.

The ASP supports multichannel operation in I²S, left-justified, and TDM data formats. Four data-input pins support 32-bit multichannel operation up to 384 kHz (eight channels) or 768 kHz (four channels).

The Direct Stream Digital (DSD) input path supports four-channel operation at oversample rates up to 512×fs.

Clocking for the CS4304P can be derived from the ASP or DSD interface, or else provided from a separate clock source. An integrated phase-locked loop (PLL) is used to reduce jitter and to support a range of reference-clock frequency options. The DAC-conversion timing is referenced to the ASP data frame, enabling time-aligned operation across multiple devices sharing a common data bus.

The CS4304P can be powered from a single 3.3 V supply; an integrated regulator provides the 1.2 V digital-core supply. Digital input/output at 1.8 V logic levels is also possible using a separate external supply. The device combines high performance with low power consumption.

The CS4304P is available in a commercial-grade 0.4 mm pitch, 48-pin QFN package for operation from –40° to +85°C.

See Section 11 for ordering information.

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1 Pin Assignments and Descriptions

1.1 48-Pin QFN (Top View, Through-Package)

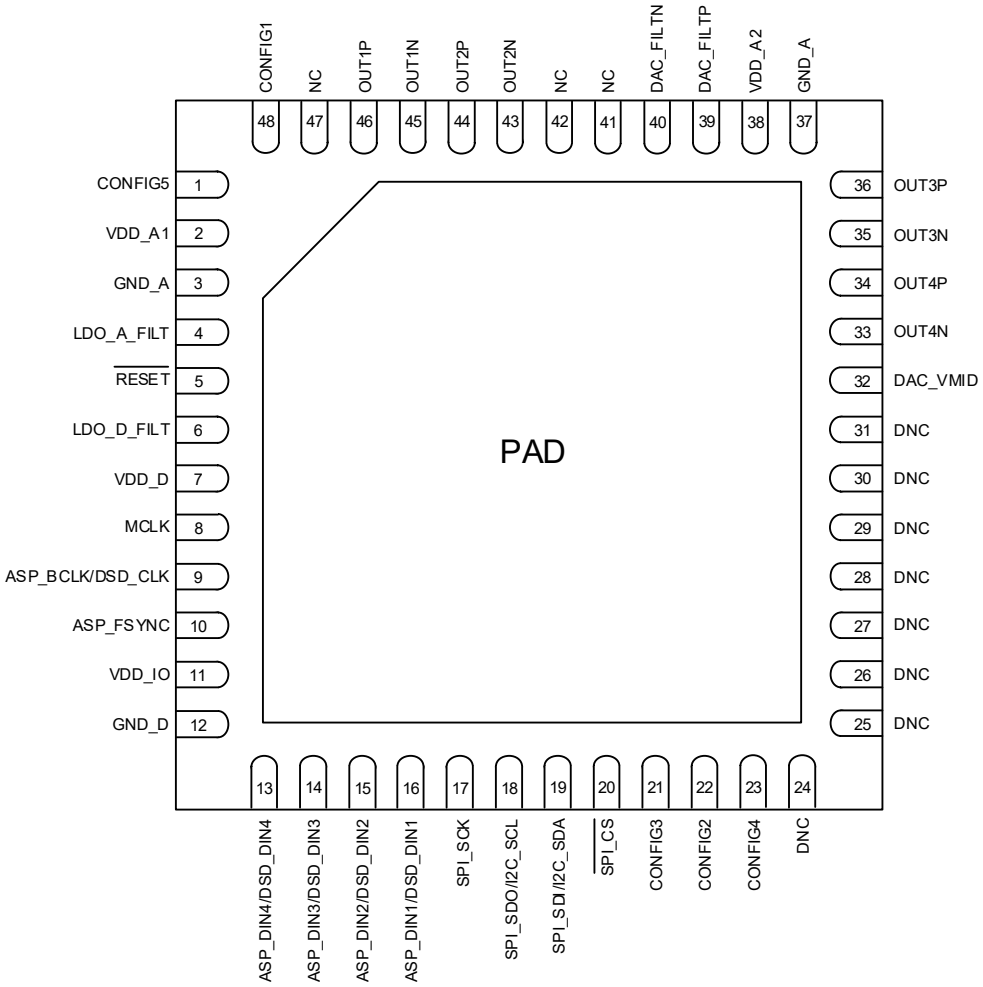


Figure 1-1. QFN 48-pin diagram (Top View, Through Package)

1.2 QFN Pin Descriptions

Table 1-1. QFN Pin Descriptions

Pin Name	Pin #	Power Supply	I/O	Description
				Digital I/O
ASP_BCLK/DSD_CLK	9	VDD_IO	I/O	Audio serial port bit clock/DSD clock.
ASP_DIN1/DSD_DIN1 ASP_DIN2/DSD_DIN2 ASP_DIN3/DSD_DIN3 ASP_DIN4/DSD_DIN4	16 15 14 13	VDD_IO	O	Audio serial port data input/DSD data input.
ASP_FSYNC	10	VDD_IO	I/O	Audio serial port frame sync.
MCLK	8	VDD_IO	I	Master clock input (active low).
$\overline{\text{RESET}}$	5	VDD_IO	I	Hardware reset control.
$\overline{\text{SPI\_CS}}$	20	VDD_IO	I	SPI chip select (active low).

Table 1-1. QFN Pin Descriptions *(Cont.)*

Pin Name	Pin #	Power Supply	I/O	Description
SPI_SCK	17	VDD_IO	I	SPI clock.
SPI_SDI/I2C_SDA	19	VDD_IO	I/O	SPI data input/I2C data input/output.
SPI_SDO/I2C_SCL	18	VDD_IO	I/O	SPI data output/I2C clock input.
				Analog I/O
CONFIG1	48	VDD_A	I/O	Hardware control pins.
CONFIG2	22	VDD_IO		In software control mode, CONFIG5 selects the I2C target address.
CONFIG3	21	VDD_IO		
CONFIG4	23	VDD_IO		
CONFIG5	1	VDD_A		
DAC_FILTN	40	VDD_A	O	DAC external capacitor connection.
DAC_FILTP	39			The DAC_FILTP capacitor should be connected to VDD_A2.
DAC_VMID	32	VDD_A	O	DAC mid-rail voltage reference output.
LDO_A_FILT	4	VDD_A	O	LDO_A regulator external capacitor connection.
LDO_D_FILT	6	VDD_A	O	LDO_D regulator external capacitor connection.
OUT1N	45	VDD_A	O	Analog Output 1.
OUT1P	46			
OUT2N	43	VDD_A	O	Analog Output 2.
OUT2P	44			
OUT3N	35	VDD_A	O	Analog Output 3.
OUT3P	36			
OUT4N	33	VDD_A	O	Analog Output 4.
OUT4P	34			
				Power Supplies
VDD_D	7	—	—	Digital supply (powered from internal LDO)
VDD_A1	2	—	—	Analog supply
VDD_A2	38	—	—	Analog supply
VDD_IO	11	—	—	Digital I/O supply
GND_D	12	—	—	Digital ground [1]
GND_A	3, 37, PAD	—	—	Analog ground [1]
				No Connect
DNC	24, 25, 26, 27, 28, 29, 30, 31	—	—	Do not connect.
NC	41, 42, 47	—	—	No connect

1.All ground pins, including the ground paddle, must be tied to a common ground plane directly underneath the CS4304P.

1.3 Termination of Unused Pins

Table 1-2 shows the required termination for unused pins (i.e., if the functionality of the pin is not being used). Pins not listed must be connected as shown in the typical connection drawings (see Section 2).

Table 1-2. Termination of Unused Pins

Name	Termination if unused
OUTnx	Float
$\overline{\text{RESET}}$	
ASP_DINx	Grounded
CONFIGx	
MCLK	
SPI_SDO/I2C_SCL	
SPI_SCK	
SPI_SDI/I2C_SDA	
$\overline{\text{SPI\_CS}}$	Connect to VDD_IO

1.4 Electrostatic Discharge (ESD) Protection

ESD-sensitive device. The CS4304P is manufactured on a CMOS process. Therefore, it is generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken while handling and storing this device. This device is qualified to current JEDEC ESD protection standards.

2 Typical Connection Diagram

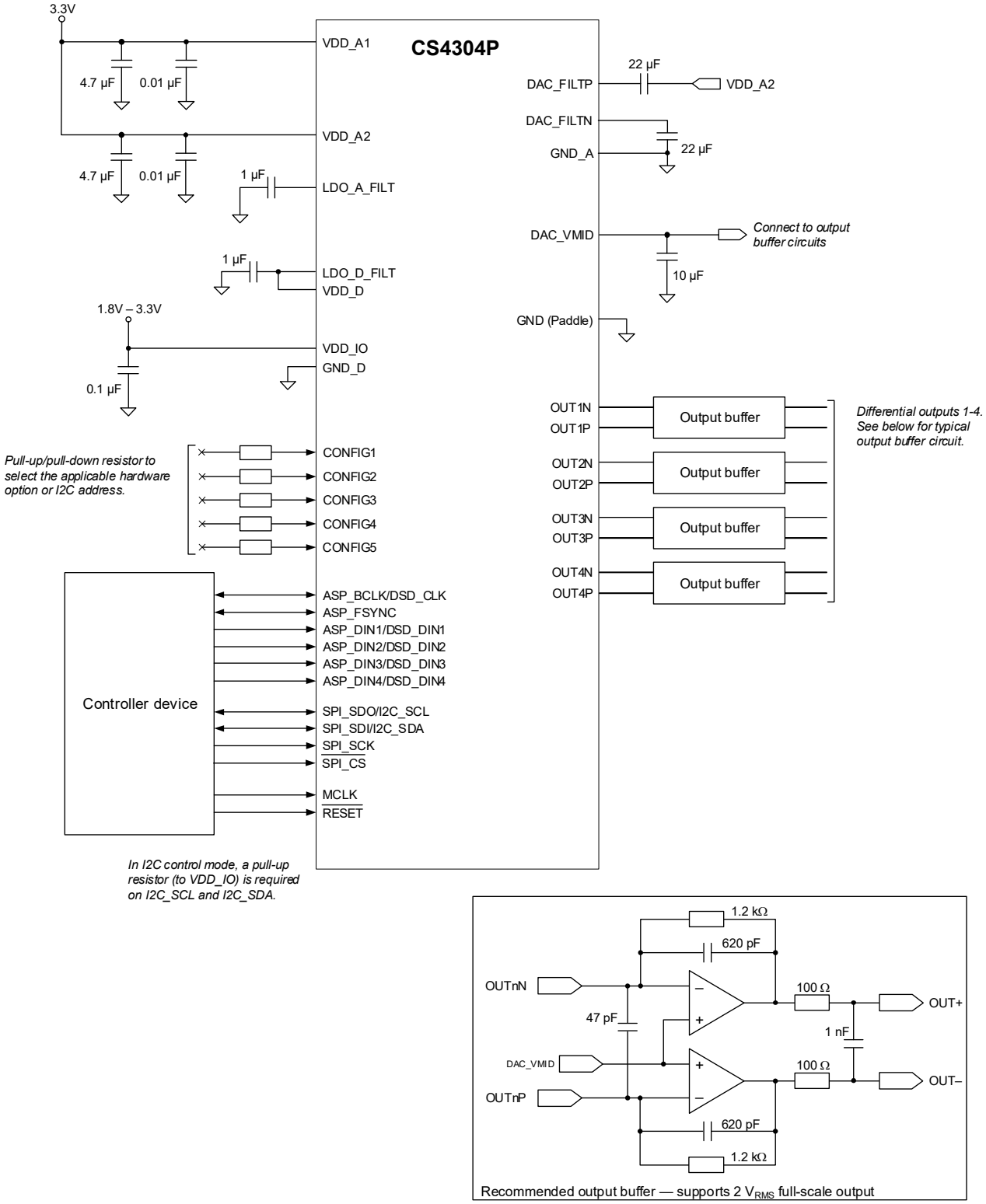


Figure 2-1. Typical Connections

3 Characteristics and Specifications

Note: Table 3-1 defines parameters as they are characterized in this section. Note that default register field configurations are used unless specified otherwise in the test conditions.

Table 3-1. Parameter Definitions

Parameter	Definition
Channel separation	The difference in level between the active channel (driven to maximum full scale output) and the measured signal level in the idle channel at the test signal frequency. The active channel is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the associated idle channel.
Common-mode rejection ratio (CMRR)	The ratio of a specified input signal (applied to both sides of a differential input), relative to the output signal that results from it.
Dynamic range	The difference in level between the maximum full scale output signal and the sum of all harmonic distortion products plus noise with a low-level input signal applied. Typically, an input signal level 60 dB below full scale is used.
Power-supply rejection ratio (PSRR)	The ratio of a specified power supply variation relative to the output signal that results from it. PSRR is measured under quiescent signal path conditions.
Total harmonic distortion plus noise (THD+N)	The ratio of the RMS sum of the harmonic distortion products plus noise in the specified bandwidth relative to the RMS amplitude of the fundamental (i.e., test frequency) output.
Note: Unless specified otherwise, all performance measurements are for a 10 Hz to 20 kHz bandwidth.	

Table 3-2. Recommended Operating Conditions

Test conditions (unless specified otherwise): Ground = GND = GND_A = GND_D = 0 V; voltages are with respect to ground.

Parameter		Symbol	Minimum	Maximum	Unit
DC power supply	Analog supply [1]	VDDA1, VDDA2	3.13	3.47	V
	Digital supply (powered from internal LDO) [2]	VDD_D	1.14	1.26	V
	Digital I/O supply	VDD_IO	1.71	3.63	V
Supply ramp up/down (all supplies)		t_{PWR-UD}	0.01	10	ms
Ambient temperature		T_A	–40	+85	ºC

Note: The device is fully functional and meets all parametric specifications in this section if operated within the specified conditions. Functionality and parametric performance is not guaranteed or implied outside of these limits. Operation outside of these limits may adversely affect device reliability.

1. The VDD_A1 and VDD_A2 rails should be tied together and powered from a single supply. The associated power domain is referred to as VDD_A.
2. The digital supply is powered from an internal LDO regulator. The VDD_D pin must be connected to the LDO output pin, LDO_D_FILT.

Table 3-3. Absolute Maximum Ratings

Test conditions (unless specified otherwise): Ground = GND = GND_A = GND_D = 0 V; voltages are with respect to ground.

Parameter		Symbol	Minimum	Maximum	Unit
DC power supply	Analog supply [1]	VDDA1, VDDA2	–0.3	4.32	V
	Digital supply	VDD_D	–0.3	1.52	V
	Digital I/O supply	VDD_IO	–0.3	4.32	V
External voltage applied to digital input/output		V_{INDI}	–0.3	VDD_IO + 0.3	V
External voltage applied to analog inputs	CONFIG2, CONFIG3, CONFIG4 All other analog inputs	V_{INAI}	–0.3 –0.3	VDD_IO + 0.3 VDD_A + 0.3	V V
Input current	digital input/output analog inputs	I_{in}	— —	±10 ±10	mA mA
Ambient operating temperature		T_A	–40	+115	°C
Junction operating temperature		T_J	–40	+125	°C
Storage temperature		T_{STG}	–65	+150	°C

Caution: Stresses beyond “Absolute Maximum Ratings” levels may cause permanent damage to the device. These levels are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Table 3-2 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. The VDD_A1 and VDD_A2 rails should be tied together and powered from a single supply. The associated power domain is referred to as VDD_A.

Table 3-4. DAC Path Characteristics

Test conditions (unless specified otherwise): External components as shown in Fig. 2-1; VDD_A = VDD_IO = 3.3 V; VDD_D = 1.2 V (powered from internal LDO); Ground = GND_A = GND_D = 0 V; voltages are with respect to ground; T_A = +25ºC; 1 kHz sine wave test signal; Fs = 48 kHz, 32-bit audio data, MCLK = 24.576 MHz; measured with output connected to a 1.2 kΩ transimpedance amplifier as shown in Fig. 2-1.

Parameter		Min	Typ	Max	Units
Full scale output	0 dBFS input	—	1.67	—	mA_{RMS}
Dynamic range	A-weighted unweighted	120 117	123 120	— —	dB dB
THD+N	0 dBFS input –20 dBFS input –60 dBFS input	— — —	–115 –97 –57	TBD — —	dB dB dB
Idle channel noise	A-weighted	—	1.15	—	nA_{RMS} nA_{RMS}
Channel separation	1 kHz 20 kHz	— —	110 100	— —	dB dB
PSRR (VDD_A)	100 mV (peak-peak) 1 kHz sine wave	—	75	—	dB

Table 3-5. DAC Filter Characteristics

Test conditions (unless specified otherwise): VDD_A = VDD_IO = 3.3 V; VDD_D = 1.2 V (powered from internal LDO); Ground = GND_A = GND_D = 0 V; voltages are with respect to ground; T_A = +25ºC; 1 kHz sine wave test signal; Fs = 48 kHz, 32-bit audio data.

Parameter [1]				Min	Typ	Max	Units
Fs = 32 kHz	Fast roll-off	Passband	to –3 dB corner	—	—	0.49	Fs
		Passband ripple	f ≤ 0.45 Fs	–0.001	—	0.001	dB
		Stopband attenuation	f ≥ 0.55 Fs	100	—	—	dB
		Group delay [2]	linear phase minimum phase	— —	32.5/Fs 4.6/Fs	— —	s s
Fs = 44.1 or 48 kHz	Fast roll-off	Passband	to –3 dB corner	—	—	0.49	Fs
		Passband ripple	f ≤ 0.45 Fs	–0.001	—	0.001	dB
		Stopband attenuation	f ≥ 0.55 Fs	100	—	—	dB
		Group delay [2]	linear phase minimum phase	— —	32.6/Fs 4.7/Fs	— —	s s
	Slow roll-off	Passband	to –3 dB corner	—	—	0.47	Fs
		Passband ripple	f ≤ 0.42 Fs	–0.004	—	0.005	dB
		Stopband attenuation	f ≥ 0.59 Fs	101	—	—	dB
		Group delay [2]	linear phase minimum phase	— —	17.1/Fs 4.6/Fs	— —	s s
Fs = 88.2 or 96 kHz	Fast roll-off	Passband	to –3 dB corner	—	—	0.49	Fs
		Passband ripple	f ≤ 0.45 Fs	–0.001	—	0.001	dB
		Stopband attenuation	f ≥ 0.55 Fs	101	—	—	dB
		Group delay [2]	linear phase minimum phase	— —	32.9/Fs 5.0/Fs	— —	s s
	Slow roll-off	Passband	to –3 dB corner	—	—	0.39	Fs
		Passband ripple	f ≤ 0.23 Fs	–0.005	—	0.005	dB
		Stopband attenuation	f ≥ 0.70 Fs	90	—	—	dB
		Group delay [2]	linear phase minimum phase	— —	7.4/Fs 4.5/Fs	— —	s s
	Balanced roll-off	Passband	to –3 dB corner	—	—	0.35	Fs
		Passband ripple	f ≤ 0.23 Fs	–0.001	—	0.001	dB
		Stopband attenuation	f ≥ 0.55 Fs	101	—	—	dB
		Group delay [2]	linear phase minimum phase	— —	11.6/Fs 5.2/Fs	— —	s s

Table 3-5. DAC Filter Characteristics *(Cont.)*

Test conditions (unless specified otherwise): VDD_A = VDD_IO = 3.3 V; VDD_D = 1.2 V (powered from internal LDO); Ground = GND_A = GND_D = 0 V; voltages are with respect to ground; T_A = +25ºC; 1 kHz sine wave test signal; Fs = 48 kHz, 32-bit audio data.

Parameter [1]				Min	Typ	Max	Units
Fs = 176.4 or 192 kHz	Fast roll-off	Passband	to –3 dB corner	—	—	0.48	Fs
		Passband ripple	f ≤ 0.45 Fs	–0.004	—	0.005	dB
		Stopband attenuation	f ≥ 0.55 Fs	103	—	—	dB
		Group delay [2]	linear phase	—	35.1/Fs	—	s
			minimum phase	—	6.6/Fs	—	s
	Slow roll-off	Passband	to –3 dB corner	—	—	0.36	Fs
		Passband ripple	f ≤ 0.11 Fs	–0.001	—	0.001	dB
		Stopband attenuation	f ≥ 0.80 Fs	108	—	—	dB
		Group delay [2]	linear phase	—	7.6/Fs	—	s
			minimum phase	—	5.4/Fs	—	s
	Balanced roll-off	Passband	to –3 dB corner	—	—	0.28	Fs
		Passband ripple	f ≤ 0.11 Fs	–0.001	—	0.001	dB
		Stopband attenuation	f ≥ 0.55 Fs	110	—	—	dB
		Group delay [2]	linear phase	—	10.6/Fs	—	s
			minimum phase	—	6.7/Fs	—	s
Fs = 352.8 or 384 kHz	Fast roll-off	Passband	to –3 dB corner	—	—	0.30	Fs
		Passband ripple	f ≤ 0.23 Fs	–0.004	—	0.000	dB
		Stopband attenuation	f ≥ 0.55 Fs	116	—	—	dB
		Group delay [2]	linear phase	—	14.4/Fs	—	s
			minimum phase	—	7.7/Fs	—	s
	Balanced roll-off	Passband	to –3 dB corner	—	—	0.23	Fs
		Passband ripple	f ≤ 0.06 Fs	–0.001	—	0.000	dB
		Stopband attenuation	f ≥ 0.55 Fs	116	—	—	dB
		Group delay [2]	linear phase	—	10.4/Fs	—	s
			minimum phase	—	7.6/Fs	—	s
Fs = 705.6 or 768 kHz	Fast roll-off	Passband	to –3 dB corner	—	—	0.15	Fs
		Passband ripple	f ≤ 0.11 Fs	–0.005	—	0.001	dB
		Stopband attenuation	f ≥ 0.30 Fs	101	—	—	dB
		Group delay [2]	linear phase	—	23.9/Fs	—	s
			minimum phase	—	13.7/Fs	—	s
	Balanced roll-off	Passband	to –3 dB corner	—	—	0.12	Fs
		Passband ripple	f ≤ 0.03 Fs	–0.001	—	0.000	dB
		Stopband attenuation	f ≥ 0.27 Fs	116	—	—	dB
		Group delay [2]	linear phase	—	19.9/Fs	—	s
			minimum phase	—	14.3/Fs	—	s

1. The DAC filters are supported on the ASP path only; they are not supported for the DSD input path.
2. Group delay is measured from the start of the FSYNC frame containing the audio data on the ASP_DINn pin to the time at which the signal is presented on the output pins (OUTnP/OUTnN).

Table 3-6. DAC High-Pass Filter (HPF)

Test conditions (unless specified otherwise): VDD_A = VDD_IO = 3.3 V; VDD_D = 1.2 V (powered from internal LDO); Ground = GND_A = GND_D = 0 V; voltages are with respect to ground; T_A = +25ºC; 1 kHz sine wave test signal; Fs = 48 kHz, 32-bit audio data.

Parameter [1]		Min	Typ	Max	Units
Passband	–0.01 dB corner	—	19	—	Hz
	–3 dB corner	—	1	—	Hz
Phase deviation	f = 20 Hz	—	0.001	—	degree
Filter settling time		—	0.4	—	s

1. The DAC high-pass filter is supported on the ASP path only; it is not supported for the DSD input path.

Table 3-7. Device Power Consumption

Test conditions (unless specified otherwise): VDD_A = VDD_IO = 3.3 V; VDD_D = 1.2 V (powered from internal LDO); Ground = GND = GND_A = GND_D = 0 V; voltages are with respect to ground; T_A = +25ºC; 1 kHz sine wave test signal; Fs = 48 kHz, 32-bit audio data.

Use Configuration	Typical Current (mA)		Total Power (mW)
	I_{VDD_A}	I_{VDD_IO}	
Reset — $\overline{RESET}$ = Logic 0	0.70	0.04	2.4
Four channels enabled	TBD	TBD	TBD

Table 3-8. Digital Interface Specifications and Characteristics

Test conditions (unless specified otherwise): Ground = GND = GND_A = GND_D = 0 V; voltages are with respect to ground; T_A = +25ºC.

Parameter		Symbol	Minimum	Maximum	Unit
Input leakage current (per pin)		I_{IN}	—	±10	µA
Input capacitance (per pin)		—	—	5	pF
Digital I/O (VDD_IO logic—all pins except CONFIG1 and CONFIG5) [1]	High-level output	V_{OH}	0.9×VDD_IO	—	V
	Low-level output	V_{OL}	—	0.1×VDD_IO	V
	High-level input	V_{IH}	0.7×VDD_IO	—	V
	Low-level input	V_{IL}	—	0.3×VDD_IO	V
Digital I/O (VDD_A logic—CONFIG1 and CONFIG5 pins) [1]	High-level output	V_{OH}	0.9×VDD_A	—	V
	Low-level output	V_{OL}	—	0.1×VDD_A	V

1. The CONFIGx pins support digital output if configured as GP output (see Section 4.10).

Table 3-9. DC Characteristics

Test conditions (unless specified otherwise): VDD_A = VDD_IO = 3.3 V; VDD_D = 1.2 V (powered from internal LDO); Ground = GND = GND_A = GND_D = 0 V; voltages are with respect to ground; T_A = +25ºC.

Parameter			Minimum	Typical	Maximum	Unit
DAC_FILT [1]	Nominal voltage	VDD_A to DAC_FILTP	—	2.00	—	V
		DAC_FILTN to GND	—	1.25	—	V
	Maximum output current		—	50	—	µA
DAC_VMID [2]	Nominal voltage		—	1.65	—	V
	Maximum output current		—	0.01	—	mA
VDD_A power-on reset (POR) threshold (V_{POR})		VDD_A rising	1.9	—	2.7	V
		VDD_A falling	1.8	—	2.6	V
VDD_D power-on reset (POR) threshold (V_{POR})		VDD_D rising	0.90	—	1.05	V
		VDD_D falling	0.75	—	0.90	V

1. DAC_FILT characteristics are provided as a guide for external component selection. The output current (arising from capacitor leakage) must be less than the maximum output current of the DAC_FILT pin.
2. The output current (arising from capacitor leakage and the input-buffer circuit) must be less than the maximum output current of the DAC_VMID pin. If a larger current is required, an external VMID buffer should be used. A buffer can be provided using a standard op-amp (noise voltage < 5 nV/√Hz, input current < 10 µA). An example circuit is as follows:

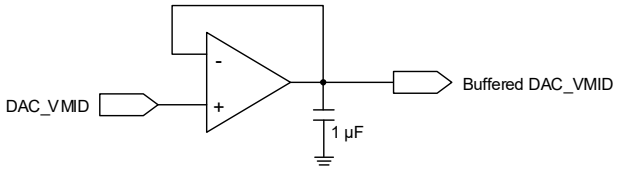


Table 3-10. Switching Specifications—Reset and Clock References

Test conditions (unless specified otherwise): VDD_A = VDD_IO = 3.3 V; VDD_D = 1.2 V (powered from internal LDO); Ground = GND = GND_A = GND_D = 0 V; voltages are with respect to ground; T_A = +25ºC.

Parameter		Symbol	Minimum	Typical	Maximum	Unit
Reset	$\overline{\text{RESET}}$ low (logic 0) pulse width	t_{RLPW}	1	—	—	ms
	$\overline{\text{RESET}}$ rising edge to control port active	t_{IRS}	—	—	5	ms
MCLK input	MCLK frequency (MCLK as clock source, PLL not used)	f_{MCLK}	— —	45.1584 49.152	— —	MHz MHz
	MCLK duty cycle (MCLK as clock source, PLL not used)	D_{MCLK}	40	—	60	%
	MCLK frequency tolerance (MCLK as clock source, PLL not used)	—	–1	—	1	%
Phase-locked loop (PLL)	REFCLK input frequency (BCLK or MCLK reference) [1]	f_{REFCLK}	— — — — — — — —	2.8224 5.6448 11.2896 22.5792 3.072 6.144 12.288 24.576	— — — — — — — —	MHz MHz MHz MHz MHz MHz MHz MHz
	REFCLK input duty cycle	D_{REFCLK}	45	—	55	%
	REFCLK frequency tolerance	—	–1	—	1	%
	PLL output frequency Fs = 32, 48, 96, 192, 384, 768 kHz Fs = 44.1, 88.2, 176.4, 352.8, 705.6 kHz	f_{PLL_OUT}	— —	49.152 45.1584	— —	MHz MHz
	PLL output jitter	j_{PLL_OUT}	—	500	—	ps_{RMS}
	PLL output period jitter	$j_{PLL\_OUT-PER}$	—	—	500	ps
	PLL lock time	t_{PLL_LOCK}	—	0.3	1	ms

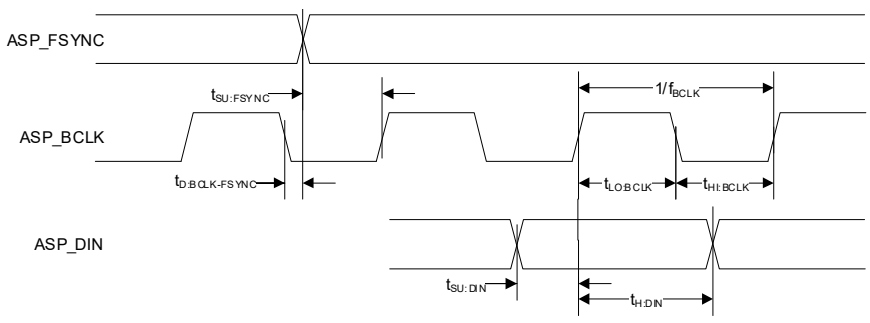
1.Note the REFCLK input frequency must be integer-related to the sample rate. See Section 4.4 for further details.

Table 3-11. Switching Specifications—Audio Serial Port (ASP)

Test conditions (unless specified otherwise): VDD_A = 3.3 V; VDD_D = 1.2 V (powered from internal LDO); Ground = GND = GND_A = GND_D = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds for VDD_IO logic (as specified in Table 3-8); T_A = 25°C.

Parameter [1,2,3]		Symbol	Minimum	Maximum	Unit
Secondary Mode, VDD_IO = 3.3 V	ASP_FSYNC input sample/frame rate	Fs	32	768	kHz
	ASP_FSYNC pulse width	$t_{HI:FSYNC}$	$1/f_{ASP\_BCLK}$	—	ns
	ASP_BCLK frequency	f_{BCLK}	2.048	24.576	MHz
	ASP_BCLK high period	$t_{HI:BCLK}$	18	—	ns
	ASP_BCLK low period	$t_{LO:BCLK}$	18	—	ns
	ASP_FSYNC setup time before ASP_BCLK latching edge	$t_{SU:FSYNC}$	5	—	ns
	ASP_FSYNC hold time after ASP_BCLK latching edge	$t_{H:FSYNC}$	5	—	ns
	ASP_DIN setup time before ASP_BCLK latching edge	$t_{SU:DIN}$	10	—	ns
	ASP_DIN hold time after ASP_BCLK latching	$t_{H:DIN}$	5	—	ns
Primary Mode, VDD_IO = 3.3 V	ASP_FSYNC output sample/frame rate	Fs	32	768	kHz
	ASP_BCLK frequency	f_{BCLK}	2.8224	24.576	MHz
	ASP_BCLK duty cycle PLL enabled, MCLK duty cycle 40–60% PLL bypass, BCLK < 22.5792 MHz, MCLK 40–60% PLL bypass, BCLK ≥ 22.5792 MHz, MCLK 45–55% PLL bypass, BCLK ≥ 22.5792 MHz, MCLK 40–60%	D_{BCLK}	 45 45 42 37	 55 55 58 63	 % % % %
	ASP_FSYNC delay time after ASP_BCLK launching edge	$t_{D:BCLK–FSYNC}$	0	20	ns
	ASP_DIN setup time before ASP_BCLK latching edge	$t_{SU:DIN}$	6	—	ns
	ASP_DIN hold time after ASP_BCLK latching edge	$t_{H:DIN}$	5	—	ns
	ASP_x load capacitance ASP_BCLK ASP_FSYNC	—	 0 0	 50 50	 pF pF
Secondary Mode, VDD_IO = 1.8 V	ASP_FSYNC input sample/frame rate	Fs	32	768	kHz
	ASP_FSYNC pulse width	$t_{HI:FSYNC}$	$1/f_{ASP\_BCLK}$	—	ns
	ASP_BCLK frequency	f_{BCLK}	2.048	24.576	MHz
	ASP_BCLK high period	$t_{HI:BCLK}$	18	—	ns
	ASP_BCLK low period	$t_{LO:BCLK}$	18	—	ns
	ASP_FSYNC setup time before ASP_BCLK latching edge	$t_{SU:FSYNC}$	5	—	ns
	ASP_FSYNC hold time after ASP_BCLK latching edge	$t_{H:FSYNC}$	5	—	ns
	ASP_DIN setup time before ASP_BCLK latching edge	$t_{SU:DIN}$	10	—	ns
	ASP_DIN hold time after ASP_BCLK latching	$t_{H:DIN}$	5	—	ns
Primary Mode, VDD_IO = 1.8 V	ASP_FSYNC output sample/frame rate	Fs	32	768	kHz
	ASP_BCLK frequency	f_{BCLK}	2.8224	24.576	Mhz
	ASP_BCLK duty cycle PLL enabled, MCLK duty cycle 40–60% PLL bypass, BCLK < 22.5792 MHz, MCLK 40–60% PLL bypass, BCLK ≥ 22.5792 MHz, MCLK 45–55% PLL bypass, BCLK ≥ 22.5792 MHz, MCLK 40–60%	D_{BCLK}	 45 45 42 37	 55 55 58 63	 % % % %
	ASP_FSYNC delay time after ASP_BCLK launching edge	$t_{D:BCLK–FSYNC}$	0	20	ns
	ASP_DIN setup time before ASP_BCLK latching edge	$t_{SU:DIN}$	6	—	ns
	ASP_DIN hold time after ASP_BCLK latching edge	$t_{H:DIN}$	5	—	ns
	ASP_x load capacitance ASP_BCLK ASP_FSYNC	—	 0 0	 50 50	 pF pF

1. The ASP_BCLK launching edge is selectable. Half-cycle mode = ASP_BCLK launching edge is opposite to latching edge. Full-cycle mode = ASP_BCLK launching edge is same as latching edge.
2. ASP timing in I²S and Left-Justified Modes.
   Note that ASP_BCLK can be inverted if required; the figure shows the default polarity.



3.ASP timing in TDM Mode.
Note that ASP_BCLK can be inverted if required; the figure shows the default polarity.

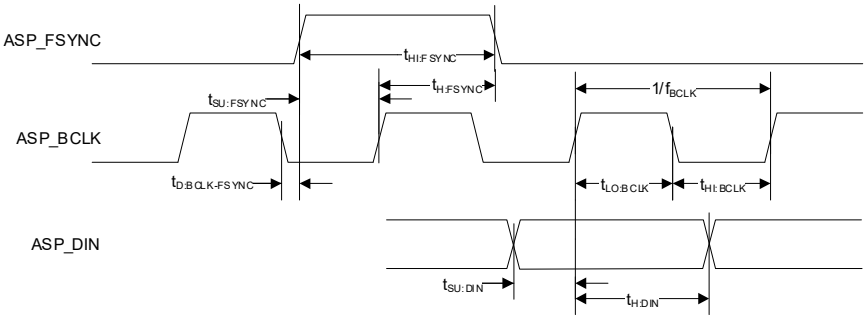
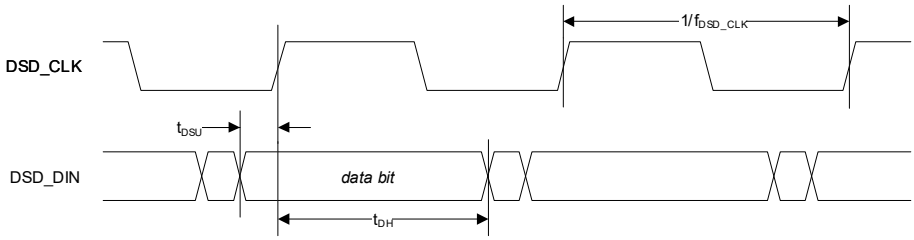


Table 3-12. Switching Specifications—Direct Stream Digital (DSD) Interface

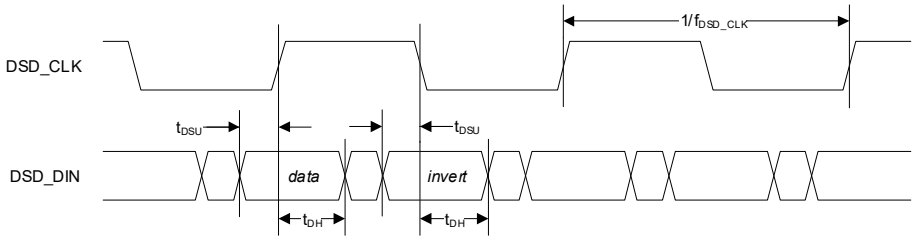
Test conditions (unless specified otherwise): VDD_A = VDD_IO = 3.3 V; VDD_D = 1.2 V (powered from internal LDO); Ground = GND = GND_A = GND_D = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds for VDD_IO logic (as specified in Table 3-8); T_A = 25°C.

Parameter [1,2,3]		Symbol	Minimum	Maximum	Unit
Normal Mode	DSD_CLK frequency	f_{DSD_CLK}	2.8224	22.5792	MHz
	DSD_CLK duty cycle	—	45	55	%
	DSD_DIN setup time to active DSD_CLK edge	t_{DSU}	10	—	ns
	DSD_DIN fall time from active DSD_CLK edge	t_{DH}	10	—	ns
Phase Modulation Mode	DSD_CLK frequency 64fs CLK (DSD_PM_SEL = 1) 128fs CLK (DSD_PM_SEL = 0)	f_{DSD_CLK}	2.8224 5.6448	2.8224 5.6448	MHz MHz
	DSD_CLK duty cycle	—	45	55	%
	DSD_DIN setup time to active DSD_CLK edge	t_{DSU}	10	—	ns
	DSD_DIN fall time from active DSD_CLK edge	t_{DH}	10	—	ns

1.DSD Normal Mode.



2.DSD Phase Modulation, (64fs CLK).



3.DSD Phase Modulation, (128fs CLK).

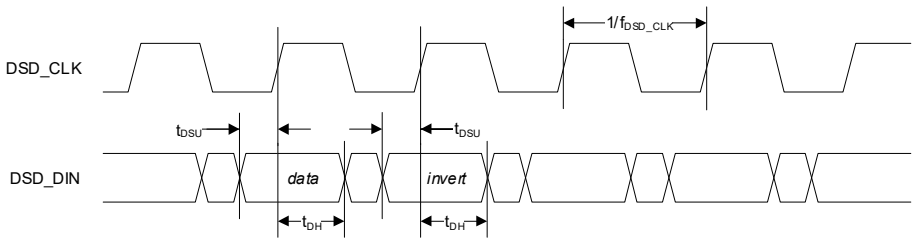
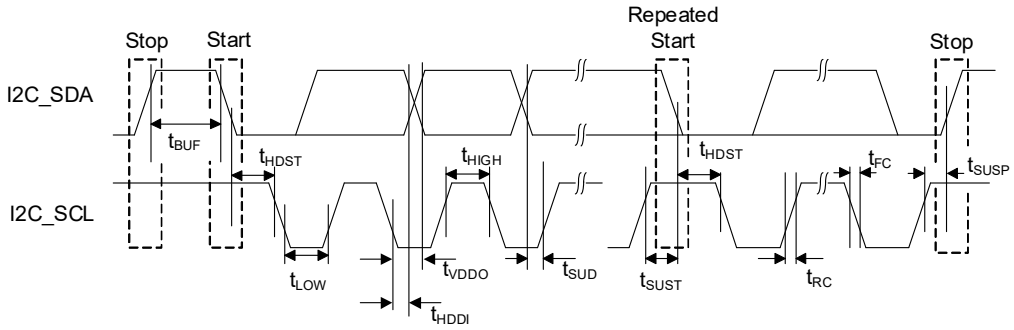


Table 3-13. Switching Specifications—I²C Control Port

Test conditions (unless specified otherwise): VDD_A = VDD_IO = 3.3 V; VDD_D = 1.2 V (powered from internal LDO); Ground = GND = GND_A = GND_D = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds for VDD_IO logic (as specified in Table 3-8); T_A = 25°C.

Parameter [1,2]		Symbol	Minimum	Maximum	Unit
SCL clock frequency		f_{SCL}	—	1000	kHz
Clock low time		t_{LOW}	500	—	ns
Clock high time		t_{HIGH}	260	—	ns
Start condition hold time (before first clock pulse)		t_{HDST}	260	—	ns
Setup time for repeated start		t_{SUST}	260	—	ns
Rise time of SCL and SDA	$f_{SCL} \le 100$ kHz 100 kHz < $f_{SCL} \le 400$ kHz 400 kHz < $f_{SCL} \le 1000$ kHz	t_{RC}	600 180 72	1000 300 120	ns ns ns
Fall time of SCL and SDA	$f_{SCL} \le 100$ kHz 100 kHz < $f_{SCL} \le 400$ kHz 400 kHz < $f_{SCL} \le 1000$ kHz	t_{FC}	6.5 6.5 6.5	300 300 120	ns ns ns
Rise time variation between SDA and SCL		—	—	1.67	x
Fall time variation between SDA and SCL	$f_{SCL} \le 100$ kHz 100 kHz < $f_{SCL} \le 400$ kHz 400 kHz < $f_{SCL} \le 1000$ kHz	—	— — —	100 100 75	ns ns ns
Setup time for stop condition		t_{SUSP}	260	—	ns
SDA setup time to SCL rising		t_{SUD}	50	—	ns
SDA input hold time from SCL falling [3]		t_{HDDI}	0	—	ns
Output data valid (Data/ACK) [4]	$f_{SCL} \le 100$ kHz 100 kHz < $f_{SCL} \le 400$ kHz 400 kHz < $f_{SCL} \le 1000$ kHz	t_{VDDO}	— — —	3450 900 450	ns ns ns
Bus free time between transmissions		t_{BUF}	500	—	ns
SDA bus capacitance		C_B	—	550	pF
SCL/SDA pull-up resistance		R_P	500	—	Ω
Pulse width of spikes to be suppressed		t_{ps}	0	50	ns

1.All timing is relative to thresholds specified in Table 3-8, V_{IL} and V_{IH} for input signals, and V_{OL} and V_{OH} for output signals.
2.I²C control-port timing.



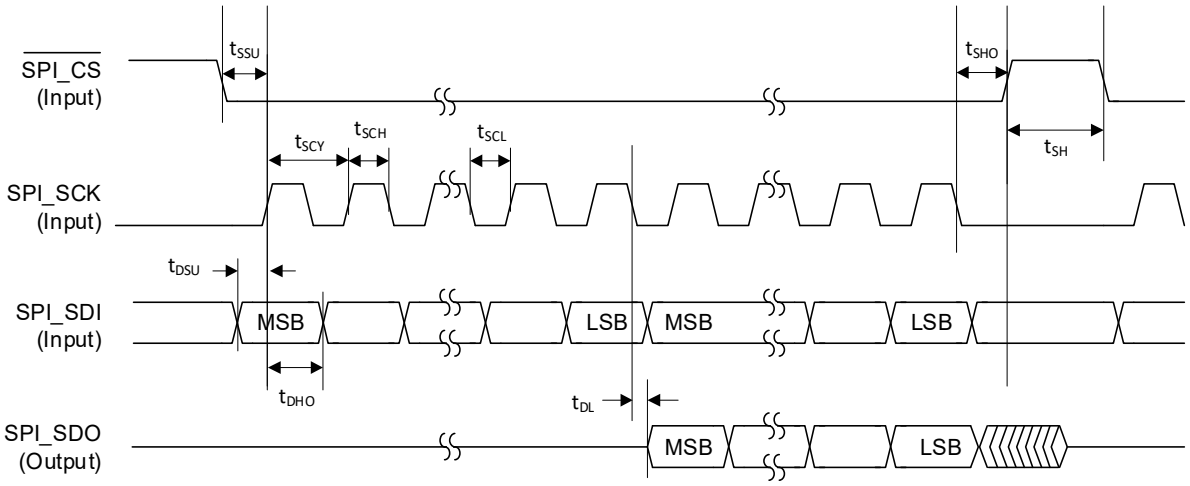
3.Data must be held long enough to bridge the transition time, t_{FC}, of SCL.
4.Time from falling edge of SCL until data output is valid.

Table 3-14. Switching Specifications—SPI Control Port

Test conditions (unless specified otherwise): VDD_A = VDD_IO = 3.3 V; VDD_D = 1.2 V (powered from internal LDO); Ground = GND = GND_A = GND_D = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds for VDD_IO logic (as specified in Table 3-8); T_A = 25°C.

Parameter [1]	Symbol	Minimum	Maximum	Unit
SPI_SCK frequency	f_{SCY}	—	24	MHz
$\overline{\text{SPI\_CS}}$ falling edge to SPI_SCK rising edge	t_{SSU}	5	—	ns
SPI_SCK falling edge to $\overline{\text{SPI\_CS}}$ rising edge	t_{SHO}	0.5	—	ns
SPI_SCK pulse width low	t_{SCL}	18.5	—	ns
SPI_SCK pulse width high	t_{SCH}	18.5	—	ns
SPI_SDI to SPI_SCK setup time	t_{DSU}	5	—	ns
SPI_SDI to SPI_SCK hold time	t_{DHO}	2.5	—	ns
SPI_SCK falling edge to SPI_SDO transition	t_{DL}	0	15	ns
$\overline{\text{SPI\_CS}}$ rising edge to SPI_SDO output high-Z	—	0	15	ns
Bus free time between active $\overline{\text{SPI\_CS}}$	t_{SH}	20	—	ns

1.SPI control-port timing.



4 Functional Description

4.1 Device Power and Reset

The CS4304P is powered using VDD_A1, VDD_A2, VDD_D, and VDD_IO external supplies.

Notes: The VDD_A1 and VDD_A2 rails should be tied together and powered from a single supply. The associated power domain is referred to as VDD_A.

The digital supply, VDD_D, is powered from an internal LDO regulator. The output of the LDO regulator is provided on the LDO_D_FILT pin—the VDD_D pin should be connected to LDO_D_FILT.

There are no power-sequencing requirements—supplies can be enabled in any order.

The CS4304P is in reset if the $\overline{\text{RESET}}$ pin is asserted (Logic 0), or if the VDD_A or VDD_D supply is below the respective reset threshold defined in Table 3-9.

All ground pins, including the ground paddle, must be tied to a common ground plane directly underneath the CS4304P.

4.2 Hardware Configuration

The CS4304P supports hardware and software control modes. In hardware mode, the device configuration is determined entirely by external resistors connected to the hardware-control pins. In software mode, the I²C/SPI control port is used to configure the device.

Note: The hardware-control pins CONFIG1 and CONFIG5 are powered by VDD_A. The CONFIG2, CONFIG3, and CONFIG4 pins are powered by VDD_IO. Care must be taken to ensure any external pull-up resistors on these pins are connected to the applicable power domain.

In hardware mode, the audio serial port (ASP) configuration is selected using the CONFIG1 and CONFIG2 pins as described in Table 4-1. See Section 4.4 for more details of the sample-rate selection. See Section 4.7 for more details of the ASP operation.

Note that the DSD interface (Section 4.8) is not supported in hardware control mode.

Table 4-1. Hardware Control—ASP Configuration

Pin Name	Pin Configuration		Description
CONFIG1	Pull-up to VDD_A	0 Ω	Software control mode (I²C/SPI)
		4.7 kΩ	ASP Primary Mode, 44.1 kHz, 48 kHz sample rate
		22 kΩ	ASP Primary Mode, 88.2 kHz, 96 kHz sample rate
		100 kΩ	ASP Primary Mode, 176.4 kHz, 192 kHz sample rate
	Pull-down to GND_A	100 kΩ	ASP Secondary Mode, 176.4 kHz, 192 kHz sample rate
		22 kΩ	ASP Secondary Mode, 88.2 kHz, 96 kHz sample rate
		4.7 kΩ	ASP Secondary Mode, 44.1 kHz, 48 kHz sample rate
		0 Ω	ASP Secondary Mode, autodetect sample rate [1,2]
CONFIG2	Pull-up to VDD_IO	0 Ω	ASP TDM Mode—minimum time slots [3]
		4.7 kΩ	ASP TDM Mode—maximum time slots [4]
		22 kΩ	—
		100 kΩ	—
	Pull-down to GND_D	100 kΩ	—
		22 kΩ	—
		4.7 kΩ	ASP Left-Justified Mode
		0 Ω	ASP I²S Mode

1. Valid sample rates for autodetect are 32, 44.1, 48, 88.2, 96, 176.4, and 192 kHz.
2. Autodetect sample rate is only supported in MCLK = 256 fs(base), MCLK = 512 fs(base), or MCLK 1024 fs(base) clocking configurations (see Table 4-3).
3. The ASP data format is configured to support the minimum number of time slots necessary for the 4-channel CS4304P input.
4. The ASP data format is configured to support the maximum number of time slots for the applicable BCLK rate.

If the ASP is configured for TDM data format with maximum time slots, the TDM slot selection is determined using the CONFIG3 pin as described in Table 4-2. See Section 4.7 for more details of the ASP TDM modes.

Table 4-2. Hardware Control—TDM Slot Selection

Pin Name	Pin Configuration		Description
CONFIG3	Pull-up to VDD_IO	0 Ω	Slots 12–15 [1]
		4.7 kΩ	
		22 kΩ	Slots 8–11 [1]
		100 kΩ	
	Pull-down to GND_D	100 kΩ	Slots 4–7 [2]
		22 kΩ	
		4.7 kΩ	Slots 0–3
		0 Ω	

1.Slots 8–15 are only valid in 16-slot TDM Mode.
2.Slots 4–7 are only valid in 8-slot or 16-slot TDM Mode.

The clock-reference and ASP channel-ordering configuration is determined using the CONFIG4 pin as described in Table 4-3. See Section 4.4 for more details of the CS4304P clocking architecture. See Section 4.7.5 for more details of the ASP reverse channel-order option.

Table 4-3. Hardware Control—Clocking Configuration

Pin Name	Pin Configuration		Clock Reference [1,2,3,4]	PLL	Channel Order
CONFIG4	Pull-up to VDD_IO	0 Ω	BCLK = 64 fs	Enabled	Default
		4.7 kΩ	MCLK = 1024 fs(base)	Bypass	Default
		22 kΩ	MCLK = 256 fs(base)	Enabled	Default
		100 kΩ	MCLK = 512 fs(base)	Enabled	Default
	Pull-down to GND_A	100 kΩ	MCLK = 512 fs(base)	Enabled	Reversed
		22 kΩ	MCLK = 256 fs(base)	Enabled	Reversed
		4.7 kΩ	MCLK = 1024 fs(base)	Bypass	Reversed
		0 Ω	BCLK = 64 fs	Enabled	Reversed

1.fs = sample rate, 44.1, 48, 88.2, 96, 176.4, or 192 kHz.
2.fs(base) is the base sample rate. fs(base) = 48 kHz for 48 kHz-related sample rates; fs(base) = 44.1 kHz for 44.1 kHz-related sample rates.
3.BCLK 64 fs configuration is only supported in ASP Secondary Mode.
4.Autodetect sample rate (see Table 4-1) is only supported in MCLK = 256 fs(base), MCLK = 512 fs(base), or MCLK 1024 fs(base) clocking configurations.

In hardware mode, the digital filter is selected using the CONFIG5 pin as described in Table 4-4. Note the filter selection is also dependent on the sample rate. See Section 4.6 for more details of the digital filters.

Table 4-4. Hardware Control—DAC Output Digital Filter Selection

Pin Name	Pin Configuration		DAC Interpolation Filter		High-Pass Filter (HPF)
			32–48 kHz Sample Rate [1]	88.2–192 kHz Sample Rate	
CONFIG5	Pull-up to VDD_A	0 Ω	Minimum phase, slow roll-off	Minimum phase, balanced roll-off	Bypass
		4.7 kΩ	Minimum phase, fast roll-off	Minimum phase, fast roll-off	Bypass
		22 kΩ	Linear phase, slow roll-off	Linear phase, balanced roll-off	Bypass
		100 kΩ	Linear phase, fast roll-off	Linear phase, fast roll-off	Bypass
	Pull-down to GND_A	100 kΩ	Linear phase, fast roll-off	Linear phase, fast roll-off	Enabled
		22 kΩ	Linear phase, slow roll-off	Linear phase, balanced roll-off	Enabled
		4.7 kΩ	Minimum phase, fast roll-off	Minimum phase, fast roll-off	Enabled
		0 Ω	Minimum phase, slow roll-off	Minimum phase, balanced roll-off	Enabled

1.Fast roll-off filters are supported for all sample rates. Slow roll-off filters are not valid for 32 kHz sample rate.

In hardware mode, the device configuration is latched when reset is released (either power-on reset or deassertion of the $\overline{\text{RESET}}$ pin). In hardware mode, the configuration cannot be changed while the device is operational. To update the device configuration, the $\overline{\text{RESET}}$ pin must be asserted (Logic 0), or the device power cycled, in order to read new settings on the CONFIGx pins.

If software mode is selected (i.e., CONFIG1 has a 0 Ω pull-up to VDD_A), the ASP configuration and digital-filter selection are controlled by register writes via the applicable control interface. Unused CONFIGx pins should be terminated as described in Section 1.3.

Notes: In software mode, the CONFIG2 and CONFIG3 pins can optionally be used to support the DSD interface (see Section 4.8).

In software mode, the CONFIG5 pin is used to select the I²C target address (see Section 4.9). If the SPI control interface is used, it is recommended to connect the CONFIG5 pin to GND.

4.3 Software Configuration

Software control mode is enabled if the CONFIG1 pin is connected to VDD_A. In software control mode, the CS4304P is configured by writing to control registers using the control port.

The control port supports I²C and SPI modes of operation; the applicable mode is detected automatically on the respective interface pins. In I²C mode, the target address is selectable using the CONFIG5 pin. See Section 4.9 for further details of the I²C/SPI control port.

In software control mode, GLOBAL_EN is used as the global control field for enabling/disabling the CS4304P functions. The device should be configured using the applicable control registers before setting GLOBAL_EN.

Notes: The clocking (Section 4.4) and ASP (Section 4.7) control registers are only valid on the rising edge of GLOBAL_EN. Writing to these registers has no effect at any other time. It is recommended to select the disabled state (GLOBAL_EN = 0) before writing to these registers.

See Section 4.5.1 to minimize the CS4304P power consumption when all output paths are disabled.

A reset of the CS4304P can be triggered by writing 0x5A to the SW_RESET field. A software reset disables all functions and sets the control registers to their default states.

4.4 System Clocking

Clocking for the CS4304P is provided from the digital audio input (ASP_BCLK or DSD_CLK) or else using the dedicated MCLK input.

The integrated PLL can be used to generate the internal system clock from the external reference. The MCLK signal can be used as a direct clock source, bypassing the PLL. If ASP_BCLK or DSD_CLK is selected as the clock reference, the PLL is always used and cannot be bypassed.

In ASP Secondary Mode, the FSYNC input is used to control the DAC-conversion timing, enabling multiple CS4304P devices to operate synchronously in a system. See Section 4.7 for more details of the ASP.

The clocking architecture is illustrated in Fig. 4-1.

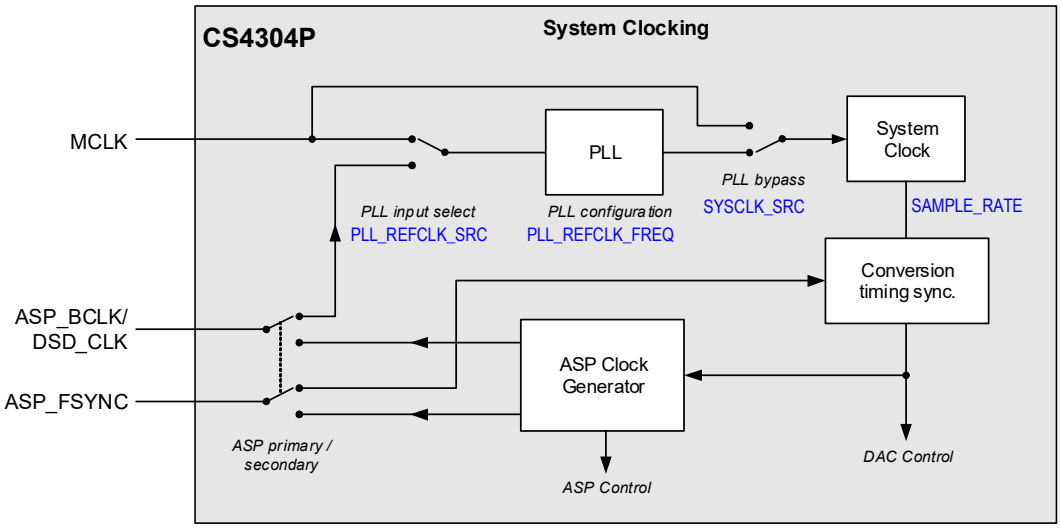


Figure 4-1. System Clocking

4.4.1 Hardware Control Mode

In hardware control mode, the clocking configuration is determined by the CONFIG4 pin (see Section 4.2). Four possible clocking configurations are supported as follows:

- BCLK reference—64 fs, PLL enabled
- MCLK reference—1024 fs(base), PLL bypass
- MCLK reference—256 fs(base), PLL enabled
- MCLK reference—512 fs(base), PLL enabled

The clocking configuration is defined with reference to the sample rate (fs). Note that fs(base) is the *base sample rate*; fs(base) = 48 kHz for 48 kHz-related sample rates, fs(base) = 44.1 kHz for 44.1 kHz-related sample rates.

The sample rate is selected using the CONFIG1 pin as described in Section 4.2. Sample rates 44.1 kHz–192 kHz can be configured, or else the autodetect option (32 kHz–192 kHz) automatically configures the device according to the ASP interface clock signals. Note the autodetect sample-rate option is only valid if the clock reference source is MCLK and the ASP is operating in Secondary Mode (see Section 4.7).

The BCLK 64 fs configuration enables the CS4304P to be clocked from the audio serial port (ASP) operating in Secondary Mode, with no requirement for any other clock reference. Note that, in the BCLK 64 fs clocking configuration, the ASP data format must be either I²S or left-justified.

The MCLK-referenced configurations use a fixed clock frequency of 12.288 / 24.576 / 49.152 MHz (for 48 kHz-related sample rates), or 11.2896 / 22.5792 / 45.1584 MHz (for 44.1 kHz-related sample rates).

The supported clocking configurations are summarized in Table 4-5.

Table 4-5. System Clock Configuration

Description	PLL Select	Reference Source	Reference Frequency	ASP Operating Conditions [1]
BCLK = 64 fs	Enabled	BCLK	64 × sample rate	Secondary Mode only, I²S or left-justified data formats, sample rates 44.1–192 kHz, sample-rate autodetect not supported.
MCLK = 1024 fs(base)	Bypass	MCLK	49.152 MHz or 45.1584 MHz	Primary or Secondary Mode, I²S, left-justified, or TDM data formats, sample rates 32–192 kHz, sample-rate autodetect supported.
MCLK = 256 fs(base)	Enabled	MCLK	12.288 MHz or 11.2896 MHz	
MCLK = 512 fs(base)	Enabled	MCLK	24.576 MHz or 22.5792 MHz	

1. See Section 4.7 for details of the audio serial port (ASP).

The sample rate must be related to the system clock reference as described in Table 4-6.

Table 4-6. Sample Rate Options

Reference Source	Clocking Configuration	Reference Frequency (MHz)	Sample Rate (kHz)
BCLK	BCLK = 64 fs	2.8224	44.1
		5.6448	88.2
		11.2896	176.4
		3.072	48
		6.144	96
		12.288	192
MCLK	MCLK = 1024 fs(base)	45.1584	44.1, 88.2, 176.4
		49.152	32, 48, 96, 192
	MCLK = 256 fs(base)	11.2896	44.1, 88.2, 176.4
		12.288	32, 48, 96, 192
	MCLK = 512 fs(base)	22.5792	44.1, 88.2, 176.4
		24.576	32, 48, 96, 192

Note that, if MCLK is configured as the clock source (with or without PLL) and the ASP is configured in Secondary Mode, the external clocks (MCLK, BCLK, and FSYNC) must be derived from a common clock source. The clocks must be synchronized, but the phase difference is not important.

4.4.2 Software Control Mode—ASP Input

In software (I²C/SPI) control mode, with the ASP selected as the audio source (see Section 4.7), the clocking configuration is selected using the following control fields:

- The sample rate is configured using SAMPLE_RATE. Sample rates 32 kHz–768 kHz can be configured, or else the autodetect option automatically configures the device according to the ASP interface signals. The sample rate must be related to the system clock reference as described in Table 4-8.

  Note that the sample-rate autodetect option is only valid if all the following conditions are met:
  - Sample rate is 32 kHz–192 kHz
  - The clock reference source is MCLK
  - ASP is operating in Secondary Mode (see Section 4.7).
- The system clock source is selected using SYSCLK_SRC. The clock source can be either MCLK or the output from the PLL. If MCLK is selected (i.e., PLL bypass), the MCLK frequency must be 49.152 MHz (for 48 kHz-related sample rates) or 45.1584 MHz (for 44.1 kHz-related sample rates).
- The input reference to the PLL is selected using PLL_REFCLK_SRC. The reference can be either MCLK or BCLK. Note the BCLK reference is only valid if the ASP is operating in Secondary Mode.
- The frequency of the PLL input reference is configured using PLL_REFCLK_FREQ.

The supported clocking configurations are summarized in Table 4-7.

Table 4-7. System Clock Configuration

SYSCLK_SRC	PLL_REFCLK_SRC	Description	Reference Frequency	Sample Rate Autodetect Supported
0	X	MCLK reference, PLL bypass	49.152 MHz or 45.1584 MHz	Yes
1	1	MCLK reference, PLL enabled	Configured by PLL_REFCLK_FREQ	Yes
1	0	BCLK reference, PLL enabled		No

The sample rate must be related to the system clock reference as described in Table 4-8.

Table 4-8. Sample Rate Options

Reference Frequency (MHz)	PLL_REFCLK_FREQ	Sample Rate (kHz) [1]
2.8224	00	44.1, 88.2, 176.4, 352.8, 705.6
5.6448	01	
11.2896	10	
22.5792	11	
45.1584	See note [2]	
3.072	00	32, 48, 96, 192, 384, 768
6.144	01	
12.288	10	
24.576	11	
49.152	See note [2]	

1. Sample rate is configured using SAMPLE_RATE.
2. Only valid in PLL-bypass configuration. The PLL_REFCLK_FREQ setting is not used.

Note that, if MCLK is configured as the clock source (with or without PLL) and the ASP is configured in Secondary Mode, the external clocks (MCLK, BCLK, and FSYNC) must be derived from a common clock source. The clocks must be synchronized, but the phase difference is not important.

4.4.3 Software Control Mode—DSD Input

In software (I²C/SPI) control mode, with the DSD interface selected as the audio source (see Section 4.8), the clocking configuration is selected using the following control fields:

- The system clock source is selected using SYSCLK_SRC. The clock source can be either MCLK or the output from the PLL. If MCLK is selected (i.e., PLL bypass), the MCLK frequency must be 45.1584 MHz.
- The input reference to the PLL is selected using PLL_REFCLK_SRC. The reference can be either MCLK or DSD_CLK. The DSD_CLK frequency is configured using DSD_OSR as described in Section 4.8.2.
- The frequency of the PLL input reference is configured using PLL_REFCLK_FREQ.

The supported clocking configurations are summarized in Table 4-9.

Table 4-9. System Clock Configuration

SYSCLK_SRC	PLL_REFCLK_SRC	Description	Reference Frequency
0	X	MCLK reference, PLL bypass	45.1584 MHz
1	1	MCLK reference, PLL enabled	Configured by PLL_REFCLK_FREQ
1	0	DSD_CLK reference, PLL enabled	

The supported reference frequencies for the PLL are noted in Table 4-10.

Table 4-10. PLL Reference Selection

Reference Frequency (MHz)	PLL_REFCLK_FREQ
2.8224	00
5.6448	01
11.2896	10
22.5792	11
45.1584	See note [1]

1. Only valid in PLL-bypass configuration. The PLL_REFCLK_FREQ setting is not used.

Note that, if MCLK is configured as the clock source (with or without PLL), the external clocks (MCLK and DSD_CLK) must be derived from a common clock source. The clocks must be synchronized, but the phase difference is not important.

4.5 DAC and Analog Output

The CS4304P supports four analog output channels, each incorporating a high-performance sigma-delta digital-to-analog converter (DAC). Digital volume and mute control is provided on each output channel.

Note that the digital volume and mute controls are supported in software (I^2C/SPI) control mode only. In hardware control mode, all channels are enabled with 0 dB gain.

4.5.1 DAC Path Enable

The analog output and DAC paths are enabled using OUTx_DAC_EN (where x indicates the channel number 1–4).

To minimize power consumption when all output paths are disabled, the DAC reference circuit can be disabled by setting DAC_REF_DISABLE. If this bit is set, all output paths are disabled, regardless of the OUTx_DAC_EN bits.

Note: Power consumption is only reduced if the output paths have previously been enabled. Until they are enabled for the first time, the power consumption is already minimized as far as possible.

When the output paths are enabled for the first time after power-up or after the DAC reference has been disabled, the paths do not become active until a startup delay has elapsed. The time delay (1 s default) is applied when the output paths are enabled using DAC_REF_DISABLE, GLOBAL_EN, or OUTx_DAC_EN ; the delay ensures the noise floor of the output path has settled before it becomes active.

The startup delay can be disabled using STARTUP_DELAY_EN. The delay duration is configurable using STARTUP_DELAY_TIME. If the delay is disabled or is shorter than 1 s, an elevated noise floor (~20 dB above specification) may be observed during the settling period.

The polarity of the DAC output can be inverted using OUTx_INV for the respective channel.

4.5.2 Digital Volume and Mute

The DAC signal path incorporates a digital volume control, supporting a gain range of –127.5 dB to 0 dB in 0.5 dB steps. Volume ramping and digital mute is also supported.

The digital volume is configured using OUTx_VOL for the respective output channel. The digital mute is enabled by setting OUTx_MUTE.

Writing to the volume or mute fields has no effect on the signal path until a 1 is written to OUT_VU. Writing 1 to OUT_VU causes the volume and mute settings to be updated on all output paths simultaneously.

When the volume or mute is changed, the gain of the affected signal paths is ramped up or down to the new setting. For increasing gain, the rate is controlled by OUT_RAMP_RATE_INC; for decreasing gain, the rate is controlled by OUT_RAMP_RATE_DEC.

Note: The OUT_RAMP_RATE_INC and OUT_RAMP_RATE_DEC fields should not be changed while a volume ramp is in progress.

4.5.3 DAC Output Summing

The CS4304P supports the option to combine the DAC signal paths in groups of two or four channels; this can be used to achieve enhanced dynamic-range performance on the respective paths.

In the summing configuration, the signal paths are routed and controlled differently to normal operation—the input signals are routed to groups of two or more DACs (depending on the selected configuration), and the grouped paths are each controlled as a single channel.

The DAC output summing is configured using OUT_SUM_MODE. The supported options are described in Table 4-11.

Note: The OUT_SUM_MODE field should not be changed while GLOBAL_EN is set. The GLOBAL_EN bit should always be cleared before writing to OUT_SUM_MODE.

Table 4-11. DAC Output Summing

Configuration	Description	Output Summing Configuration	Summed Channel Number
Default	4-channel input	OUT1–OUT4 as individual outputs	1–4
DACs combined in groups of two	2-channel input	OUT1+OUT2 OUT3+OUT4	1 2
DACs combined as a group of four	1-channel input	OUT1+OUT2+OUT3+OUT4	1

In the summing configuration, the respective analog output connections must be linked externally to achieve the performance enhancement. The analog outputs are current-mode outputs; the external linking of the outputs results in the summing of the respective output signals.

Note: The increased current in the summing configuration affects the choice of components for the output buffer—see Section 4.5.4 for further details.

The grouped output paths are configured using the control registers associated with the respective summed channel number (see Table 4-11). For example, the OUT3+OUT4 group is configured using the OUT2 control registers.

Typical connections, with outputs combined in groups of two, are shown in Fig. 4-2.

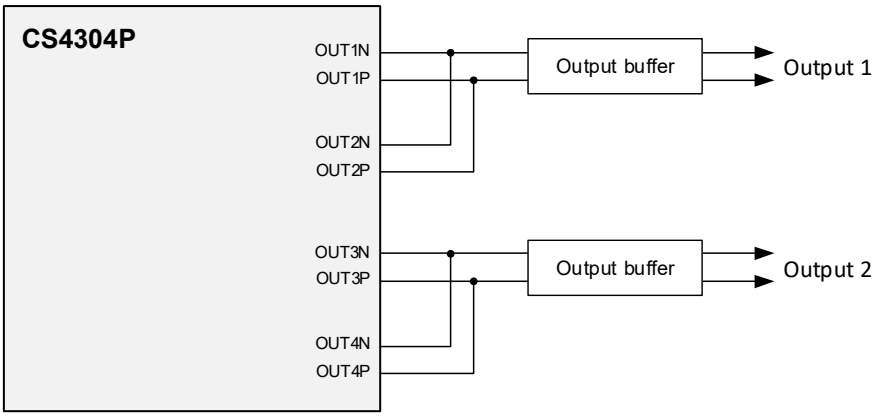


Figure 4-2. Output Summing

4.5.4 External Components

The analog output channels are supported using external buffer circuits, also incorporating anti-alias filters. A typical buffer circuit is shown in Fig. 4-3; the typical buffer circuit shown produces a 2 V_{RMS} differential output from a full-scale (0 dBFS) digital input.

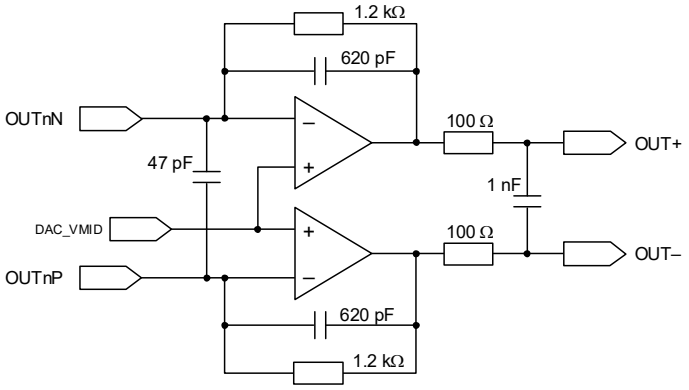


Figure 4-3. Output Buffer

In the summing configuration (see Section 4.5.3), the increased output current affects the choice of components for the output buffer. The feedback resistance must be selected according to the number of outputs that are summed, as described in Table 4-12. The 47 pF capacitance should be changed to 100 pF in the output-summing configurations.

Table 4-12. Output Buffer Components

Configuration	Capacitance	Resistance
No summing	47 pF	1.2 kΩ
2 outputs summed	100 pF	600 Ω
4 outputs summed	100 pF	300 Ω

Note: The specified resistance assumes 2 V_{RMS} full-scale output

Note that other output-buffer circuit topologies are possible, including support for single-ended output signals.

4.6 Digital Filter Selection

The DAC output path incorporates an interpolation filter and a high-pass filter. Six types of filter are supported:

- Fast roll-off, minimum phase
- Fast roll-off, linear phase
- Slow roll-off, minimum phase
- Slow roll-off, linear phase
- Balanced roll-off, minimum phase
- Balanced roll-off, linear phase

The phase-response options is characterized as follows:

- The **minimum-phase** filters offer the lowest latency and an impulse response with no pre-ringing, at the expense of potential in-band phase distortion.
- The **linear-phase** filters have no phase distortion, but also higher latency and a symmetric impulse response.

The frequency-response options are characterized as follows:

- The **fast roll-off** filters maximize the audio signal bandwidth (as a function of the selected sample rate) and provide deep stopband attenuation. The signal bandwidth and stopband attenuation are prioritized over impulse response and group delay. The deep stopband attenuation minimizes out-of-band noise and aliased signal content.

- The **slow roll-off** filters are optimized for impulse response and group delay, with flat passband over the audible range to 20 kHz and a more relaxed stopband specification. The enhanced impulse response may improve perceived sound quality, especially for transient signal content.

  Note the slow roll-off filters provide less stopband attenuation than other filter types. To avoid out-of-band noise above the stopband attenuation level, the system design must ensure the DAC input data does not contain significant energy above 20 kHz (for 48 kHz sample rate), 30 kHz (for 96 kHz sample rate), or 40 kHz (for 192 kHz sample rate).
- The **balanced roll-off** filters offer a superior impulse response and group delay as compared with the fast roll-off filters, while retaining a flat passband over the audible range to 20 kHz and deep stopband attenuation.

The supported filter options for different sample rates are indicated in Table 4-13.

Table 4-13. Digital Filter Options

Description	Sample Rate (kHz)										
	32	44.1	48	88.2	96	176.4	192	352.8	384	705.6	768
Fast roll-off, minimum phase	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Fast roll-off, linear phase	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Slow roll-off, minimum phase	—	Yes	Yes	Yes	Yes	Yes	Yes	—	—	—	—
Slow roll-off, linear phase	—	Yes	Yes	Yes	Yes	Yes	Yes	—	—	—	—
Balanced roll-off, minimum phase	—	—	—	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Balanced roll-off, linear phase	—	—	—	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

In hardware control mode, the filter selection is determined by the CONFIG5 pin (see Section 4.2). In software (I^2C/SPI) control mode, the interpolation filter is selected using OUT_FILTER_SEL; the high-pass filter is enabled using OUT_HPF_EN.

Performance plots showing the characteristics of the interpolation filters are shown in Section 7.

A deemphasis filter can also be enabled in the DAC output path. The filter provides standard *Red Book* deemphasis, with corner frequencies corresponding to 15 µs/50 µs time constants, as illustrated in Fig. 4-4.

The deemphasis filter is supported for 32 kHz, 44.1 kHz, and 48 kHz sample rates. The filter is enabled using OUT_DEEMPH_EN. If the sample rate is 44.1 kHz or 48 kHz, the applicable rate must be configured using OUT_DEEMPH_FILT_SEL.

Note: The deemphasis filter is not supported for sample rates above 48 kHz; enabling the filter at sample rates higher than 48 kHz has no effect.

The de-emphasis filter response is illustrated in Fig. 4-4.

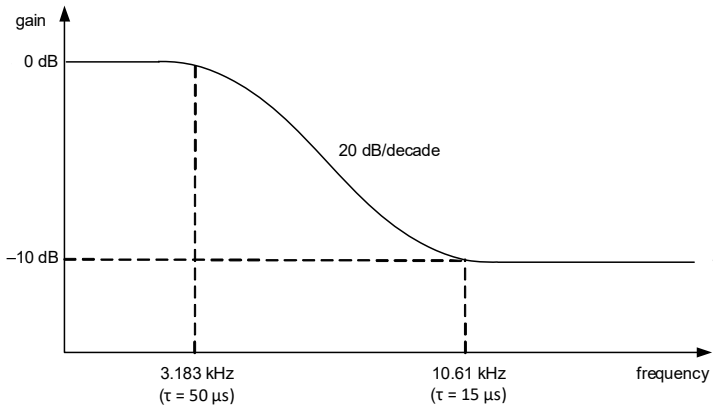


Figure 4-4. Deemphasis Filter Response

Note the interpolation and deemphasis filters are not supported on the DSD signal path (see Section 4.8).

4.7 Audio Serial Port (ASP)

The multichannel ASP supports the input of digital audio samples to the CS4304P. The ASP can be configured as a primary or secondary interface, and supports I²S, left-justified, and TDM data formats. The audio samples can be distributed across four data lines, enabling additional bandwidth and flexibility.

In hardware control mode, the ASP data format is determined by the CONFIGx pins (see Section 4.2). In software (I²C/SPI) control mode, the ASP data format is configured using register fields.

In hardware mode, sample rates 32 kHz–192 kHz are supported. In software mode, the CS4304P supports sample rates 32 kHz–768 kHz.

Note that the ASP interface is not supported if the DSD interface is enabled (see Section 4.8).

4.7.1 Primary and Secondary Operation

The ASP interface can operate as a primary or secondary interface. In the primary configuration, the BCLK and FSYNC signals are generated by the CS4304P. In the secondary configuration, the BCLK and FSYNC pins are inputs, allowing another device to drive the respective signals.

In hardware control mode, the ASP is configured as a primary or secondary interface using the CONFIG1 pin (see Section 4.2). In software control mode, the ASP primary/secondary configuration is selected using ASP_PRIMARY.

The ASP operation as a primary or secondary interface is illustrated in Fig. 4-5 and Fig. 4-6.

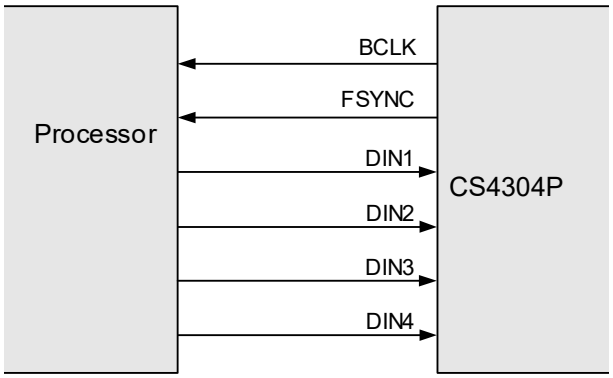


Figure 4-5. Primary Mode

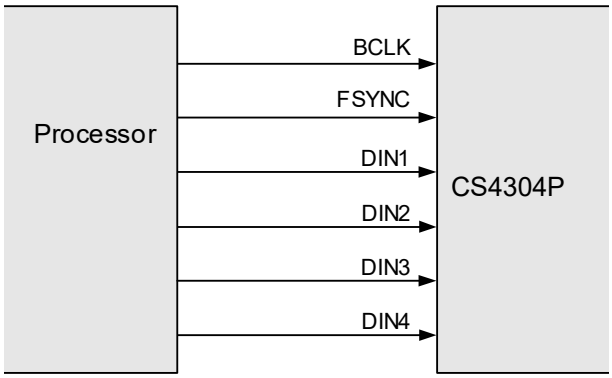


Figure 4-6. Secondary Mode

4.7.2 ASP Data Formats

The ASP interface can be configured to operate in I²S, left-justified, or TDM data formats as illustrated in Fig. 4-7 through Fig. 4-9. The data-bit order is MSB first in each case; data words are encoded in 2's complement (signed, fixed-point) format. Each audio sample is allocated a time slot within the FSYNC frame. Multiple data lines provide capacity to support different audio channels concurrently on different data pins.

- In I²S Mode, the MSB is valid on the second BCLK rising edge following a FSYNC transition. The other bits up to the LSB are valid on each successive BCLK cycle. Depending on word length, BCLK frequency, and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

  I²S Mode data format is shown in Fig. 4-7.

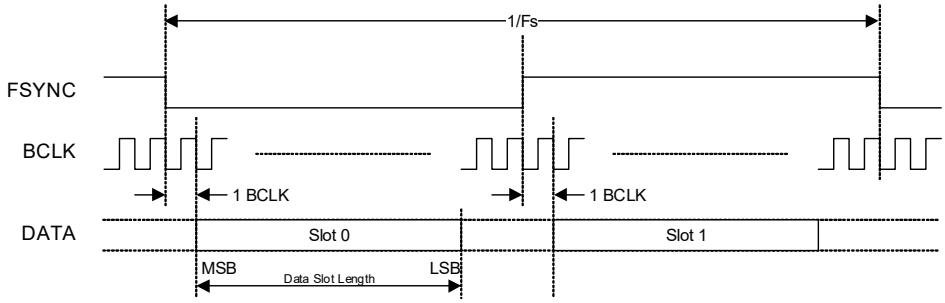


Figure 4-7. I²S Data Format

- In Left-Justified Mode, the MSB is valid on the first BCLK rising edge following a FSYNC transition. The other bits up to the LSB are valid on each successive BCLK cycle. Depending on word length, BCLK frequency, and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

  Left-Justified Mode data format is shown in Fig. 4-8.

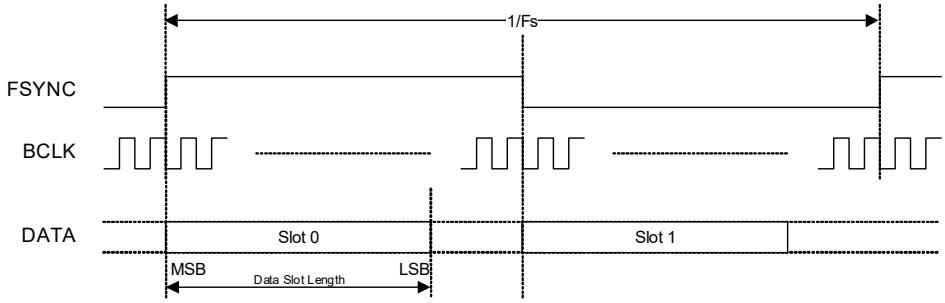


Figure 4-8. Left-Justified Data Format

- In TDM modes, the MSB of the first channel is valid on the second BCLK rising edge following the rising FSYNC edge. Subsequent channels follow immediately after the previous one. Depending on word length, BCLK frequency, and sample rate, there may be unused BCLK cycles between the LSB of the last channel data and the start of the next FSYNC frame.

  In Primary Mode, the FSYNC output resembles the frame pulse shown in Fig. 4-9. In Secondary Mode, the FSYNC pulse duration can be anything less than 1/Fs, provided the falling edge of the frame pulse occurs at least one BCLK period before the rising edge of the next frame pulse.

  TDM Mode data format is shown in Fig. 4-9.

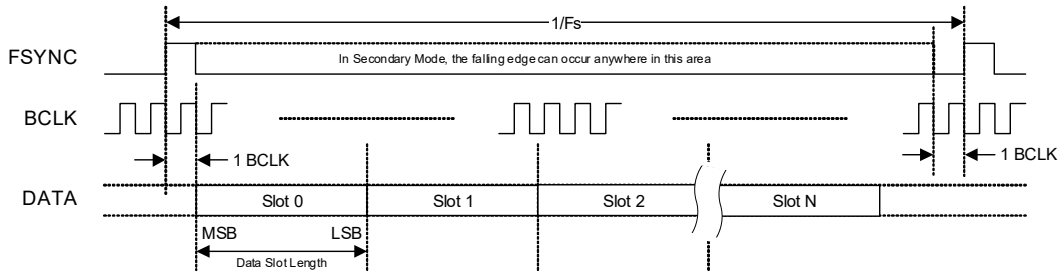


Figure 4-9. TDM Data Format

4.7.3 ASP Configuration

In hardware control mode, the ASP data format is determined by the CONFIG1 and CONFIG2 pins (see Section 4.2).

In software control mode, the ASP data format is configured using SAMPLE_RATE and ASP_FORMAT. If ASP Primary Mode is selected (see Section 4.7.1), the BCLK frequency is configured using ASP_BCLK_FREQ.

In software control mode, the BCLK polarity is selected using ASP_BCLK_INV. The polarity selection is valid in primary and secondary modes, and determines whether the data is valid for sampling on the rising edge or the falling edge.

The BCLK polarity is illustrated in Fig. 4-10 and Fig. 4-11. Note that, in hardware control mode, the BCLK polarity is assumed to be noninverted.

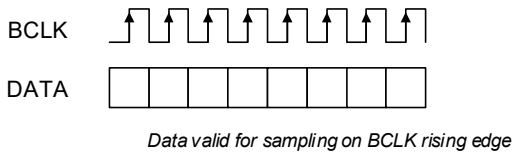


Figure 4-10. Noninverted BCLK

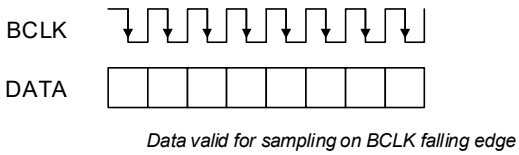


Figure 4-11. Inverted BCLK

In TDM Mode, the two data-format options are supported as follows:

- TDM Mode—minimum time slots. The ASP data format is configured to support the minimum number of time slots necessary for the 4-channel CS4304P output. This mode allows the BCLK rate to be as low as possible, equating to a minimum of 32 BCLK cycles per audio sample.
- TDM Mode—maximum time slots. The ASP data format is configured to support the maximum number of time slots for the applicable BCLK rate. The mode is designed for the maximum BCLK rate (22.5792 MHz for 44.1 kHz-related sample rates, or 24.576 MHz for 48 kHz-related sample rates), enabling the maximum possible bandwidth on the ASP data bus to be shared with other devices.

  Note that, for sample rates >96 kHz, the TDM data format is the same regardless of the minimum/maximum time-slot option.

The ASP configuration depends on the sample rate and the selected data format as described in Table 4-14. The output data is provided on one or more ASP_DINx pins, depending on the selected data format.

Table 4-14. ASP Data Format

ASP Format [1]	ASP Sample Rate [2,3]	DIN pins used	Time slots per frame [4]	BCLK [5,6]
I²S, Left-Justified	32 kHz	2	2	BCLK ≥ 64 fs [7]
	44.1 kHz, 48 kHz	2	2	BCLK ≥ 64 fs
	88.2 kHz, 96 kHz	2	2	BCLK ≥ 64 fs
	176.4 kHz, 192 kHz	2	2	BCLK ≥ 64 fs
	352.8 kHz, 384 kHz	2	2	BCLK = 64 fs
	705.6 kHz, 768 kHz	—	—	—
	Autodetect (32 kHz–192 kHz)	2	2	BCLK ≥ 64 fs
TDM—minimum time slots	32 kHz	1	4	BCLK ≥ 128 fs [7]
	44.1 kHz, 48 kHz	1	4	BCLK ≥ 128 fs
	88.2 kHz, 96 kHz	1	4	BCLK ≥ 128 fs
	176.4 kHz, 192 kHz	1	4	BCLK = 128 fs
	352.8 kHz, 384 kHz	2	2	BCLK = 64 fs
	705.6 kHz, 768 kHz	4	1	BCLK = 32 fs
	Autodetect (32 kHz–192 kHz)	1	4	BCLK ≥ 128 fs
TDM—maximum time slots	32 kHz	1	16	BCLK ≥ 512 fs [7]
	44.1 kHz, 48 kHz	1	16	BCLK = 512 fs
	88.2 kHz, 96 kHz	1	8	BCLK = 256 fs
	176.4 kHz, 192 kHz	1	4	BCLK = 128 fs
	352.8 kHz, 384 kHz	2	2	BCLK = 64 fs
	705.6 kHz, 768 kHz	4	1	BCLK = 32 fs
	Autodetect (32 kHz–192 kHz)	1	4	BCLK ≥ 128 fs

1. The ASP format is selected using the CONFIG2 pin (in hardware control mode) or ASP_FORMAT (in software control mode).
2. The sample rate is selected using the CONFIG1 pin (in hardware control mode) or SAMPLE_RATE (in software control mode).
3. Sample rates 32 kHz–768 kHz supported in software control mode, 32 kHz–192 kHz in hardware control mode.
4. Time slots per frame is the number of data-sample time slots supported on each of the active DIN pins.
5. The BCLK rate must be a constant integer multiple of the sample rate (fs).
6. In ASP primary mode (hardware control), the BCLK frequency is the minimum specified rate. In ASP primary mode (software control), the BCLK frequency is configured using ASP_BCLK_FREQ.
7. In ASP primary mode, the specified minimum BCLK frequency for 32 kHz sample rate is not supported. The available options correspond to 96 fs, 192 fs, 384 fs, or 768 fs.

The ASP data format in I²S, Left-Justified, and TDM interface modes as illustrated in Fig. 4-12 through Fig. 4-16. Refer to Table 4-14 for the applicable definition.

- If I²S data format is selected, the ASP supports audio channels 1–4 as shown in Fig. 4-12. The minimum BCLK rate is 64 fs (where fs is the sample rate). A higher BCLK frequency can be used, resulting in unused BCLK cycles between the LSB of one sample and the MSB of the next.

  Note that the input data is provided on ASP_DIN1 and ASP_DIN2; the ASP_DIN3 and ASP_DIN4 pins are not used.

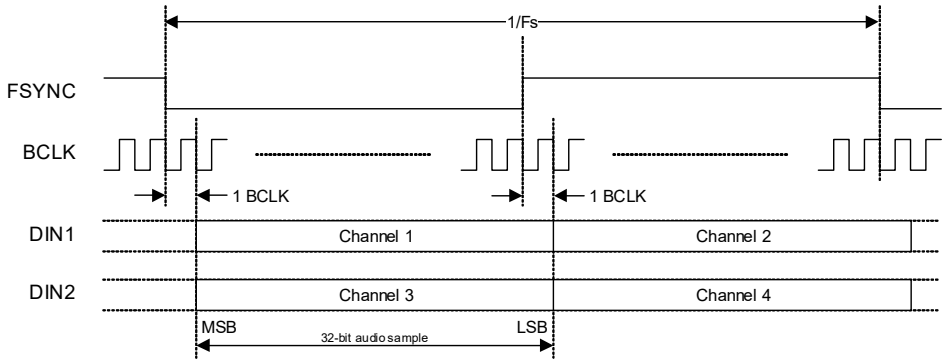


Figure 4-12. I²S Data Format

- If Left-Justified data format is selected, the ASP supports audio channels 1–4 as shown in Fig. 4-13. The minimum BCLK rate is 64 fs (where fs is the sample rate). A higher BCLK frequency can be used, resulting in unused BCLK cycles between the LSB of one sample and the MSB of the next.

  Note that the input data is provided on ASP_DIN1 and ASP_DIN2; the ASP_DIN3 and ASP_DIN4 pins are not used.

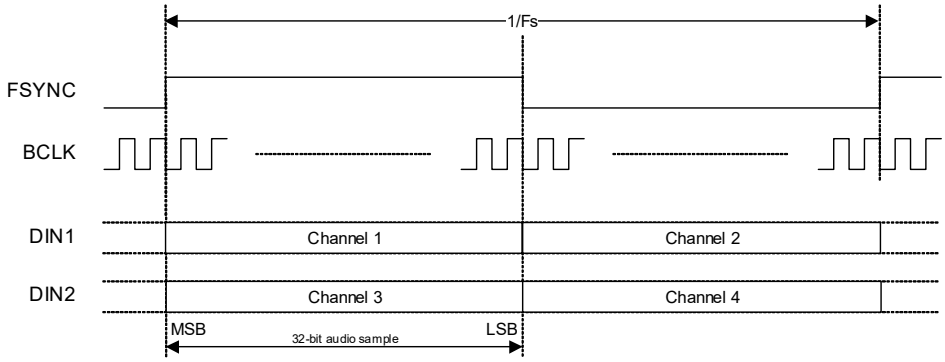


Figure 4-13. Left-Justified Data Format

- In TDM Mode, the FSYNC frame is configured for 1, 2, 4, 8, or 16 slots as specified in Table 4-14.

  In 8- and 16-slot modes, the slot assignment for audio channels 1–4 is selected using the CONFIG3 pin (in hardware control mode—see Section 4.2) or else using ASP_TDM_SLOT (in software control mode). In 1-, 2-, and 4-slot modes, the default slot assignment (slots 0–3) should be selected.

  The BCLK rate is related to the sample rate (fs) as described in Table 4-14. Where applicable, the BCLK rate can be higher than the stated minimum, resulting in additional unused BCLK cycles between the last slot in the frame and the start of the next frame.

  In 4-, 8-, and 16-slot modes, the input data is provided on ASP_DIN1; the ASP_DIN2, ASP_DIN3, and ASP_DIN4 pins are not used.

  The 8-slot TDM format is shown in Fig. 4-14. In the example shown, audio channels 1–4 occupy TDM slots 0–3 respectively.

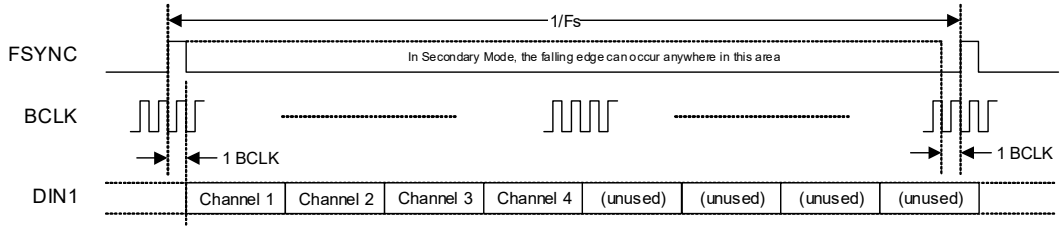


Figure 4-14. TDM Data Format—1 x DIN

In 2-slot mode, the input data is provided on ASP_DIN1 and ASP_DIN2. Note the 2-slot format is used to support 352.8 kHz and 384 kHz sample rates only.

The 2-slot TDM format is shown in Fig. 4-15.

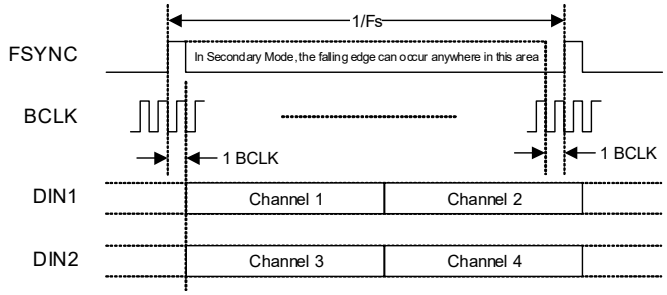


Figure 4-15. TDM Data Format—2 x DIN

In 1-slot mode, the input data is provided on ASP_DIN1, ASP_DIN2, ASP_DIN3, and ASP_DIN4. Note the 1-slot format is used to support 705.6 kHz and 768 kHz sample rates only.

The 1-slot TDM format is shown in Fig. 4-16.

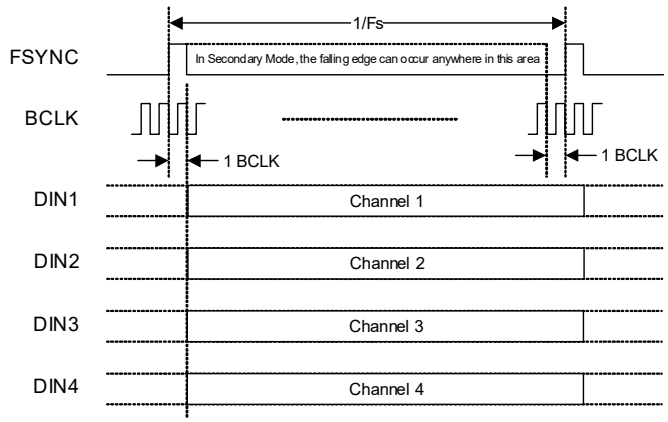


Figure 4-16. TDM Data Format—4 x DIN

4.7.4 Output Channel Summing

The DAC signal paths can be combined as described in Section 4.5.3; this can be used to achieve enhanced performance on the respective paths. If the DAC paths are combined, the ASP data format is redefined as a 2- or 1-channel output.

If the output channels are combined in groups of two, the CS4304P supports a 2-channel input. The ASP configuration depends on the sample rate and the selected data format as described in Table 4-15. The input data is provided on ASP_DIN1 in most cases; the ASP_DIN2 pin is used for 705.6 kHz/768 kHz operation only.

Table 4-15. ASP Data Format—2-channel

ASP Format [1]	ASP Sample Rate [2]	DIN pins used	Time slots per frame [3]	BCLK [4,5]
I²S, Left-Justified	32 kHz	1	2	BCLK ≥ 64 fs [6]
	44.1 kHz, 48 kHz	1	2	BCLK ≥ 64 fs
	88.2 kHz, 96 kHz	1	2	BCLK ≥ 64 fs
	176.4 kHz, 192 kHz	1	2	BCLK ≥ 64 fs
	352.8 kHz, 384 kHz	1	2	BCLK = 64 fs
	705.6 kHz, 768 kHz	—	—	—
	Autodetect (32 kHz–192 kHz)	1	2	BCLK ≥ 64 fs
TDM—minimum time slots	32 kHz	1	2	BCLK ≥ 64 fs [6]
	44.1 kHz, 48 kHz	1	2	BCLK ≥ 64 fs
	88.2 kHz, 96 kHz	1	2	BCLK ≥ 64 fs
	176.4 kHz, 192 kHz	1	2	BCLK ≥ 64 fs
	352.8 kHz, 384 kHz	1	2	BCLK = 64 fs
	705.6 kHz, 768 kHz	2	1	BCLK = 32 fs
	Autodetect (32 kHz–192 kHz)	1	2	BCLK ≥ 64 fs
TDM—maximum time slots	32 kHz	1	16	BCLK ≥ 512 fs [6]
	44.1 kHz, 48 kHz	1	16	BCLK = 512 fs
	88.2 kHz, 96 kHz	1	8	BCLK = 256 fs
	176.4 kHz, 192 kHz	1	4	BCLK = 128 fs
	352.8 kHz, 384 kHz	1	2	BCLK = 64 fs
	705.6 kHz, 768 kHz	2	1	BCLK = 32 fs
	Autodetect (32 kHz–192 kHz)	1	4	BCLK ≥ 128 fs

1. The ASP format is selected using ASP_FORMAT.
2. The sample rate is selected using SAMPLE_RATE.
3. Time slots per frame is the number of data-sample time slots supported on each of the active DIN pins.
4. The BCLK rate must be a constant integer multiple of the sample rate (fs).
5. fs = sample rate. In ASP primary mode, the BCLK frequency is configured using ASP_BCLK_FREQ.

6. In ASP primary mode, the specified minimum BCLK frequency for 32 kHz sample rate is not supported. The available options correspond to 96 fs, 192 fs, 384 fs, or 768 fs.

The 2-channel ASP format is illustrated in Fig. 4-17 through Fig. 4-20.

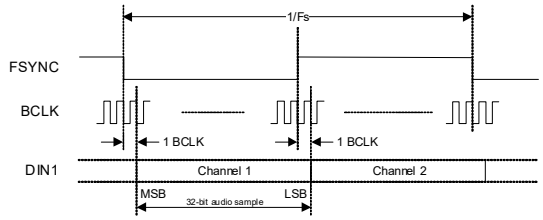


Figure 4-17. I2S Data Format

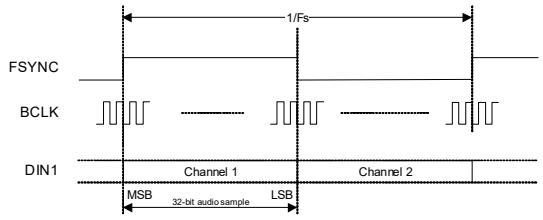


Figure 4-18. Left-Justified Data Format

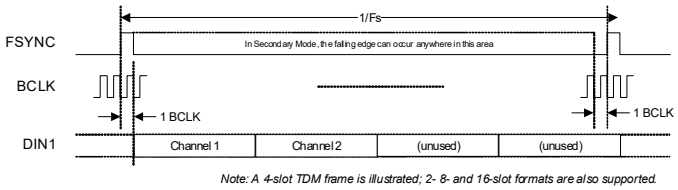


Figure 4-19. TDM Data Format—1 x DIN

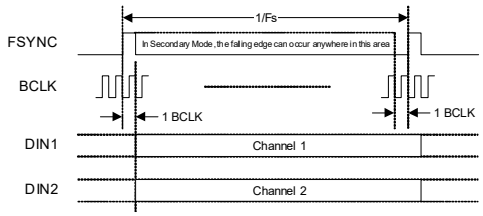


Figure 4-20. TDM Data Format—2 x DIN

If the output channels are combined in a group of four, the CS4304P supports a 1-channel input. The ASP configuration depends on the sample rate and the selected data format as described in Table 4-16. The input data is provided on ASP_DIN1; the ASP_DIN2, ASP_DIN3 and ASP_DIN4 pins are not used.

Table 4-16. ASP Data Format—1-channel

ASP Format [1]	ASP Sample Rate [2]	DIN pins used	Time slots per frame [3]	BCLK [4,5]
I2S, Left-Justified	32 kHz	1	2	BCLK ≥ 64 fs [6]
	44.1 kHz, 48 kHz	1	2	BCLK ≥ 64 fs
	88.2 kHz, 96 kHz	1	2	BCLK ≥ 64 fs
	176.4 kHz, 192 kHz	1	2	BCLK ≥ 64 fs
	352.8 kHz, 384 kHz	1	2	BCLK = 64 fs
	705.6 kHz, 768 kHz	—	—	—
	Autodetect (32 kHz–192 kHz)	1	2	BCLK ≥ 64 fs
TDM—minimum time slots	32 kHz	1	1	BCLK ≥ 64 fs [6]
	44.1 kHz, 48 kHz	1	1	BCLK ≥ 64 fs
	88.2 kHz, 96 kHz	1	1	BCLK ≥ 32 fs
	176.4 kHz, 192 kHz	1	1	BCLK ≥ 32 fs
	352.8 kHz, 384 kHz	1	1	BCLK ≥ 32 fs
	705.6 kHz, 768 kHz	1	1	BCLK = 32 fs
	Autodetect (32 kHz–192 kHz)	1	1	BCLK ≥ 64 fs
TDM—maximum time slots	32 kHz	1	16	BCLK ≥ 512 fs [6]
	44.1 kHz, 48 kHz	1	16	BCLK = 512 fs
	88.2 kHz, 96 kHz	1	8	BCLK = 256 fs
	176.4 kHz, 192 kHz	1	4	BCLK = 128 fs
	352.8 kHz, 384 kHz	1	2	BCLK = 64 fs
	705.6 kHz, 768 kHz	1	1	BCLK = 32 fs
	Autodetect (32 kHz–192 kHz)	1	4	BCLK ≥ 128 fs

1. The ASP format is selected using ASP_FORMAT (in software control mode).
2. The sample rate is selected using SAMPLE_RATE (in software control mode).
3. Time slots per frame is the number of data-sample time slots supported on each of the active DIN pins.
4. The BCLK rate must be a constant integer multiple of the sample rate (fs).
5. fs = sample rate. In ASP primary mode, the BCLK frequency is configured using ASP_BCLK_FREQ.
6. In ASP primary mode, the specified minimum BCLK frequency for 32 kHz sample rate is not supported. The available options correspond to 96 fs, 192 fs, 384 fs, or 768 fs.

The 1-channel ASP format is illustrated in Fig. 4-21 through Fig. 4-23.

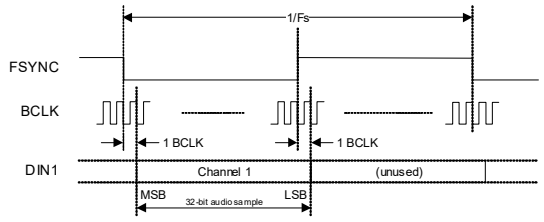


Figure 4-21. I2S Data Format

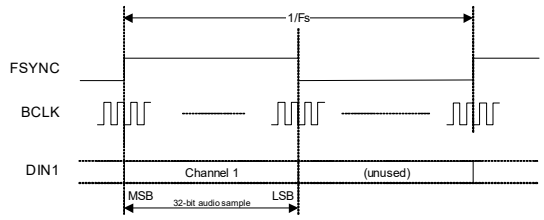


Figure 4-22. Left-Justified Data Format

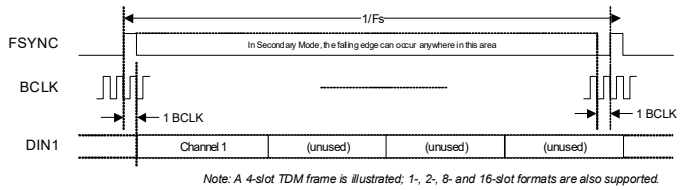


Figure 4-23. TDM Data Format

4.7.5 ASP Channel Reverse Order

The CS4304P supports an option to reverse the ASP channel order. If the reverse channel order is selected, the ASP data format is reconfigured to map the input channels in the opposite order to the default order shown in Section 4.7.3 and Section 4.7.4.

The reverse channel-order option can be used to ease PCB layout constraints, enabling the ASP data ordering to be aligned with the external pin connections, regardless of the orientation of the device on the PCB.

The reverse channel order is illustrated in Fig. 4-24 and Fig. 4-25. The I²S data format is shown as an example; the equivalent channel substitutions are supported in left-justified and TDM format also.

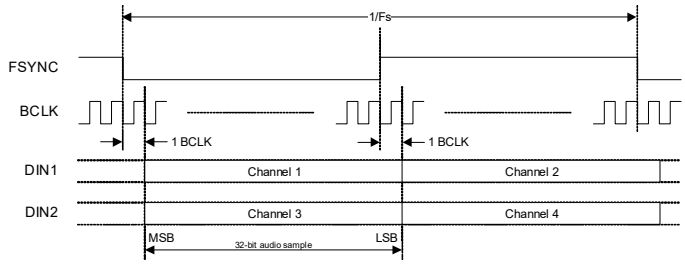


Figure 4-24. Default Channel Order

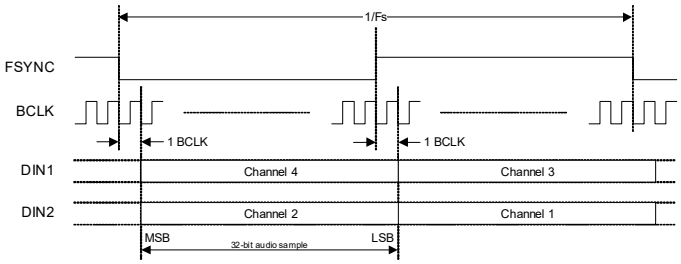


Figure 4-25. Reverse Channel Order

In hardware control mode, the ASP channel order is selected using the CONFIG4 hardware control pin, as described in Section 4.2. In software (I²C/SPI) control mode, the ASP channel order is selected using ASP_CH_REVERSE.

4.8 DSD Interface

Direct Stream Digital (DSD) is a high-resolution audio-coding standard that employs 1-bit sampling at high oversample rates. The DSD interface uses noise shaping and other filters to decode the data for the purposes of analog audio playback. The CS4304P supports a four-channel DSD interface.

The DSD interface supports digital input at oversample rates up to 512×fs. Phase modulation of the digital input is also supported at 64×fs oversample rate. A selectable high-pass filter is provided in the DSD signal path.

The DSD clock input (DSD_CLK) can be used as the system-clock reference for the CS4304P. See Section 4.4 for further details.

Note the DSD interface is supported in software control mode only.

4.8.1 DSD Enable

The DSD interface is enabled using DSD_EN. Note that the ASP interface (see Section 4.7) is disabled if the DSD interface is enabled.

The DSD interface supports four-channel input using the respective DSD_DINx data pins. The timing of the DSD data is supported using the DSD_CLK clock input. The DSD interface connections are illustrated in Fig. 4-26.

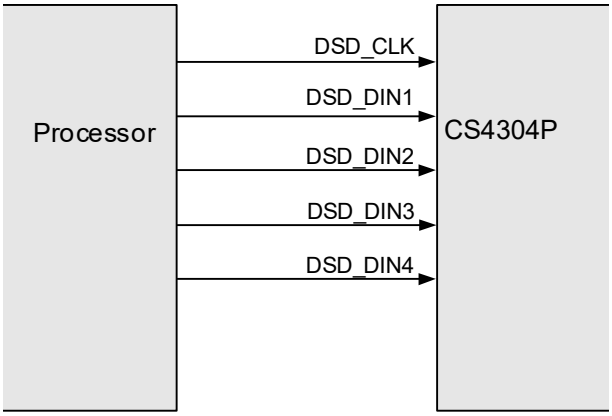


Figure 4-26. DSD Interface Connection

4.8.2 DSD Format

The DSD interface format is shown in Fig. 4-27. In this default configuration, a new data bit is received on each falling CLK edge, for sampling at the next rising edge. See Table 3-12 for timing specifications.

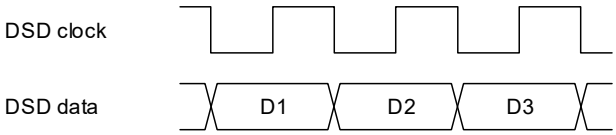


Figure 4-27. DSD Interface Timing

The oversample rate is configured using DSD_OSR. This field must be configured to match the DSD input stream. Oversample rates 64×fs, 128×fs, 256×fs, and 512×fs rates are supported (where fs = 44.1 kHz).

The CS4304P supports DSD phase modulation, where the DSD data is represented in *data plus data-inverted* format as shown in Fig. 4-28. Phase modulation is configured by setting DSD_PM_EN. Note that phase modulation supported for 64×fs data rate only.

If phase modulation is enabled, the DSD clock rate is configured using DSD_PM_SEL. By default, the clock rate is 128×fs (i.e., 2 x OSR rate). The clock rate can be adjusted to 64×fs if required.

The phase-modulation data formats are shown in Fig. 4-28 and Fig. 4-29.

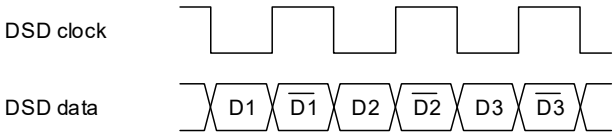


Figure 4-28. DSD Phase Modulation—64fs CLK

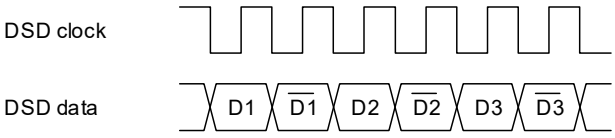


Figure 4-29. DSD Phase Modulation—128fs CLK

4.8.3 Signal Level Control

The scaling of the DSD signal level, relative to the full-scale level of the CS4304P DAC output path, is configurable using DSD_ZERODB. The scaling is defined with reference to the SACD standard for DSD signal levels.

4.8.4 High-Pass Filter

A high-pass filter is incorporated in the DSD signal path. The filter is selected using DSD_HPF_EN. The filter is enabled by default.

Note the digital filters described in Section 4.6 are not supported on the DSD path.

4.9 I²C/SPI Control Port

The CS4304P incorporates a control port, supporting I²C or SPI modes of operation. In software control mode, the CS4304P is configured by writing to control registers using the control port.

The control port is automatically configured in I²C mode or SPI mode following the first valid I²C/SPI activity detected after power-on or hardware reset.

4.9.1 I²C Control Port

The I²C control port is supported using the I2C_SCL and I2C_SDA pins.

The CS4304P is a target device on the I²C bus—SCL is a clock input, while SDA is a bidirectional data pin. To allow arbitration of multiple targets (and/or multiple controllers) on the same interface, the CS4304P transmits Logic 1 by tristating the SDA pin, rather than pulling it high. An external pull-up resistor is required to pull the SDA line high so that the Logic 1 can be recognized by the controller.

In order to allow many devices to share a single two-wire control bus, every device on the bus has a unique 8-bit device address (this is not the same as the address of each register in the CS4304P). Note that the LSB of the device address is the read/write bit; this bit is set to Logic 1 for read and Logic 0 for write.

The I²C device address is configured using the CONFIG5 pin as described in Table 4-17.

Table 4-17. I2C Address Selection—CONFIG5 pin

Pin Configuration		I2C Address
Pull-up to VDD_A	0 Ω	0x6E (write), 0x6F (read)
	4.7 kΩ	0x6C (write), 0x6D (read)
	22 kΩ	0x6A (write), 0x6B (read)
	100 kΩ	0x68 (write), 0x69 (read)
Pull-down to GND_A	100 kΩ	0x66 (write), 0x67 (read)
	22 kΩ	0x64 (write), 0x65 (read)
	4.7 kΩ	0x62 (write), 0x63 (read)
	0 Ω	0x60 (write), 0x61 (read)

The host device indicates the start of data transfer with a high-to-low transition on SDA while SCL remains high. This indicates that a device address and subsequent address/data bytes follow. The CS4304P responds to the start condition and shifts in the next 8 bits on SDA (8-bit device address, including read/write bit, MSB first). If the device address received matches the device address of the CS4304P, the CS4304P responds by pulling SDA low on the next clock pulse (ACK). If the device address is not recognized or the R/W bit is set incorrectly, the CS4304P returns to the idle condition and waits for a new start condition.

If the device address matches the device address of the CS4304P, the data transfer continues. The controller indicates the end of data transfer with a low-to-high transition on SDA while SCL remains high. After receiving a complete address and data sequence the CS4304P returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e., SDA changes while SCL is high), the device returns to the idle condition.

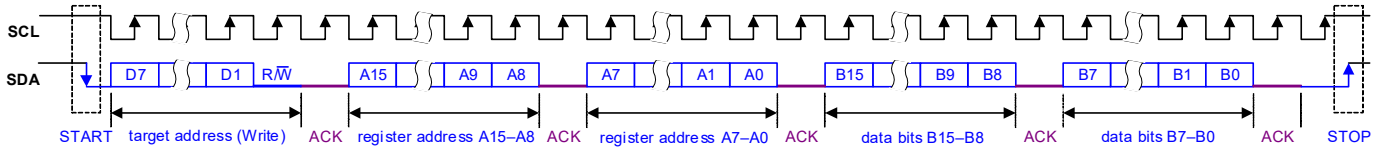
The I²C interface uses a 16-bit register address and 16-bit data words. The register address must be aligned to a 16-bit word boundary (i.e., the LSB must be 0). Note that the full I²C message protocol also includes a device address, a read/write bit, and other signaling bits (see Fig. 4-30 and Fig. 4-31).

The CS4304P supports the following read and write operations:

- Single write
- Single read
- Multiple write
- Multiple read

Continuous (multiple) read and write modes allow register operations to be scheduled faster than is possible with single register operations. In these modes, the CS4304P automatically increments the register address after each data word. Successive data words can be input/output every two data bytes.

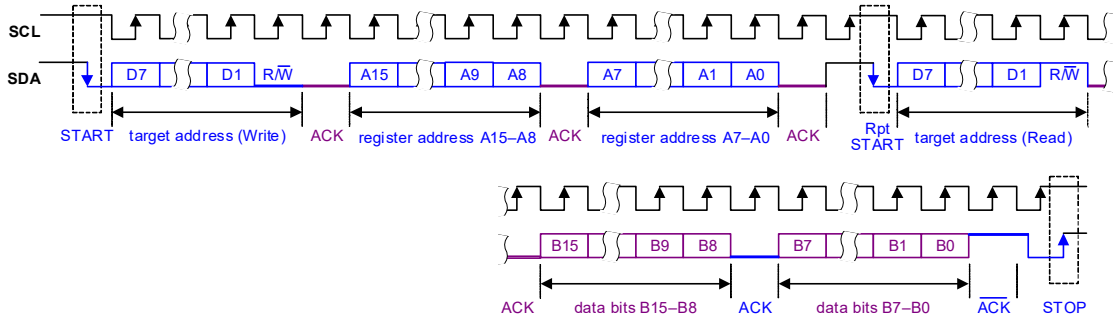
The I²C protocol for a single, 16-bit register write operation is shown in Fig. 4-30.



Note: The SDA pin is used as input for the control register address and data; SDA is pulled low by the receiving device to provide the acknowledge (ACK) response

Figure 4-30. Control Interface I²C Register Write

The I²C protocol for a single, 16-bit register read operation is shown in Fig. 4-31.



Note: The SDA pin is driven by both the controller and target devices in turn to transfer target address, register address, data and ACK responses

Figure 4-31. Control Interface I²C Register Read

The control interface also supports other register operations; the interface protocol for these operations is shown in Fig. 4-32 through Fig. 4-35. The terminology used in the following figures is detailed in Table 4-18.

Table 4-18. Control Interface (I2C) Terminology

Terminology	Description
S	Start condition
Sr	Repeated start
A	Acknowledge (SDA low)
$\overline{A}$	No Acknowledge (SDA high)
P	Stop condition
R/$\overline{W}$	Read/not Write: 0 = Write, 1 = Read
[White field]	Data flow from bus controller to CS4304P
[Gray field]	Data from CS4304P to bus controller

Fig. 4-32 shows a single register write to a specified address.

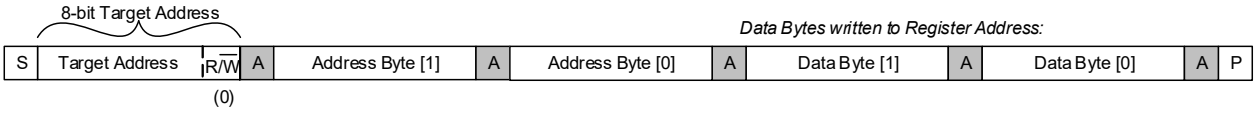


Figure 4-32. Single-Register Write to Specified Address

Fig. 4-33 shows a single register read from a specified address.

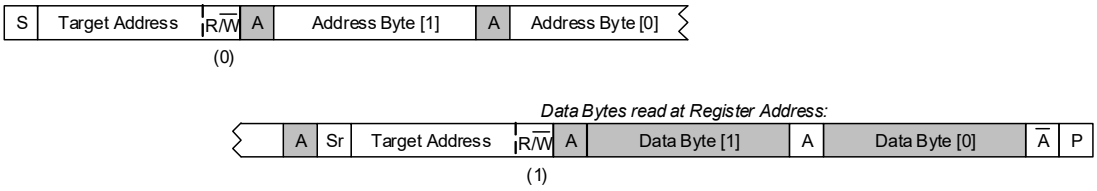


Figure 4-33. Single-Register Read from Specified Address

Fig. 4-34 shows a multiple register write to a specified address.

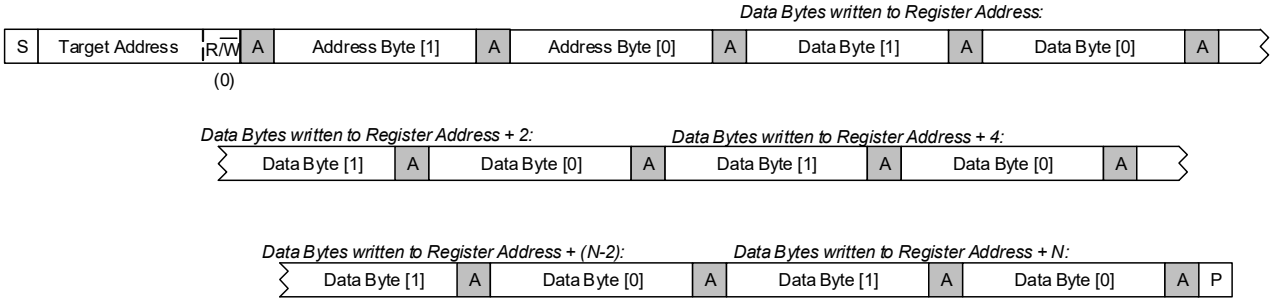


Figure 4-34. Multiple-Register Write to Specified Address

Fig. 4-35 shows a multiple register read from a specified address.

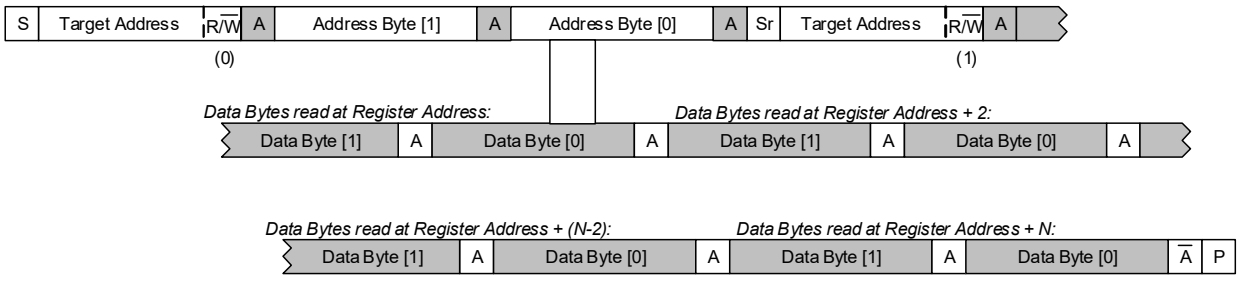


Figure 4-35. Multiple-Register Read from Specified Address

4.9.2 SPI Interface

The SPI interface is supported using the $\overline{\text{SPI\_CS}}$, SPI_SCK, SPI_SDI, and SPI_SDO pins.

The SDI (data-input) pin supports the following behavior:

- In write operations (R/$\overline{W}$ = 0), the SDI pin input is driven by the controlling device.
- In read operations (R/$\overline{W}$ = 1), the SDI pin is ignored following receipt of the valid register address.

The SDO (data-output) pin supports the following behavior:

- If $\overline{CS}$ is asserted (Logic 0), the SDO output is actively driven when outputting data and is high impedance at other times. If $\overline{CS}$ is not asserted, the SDO output is high impedance.
- The high-impedance state of the SDO output allows the pin to be shared with other peripheral devices.
- The output (SDO) data bit is available to the host device at the rising edge of SCK. See Table 3-14 for timing information.

The SPI interface uses a 15-bit register address and 16-bit data words. Note that the full SPI message protocol also includes a read/write bit and a 16-bit padding phase (see Fig. 4-36 and Fig. 4-37).

Continuous read and write modes enable multiple register operations to be scheduled faster than is possible with single register operations. In these modes, the CS4304P automatically increments the register address at the end of each data word, for as long as $\overline{SS}$ is held low and SCK is toggled. Successive data words can be input/output every 16 clock cycles.

The SPI protocol is shown in Fig. 4-36 and Fig. 4-37.

Fig. 4-36 shows a single register write to a specified address.

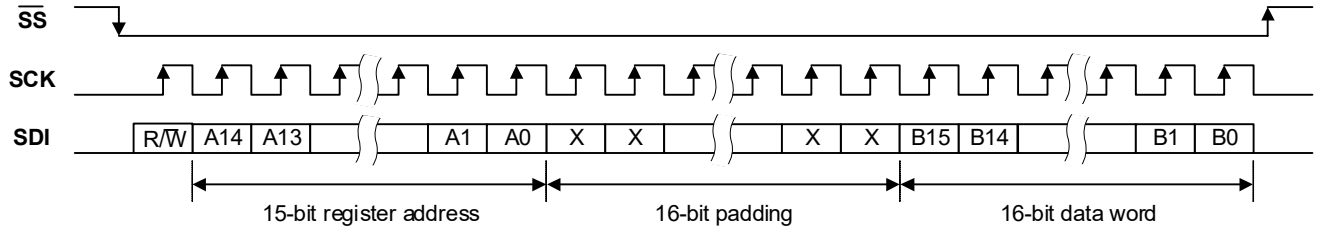


Figure 4-36. Control Interface SPI Register Write

Fig. 4-37 shows a single register read from a specified address.

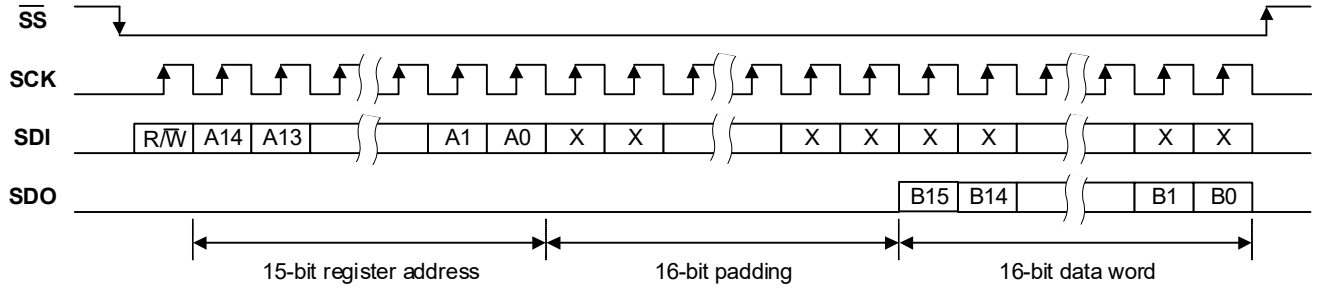


Figure 4-37. Control Interface SPI Register Read

Fig. 4-38 shows a multiple register write to a specified address.

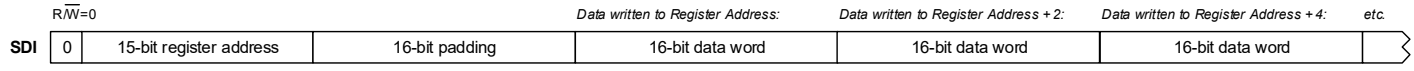


Figure 4-38. Multiple-Register Write to Specified Address

Fig. 4-39 shows a multiple register read from a specified address.

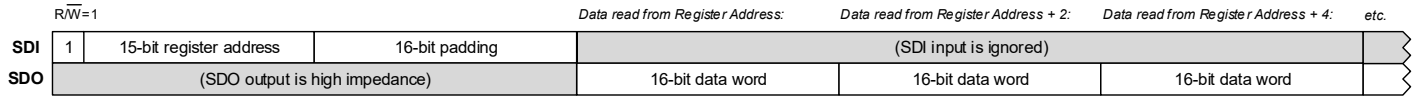


Figure 4-39. Multiple-Register Read from Specified Address

4.10 General-Purpose Output

The CS4304P supports general-purpose outputs on selected digital I/O pins. General-purpose (GP) outputs can be used to provide hardware control signals to other devices.

The general-purpose outputs are multiplexed with other pin functions (e.g., I²C/SPI control port, or the audio serial port). Note that care must be taken not to configure a pin for GP output if the shared pin function is required.

Each pin is configured for GP output by setting the respective _FN bit as noted in Table 4-19. If a pin is configured for GP output, the logic output level is selected using the respective _LVL bit.

Table 4-19. General Purpose Output

Pin Name	Power Supply [1]	Pin Function Select	Output Level Select	Notes
CONFIG5	VDD_A	CONFIG5_FN	CONFIG5_LVL	GP output is not supported if the I2C control port (see Section 4.9.1) is used.
CONFIG4	VDD_A	CONFIG4_FN	CONFIG4_LVL	
CONFIG3	VDD_IO	CONFIG3_FN	CONFIG3_LVL	
CONFIG2	VDD_IO	CONFIG2_FN	CONFIG2_LVL	
SPI_SCK	VDD_IO	SPI_SCK_FN	SPI_SCK_LVL	GP output is not supported if the SPI control port (see Section 4.9.2) is used.
SPI_CS	VDD_IO	SPI_CS_FN	SPI_CS_LVL	
ASP_DIN4	VDD_IO	ASP_DIN4_FN	ASP_DIN4_LVL	Refer to Section 4.7 to determine which pins are required for ASP output, depending on the applicable data format. Unused pins can be configured for GP output.
ASP_DIN3	VDD_IO	ASP_DIN3_FN	ASP_DIN3_LVL	
ASP_DIN2	VDD_IO	ASP_DIN2_FN	ASP_DIN2_LVL	

1. The digital I/O logic levels for each pin are defined with respect to the applicable power supply. See Table 3-8 for details.

4.11 Device ID

The device ID, and other associated data, can be read from the control fields listed in Table 4-20.

Table 4-20. Device ID

Label	Description
DEVID	Device ID
AREVID	All-layer device revision
MTLREVID	Metal-layer device revision

5 Register Quick Reference

This section gives an overview of the control port registers. Refer to the following bit definition tables for bit assignment information.

This register view is for the CS4304P.

- The register field default values are established upon the deassertion of the $\overline{\text{RESET}}$ pin or following soft reset.
- A "—" represents a reserved field/access type.
- The reserved field values must not be modified.
- The registers are 16 bits wide, and only word transactions are allowed.
- All visible fields are read/write except where indicated with the following shading:

Read/write access Read-only access Write-only access

Table 5-1. Block Base Addresses

Base Address	Block Name	Register Quick Reference	Register Description Reference
0x0000 0000	**DEVID**	Section 5.1	Section 6.1
0x0000 0040	**CONFIG**	Section 5.2	Section 6.2
0x0000 00C0	**OUTPUT_PATH**	Section 5.3	Section 6.3
0x0000 3D00	**PIN_CONFIG**	Section 5.4	Section 6.4

5.1 DEVID

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 0000	DEVID	DEVID															
p. 43		0	1	0	0	0	0	1	1	0	0	0	0	0	1	0	0
0x0000 0004	REVID	—								AREVID				MTLREVID			
p. 43		0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0
0x0000 0022	SW_RESET	SW_RESET								—							
p. 43		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

5.2 CONFIG

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 0040	CLK_CFG_0	—			SYSCLK_SRC	—						PLL_REFCLK_FREQ		—			PLL_REFCLK_SRC
p. 44		0	0	0	1	0	0	0	0	0	0	1	1	0	0	0	0
0x0000 0042	CLK_CFG_1	—													SAMPLE_RATE		
p. 44		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0x0000 0044	CHIP_ENABLE	—															GLOBAL_EN
p. 44		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0048	ASP_CFG	—									ASP_BCLK_INV	ASP_PRIMARY		—			ASP_BCLK_FREQ
p. 45		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0050	SIGNAL_PATH_CFG	—						ASP_CH_REVERSE	—			ASP_TDM_SLOT			ASP_FORMAT		
p. 45		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

5.3 OUTPUT_PATH

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 00C0	OUT_ENABLES	—												OUT4_DAC_EN	OUT3_DAC_EN	OUT2_DAC_EN	OUT1_DAC_EN
p. 46		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00C2	OUT_RAMP_SUM	OUT_SUM_MODE			—						OUT_RAMP_RATE_DEC			—	OUT_RAMP_RATE_INC		
p. 46		0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0
0x0000 00C4	OUT_DEEMPH	—														OUT_DEEMPH_FILT_SEL	OUT_DEEMPH_EN
p. 46		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00C6	OUT_FILTER	—			OUT_HPF_EN	—	OUT_FILTER_SEL			—							
p. 47		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00CA	OUT_INV	—												OUT4_INV	OUT3_INV	OUT2_INV	OUT1_INV
p. 47		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00D0	OUT_VOL_CTRL1_0	OUT1_MUTE	—							OUT1_VOL							
p. 48		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00D2	OUT_VOL_CTRL1_1	OUT2_MUTE	—							OUT2_VOL							
p. 48		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00D4	OUT_VOL_CTRL2_0	OUT3_MUTE	—							OUT3_VOL							
p. 48		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00D6	OUT_VOL_CTRL2_1	OUT4_MUTE	—							OUT4_VOL							
p. 48		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00E0	OUT_VOL_CTRL5	—															OUT_VU
p. 49		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00E4	SHUTDOWN_CTRL	—															DAC_REF_DISABLE
p. 49		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00E6	STARTUP_DELAY	—												STARTUP_DELAY_EN	STARTUP_DELAY_TIME		
p. 49		0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
0x0000 00E8	DSD_CTRL	—									DSD_PM_SEL	DSD_PM_EN	DSD_ZERODB	DSD_OSR			DSD_EN
p. 49		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00EC	DSD_FILT	—											DSD_HPF_EN	—			
p. 50		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

5.4 PIN_CONFIG

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 3D24	PAD_FN	—						CONFIG5_FN	CONFIG4_FN	CONFIG3_FN	CONFIG2_FN	SPI_SCK_FN	SPI_CS_FN	ASP_DIN4_FN	ASP_DIN3_FN	ASP_DIN2_FN	—
p. 50		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 3D28	PAD_LVL	—						CONFIG5_LVL	CONFIG4_LVL	CONFIG3_LVL	CONFIG2_LVL	SPI_SCK_LVL	SPI_CS_LVL	ASP_DIN4_LVL	ASP_DIN3_LVL	ASP_DIN2_LVL	—
p. 51		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6 Register Descriptions

This section describes each of the control port registers.

This register view is for the CS4304P.

- The register field default values are established upon the deassertion of the $\overline{\text{RESET}}$ pin or following soft reset.
- A "—" represents a reserved field/access type.
- The reserved field values must not be modified.
- The registers are 16 bits wide, and only word transactions are allowed.
- All visible fields are read/write except where indicated with the following shading:

Read/write access Read-only access Write-only access

6.1 DEVID

6.1.1 DEVID

Address: 0x0000 0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO	DEVID															
Default	0	1	0	0	0	0	1	1	0	0	0	0	0	1	0	0

Bits	Name	Description
15:0	DEVID	This register indicates the Device ID CS4304P. 0x0000–0x4303 = Reserved 0x4304 = CS4304P 0x4305–0xFFFF = Reserved

6.1.2 REVID

Address: 0x0000 0004

	15…8	7	6	5	4	3	2	1	0
RO	—	AREVID				MTLREVID			
Default	0x00	1	0	1	0	0	0	0	0

Bits	Name	Description
15:8	—	Reserved
7:4	AREVID	This field indicates the all-layer device revision. 0x0–0x9 = Reserved 0xA = (Default) Revision Ax 0xB–0xF = Reserved
3:0	MTLREVID	This field indicates the metal-layer device revision. 0x0 = (Default) Revision x0 0x1–0xF = Reserved

6.1.3 SW_RESET

Address: 0x0000 0022

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WO	SW_RESET								—							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	SW_RESET	Software Reset. Writing 0x5A triggers a reset. 0x00 = (Default) No action 0x01–0x59 = Reserved 0x5A = Software reset 0x5B–0xFF = Reserved
7:0	—	Reserved

6.2 CONFIG

6.2.1 CLK_CFG_0

Address: 0x0000 0040

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—			SYSCLK_SRC	—						PLL_REFCLK_FREQ		—			PLL_REFCLK_SRC
Default	0	0	0	1	0	0	0	0	0	0	1	1	0	0	0	0

Bits	Name	Description
15:13	—	Reserved
12	SYSCLK_SRC	System clock source. If MCLK is selected, the PLL is bypassed. 0 = MCLK 1 = (Default) PLL
11:6	—	Reserved
5:4	PLL_REFCLK_FREQ	PLL reference clock frequency. The selection must match the frequency of the selected input reference. 00 = 3.072/2.8224 MHz 01 = 6.144/5.6448 MHz 10 = 12.288/11.2896 MHz 11 = (Default) 24.576/22.5792 MHz
3:1	—	Reserved
0	PLL_REFCLK_SRC	PLL reference clock source. Note the BCLK reference is only valid in ASP Secondary Mode. 0 = (Default) BCLK 1 = MCLK

6.2.2 CLK_CFG_1

Address: 0x0000 0042

RW	15…8	7	6	5	4	3	2	1	0
	—	—						SAMPLE_RATE	
Default	0x00	0	0	0	0	0	0	0	1

Bits	Name	Description
15:3	—	Reserved
2:0	SAMPLE_RATE	Audio sample frequency. Note the sample rate must be integer-related to the system clock frequency. Auto-detect is only valid if sample rate = 32-192kHz, clock reference = MCLK, and the ASP is in Secondary Mode. 000 = 32 kHz 001 = (Default) 48/44.1 kHz 010 = 96/88.2 kHz 011 = 192/176.4 kHz 100 = 384/356.8 kHz 101 = 768/705.6 kHz 110 = Auto-detect 111 = Reserved

6.2.3 CHIP_ENABLE

Address: 0x0000 0044

RW	15…8	7	6	5	4	3	2	1	0
	—	—							GLOBAL_EN
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:1	—	Reserved
0	GLOBAL_EN	Global enable. Set to 1 to configure and enable all functions. Clear to 0 to disable. Note the clocking and ASP control registers are only valid on the rising edge of GLOBAL_EN. It is recommended to select the disabled state (GLOBAL_EN=0) before writing to these registers.

6.2.4 ASP_CFG

Address: 0x0000 0048

RW	15…8	7	6	5	4	3	2	1	0
	—	—	ASP_BCLK_INV	ASP_PRIMARY	—			ASP_BCLK_FREQ	
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:7	—	Reserved
6	ASP_BCLK_INV	ASP BCLK polarity. Selects the valid BCLK edge for data sampling. In non-inverted mode, DIN data is valid on BCLK rising edge. In inverted mode, DIN data is valid on BCLK falling edge. 0 = (Default) Non-inverted 1 = Inverted
5	ASP_PRIMARY	ASP Primary/Secondary Mode select. In ASP Primary Mode, BCLK and FSYNC are outputs. In ASP Secondary Mode, BCLK and FSYNC are inputs. 0 = (Default) Secondary Mode 1 = Primary Mode
4:2	—	Reserved
1:0	ASP_BCLK_FREQ	ASP BCLK frequency. The BCLK frequency must be high enough to support the required number of data bits at the selected sample rate. Only valid in ASP Primary Mode. Note the BCLK frequency is integer-related to the system clock frequency i.e., multiples of 3.072 MHz for 12.288 / 24.576 MHz system clock, or multiples of 2.8224 MHz for 11.2896 / 22.5792 MHz system clock. 00 = (Default) 3.072/2.8224 MHz 01 = 6.144/5.6448 MHz 10 = 12.288/11.2896 MHz 11 = 24.576/22.5792 MHz

6.2.5 SIGNAL_PATH_CFG

Address: 0x0000 0050

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—						ASP_CH_REVERSE		—		ASP_TDM_SLOT			ASP_FORMAT		
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:10	—	Reserved
9	ASP_CH_REVERSE	ASP channel-ordering reversal. Selects normal- or reverse-order ASP data format. 0 = (Default) Normal 1 = Reverse
8:6	—	Reserved
5:3	ASP_TDM_SLOT	TDM slot select. Configures which TDM slots are used in TDM maximum-time-slots mode. Note the valid selections vary depending on whether the device is configured in 4-channel mode (default), or in 2-channel summing mode. In 4-channel mode (default), valid selections are 0x0, 0x2, 0x4, or 0x6 only. 000 = (Default) Slots 0-3 (4-ch), Slots 0-1 (2-ch) 001 = Slots 2-3 (2-ch) 010 = Slots 4-7 (4-ch), Slots 4-5 (2-ch) 011 = Slots 6-7 (2-ch) 100 = Slots 8-11 (4-ch), Slots 8-9 (2-ch) 101 = Slots 10-11 (2-ch) 110 = Slots 12-15 (4-ch), Slots 12-13 (2-ch) 111 = Slots 14-15 (2-ch)
2:0	ASP_FORMAT	ASP data format. Selects how the audio samples are arranged within the FSYNC frame. 000 = (Default) I2S Mode 001 = Left-Justified Mode 010–101 = Reserved 110 = TDM Maximum Time Slots Mode 111 = TDM Minimum Time Slots Mode

6.3 OUTPUT_PATH

6.3.1 OUT_ENABLES

Address: 0x0000 00C0

RW	15…8	7	6	5	4	3	2	1	0
	—	—				OUT4_DAC_EN	OUT3_DAC_EN	OUT2_DAC_EN	OUT1_DAC_EN
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:4	—	Reserved
3	OUT4_DAC_EN	Channel 4 output enable. 0 = (Default) Disabled 1 = Enabled
2	OUT3_DAC_EN	Channel 3 output enable. 0 = (Default) Disabled 1 = Enabled
1	OUT2_DAC_EN	Channel 2 output enable. 0 = (Default) Disabled 1 = Enabled
0	OUT1_DAC_EN	Channel 1 output enable. 0 = (Default) Disabled 1 = Enabled

6.3.2 OUT_RAMP_SUM

Address: 0x0000 00C2

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OUT_SUM_MODE				—					OUT_RAMP_RATE_DEC			—	OUT_RAMP_RATE_INC		
Default	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0

Bits	Name	Description
15:13	OUT_SUM_MODE	DAC output summing select. Combines the output paths in groups of two or four channels. The grouped channels must be linked together at the respective inoutputput pins. The grouped paths are configured using the control registers associated with the respective summed channel number (1 to n). 000 = (Default) No summing of channels 001 = Outputs combined in groups of two. DAC1+DAC2, DAC3+DAC4 010 = Outputs combined in groups of four. DAC1+DAC2+DAC3+DAC4 011–111 = Reserved
12:7	—	Reserved
6:4	OUT_RAMP_RATE_DEC	DAC output volume decrease Ramp Rate (ms/6 dB), used for gain changes. This field should not be changed while a volume ramp is in progress. 000 = 0 ms 001 = 0.5 ms 010 = (Default) 1 ms 011 = 2 ms 100 = 4 ms 101 = 8 ms 110 = 15 ms 111 = 30 ms
3	—	Reserved
2:0	OUT_RAMP_RATE_INC	DAC output volume increase Ramp Rate (ms/6 dB), used for gain changes. This field should not be changed while a volume ramp is in progress. 000 = 0 ms 001 = 0.5 ms 010 = (Default) 1 ms 011 = 2 ms 100 = 4 ms 101 = 8 ms 110 = 15 ms 111 = 30 ms

6.3.3 OUT_DEEMPH

Address: 0x0000 00C4

RW	15…8	7	6	5	4	3	2	1	0
	—	—						OUT_DEEMPH_FILT_SEL	OUT_DEEMPH_EN
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:2	—	Reserved

Bits	Name	Description
1	OUT_DEEMPH_FILT_SEL	Deemphasis filter sample-rate selection. 0 = (Default) 44.1 kHz 1 = 48.0 kHz
0	OUT_DEEMPH_EN	Deemphasis filter enable. 0 = (Default) Deemphasis disabled 1 = Deemphasis enabled

6.3.4 OUT_FILTER

Address: 0x0000 00C6

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—			OUT_HPF_EN	—	OUT_FILTER_SEL			—							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:13	—	Reserved
12	OUT_HPF_EN	High-pass filter enable. 0 = (Default) HPF disabled 1 = HPF enabled
11	—	Reserved
10:8	OUT_FILTER_SEL	Digital filter select. Configures the interpolation filter. 000 = (Default) Minimum phase, Slow roll-off (44.1k-192k) 001 = Minimum phase, Fast roll-off (32k-48k)/Balanced roll-off (88.2k-768k) 010 = Linear phase, Slow roll-off (44.1k-192k) 011 = Linear phase, Fast roll-off (32k-48k)/Balanced roll-off (88.2k-768k) 100 = Reserved 101 = Minimum phase, Fast roll-off (88.2k-768k) 110 = Reserved 111 = Linear phase, Fast roll-off (88.2k-768k)
7:0	—	Reserved

6.3.5 OUT_INV

Address: 0x0000 00CA

RW	15…8	7	6	5	4	3	2	1	0
	—	—				OUT4_INV	OUT3_INV	OUT2_INV	OUT1_INV
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:4	—	Reserved
3	OUT4_INV	Channel 4 DAC invert 0 = (Default) No inversion 1 = DAC data invert
2	OUT3_INV	Channel 3 DAC invert 0 = (Default) No inversion 1 = DAC data invert
1	OUT2_INV	Channel 2 DAC invert 0 = (Default) No inversion 1 = DAC data invert
0	OUT1_INV	Channel 1 DAC invert 0 = (Default) No inversion 1 = DAC data invert

6.3.6 OUT_VOL_CTRL1_0

Address: 0x0000 00D0

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OUT1_MUTE	—							OUT1_VOL							
Default	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	OUT1_MUTE	DAC output channel 1 mute 0 = Unmute 1 = (Default) Mute
14:8	—	Reserved
7:0	OUT1_VOL	DAC output channel 1 Volume, –127.5dB to 0dB in 0.5dB steps 0x00 = (Default) 0.0 dB … 0xFF = –127.5 dB 0x01 = –0.5 dB

6.3.7 OUT_VOL_CTRL1_1

Address: 0x0000 00D2

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OUT2_MUTE	—							OUT2_VOL							
Default	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	OUT2_MUTE	DAC output channel 2 mute 0 = Unmute 1 = (Default) Mute
14:8	—	Reserved
7:0	OUT2_VOL	DAC output channel 2 Volume, –127.5dB to 0dB in 0.5dB steps 0x00 = (Default) 0.0 dB … 0xFF = –127.5 dB 0x01 = –0.5 dB

6.3.8 OUT_VOL_CTRL2_0

Address: 0x0000 00D4

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OUT3_MUTE	—							OUT3_VOL							
Default	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	OUT3_MUTE	DAC output channel 3 mute 0 = Unmute 1 = (Default) Mute
14:8	—	Reserved
7:0	OUT3_VOL	DAC output channel 3 Volume, –127.5dB to 0dB in 0.5dB steps 0x00 = (Default) 0.0 dB … 0xFF = –127.5 dB 0x01 = –0.5 dB

6.3.9 OUT_VOL_CTRL2_1

Address: 0x0000 00D6

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OUT4_MUTE	—							OUT4_VOL							
Default	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	OUT4_MUTE	DAC output channel 4 mute 0 = Unmute 1 = (Default) Mute
14:8	—	Reserved
7:0	OUT4_VOL	DAC output channel 4 Volume, –127.5dB to 0dB in 0.5dB steps 0x00 = (Default) 0.0 dB … 0xFF = –127.5 dB 0x01 = –0.5 dB

6.3.10 OUT_VOL_CTRL5

Address: 0x0000 00E0

	15…8	7	6	5	4	3	2	1	0
WO	—	—							OUT_VU
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:1	—	Reserved
0	OUT_VU	Global output volume update trigger 0 = (Default) No action 1 = Write 1 to trigger an update of all output volume/mute registers

6.3.11 SHUTDOWN_CTRL

Address: 0x0000 00E4

	15…8	7	6	5	4	3	2	1	0
RW	—	—							DAC_REF_DISABLE
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:1	—	Reserved
0	DAC_REF_DISABLE	DAC reference shutdown control. Can be used to minimize power consumption if all output paths are disabled. 0 = (Default) Enable DAC reference 1 = Shutdown DAC reference

6.3.12 STARTUP_DELAY

Address: 0x0000 00E6

	15…8	7	6	5	4	3	2	1	0
RW	—	—				STARTUP_DELAY_EN	STARTUP_DELAY_TIME		
Default	0x00	0	0	0	0	1	1	0	0

Bits	Name	Description
15:4	—	Reserved
3	STARTUP_DELAY_EN	Startup delay enable. Can be used to avoid raised noise floor during DAC reference start-up. 0 = Disabled 1 = (Default) Enabled
2:0	STARTUP_DELAY_TIME	Startup delay time. Can be used to avoid raised noise floor during DAC reference start-up. 000 = 100 ms 001 = 250 ms 010 = 500 ms 011 = 750 ms 100 = (Default) 1 s 101 = 1.25 s 110 = 1.5 s 111 = 2 s

6.3.13 DSD_CTRL

Address: 0x0000 00E8

	15…8	7	6	5	4	3	2	1	0
RW	—	—	DSD_PM_SEL	DSD_PM_EN	DSD_ZERODB	DSD_OSR			DSD_EN
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:7	—	Reserved
6	DSD_PM_SEL	DSD phase modulation mode clock rate select. 0 = (Default) DSD clock at 2 x OSR rate 1 = DSD clock at OSR rate
5	DSD_PM_EN	DSD phase modulation enable. 0 = (Default) Disabled 1 = Enabled
4	DSD_ZERODB	DSD input 0 dB level. 0 = (Default) SACD +3.1 dB level matches PCM 0 dBFS level 1 = SACD 0 dB level matches PCM 0 dBFS level

Bits	Name	Description
3:1	DSD_OSR	DSD oversample rate (OSR). 000 = (Default) 64 Fs 001 = 128 Fs 010 = 256 Fs 011 = Reserved 100 = 512 Fs 101–111 = Reserved
0	DSD_EN	DSD interface enable. Selects ASP or DSD signal path. 0 = (Default) Select ASP path 1 = Select DSD path

6.3.14 DSD_FILT

Address: 0x0000 00EC

RW	15…8	7	6	5	4	3	2	1	0
	—	—			DSD_HPF_EN	—			
Default	0x00	0	0	0	1	0	0	0	0

Bits	Name	Description
15:5	—	Reserved
4	DSD_HPF_EN	DSD high-pass filter enable. 0 = Disabled 1 = (Default) Enabled
3:0	—	Reserved

6.4 PIN_CONFIG

6.4.1 PAD_FN

Address: 0x0000 3D24

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—						CONFIG5_FN	CONFIG4_FN	CONFIG3_FN	CONFIG2_FN	SPI_SCK_FN	SPI_CS_FN	ASP_DIN4_FN	ASP_DIN3_FN	ASP_DIN2_FN	—
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:10	—	Reserved
9	CONFIG5_FN	CONFIG5 pin function select 0 = (Default) HW config 1 = GP output
8	CONFIG4_FN	CONFIG4 pin function select 0 = (Default) HW config 1 = GP output
7	CONFIG3_FN	CONFIG3 pin function select 0 = (Default) HW config 1 = GP output
6	CONFIG2_FN	CONFIG2 pin function select 0 = (Default) HW config 1 = GP output
5	SPI_SCK_FN	SPI_SCK pin function select 0 = (Default) SPI_SCK 1 = GP output
4	SPI_CS_FN	SPI_CS pin function select 0 = (Default) SPI_CS 1 = GP output
3	ASP_DIN4_FN	ASP_DIN4 pin function select 0 = (Default) ASP_DIN4 1 = GP output
2	ASP_DIN3_FN	ASP_DIN3 pin function select 0 = (Default) ASP_DIN3 1 = GP output
1	ASP_DIN2_FN	ASP_DIN2 pin function select 0 = (Default) ASP_DIN2 1 = GP output
0	—	Reserved

6.4.2 PAD_LVL

Address: 0x0000 3D28

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—						CONFIG5_LVL	CONFIG4_LVL	CONFIG3_LVL	CONFIG2_LVL	SPI_SCK_LVL	SPI_CS_LVL	ASP_DIN4_LVL	ASP_DIN3_LVL	ASP_DIN2_LVL	—
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:10	—	Reserved
9	CONFIG5_LVL	CONFIG5 output level. Sets the output level if CONFIG5 is configured as GP output. 0 = (Default) Logic 0 1 = Logic 1
8	CONFIG4_LVL	CONFIG4 output level. Sets the output level if CONFIG4 is configured as GP output. 0 = (Default) Logic 0 1 = Logic 1
7	CONFIG3_LVL	CONFIG3 output level. Sets the output level if CONFIG3 is configured as GP output. 0 = (Default) Logic 0 1 = Logic 1
6	CONFIG2_LVL	CONFIG2 output level. Sets the output level if CONFIG2 is configured as GP output. 0 = (Default) Logic 0 1 = Logic 1
5	SPI_SCK_LVL	SPI_SCK output level. Sets the output level if SPI_SCK is configured as GP output. 0 = (Default) Logic 0 1 = Logic 1
4	SPI_CS_LVL	SPI_CS output level. Sets the output level if SPI_CS is configured as GP output. 0 = (Default) Logic 0 1 = Logic 1
3	ASP_DIN4_LVL	ASP_DIN4 output level. Sets the output level if ASP_DIN4 is configured as GP output. 0 = (Default) Logic 0 1 = Logic 1
2	ASP_DIN3_LVL	ASP_DIN3 output level. Sets the output level if ASP_DIN3 is configured as GP output. 0 = (Default) Logic 0 1 = Logic 1
1	ASP_DIN2_LVL	ASP_DIN2 output level. Sets the output level if ASP_DIN2 is configured as GP output. 0 = (Default) Logic 0 1 = Logic 1
0	—	Reserved

7 Performance Plots

7.1 DAC Filter Response

The DAC filter performance is described in this section. Note that the group-delay plots represent the filter only—see Table 3-5 for full-path latency.

DAC Filter Response—Fast Roll-Off, 32 kHz Sample Rate

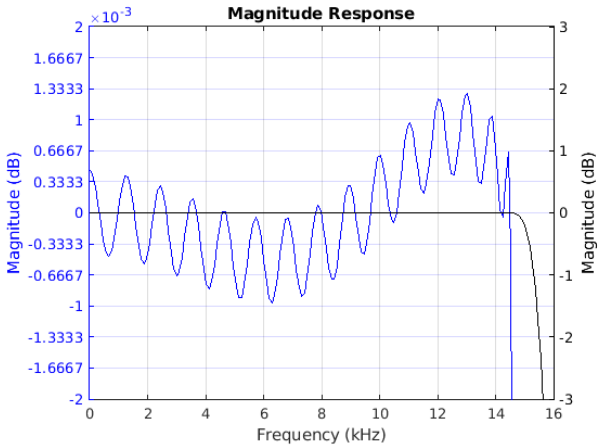


Figure 7-1. Passband Magnitude

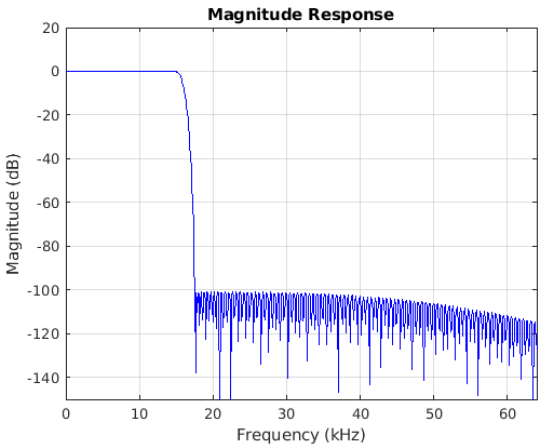


Figure 7-2. Stopband Magnitude

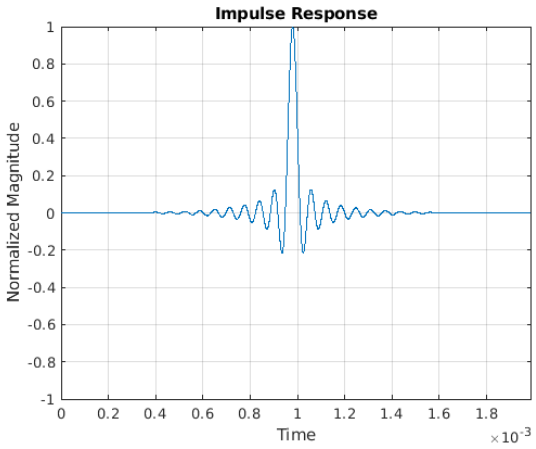


Figure 7-3. Impulse Response—Linear Phase

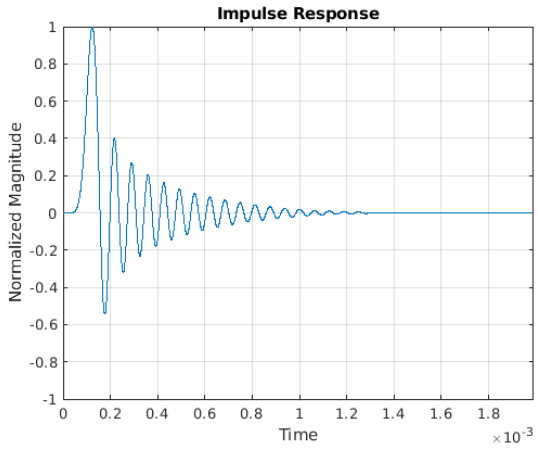


Figure 7-4. Impulse Response—Minimum Phase

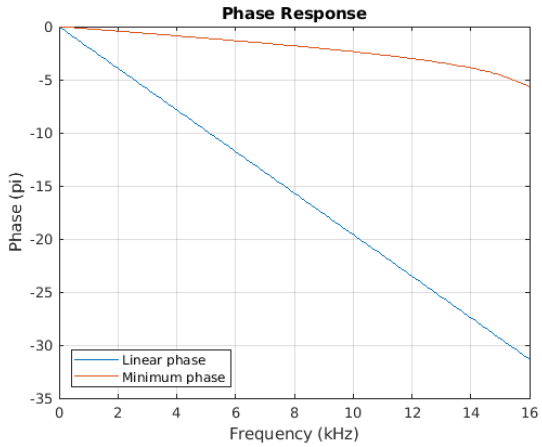


Figure 7-5. Phase vs. Frequency

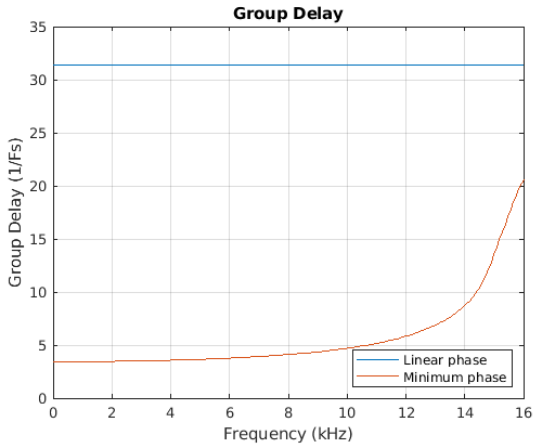


Figure 7-6. Group Delay vs. Frequency

DAC Filter Response—Fast Roll-Off, 48 kHz Sample Rate

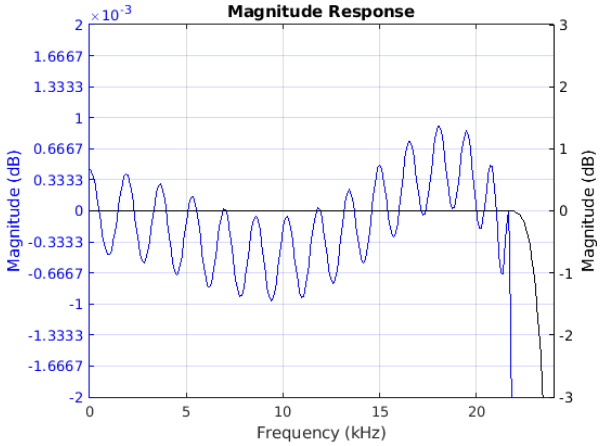


Figure 7-7. Passband Magnitude

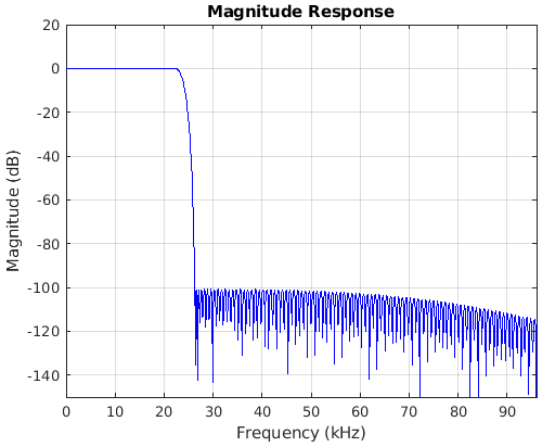


Figure 7-8. Stopband Magnitude

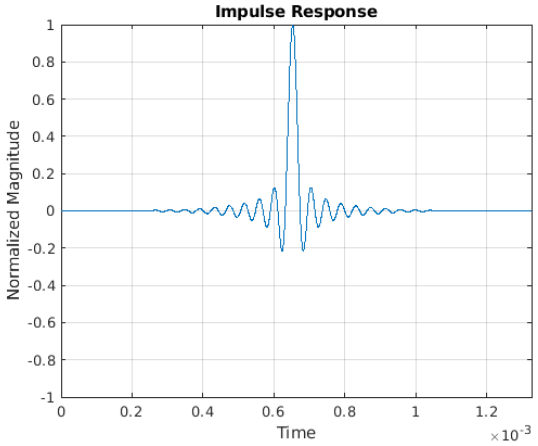


Figure 7-9. Impulse Response—Linear Phase

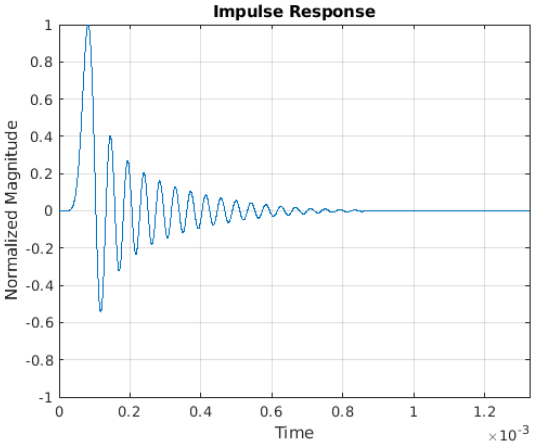


Figure 7-10. Impulse Response—Minimum Phase

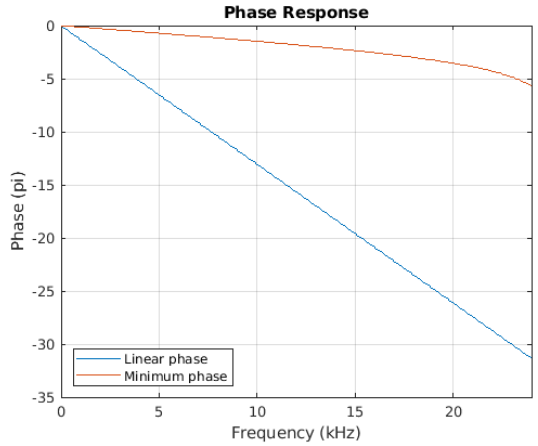


Figure 7-11. Phase vs. Frequency

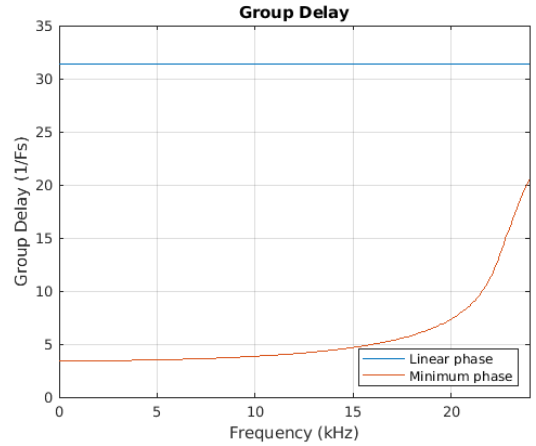


Figure 7-12. Group Delay vs. Frequency

DAC Filter Response—Slow Roll-Off, 48 kHz Sample Rate

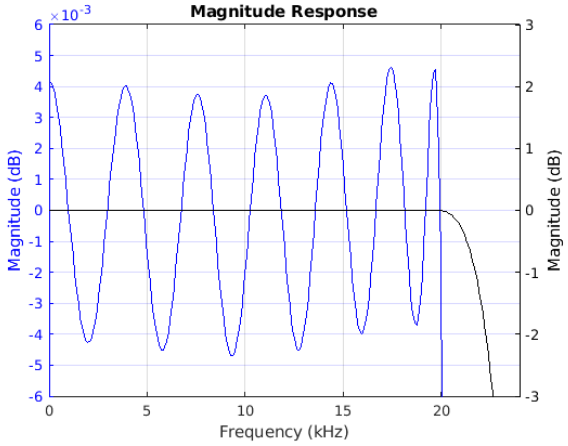


Figure 7-13. Passband Magnitude

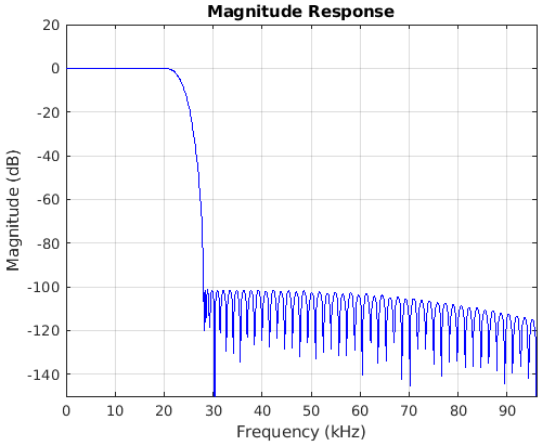


Figure 7-14. Stopband Magnitude

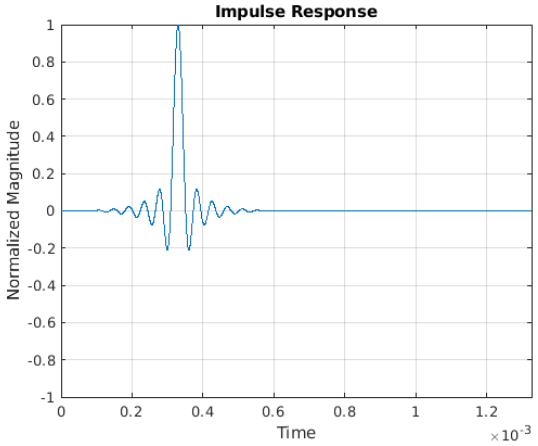


Figure 7-15. Impulse Response—Linear Phase

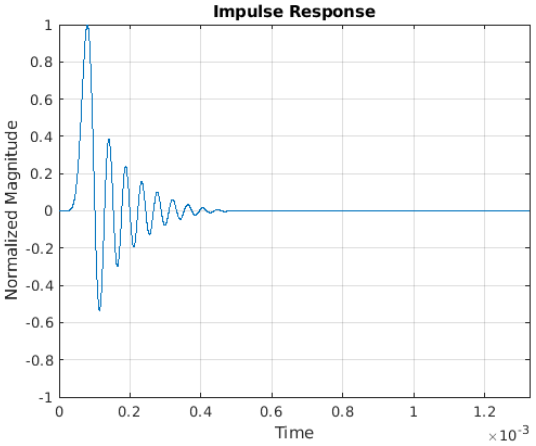


Figure 7-16. Impulse Response—Minimum Phase

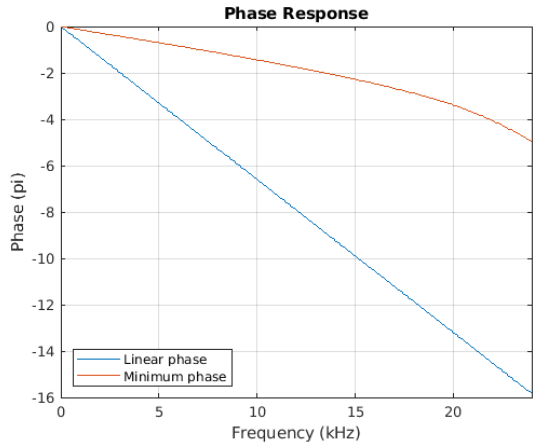


Figure 7-17. Phase vs. Frequency

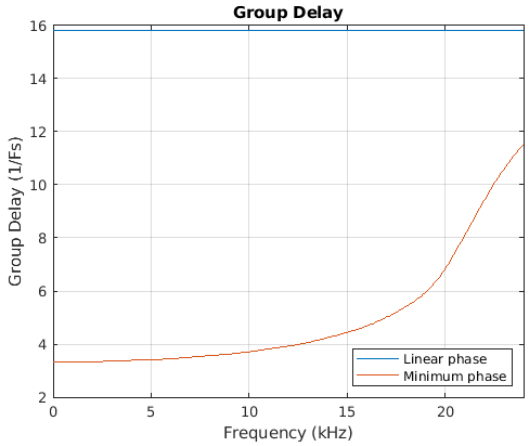


Figure 7-18. Group Delay vs. Frequency

DAC Filter Response—Fast Roll-Off, 96 kHz Sample Rate

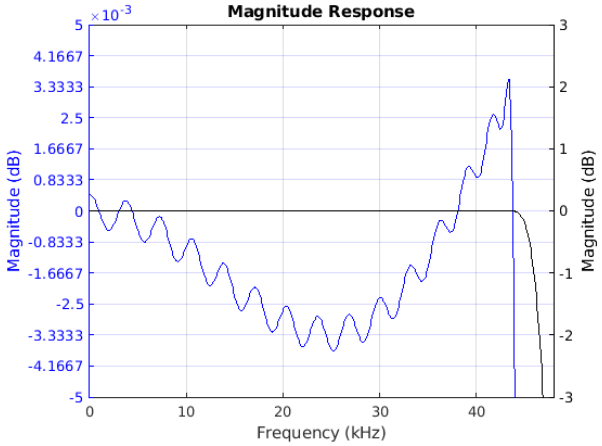


Figure 7-19. Passband Magnitude

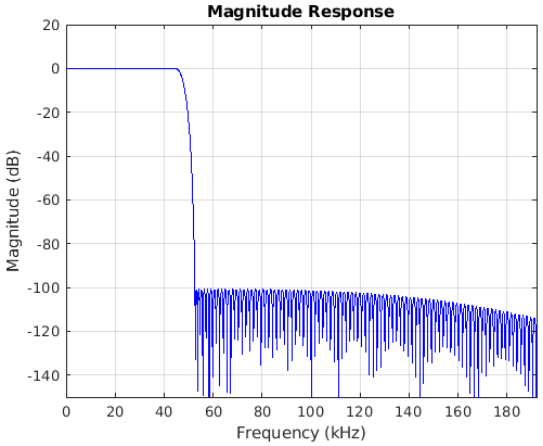


Figure 7-20. Stopband Magnitude

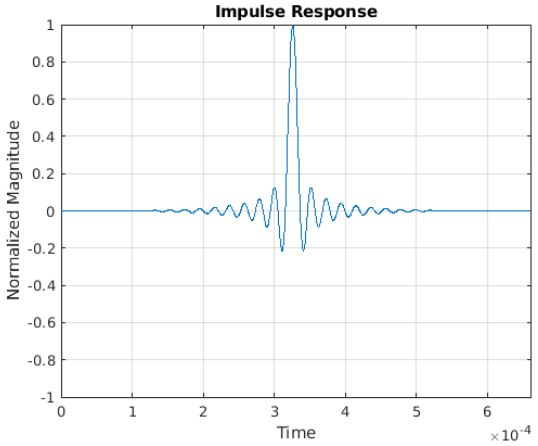


Figure 7-21. Impulse Response—Linear Phase

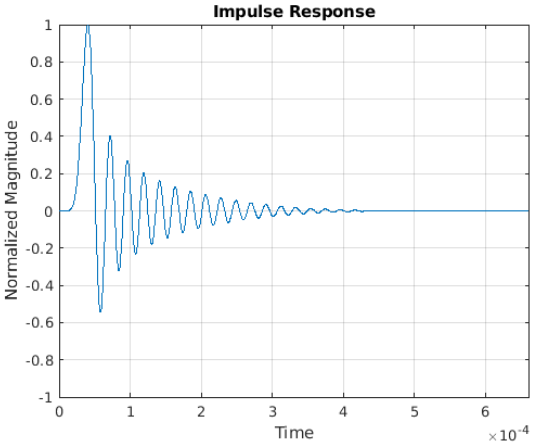


Figure 7-22. Impulse Response—Minimum Phase

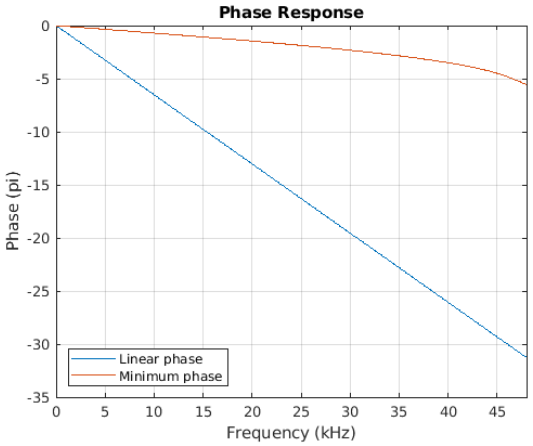


Figure 7-23. Phase vs. Frequency

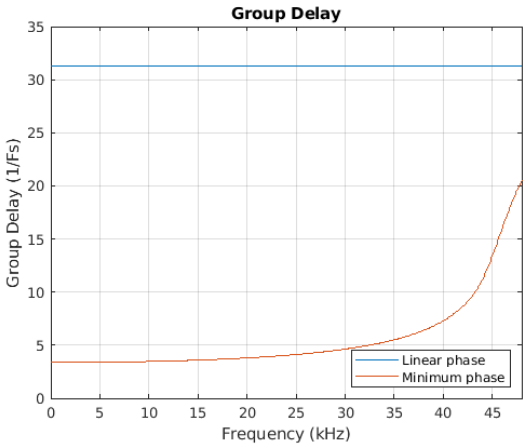


Figure 7-24. Group Delay vs. Frequency

DAC Filter Response—Slow Roll-Off, 96 kHz Sample Rate

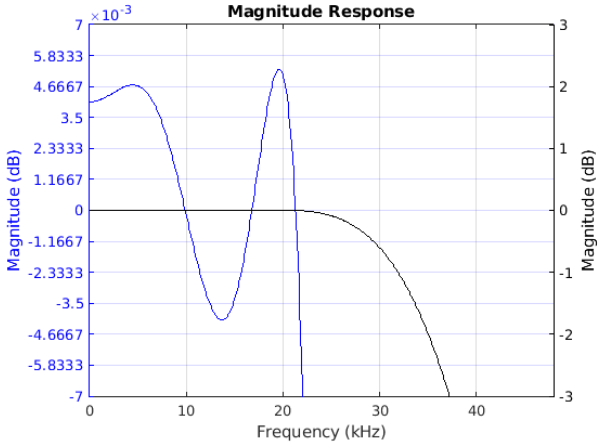


Figure 7-25. Passband Magnitude

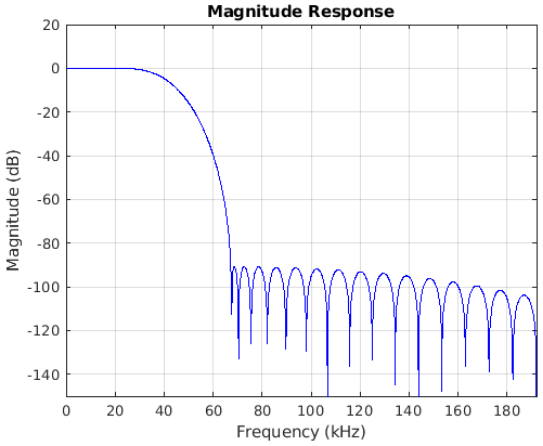


Figure 7-26. Stopband Magnitude

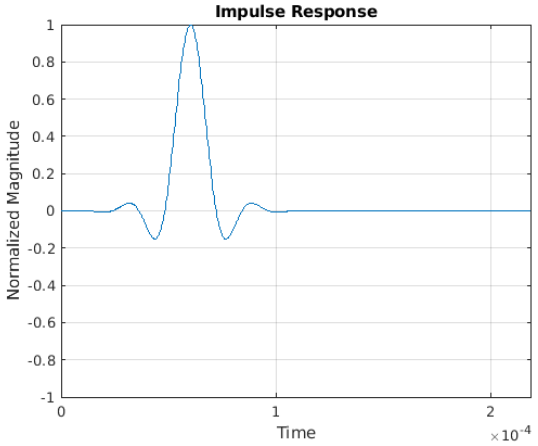


Figure 7-27. Impulse Response—Linear Phase

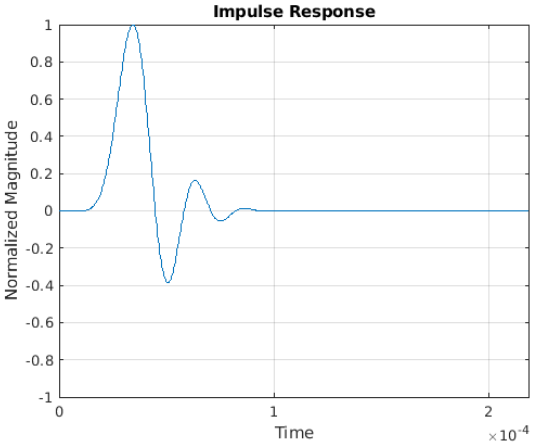


Figure 7-28. Impulse Response—Minimum Phase

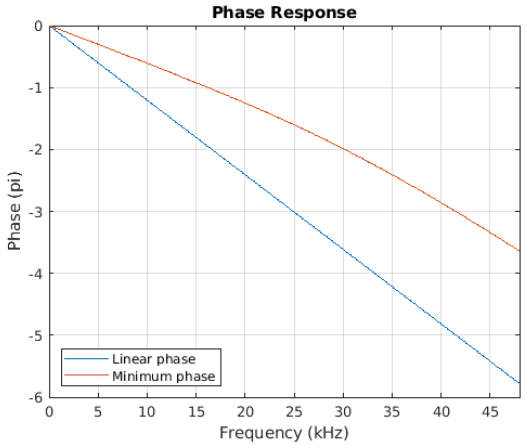


Figure 7-29. Phase vs. Frequency

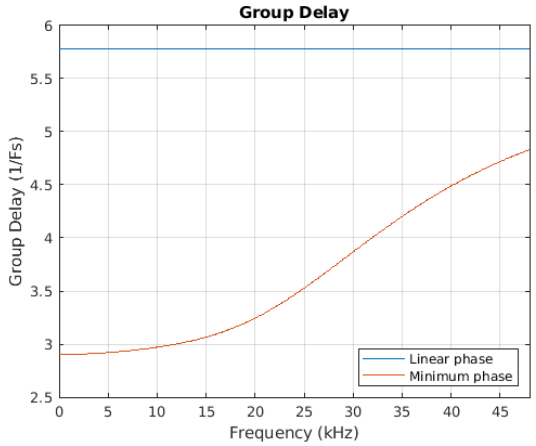


Figure 7-30. Group Delay vs. Frequency

DAC Filter Response—Balanced Roll-Off, 96 kHz Sample Rate

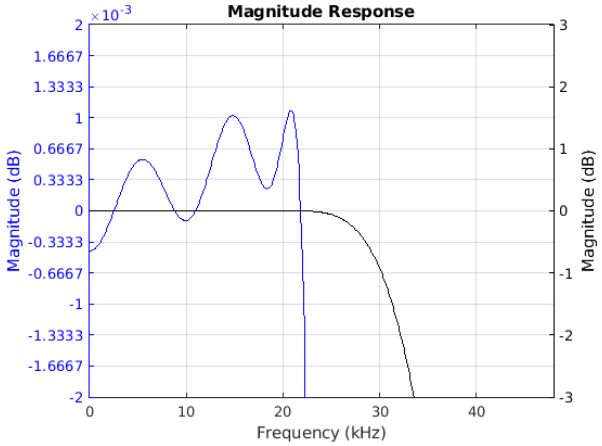


Figure 7-31. Passband Magnitude

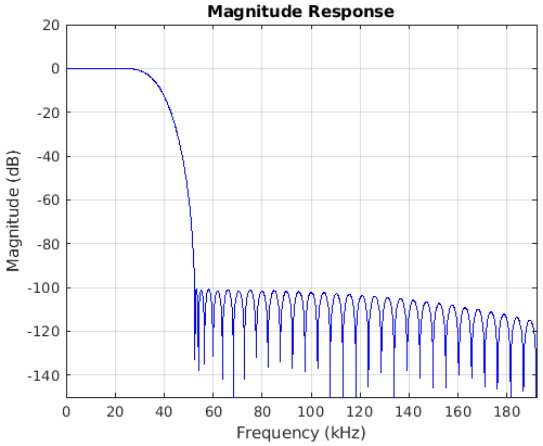


Figure 7-32. Stopband Magnitude

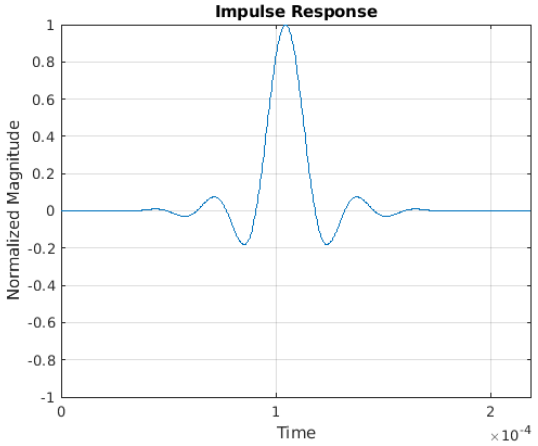


Figure 7-33. Impulse Response—Linear Phase

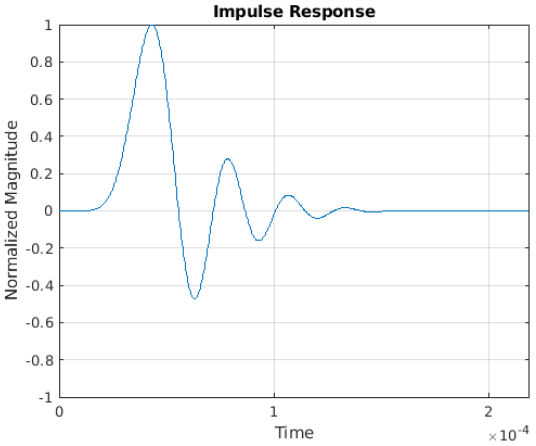


Figure 7-34. Impulse Response—Minimum Phase

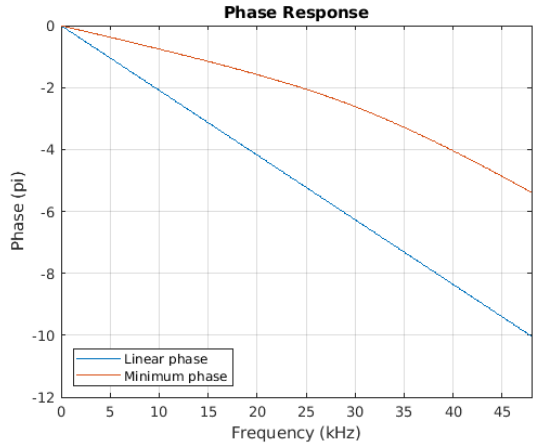


Figure 7-35. Phase vs. Frequency

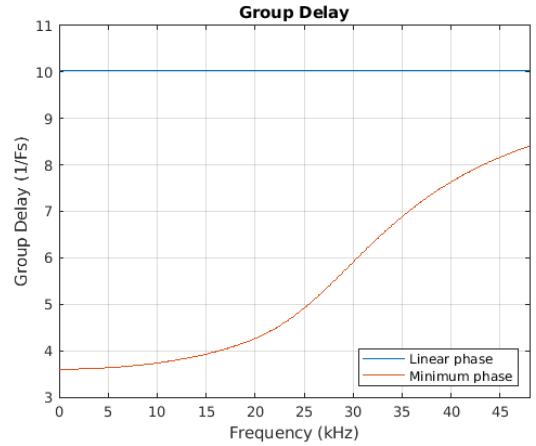


Figure 7-36. Group Delay vs. Frequency

DAC Filter Response—Fast Roll-Off, 192 kHz Sample Rate

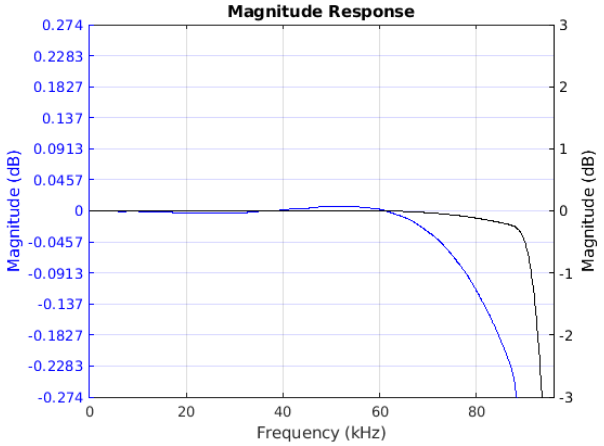


Figure 7-37. Passband Magnitude

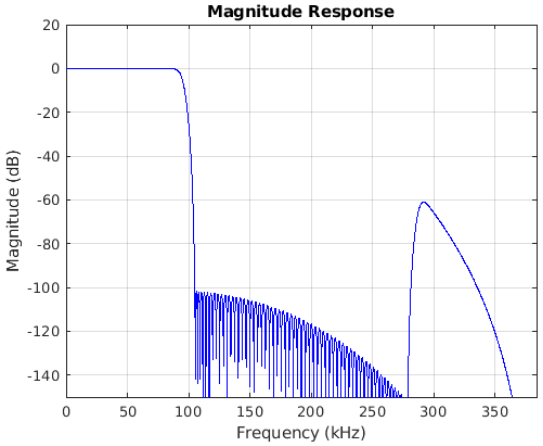


Figure 7-38. Stopband Magnitude

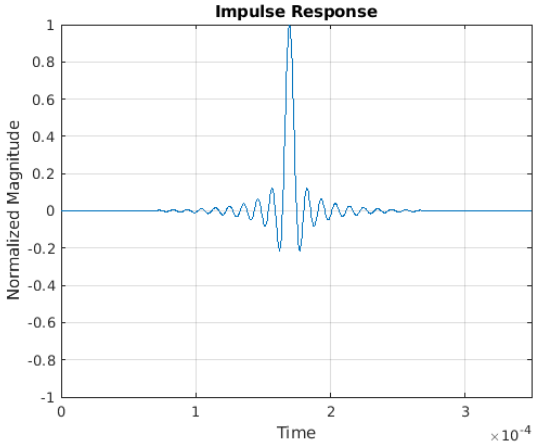


Figure 7-39. Impulse Response—Linear Phase

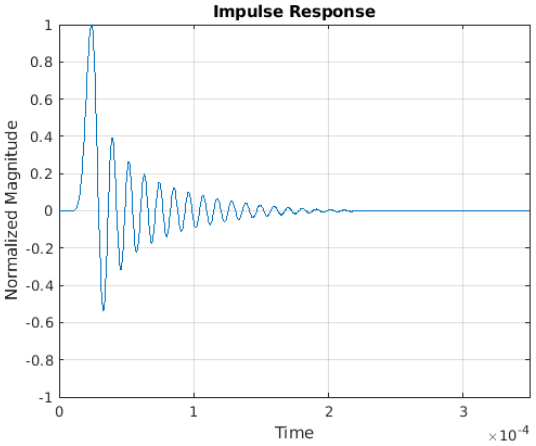


Figure 7-40. Impulse Response—Minimum Phase

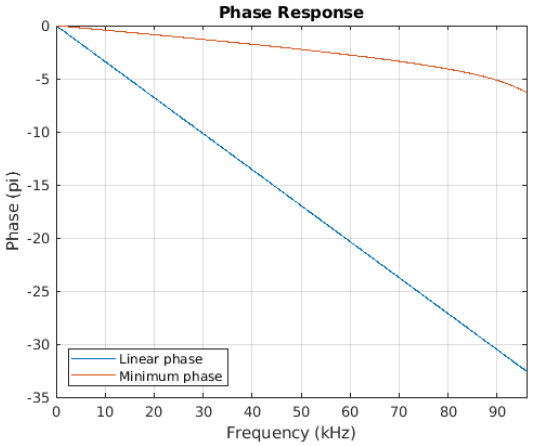


Figure 7-41. Phase vs. Frequency

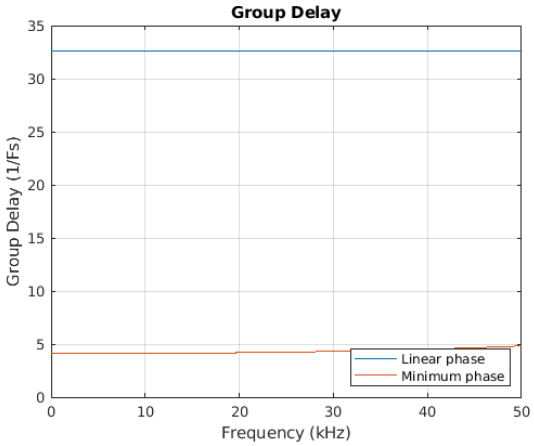


Figure 7-42. Group Delay vs. Frequency

DAC Filter Response—Slow Roll-Off, 192 kHz Sample Rate

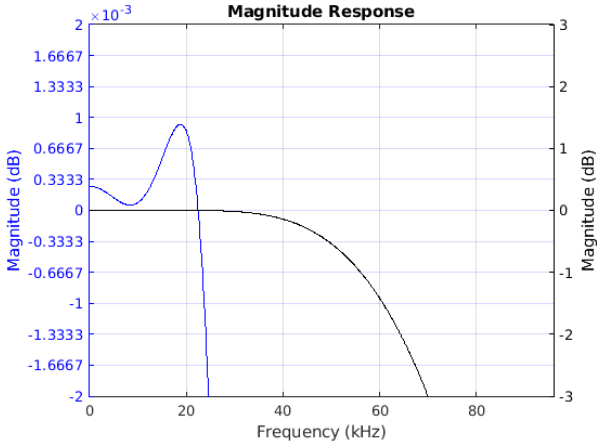


Figure 7-43. Passband Magnitude

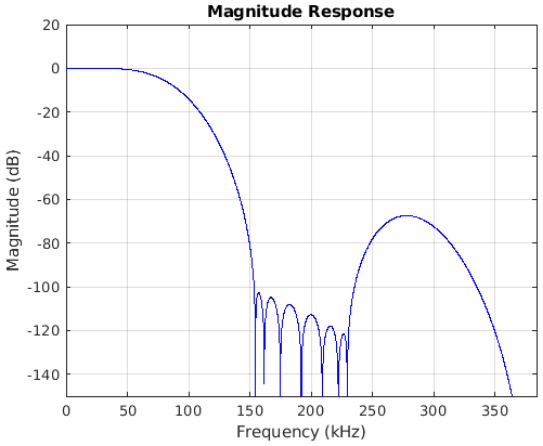


Figure 7-44. Stopband Magnitude

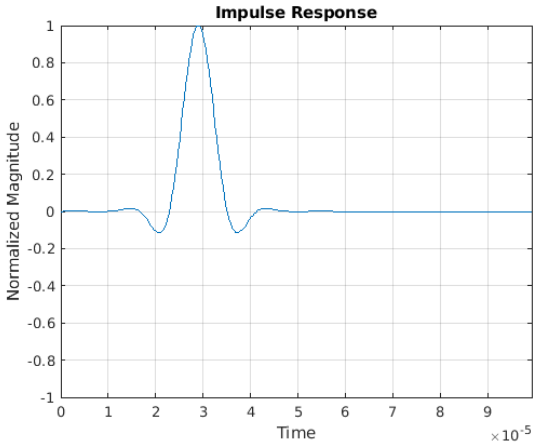


Figure 7-45. Impulse Response—Linear Phase

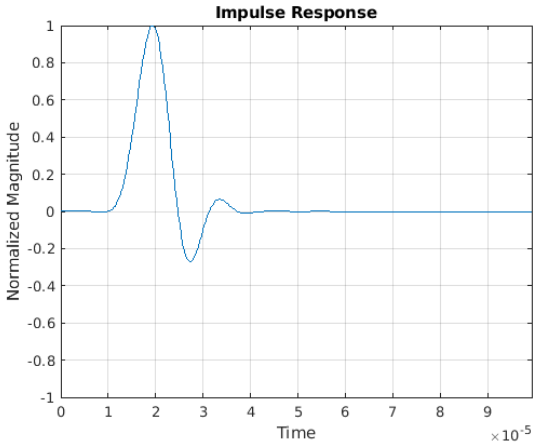


Figure 7-46. Impulse Response—Minimum Phase

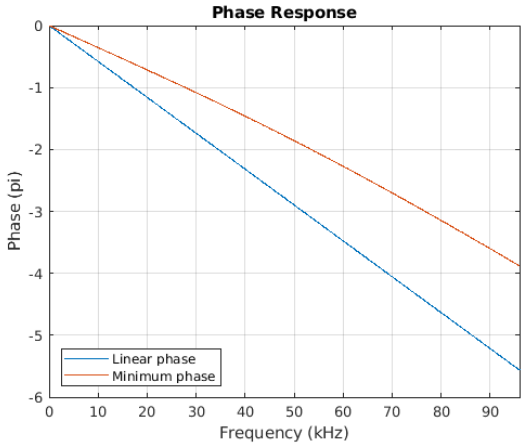


Figure 7-47. Phase vs. Frequency

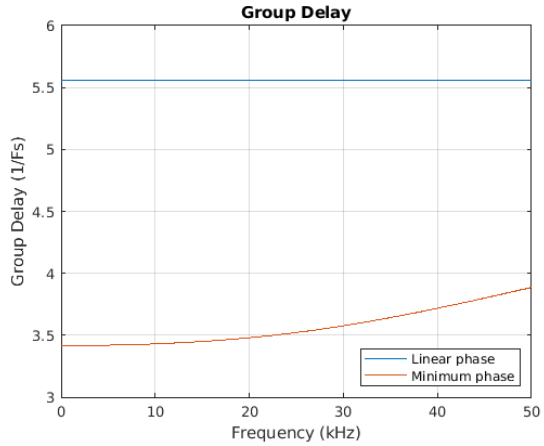


Figure 7-48. Group Delay vs. Frequency

DAC Filter Response—Balanced Roll-Off, 192 kHz Sample Rate

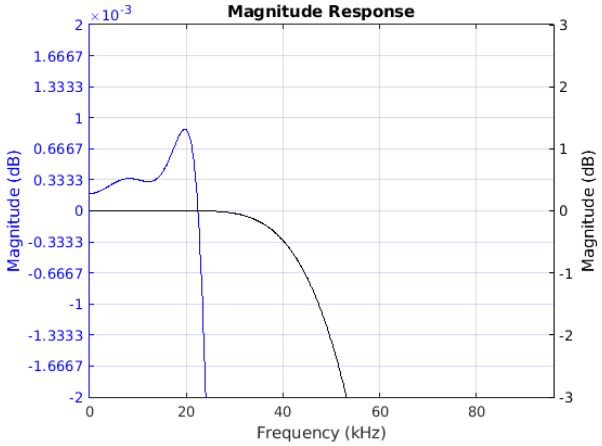


Figure 7-49. Passband Magnitude

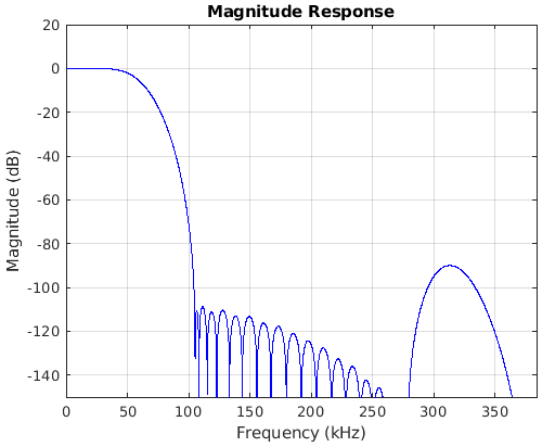


Figure 7-50. Stopband Magnitude

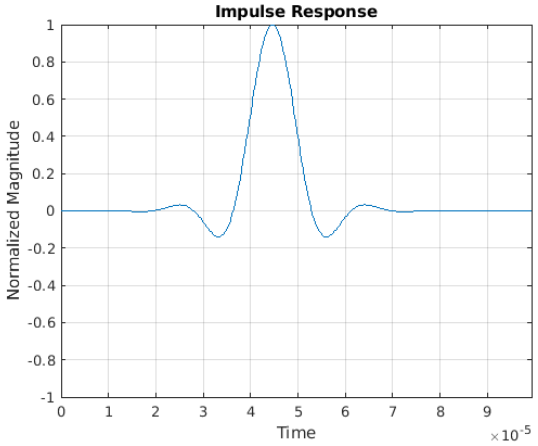


Figure 7-51. Impulse Response—Linear Phase

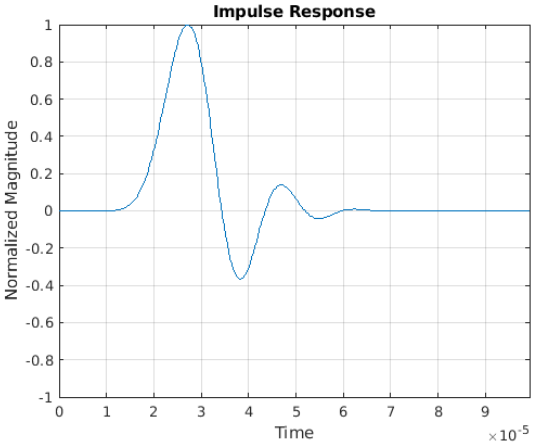


Figure 7-52. Impulse Response—Minimum Phase

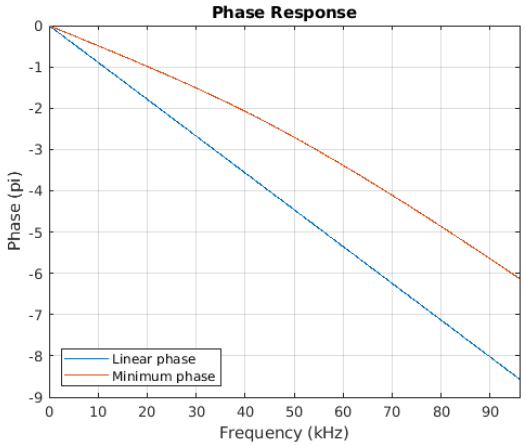


Figure 7-53. Phase vs. Frequency

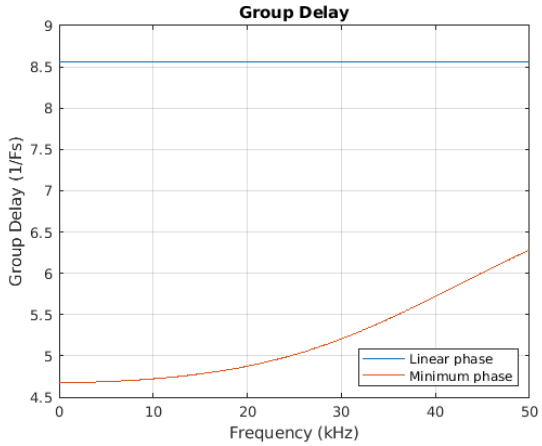


Figure 7-54. Group Delay vs. Frequency

DAC Filter Response—Fast Roll-Off, 384 kHz Sample Rate

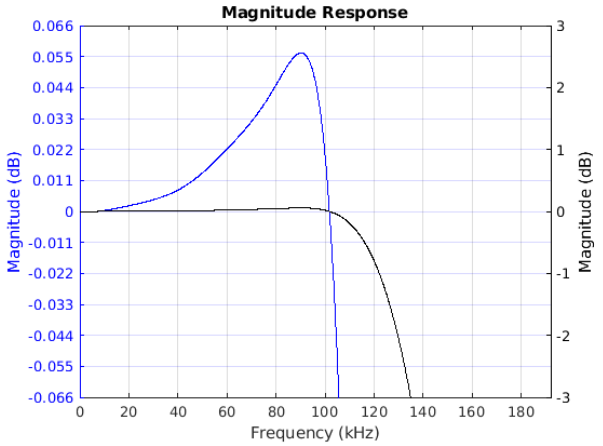


Figure 7-55. Passband Magnitude

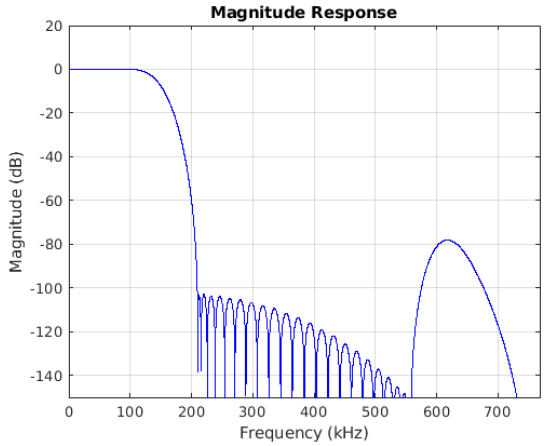


Figure 7-56. Stopband Magnitude

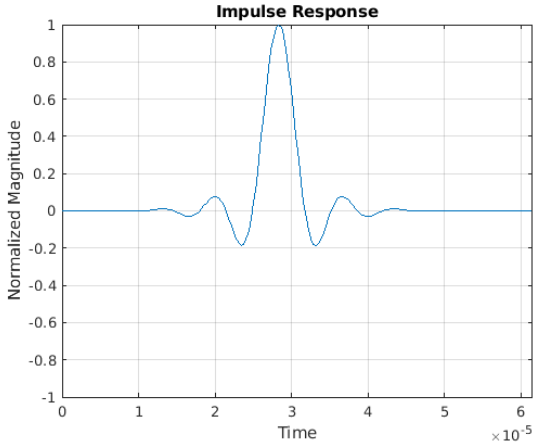


Figure 7-57. Impulse Response—Linear Phase

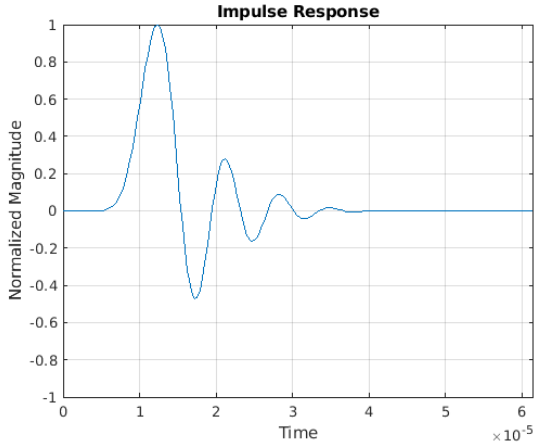


Figure 7-58. Impulse Response—Minimum Phase

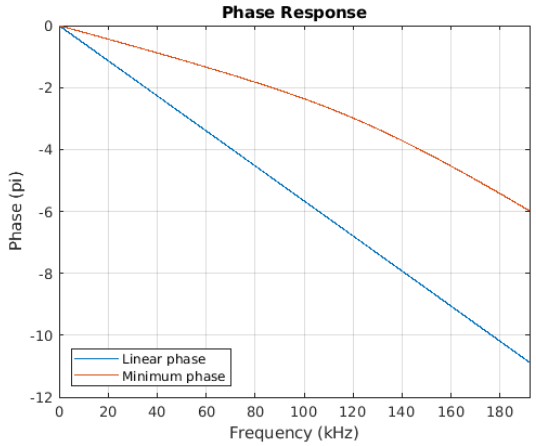


Figure 7-59. Phase vs. Frequency

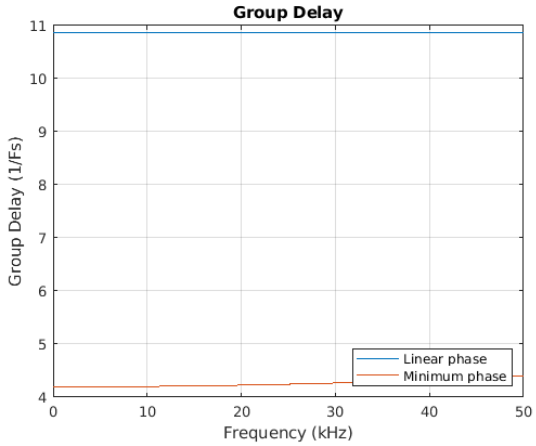


Figure 7-60. Group Delay vs. Frequency

DAC Filter Response—Balanced Roll-Off, 384 kHz Sample Rate

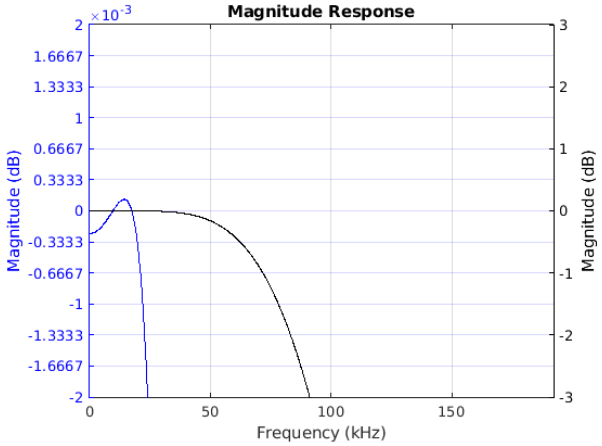


Figure 7-61. Passband Magnitude

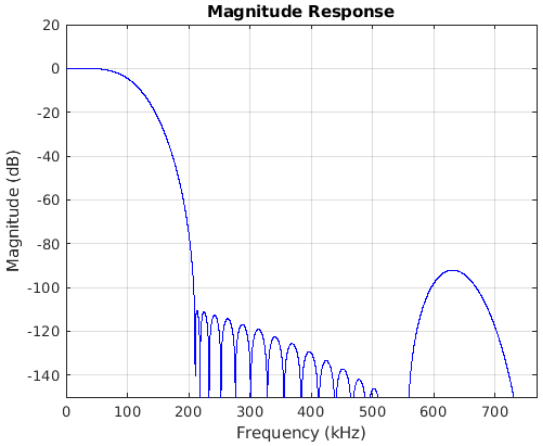


Figure 7-62. Stopband Magnitude

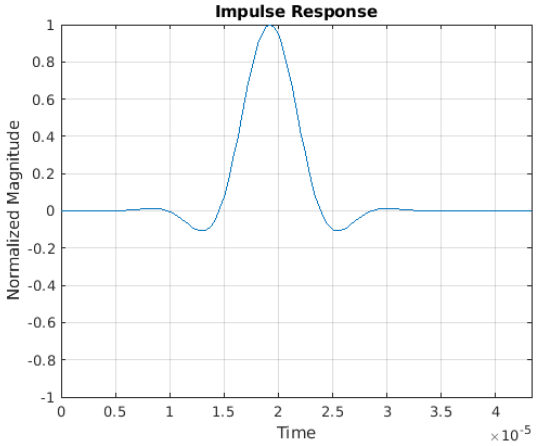


Figure 7-63. Impulse Response—Linear Phase

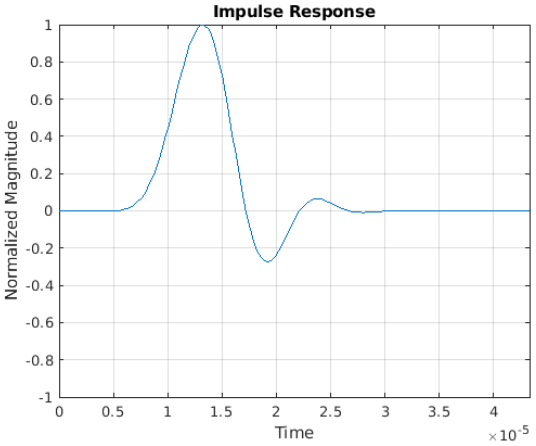


Figure 7-64. Impulse Response—Minimum Phase

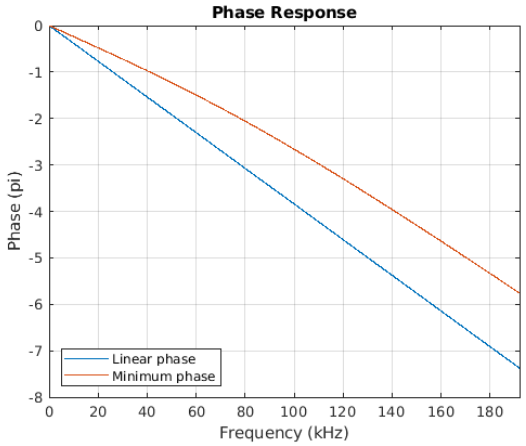


Figure 7-65. Phase vs. Frequency

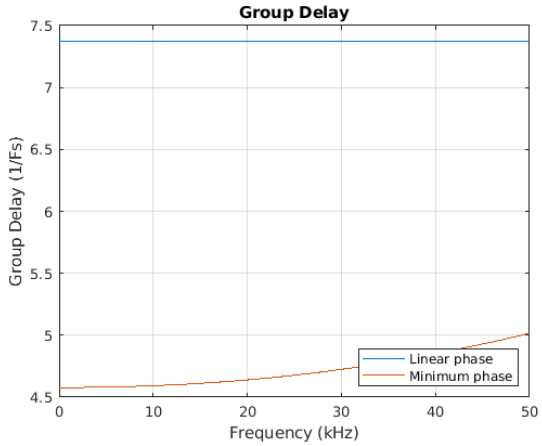


Figure 7-66. Group Delay vs. Frequency

DAC Filter Response—Fast Roll-Off, 768 kHz Sample Rate

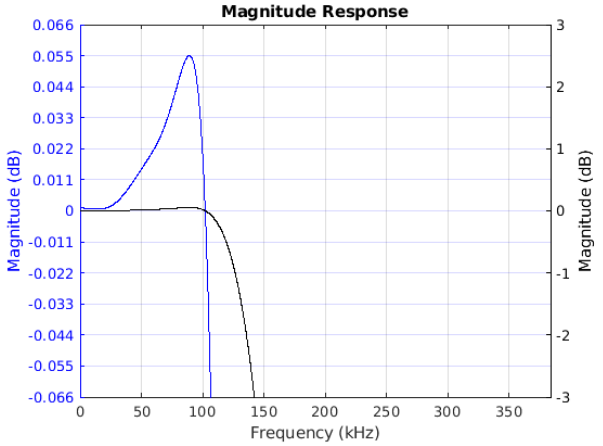


Figure 7-67. Passband Magnitude

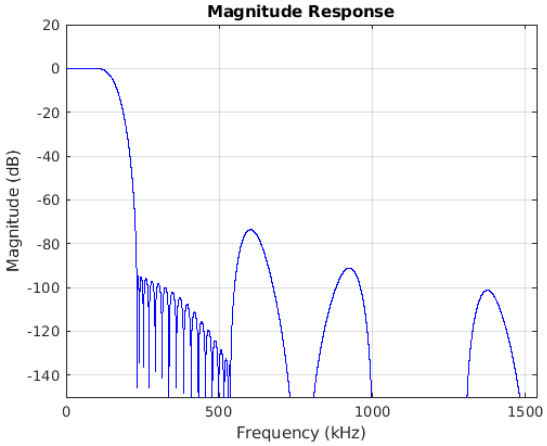


Figure 7-68. Stopband Magnitude

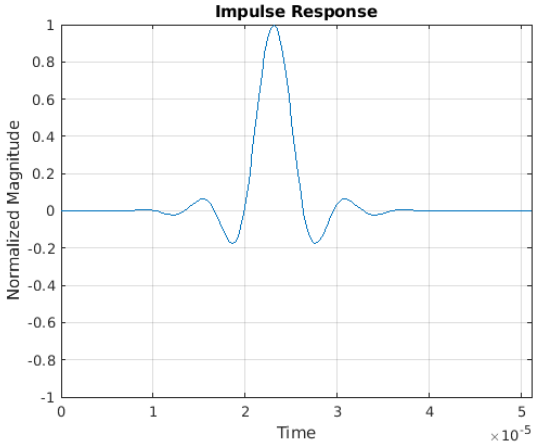


Figure 7-69. Impulse Response—Linear Phase

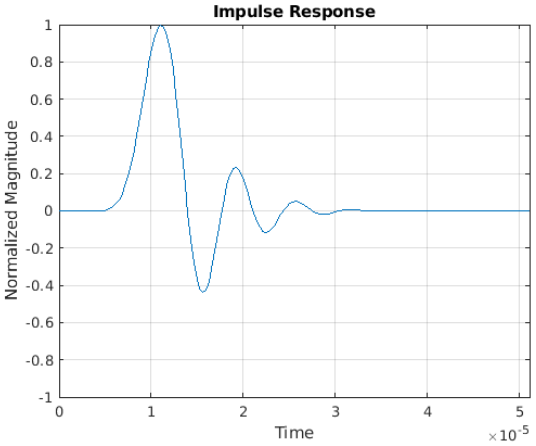


Figure 7-70. Impulse Response—Minimum Phase

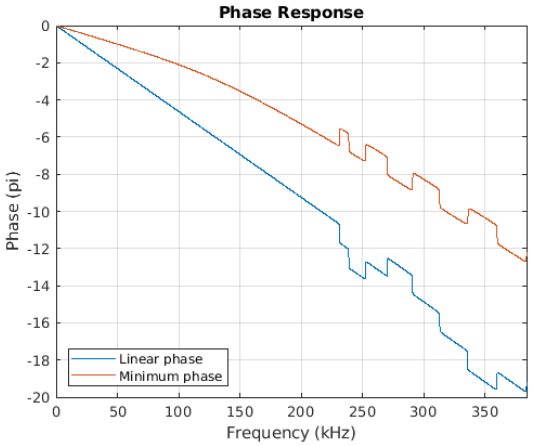


Figure 7-71. Phase vs. Frequency

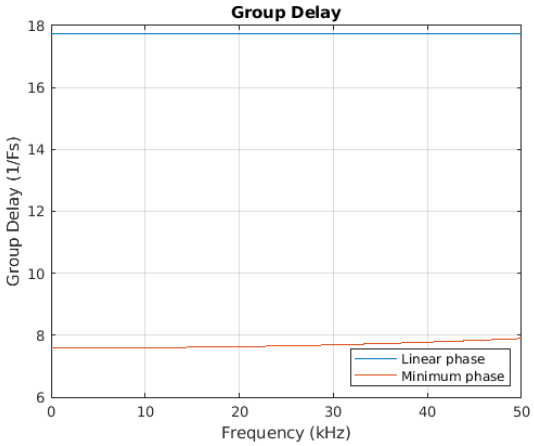


Figure 7-72. Group Delay vs. Frequency

DAC Filter Response—Balanced Roll-Off, 768 kHz Sample Rate

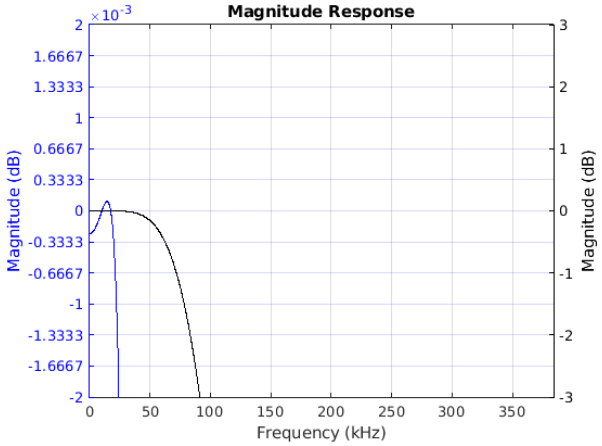


Figure 7-73. Passband Magnitude

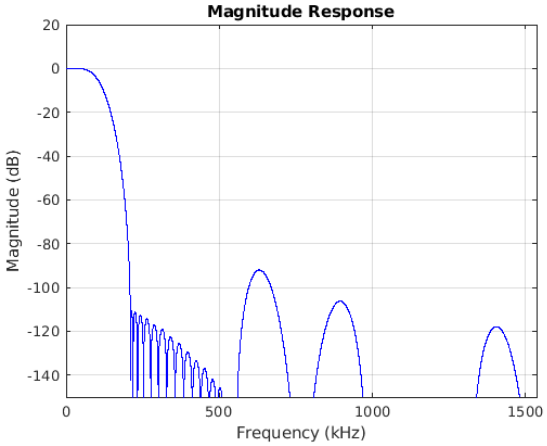


Figure 7-74. Stopband Magnitude

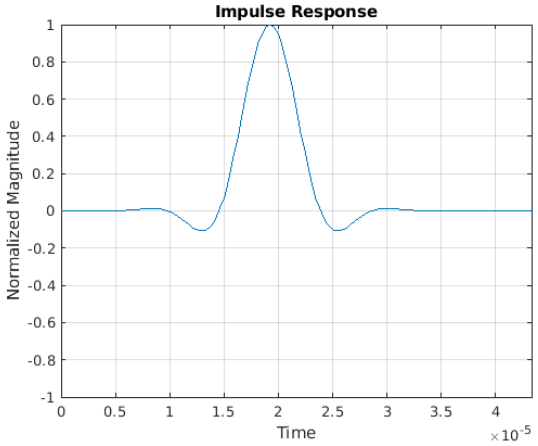


Figure 7-75. Impulse Response—Linear Phase

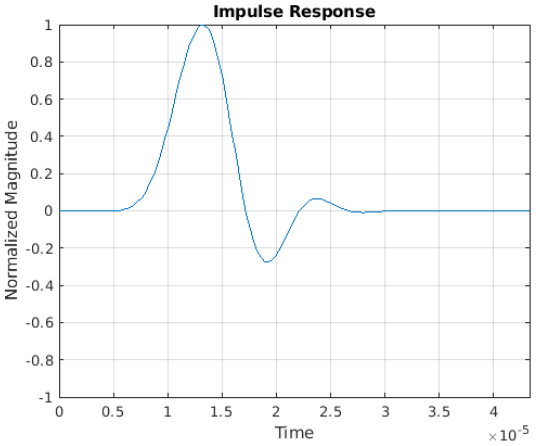


Figure 7-76. Impulse Response—Minimum Phase

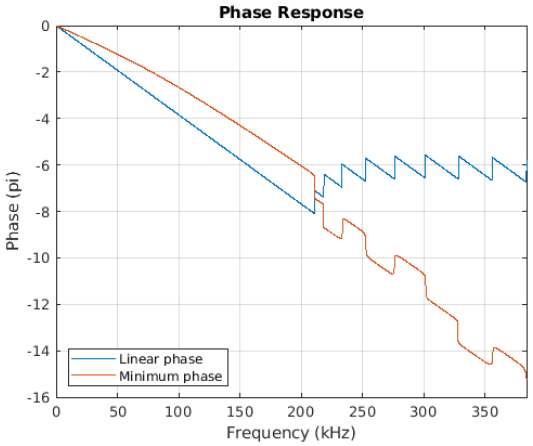


Figure 7-77. Phase vs. Frequency

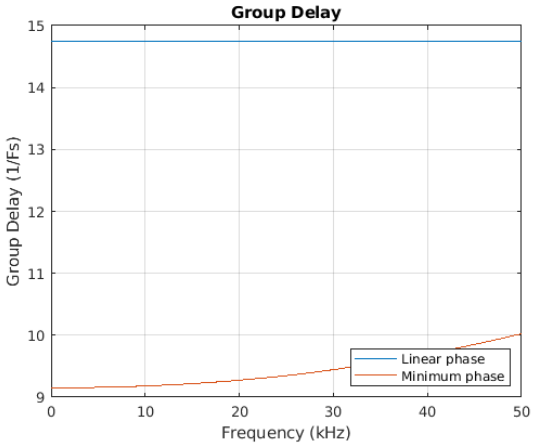


Figure 7-78. Group Delay vs. Frequency

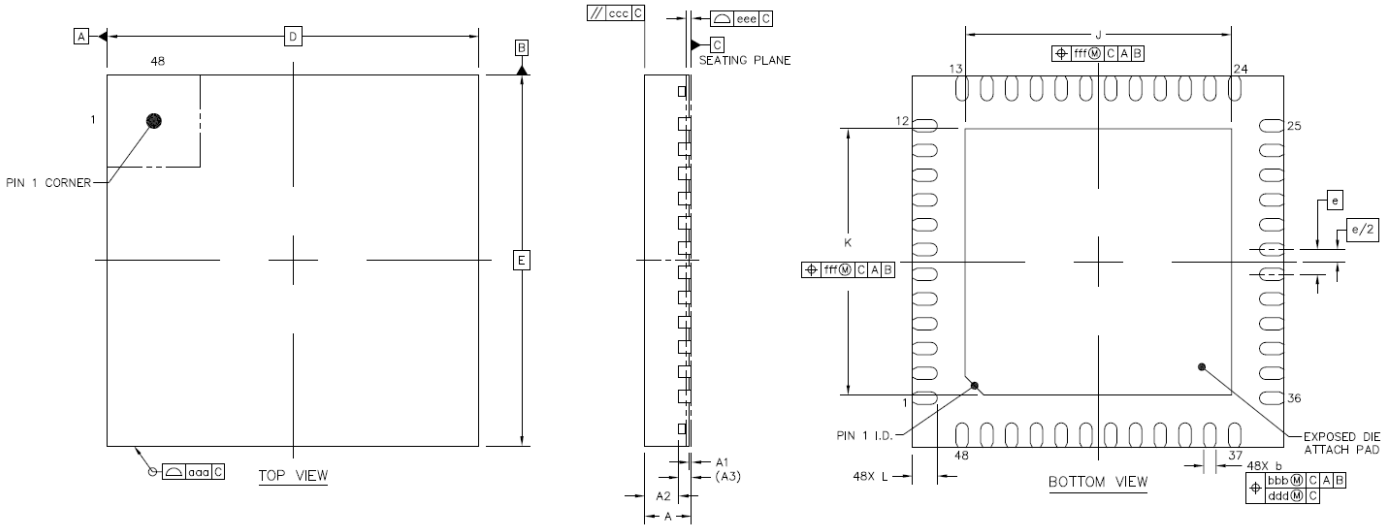
8 Thermal Characteristics

Table 8-1. Typical JEDEC Four-Layer, 2s2p Board Thermal Characteristics

Parameter	Symbol	QFN	Units
Junction-to-ambient thermal resistance	θ_{JA}	18.69	°C/W
Junction-to-board thermal resistance	θ_{JB}	5.51	°C/W
Junction-to-case (top) thermal resistance	θ_{JC}	44.75	°C/W
Junction-to-board thermal-characterization parameter	Ψ_{JB}	5.29	°C/W
Junction-to-package-top thermal-characterization parameter	Ψ_{JT}	1.26	°C/W

Notes:
- Natural convection at the maximum recommended operating temperature T_A (see Table 3-2)
- Four-layer, 2s2p PCB as specified by JESD51–9 and JESD51–11; dimensions: 101.5 x 114.5 x 1.6 mm
- Thermal parameters as defined by JESD51–12

9 Package Dimensions



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D	6 BSC		
	Y	E	6 BSC		
LEAD PITCH		e	0.4 BSC		
EP SIZE	X	J	4.2	4.3	4.4
	Y	K	4.2	4.3	4.4
LEAD LENGTH		L	0.3	0.4	0.5
PACKAGE EDGE TOLERANCE		aaa	0.1		
LEAD OFFSET		bbb	0.1		
		ddd	0.05		
MOLD FLATNESS		ccc	0.1		
COPLANARITY		eee	0.08		
EXPOSED PAD OFFSET		fff	0.1		

Figure 9-1. QFN Package Drawing

10 Package Marking

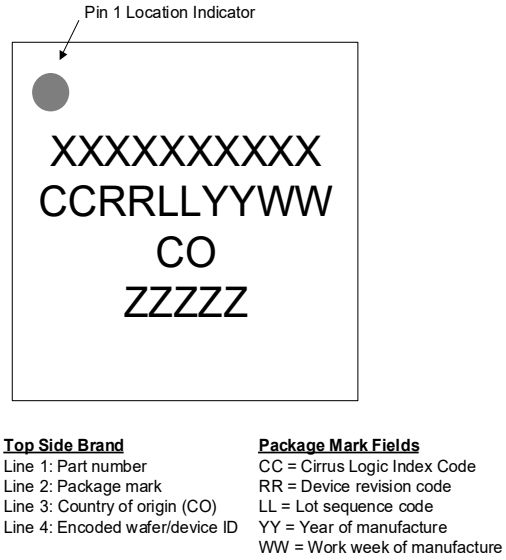


Figure 10-1. Package Marking

11 Ordering Information

Table 11-1. Ordering Information

Product	Description	Package	RoHS Compliant	Grade	Temperature Range	Container	Orderable Part Number
CS4304P	High Performance Multichannel Audio DAC	48-pin QFN	Yes	Commercial	–40 to +85°C	Tray	CS4304P–DN
CS4304P	High Performance Multichannel Audio DAC	48-pin QFN	Yes	Commercial	–40 to +85°C	Tape and Reel	CS4304P–DNR

12 References

- NXP Semiconductors, UM10204 Rev. 7, October 2021, *I2C-Bus Specification and User Manual*, http://www.nxp.com

13 Revision History

Table 13-1. Revision History

Revision	Changes
A1 NOV 2023	• Initial version
A2 JUN 2024	• Updated VDD_D reset thresholds (Table 3-9) • Updated “fsb” references to “fs(base)” (Section 4.2, Section 4.4.1)
A3 DEC 2024	• Recommended external components updated (Section 2, Section 4.5.4) • ASP_DIN setup specification updated (Table 3-11) • Thermal characteristics added (Section 8) • Orderable part numbers updated (Section 11)

Important: Please check www.cirrus.com or with your Cirrus Logic sales representative to confirm that you are using the latest revision of this document and to determine whether there are errata associated with this device.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com.