CS4340A

24-Bit, 192 kHz Stereo DAC for Audio

Features

- 101 dB Dynamic Range
- -91 dB THD+N
- +3.3 V or +5 V Power Supply
- 50 mW with 3.3 V supply
- Low Clock Jitter Sensitivity
- Filtered Line Level Outputs
- On-Chip Digital De-emphasis for 44.1 kHz
- Popguard® Technology for Control of Clicks and Pops
- Up to 200 kHz Sample Rates
- Automatic Mode Detection for Sample Rates between 4 and 200 kHz
- Pin Compatible with the CS4340

Description

The CS4340A is a complete stereo digital-to-analog system including digital interpolation, fourth-order delta-sigma digital-to-analog conversion, digital de-emphasis and switched capacitor analog filtering. The advantages of this architecture include: ideal differential linearity, no distortion mechanisms due to resistor matching errors, no linearity drift over time and temperature, and a high tolerance to clock jitter.

The CS4340A accepts data at all standard audio sample rates up to 192 kHz, consumes very little power, operates over a wide power supply range and is pin compatible with the CS4340, as described in section 3.1. These features are ideal for DVD audio players.

ORDERING INFORMATION

CS4340A-KS	16-pin SOIC, -10 to 70 °C
CS4340A-KSZ, Lead Free,	16-pin SOIC, -10 to 70 °C
CDB4340A	Evaluation Board

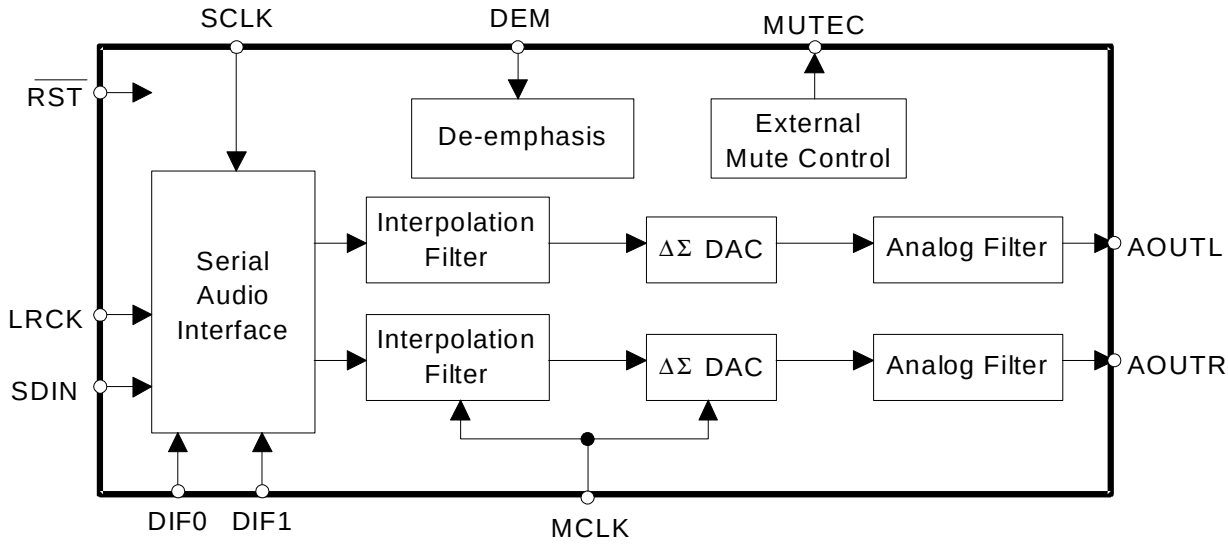
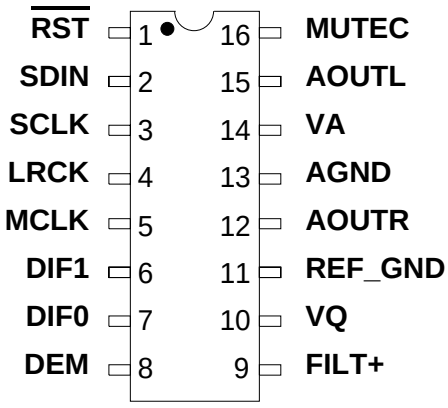


TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. PIN DESCRIPTION



Pin Name	#	Pin Description
RST	1	**Reset** (*Input*) - Powers down device.
SDIN	2	**Serial Audio Data** (*Input*) - Input for two's complement serial audio data.
SCLK	3	**Serial Clock** (*Input*) -Serial clock for the serial audio interface.
LRCK	4	**Left Right Clock** (*Input*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
MCLK	5	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters.
DIF1 **DIF0**	6 7	**Digital Interface Format** (I*nput*) - Defines the required relationship between the Left Right Clock, Serial Clock and Serial Audio Data.
DEM	8	**De-emphasis Control** (*Input*) - Selects the standard 15µs/50µs digital de-emphasis filter response for the 44.1 kHz sample rate.
FILT+	9	**Positive Voltage Reference** (*Output*) **-** Positive voltage reference for the internal sampling circuits.
VQ	10	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent reference voltage.
REF_GND	11	**Reference Ground** (*Input*) - Ground reference for the internal sampling circuits.
AOUTR **AOUTL**	12 15	**Analog Outputs** (*Output*) - The full scale analog output level is specified in the *Analog Characteristics* table.
AGND	13	**Analog Ground** (*Input*)
VA	14	**Power** (*Input*) **-** Positive power for the analog, digital and serial audio interface sections.
MUTEC	16	**Mute Control** (*Output*) - Control signal for an optional mute circuit.

2. TYPICAL CONNECTION DIAGRAM

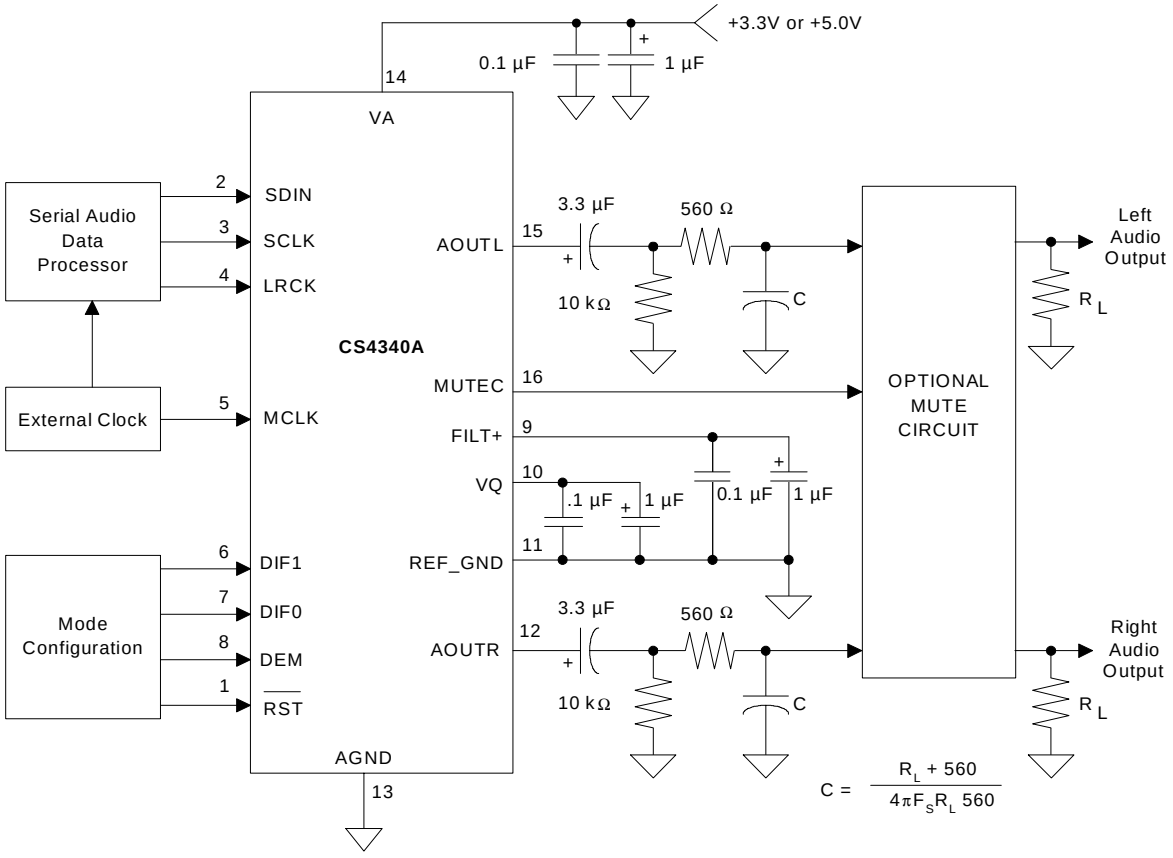


Figure 1. Typical Connection Diagram

3. APPLICATIONS

3.1 Upgrading from the CS4340 to the CS4340A

The CS4340A is pin and functionally compatible with all CS4340 designs, operating at the standard audio sample rates, that use pin 3 as a serial clock input. In addition to the features of the CS4340, the CS4340A supports standard sample rates up to 192 kHz, as well as automatic mode detection for sample rates between 4 and 200 kHz. The automatic mode detection feature allows sample rate changes between single, double and quad-speed modes without external intervention.

The CS4340A does not support an internal serial clock mode, sample rates between 50 kHz and 84 kHz, de-emphasis for 32 and 48 kHz, or 2.7 V operation as does the CS4340.

3.2 Sample Rate Range/Operational Mode Detect

The device operates in one of three operational modes. It will auto-detect the correct mode when the input sample rate (F_S), defined by the LRCK frequency, falls within one of the ranges illustrated in Table 1. Sample rates outside the specified range for each mode are not supported.

Input Sample Rate (F_S)	MODE
4 kHz - 50 kHz	Single-Speed Mode
84 kHz - 100 kHz	Double-Speed Mode
170 kHz - 200 kHz	Quad-Speed Mode

Table 1. CS4340A Auto-Detect

3.3 System Clocking

The device requires external generation of the master (MCLK), left/right (LRCK) and serial (SCLK) clocks. The LRCK, defined also as the input sample rate (F_S), must be synchronously derived from the MCLK according to specified ratios. The specified ratios of MCLK to LRCK, along with several standard audio sample rates and the required MCLK frequency, are illustrated in Tables 2-4.

Sample Rate (kHz)	MCLK (MHz)			
	256x	384x	512x	768x
32	8.1920	12.2880	16.3840	24.5760
44.1	11.2896	16.9344	22.5792	33.8688
48	12.2880	18.4320	24.5760	36.8640

Table 2. Single-Speed Mode Standard Frequencies

Sample Rate (kHz)	MCLK (MHz)			
	128x	192x	256x	384x
88.2	11.2896	16.9344	22.5792	33.8688
96	12.2880	18.4320	24.5760	36.8640

Table 3. Double-Speed Mode Standard Frequencies

Sample Rate (kHz)	MCLK (MHz)	
	128x	192x
176.4	22.5792	33.8688
192	24.5760	36.8640

Table 4. Quad-Speed Mode Standard Frequencies

3.4 Digital Interface Format

The device will accept audio samples in several digital interface formats as illustrated in Table 5. The desired format is selected via the DIF1 and DIF0 pins. For an illustration of the required relationship between LRCK, SCLK and SDIN, see Figures 2-5.

DIF1	DIF0	DESCRIPTION	FORMAT	FIGURE
0	0	I^2S, up to 24-bit data	0	2
0	1	Left Justified, up to 24-bit data	1	3
1	0	Right Justified, 24-bit Data	2	4
1	1	Right Justified, 16-bit Data	3	5

Table 5. Digital Interface Format - DIF1 and DIF0

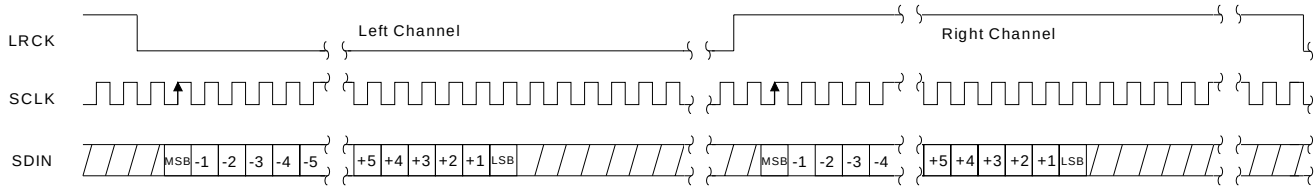


Figure 2. CS4340A Format 0 - I^2S up to 24-Bit Data

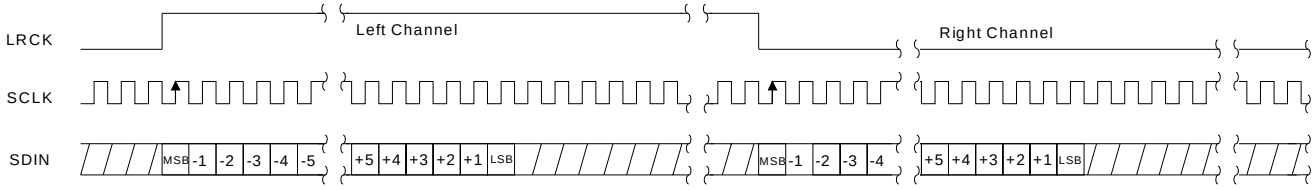


Figure 3. CS4340A Format 1 - Left Justified up to 24-Bit Data

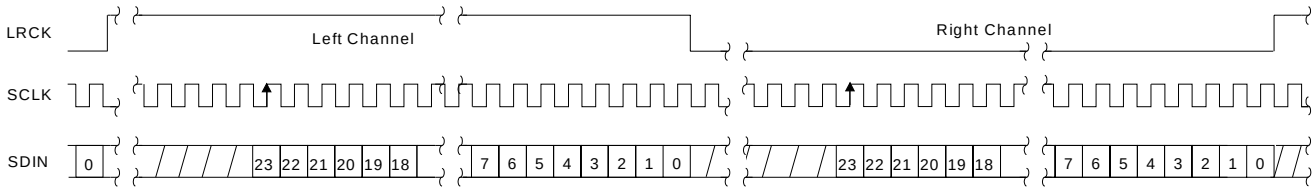


Figure 4. CS4340A Format 2 - Right Justified, 24-Bit Data

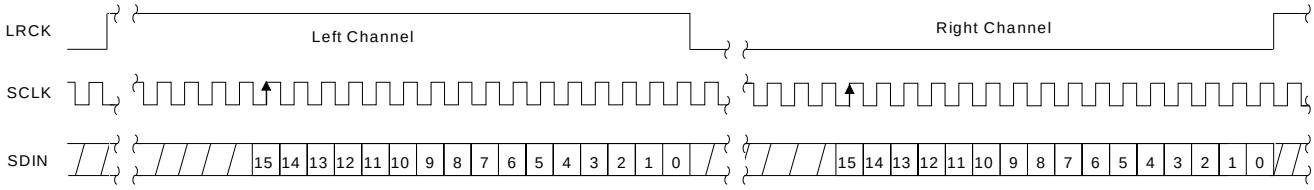


Figure 5. CS4340A Format 3 - Right Justified, 16-Bit Data

3.5 De-Emphasis

The device includes on-chip digital de-emphasis. Figure 6 shows the de-emphasis curve for F_s equal to 44.1 kHz. The frequency response of the de-emphasis curve will scale proportionally with changes in sample rate, F_s. Please see Table 6 for the desired de-emphasis control.

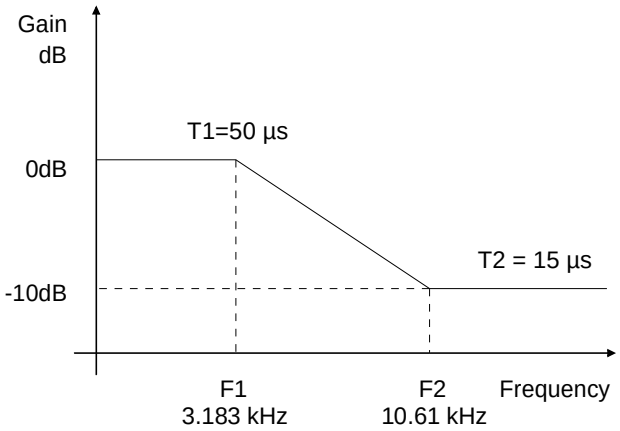


Figure 6. De-Emphasis Curve

DEM	DESCRIPTION
0	Disabled
1	44.1 kHz

Table 6. De-Emphasis Control

3.6 Power-up Sequence

Reliable power-up can be accomplished by keeping the device in reset until the power supply and configuration pins are stable, and the clocks are locked to the appropriate frequencies discussed in section 3.3. It is also recommended that reset be enabled if the analog supply drops below the minimum specified operating voltage to prevent power glitch related issues.

3.7 Popguard® Transient Control

The CS4340A uses Popguard® technology to minimize the effects of output transients during power-up and power-down. This technology, when used with external DC-blocking capacitors in series with the audio outputs, minimizes the audio transients commonly produced by single-ended single-supply converters. It is activated inside the DAC when $\overline{RST}$ is enabled/disabled and requires no other external control, aside from choosing the appropriate DC-blocking capacitors.

3.7.1 Power-up

When the device is initially powered-up, the audio outputs, AOUTL and AOUTR, are clamped to AGND. Following a delay of approximately 1000 sample periods, each output begins to ramp toward the quiescent voltage. Approximately 10,000 LRCK cycles later, the outputs reach V_Q and audio output begins. This gradual voltage ramping allows time for the external DC-blocking capacitors to charge to the quiescent voltage, minimizing the power-up transient.

3.7.2 Power-down

To prevent transients at power-down, the device must first enter its power-down state by enabling $\overline{RST}$. When this occurs, audio output ceases and the internal output buffers are disconnected from AOUTL and AOUTR. In their place, a soft-start current sink is substituted which allows the DC-blocking capacitors to slowly discharge. Once this charge is dissipated, the power to the device may be turned off and the system is ready for the next power-on.

3.7.3 Discharge Time

To prevent an audio transient at the next power-on, it is necessary to ensure that the DC-blocking capacitors have fully discharged before turning on the power or exiting the power-down state. If not, a transient will occur when the audio outputs are initially clamped to AGND. The time that the device must remain in the power-down state is related to the value of the DC-blocking capacitance. For example, with a 3.3 µF capacitor, the minimum power-down time will be approximately 0.4 seconds.

3.8 Mute Control

The Mute Control pin goes high during power-up initialization, reset, or if the MCLK to LRCK ratio is incorrect. The pin will also go high following the reception of 8192 consecutive audio samples of static 0 or -1 on both the left and right channels. A single sample of non-zero data on either channel will cause the Mute Control pin to go low. This pin is intended to be used as a control for an external mute circuit to prevent the clicks and pops that can occur in any single-ended single supply system.

Use of the Mute Control function is not mandatory but recommended for designs requiring the absolute minimum in extraneous clicks and pops. Also, use of the Mute Control function can enable the system designer to achieve idle channel noise/signal-to-noise ratios which are only limited by the external mute circuit. See the CDB4340A data sheet for a suggested mute circuit.

3.9 Grounding and Power Supply Arrangements

As with any high resolution converter, the CS4340A requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 shows the recommended power arrangements, with VA connected to a clean supply. If the ground planes are split between digital ground and analog ground, REF_GND & AGND should be connected to the analog ground plane.

Decoupling capacitors should be as close to the DAC as possible, with the low value ceramic capacitor being the closest. To further minimize impedance, these capacitors should be located on the same layer as the DAC.

All signals, especially clocks, should be kept away from the FILT+ and VQ pins in order to avoid unwanted coupling into the modulators. The FILT+ and VQ decoupling capacitors, particularly the 0.1 µF, must be positioned to minimize the electrical path from FILT+ and REF_GND (as well as VQ and REF_GND), and should also be located on the same layer as the DAC. The CDB4340A evaluation board demonstrates the optimum layout and power supply arrangements.

4. CHARACTERISTICS AND SPECIFICATIONS

(Min/Max performance characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics are derived from measurements taken at T_A = 25°C.)

RECOMMENDED OPERATING SPECIFICATION

Parameters	Symbol	Min	Typ	Max	Units
DC Power Supply					
3.3 V Nominal 5.0 V Nominal	VA	3.0 4.5	3.3 5	3.6 5.5	V V
Ambient Operating Temperature (Power Applied)	T_A	-10	-	+70	°C

ABSOLUTE MAXIMUM RATINGS (AGND = 0 V; all voltages with respect to AGND. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.)

Parameters	Symbol	Min	Max	Units
DC Power Supply	VA	-0.3	6.0	V
Input Current (Note 1)	I_{in}	-	±10	mA
Digital Input Voltage	V_{IND}	-0.3	VA+0.4	V
Ambient Operating Temperature (power applied)	T_A	-55	125	°C
Storage Temperature	T_{stg}	-65	150	°C

1. Any pin except supplies.

ANALOG CHARACTERISTICS (CS4340A-KS/KSZ) (Test conditions (unless otherwise specified): Input test signal is a 997 Hz sine wave; measurement bandwidth is 10 Hz to 20 kHz; test load R_L = 10 kΩ, C_L = 10 pF (see Figure 7).)

Parameter		VA = 5.0 V Min	VA = 5.0 V Typ	VA = 5.0 V Max	VA = 3.3 V Min	VA = 3.3 V Typ	VA = 3.3 V Max	Unit
Single-Speed Mode	**Fs = 48 kHz**							
Dynamic Range	(Note 2)							
18 to 24-Bit	unweighted	92	98	-	88	94	-	dB
	A-Weighted	95	101	-	91	97	-	dB
16-Bit	unweighted	-	92	-	-	92	-	dB
	A-Weighted	-	95	-	-	95	-	dB
Total Harmonic Distortion + Noise	(Note 2)							
18 to 24-Bit	0 dB	-	-91	-85	-	-94	-88	dB
	-20 dB	-	-78	-	-	-74	-	dB
	-60 dB	-	-38	-	-	-34	-	dB
16-Bit	0 dB	-	-90	-	-	-91	-	dB
	-20 dB	-	-72	-	-	-72	-	dB
	-60 dB	-	-32	-	-	-32	-	dB
Double-Speed Mode	**Fs = 96 kHz**							
Dynamic Range	(Note 2)							
18 to 24-Bit	unweighted	92	98	-	88	94	-	dB
	A-Weighted	95	101	-	91	97	-	dB
16-Bit	unweighted	-	92	-	-	92	-	dB
	A-Weighted	-	95	-	-	95	-	dB
Total Harmonic Distortion + Noise	(Note 2)							
18 to 24-Bit	0 dB	-	-91	-85	-	-94	-88	dB
	-20 dB	-	-78	-	-	-74	-	dB
	-60 dB	-	-38	-	-	-34	-	dB
16-Bit	0 dB	-	-90	-	-	-91	-	dB
	-20 dB	-	-72	-	-	-72	-	dB
	-60 dB	-	-32	-	-	-32	-	dB
Quad-Speed Mode	**Fs = 192 kHz**							
Dynamic Range	(Note 2)							
18 to 24-Bit	unweighted	92	98	-	88	94	-	dB
	A-Weighted	95	101	-	91	97	-	dB
16-Bit	unweighted	-	92	-	-	92	-	dB
	A-Weighted	-	95	-	-	95	-	dB
Total Harmonic Distortion + Noise	(Note 2)							
18 to 24-Bit	0 dB	-	-91	-85	-	-94	-88	dB
	-20 dB	-	-78	-	-	-74	-	dB
	-60 dB	-	-38	-	-	-34	-	dB
16-Bit	0 dB	-	-90	-	-	-91	-	dB
	-20 dB	-	-72	-	-	-72	-	dB
	-60 dB	-	-32	-	-	-32	-	dB

ANALOG CHARACTERISTICS (CS4340A-KS/KSZ) (Continued)

Parameters		Symbol	Min	Typ	Max	Units
Dynamic Performance for All Modes						
Interchannel Isolation (1 kHz)			-	102	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0.1	-	dB
Gain Drift			-	±100	-	ppm/°C
Analog Output Characteristics and Specifications						
Full Scale Output Voltage			0.6•VA	0.7•VA	0.8•VA	Vpp
Output Impedance			-	100	-	Ω
Minimum AC-Load Resistance	(Note 3)	R_L	-	3	-	kΩ
Maximum Load Capacitance	(Note 3)	C_L	-	100	-	pF

Notes: 2. One-half LSB of triangular PDF dither is added to data.

3. Refer to Figure 8.

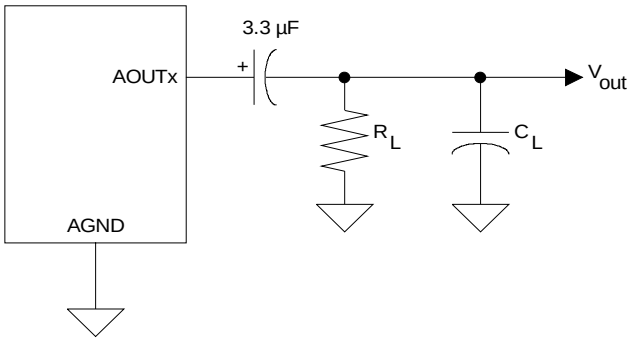


Figure 7. Output Test Load

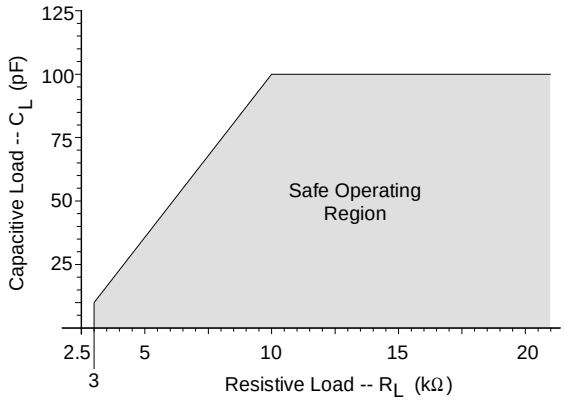


Figure 8. Maximum Loading

COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE (The filter characteristics and the X-axis of the response plots have been normalized to the sample rate (Fs) and can be referenced to the desired sample rate by multiplying the given characteristic by Fs.)

Parameter	Min	Typ	Max	Unit
Single-Speed Mode - (4 kHz to 50 kHz sample rates)				
Passband				
to -0.05 dB corner	0	-	0.4535	Fs
to -3 dB corner	0	-	0.4998	Fs
Frequency Response 10 Hz to 20 kHz	-0.02	-	+0.08	dB
StopBand	0.5465	-	-	Fs
StopBand Attenuation (Note 4)	50	-	-	dB
Group Delay	-	9/Fs	-	s
De-emphasis Error (Relative to 1 kHz) Fs = 44.1 kHz (Note 5)	-	-	+0.05/-0.14	dB
Double-Speed Mode - (84 kHz to 100 kHz sample rates)				
Passband				
to -0.1 dB corner	0	-	0.4621	Fs
to -3 dB corner	0	-	0.4982	Fs
Frequency Response 10 Hz to 20 kHz	-0.06	-	+0.2	dB
StopBand	0.577	-	-	Fs
StopBand Attenuation (Note 4)	55	-	-	dB
Group Delay	-	4/Fs	-	s
Quad-Speed Mode - (170 kHz to 200 kHz sample rates)				
Frequency Response 10 Hz to 20 kHz	-1	-	0	dB
Group Delay	-	3/Fs	-	s

Notes: 4. For Single-Speed Mode, the measurement bandwidth is 0.5465 Fs to 3 Fs.
For Double-Speed Mode, the measurement bandwidth is 0.577 Fs to 1.4 Fs.

5. De-emphasis is only available in Single-Speed Mode.

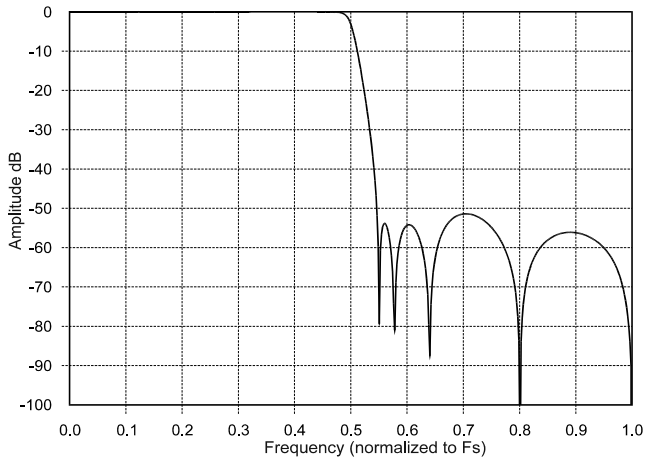


Figure 9. Single-Speed Stopband Rejection

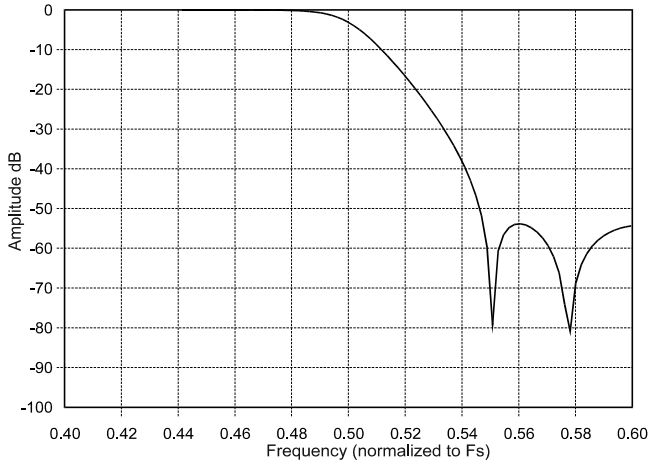


Figure 10. Single-Speed Transition Band

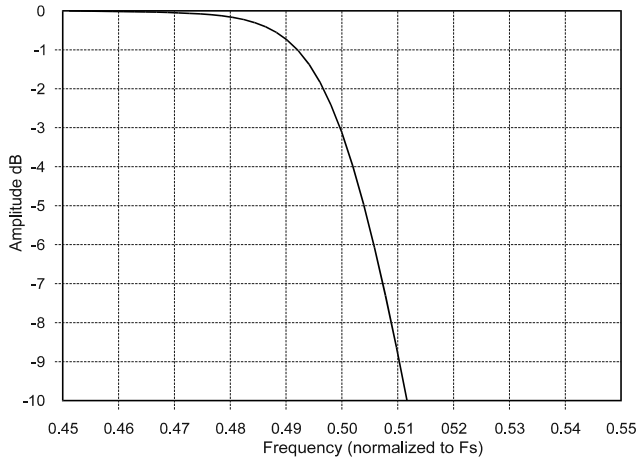


Figure 11. Single-Speed Transition Band (Detail)

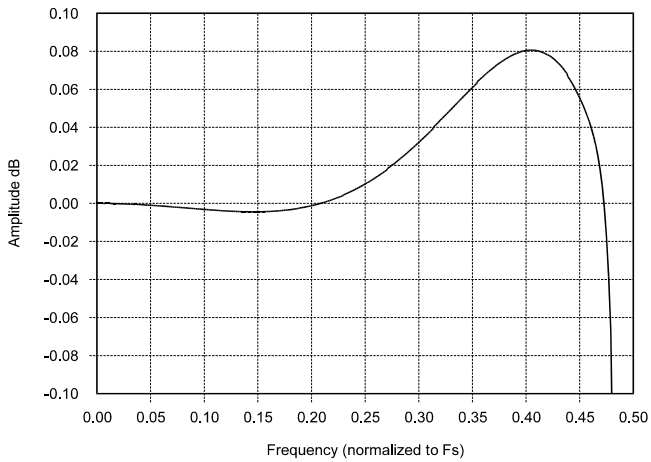


Figure 12. Single-Speed Passband Ripple

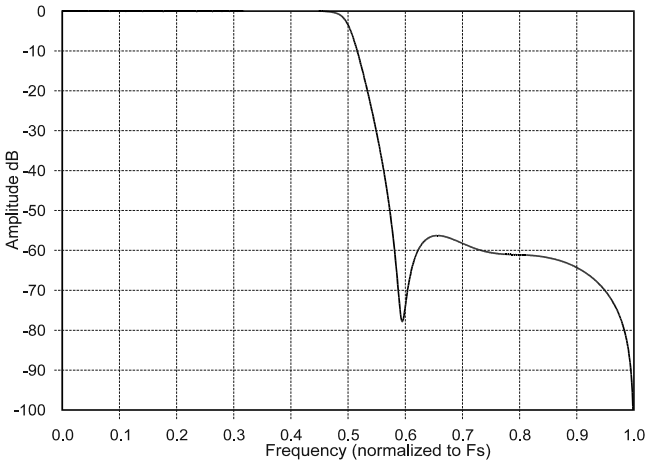


Figure 13. Double-Speed Stopband Rejection

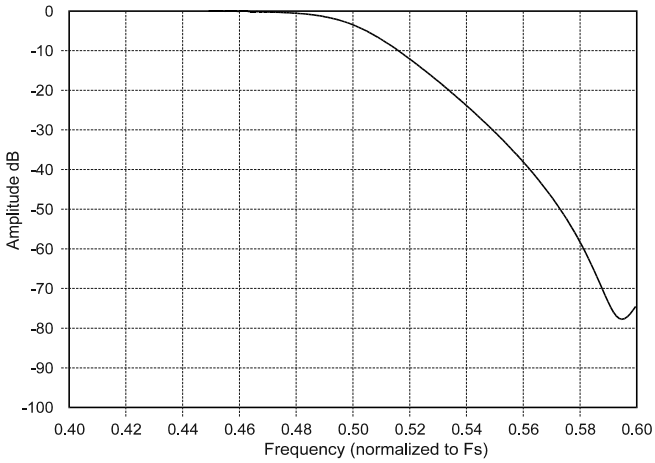


Figure 14. Double-Speed Transition Band

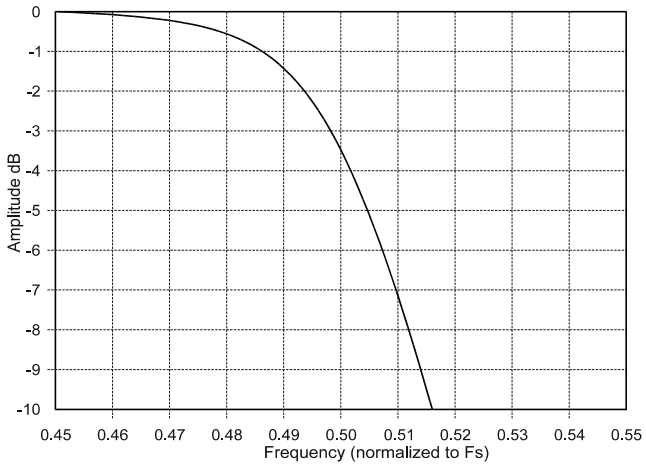


Figure 15. Double-Speed Transition Band (Detail)

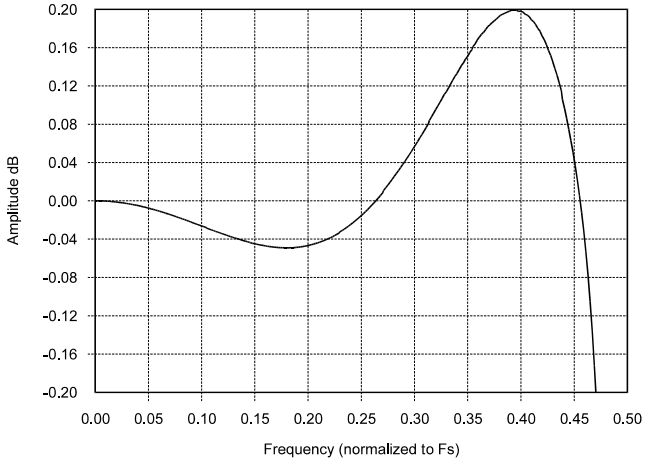


Figure 16. Double-Speed Passband Ripple

SWITCHING SPECIFICATIONS - SERIAL AUDIO INTERFACE

Parameters		Symbol	Min	Max	Units
MCLK Frequency			1.024	38.4	MHz
MCLK Duty Cycle			45	55	%
Input Sample Rate (Note 6)	Single-Speed Mode Double-Speed Mode Quad-Speed Mode	Fs Fs Fs	4 84 170	50 100 200	kHz kHz kHz
LRCK Duty Cycle			40	60	%
SCLK Frequency	Single-Speed Mode Double-Speed Mode Quad-Speed Mode		- - -	128xFs 64xFs $\frac{MCLK}{2}$	Hz Hz Hz
SCLK Pulse Width Low		t_{sclkl}	20	-	ns
SCLK Pulse Width High		t_{sclkh}	20	-	ns
SCLK rising to LRCK edge delay		t_{slrd}	20	-	ns
SCLK rising to LRCK edge setup time		t_{slrs}	20	-	ns
SDIN valid to SCLK rising setup time		t_{sdlrs}	20	-	ns
SCLK rising to SDIN hold time		t_{sdh}	20	-	ns
SCLK rising to MCLK edge delay (Note 7)		t_{smd}	8	-	ns

Notes: 6. Speed mode is detected automatically, based on the input sample rate.

7. Only required for Quad-Speed Mode.

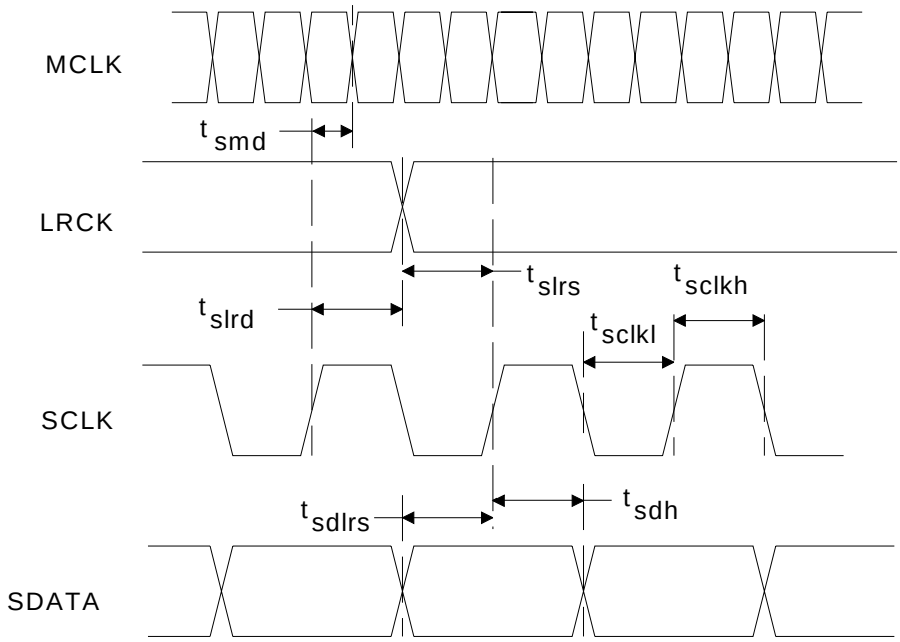


Figure 17. Serial Input Timing

DC ELECTRICAL CHARACTERISTICS (AGND = 0 V; all voltages with respect to AGND.)

Parameters		Symbol	Min	Typ	Max	Units
Normal Operation (Note 8)						
Power Supply Current	VA = 5.0 V	I_A	-	18	25	mA
	VA = 3.3 V		-	15	20	mA
Power Dissipation	VA = 5.0 V		-	90	125	mW
	VA = 3.3 V		-	50	100	mW
Power-down Mode (Note 9)						
Power Supply Current	VA = 5.0 V	I_A	-	60	-	µA
	VA = 3.3 V		-	35	-	µA
Power Dissipation	VA = 5.0 V		-	0.3	-	mW
	VA = 3.3 V		-	0.1	-	mW
All Modes of Operation						
Power Supply Rejection Ratio (Note 10)	1 kHz	PSRR	-	60	-	dB
	60 Hz		-	40	-	dB
V_Q Nominal Voltage			-	0.5•VA	-	V
Output Impedance			-	250	-	kΩ
Maximum allowable DC current source/sink			-	0.01	-	mA
Filt+ Nominal Voltage			-	VA	-	V
Output Impedance			-	250	-	kΩ
Maximum allowable DC current source/sink			-	0.01	-	mA
MUTEC Low-Level Output Voltage			-	0	-	V
MUTEC High-Level Output Voltage			-	VA	-	V
Maximum MUTEC Drive Current			-	3	-	mA

DIGITAL INTERFACE SPECIFICATIONS (GND = 0 V; all voltages with respect to GND.)

Parameters	Symbol	Min	Max	Units
3.3 V Logic *(2.7 V to 3.6 V DC Supply)*				
High-Level Input Voltage	V_{IH}	2.0	-	V
Low-Level Input Voltage	V_{IL}	-	0.8	V
5.0 V Logic *(4.5 V to 5.5 V DC Supply)*				
High-Level Input Voltage	V_{IH}	2.0	-	V
Low-Level Input Voltage	V_{IL}	-	0.8	V

DIGITAL INPUT CHARACTERISTICS (AGND = 0 V; all voltages with respect to AGND.)

Parameters	Symbol	Min	Typ	Max	Units
Input Leakage Current	I_{in}	-	-	±10	µA
Input Capacitance		-	8	-	pF

Notes: 8. Normal operation is defined as $\overline{RST}$ = HI with a 997 Hz, 0 dBFS input sampled at the highest F_S for each speed mode, and open outputs, unless otherwise specified.

9. Power Down Mode is defined as $\overline{RST}$ = LO with all clocks and data lines held static.

10. Valid with the recommended capacitor values on FILT+ and VQ as shown in Figure 1. Increasing the capacitance will also increase the PSRR.

5. PARAMETER DEFINITIONS

Total Harmonic Distortion + Noise (THD+N)

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels.

Dynamic Range

The ratio of the full scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with all zeros to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Drift

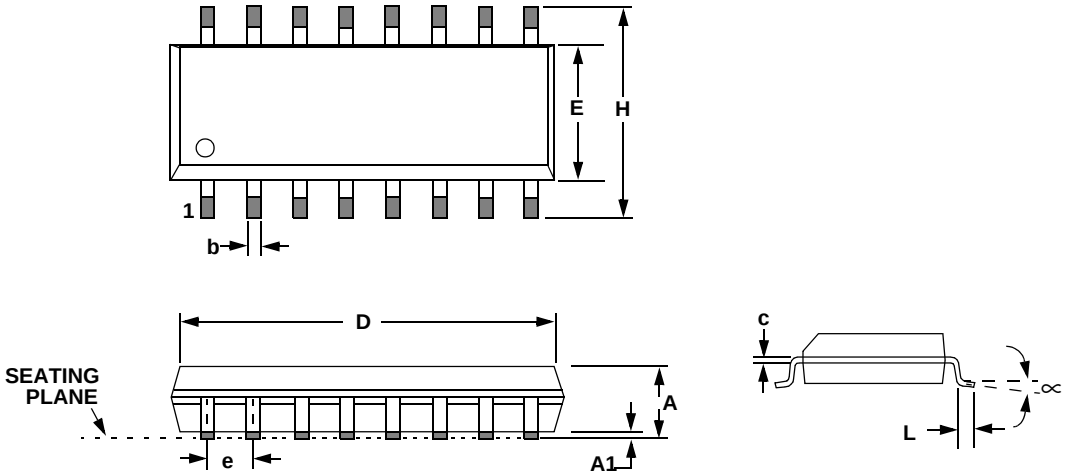
The change in gain value with temperature. Units in ppm/°C.

6. REFERENCES

1) CDB4340A Evaluation Board Datasheet

7. PACKAGE DIMENSIONS

16L SOIC (150 MIL BODY) PACKAGE DRAWING



	INCHES			MILLIMETERS		
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	0.053	0.064	0.069	1.35	1.63	1.75
A1	0.004	0.006	0.010	0.10	0.15	0.25
b	0.013	0.016	0.020	0.33	0.41	0.51
C	0.0075	0.008	0.010	0.19	0.20	0.25
D	0.386	0.390	0.394	9.80	9.91	10.00
E	0.150	0.154	0.157	3.80	3.90	4.00
e	0.040	0.050	0.060	1.02	1.27	1.52
H	0.228	0.236	0.244	5.80	6.0	6.20
L	0.016	0.025	0.050	0.40	0.64	1.27
∝	0°	4°	8°	0°	4°	8°

JEDEC #: MS-012

Controling Dimension is Millimeters

THERMAL CHARACTERISTICS AND SPECIFICATIONS

Parameters	Symbol	Min	Typ	Max	Units
Package Thermal Resistance (multi-layer boards)	θ_{JA}	-	74	-	°C/Watt

8. REVISION HISTORY

Release	Date	Changes
F2	July 2005	Added Revision History table and updated ordering information.

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to **www.cirrus.com**